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MOSFET – Dual N-Channel, Asymmetric, POWERTRENCH® Power Clip 25 V

FDPC8016S

ON Semiconductor®

www.onsemi.com

General Description

This device includes two specialized N−Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N-Channel

- Max $R_{DS(on)}$ = 3.8 mΩ at V_{GS} = 10 V, I_D = 20 A
- Max $R_{DS(on)}$ = 4.7 mΩ at V_{GS} = 4.5 V, I_D = 18 A

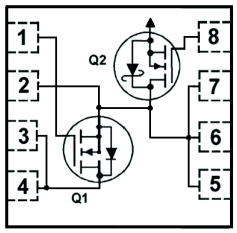
Q2: N-Channel

- Max $R_{DS(on)}$ = 1.4 mΩ at V_{GS} = 10 V, I_D = 35 A
- Max $R_{DS(on)}$ = 1.7 mΩ at V_{GS} = 4.5 V, I_D = 32 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- These Devices are Pb−Free and are RoHS Compliant

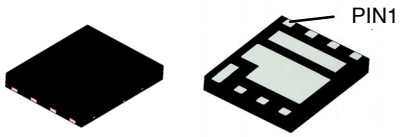
Applications

- Computing
- Communications
- General Purpose Point of Load

ELECTRICAL CONNECTION



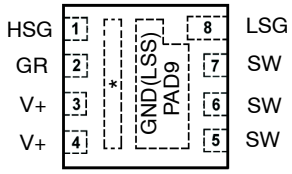
N-Channel MOSFET



Top View Bottom View

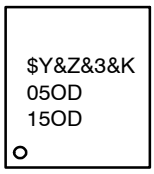
Power Clip 56
(PQFN8 5x6)
CASE 483AR

PIN ASSIGNMENT



*PAD10 V+(HSD)

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
05OD 15OD	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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PINOUT DESCRIPTION

Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3. 4, 10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5, 6, 7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter	Q1	Q2	Unit
V_{DS}	Drain to Source Voltage	25 (Note 5)	25 (Note 5)	V
V_{GS}	Gate to Source Voltage	±12	±12	V
I_D	Drain Current Continuous (T_C = 25°C) Continuous (T_A = 25°C) Pulsed (T_A = 25°C) (Note 4)	 60 20 (Note 1a) 75	 100 35 (Note 1b) 140	A
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	73	216	mJ
P_D	Power Dissipation for Single Operation (T_C = 25°C) (T_A = 25°C)	 21 2.1 (Note 1a)	 42 2.3 (Note 1b)	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.0	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 (Note 1a)	55 (Note 1b)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 (Note 1c)	120 (Note 1d)	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
05OD/15OD	FDPC8016S	Power Clip 56	13″	12 mm	3,000 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	25 25	– –	– –	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	– –	24 28	– –	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V V_{DS} = 20 V, V_{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 12 V / −8 V, V_{DS}= 0 V V_{GS} = 12 V / −8 V, V_{DS}= 0 V	Q1 Q2	– –	– –	±100 ±100	nA nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	0.8 1.0	1.3 1.5	2.5 2.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	– –	−4 −3	– –	mV/°C

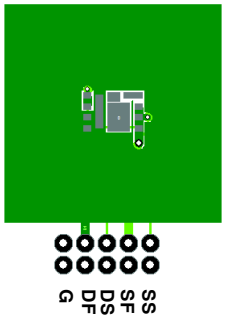
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
ON CHARACTERISTICS							
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 20 A V_{GS} = 4.5 V, I_D = 18 A V_{GS} = 10 V, I_D = 20 A, T_J =125°C	Q1	– – –	2.8 3.4 3.9	3.8 4.7 5.3	mΩ
		V_{GS} = 10 V, I_D = 35 A V_{GS} = 4.5 V, I_D = 32 A V_{GS} = 10 V, I_D = 35 A , T_J =125°C	Q2	– – –	1.1 1.3 1.5	1.4 1.7 1.9	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 20 A V_{DS} = 5 V, I_D = 35 A	Q1 Q2	– –	182 241	– –	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2	– –	1695 4715	2375 6600	pF
C_{oss}	Output Capacitance		Q1 Q2	– –	495 1195	710 1675	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	54 159	100 290	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	0.4 0.5	1.2 1.5	Ω
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 13 V, I_D = 20 A, R_{GEN} = 6 Ω Q2: V_{DD} = 13 V, I_D = 35 A, R_{GEN} = 6 Ω	Q1 Q2	– –	8 13	16 24	ns
t_r	Rise Time		Q1 Q2	– –	2 4	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2	– –	24 38	38 61	ns
t_f	Fall Time		Q1 Q2	– –	2 3	10 10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V Q1: V_{DD} = 13 V, I_D = 20 A Q2: V_{DD} = 13 V, I_D = 35 A	Q1 Q2	– –	25 67	35 94	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V Q1: V_{DD} = 13 V, I_D = 20 A Q2: V_{DD} = 13 V, I_D = 35 A	Q1 Q2	– –	11 31	16 44	nC
Q_{gs}	Gate to Source Gate Charge	Q1: V_{DD} = 13 V, I_D = 20 A Q2: V_{DD} = 13 V, I_D = 35 A	Q1 Q2	– –	3.4 10	– –	nC
Q_{gd}	Gate to Drain “Miller” Charge	Q1: V_{DD} = 13 V, I_D = 20 A Q2: V_{DD} = 13 V, I_D = 35 A	Q1 Q2	– –	2.2 6.3	– –	nC
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 20 A V_{GS} = 0 V, I_S = 35 A (Note 2)	Q1 Q2	–	0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1: I_F = 20 A, di/dt = 100 A/μs Q2: I_F = 35 A, di/dt = 200 A/μs	Q1 Q2	–	25 33	40 53	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2	–	10 31	20 50	nC

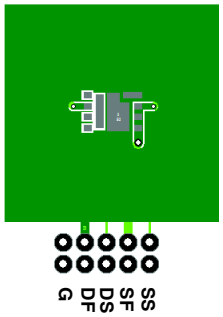
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

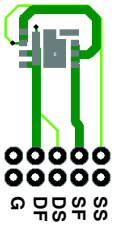
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user’s board design.



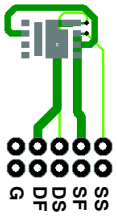
a) 60°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 55°C/W when mounted on a 1 in^2 pad of 2 oz copper.



c) 130°C/W when mounted on a minimum pad of 2 oz copper.



d) 120°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1:
   E_{AS} of 73 mJ is based on starting T_J = 25°C; N-ch: L = 3 mH, I_{AS} = 7 A, V_{DD} = 30 V, V_{GS} = 10 V, 100% tested at L = 0.1 mH, I_{AS} = 24 A.
   Q2:
   E_{AS} of 216 mJ is based on starting T_J = 25°C; N-ch: L = 3 mH, I_{AS} = 12 A, V_{DD} = 25 V, V_{GS} = 10 V, 100% tested at L = 0.1 mH, I_{AS} = 39 A.
4. Pulsed Id limited by junction temperature, td <=10 μs. Please refer to SOA curve for more details.
5. The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.

TYPICAL CHARACTERISTICS (Q1 N-Channel)

(T_J = 25°C unless otherwise noted)

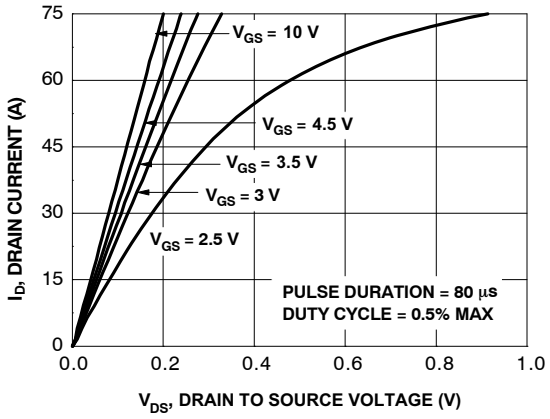


Figure 1. On-Region Characteristics

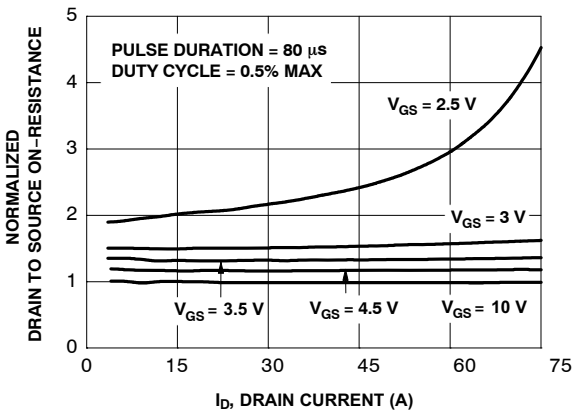


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

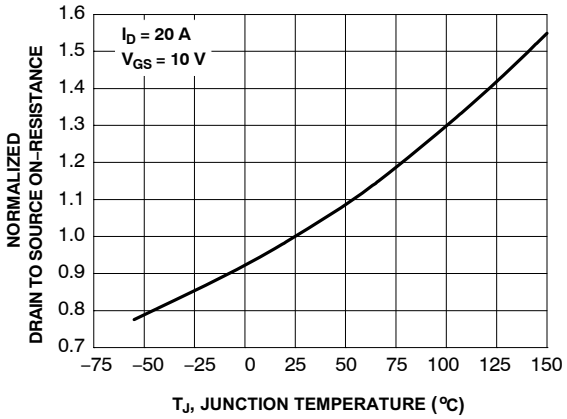


Figure 3. Normalized On-Resistance vs. Junction Temperature

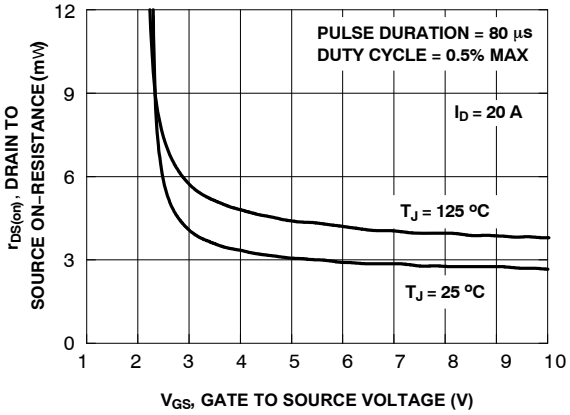


Figure 4. On-Resistance vs. Gate to Source Voltage

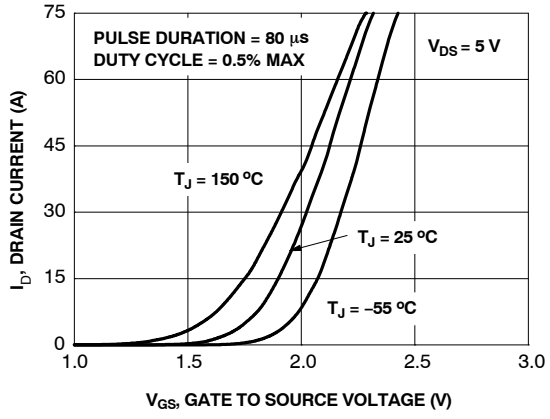


Figure 5. Transfer Characteristics

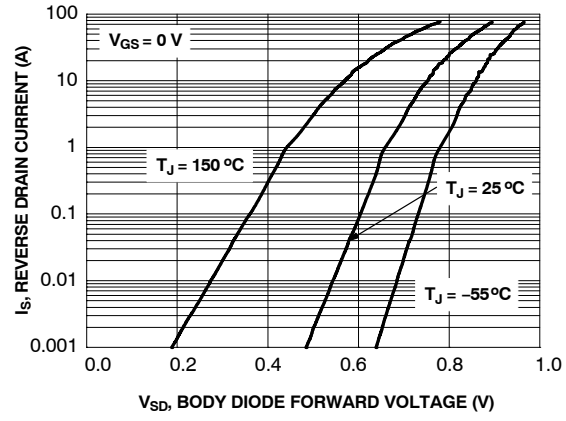


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-Channel)

(T_J = 25°C unless otherwise noted)

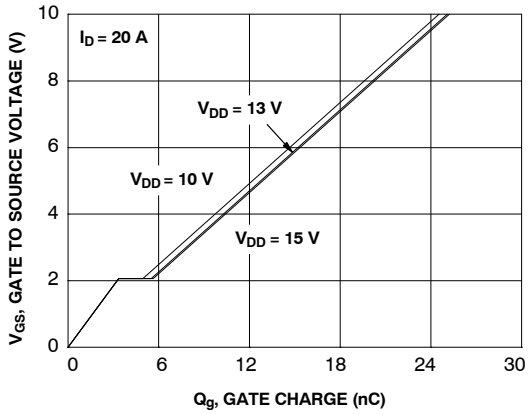


Figure 7. Gate Charge Characteristics

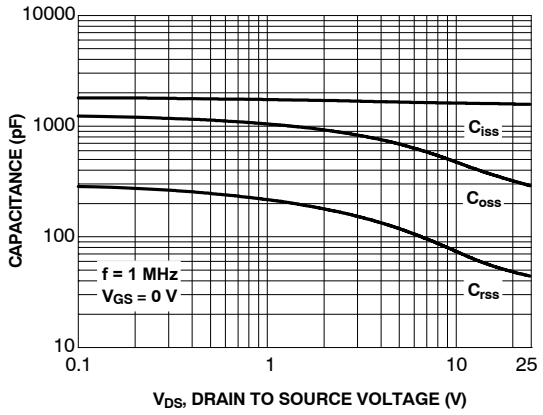


Figure 8. Capacitance vs. Drain to Source Voltage

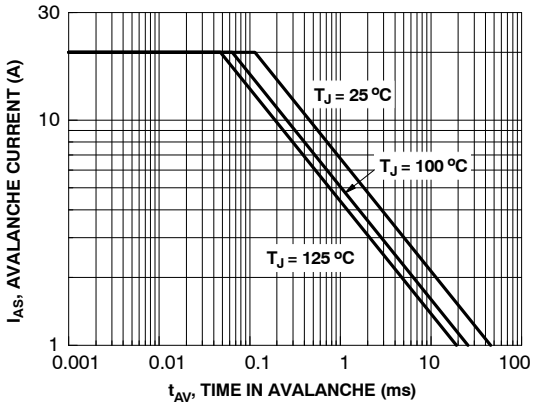


Figure 9. Unclamped Inductive Switching Capability

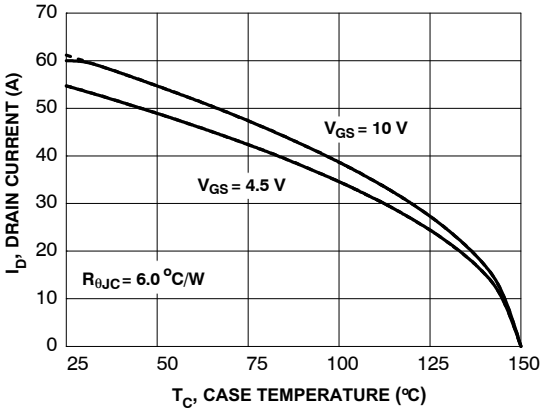


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

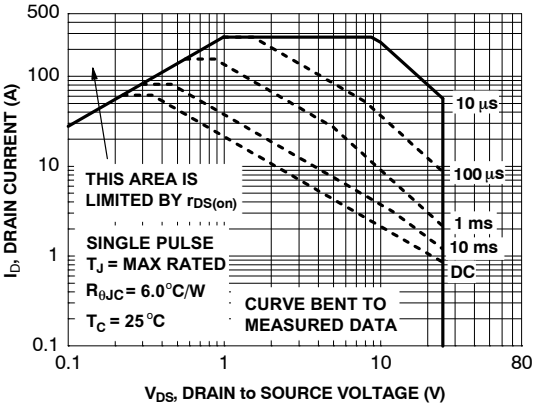


Figure 11. Forward Bias Safe Operating Area

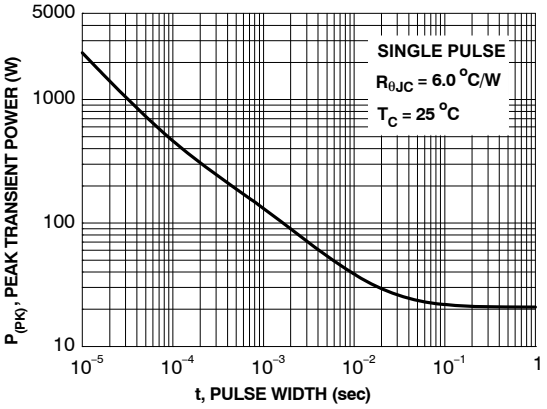


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N-Channel)

(T_J = 25°C unless otherwise noted)

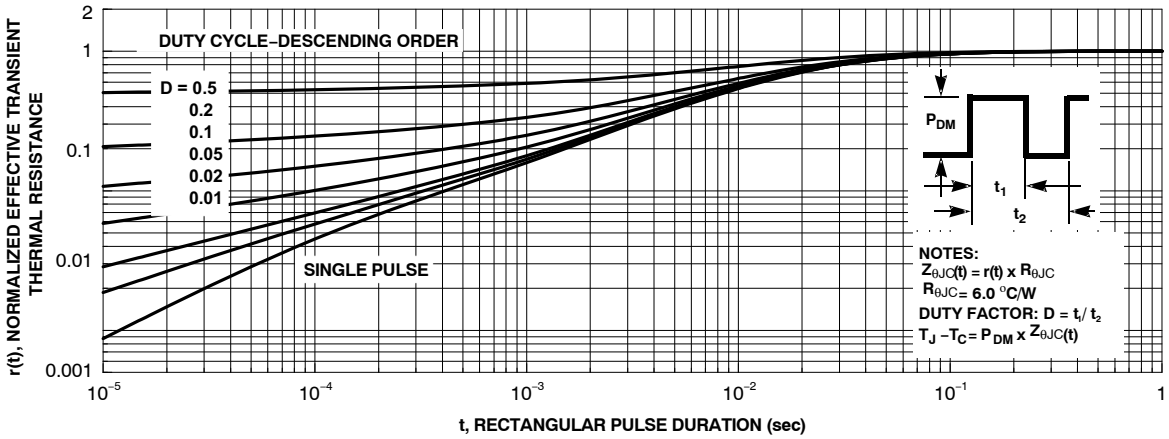


Figure 13. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-Channel)

(T_J = 25°C unless otherwise noted)

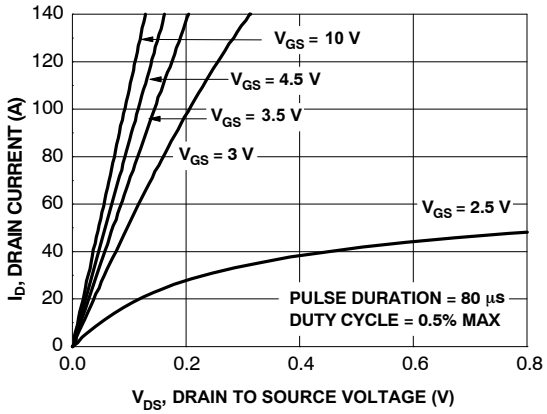


Figure 14. On-Region Characteristics

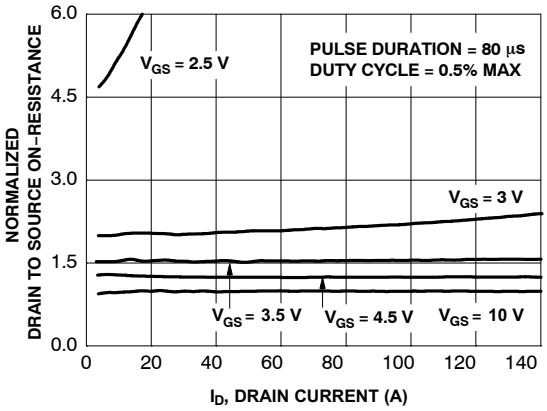


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

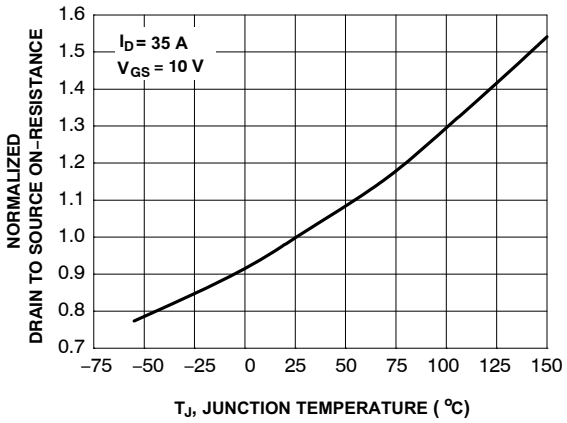


Figure 16. Normalized On-Resistance vs. Junction Temperature

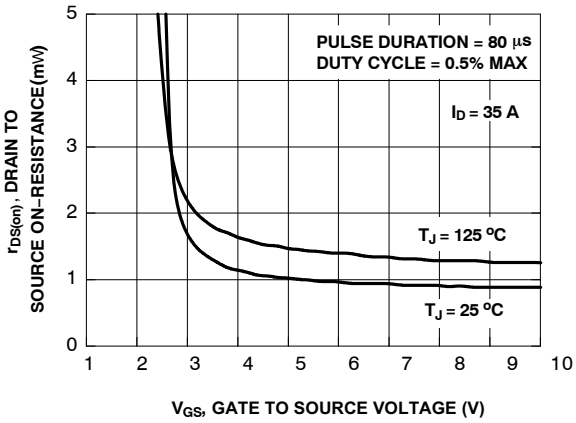


Figure 17. On-Resistance vs. Gate to Source Voltage

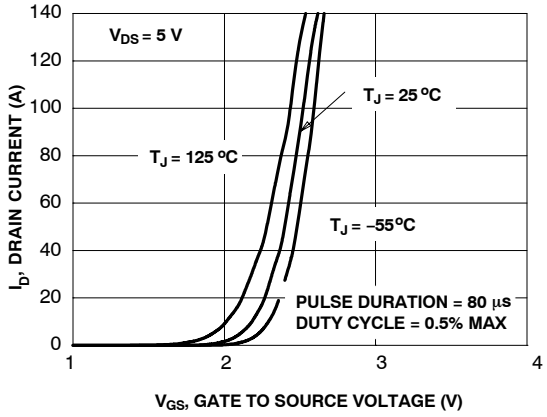


Figure 18. Transfer Characteristics

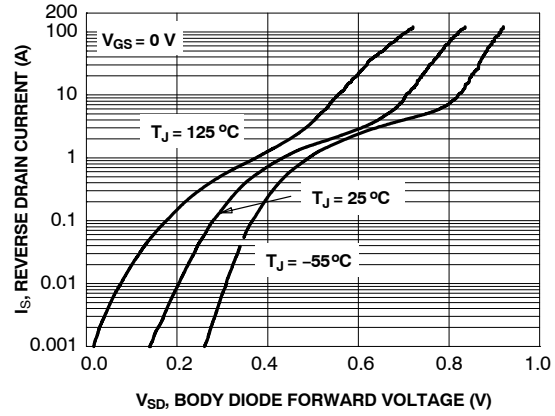


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-Channel)

(T_J = 25°C unless otherwise noted)

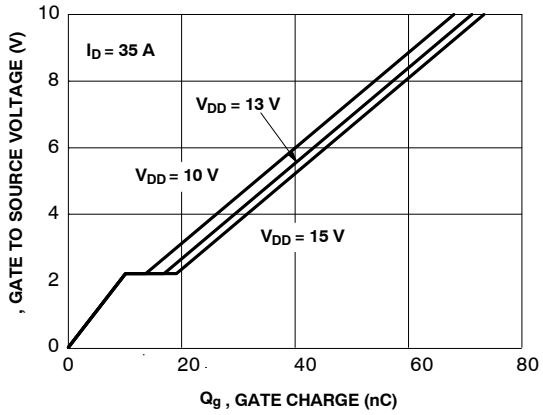


Figure 20. Gate Charge Characteristics

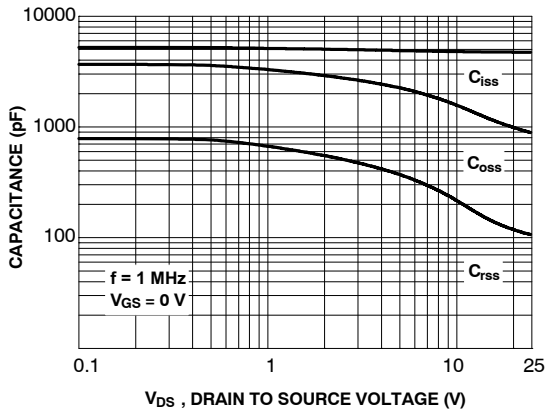


Figure 21. Capacitance vs. Drain to Source Voltage

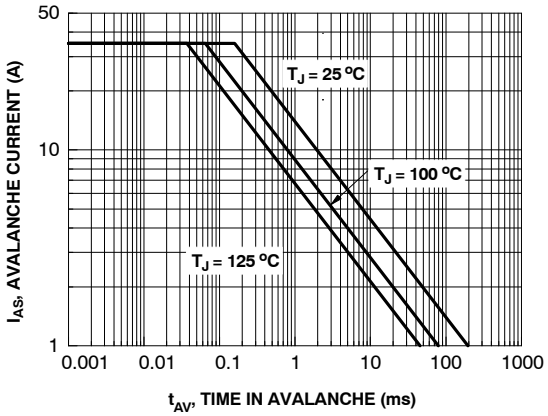


Figure 22. Unclamped Inductive Switching Capability

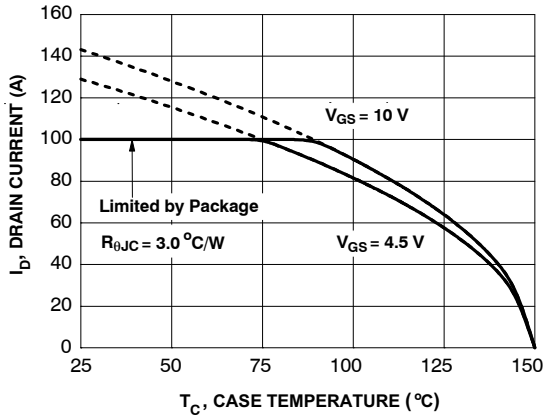


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

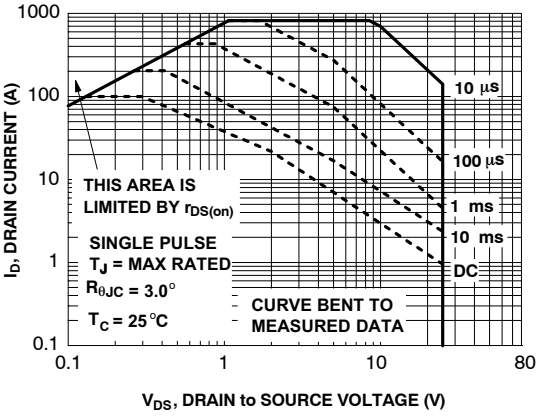


Figure 24. Forward Bias Safe Operating Area

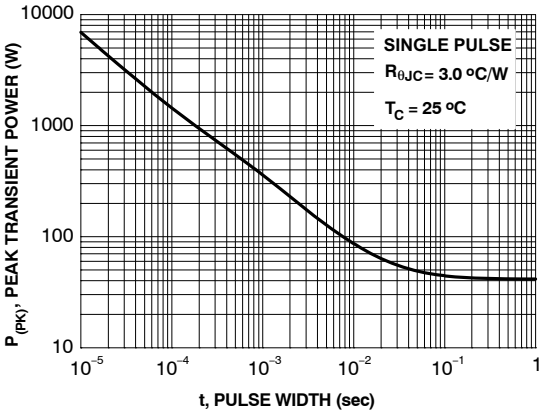


Figure 25. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N-Channel)

(T_J = 25°C unless otherwise noted)

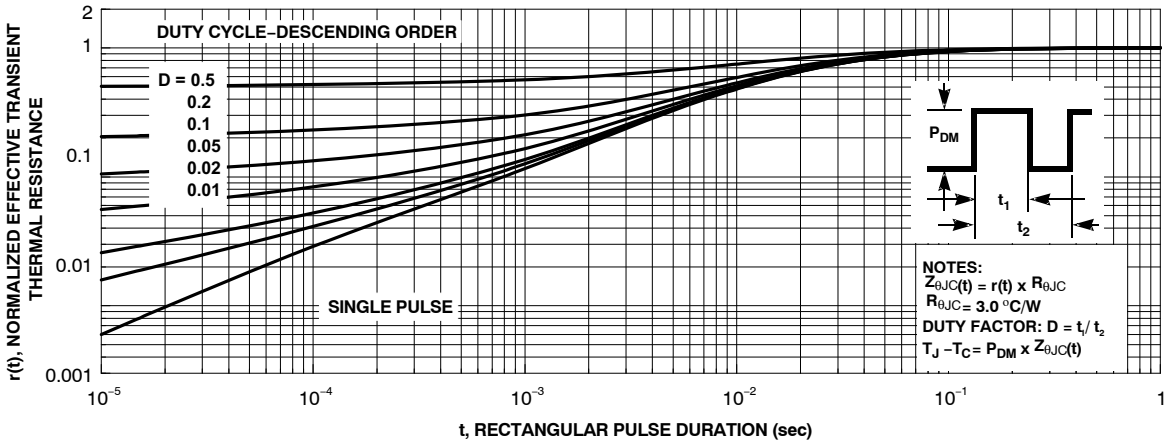


Figure 26. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

ON's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8016S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

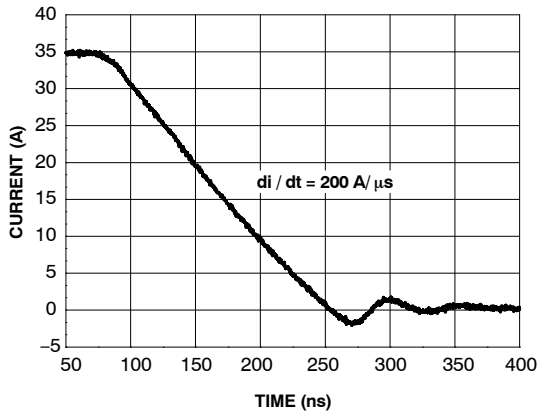


Figure 27. FDPC8016S SyncFET Body Diode Reverse Recovery Characteristic

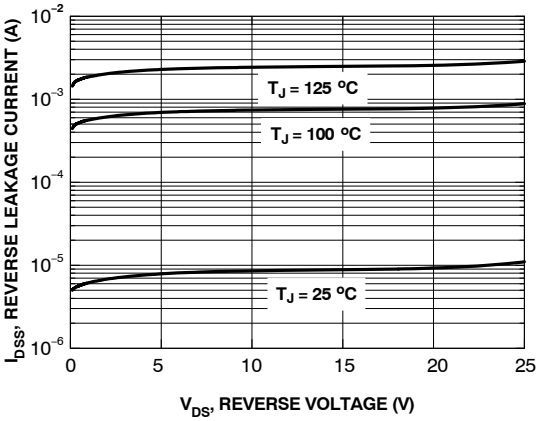


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

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