DESCRIPTION

PT2502 is an integrated 12V 3-phase sensor-less (no Hall sensor required) BLDC motor controller. Three-phase motor control with square/trapezoidal wave is based on detecting a zero-crossing signal generated from the motor back-EMF (BEMF) and provides robust control stability that is not easily affected by different motors. Soft-switching control technology outputs trapezoidal/quasi-sinusoidal-wave current and further reduces audible electro-current noise. PT2502 provides an internal +5V voltage regulator to supply power to the analog and digital blocks. For 400V high-voltage motor control applications, an external high voltage gate driver and six N-channel MOSFETs are required. For 12V to 24V operation, PT2502 can drive high-side P-channel MOSFET and low-side N-channel MOSFET with a simple level shifter circuit. Optimized parameter settings for different motors and applications may be written to OTP memory. The PT2502 is provided in an SSOP28 package.

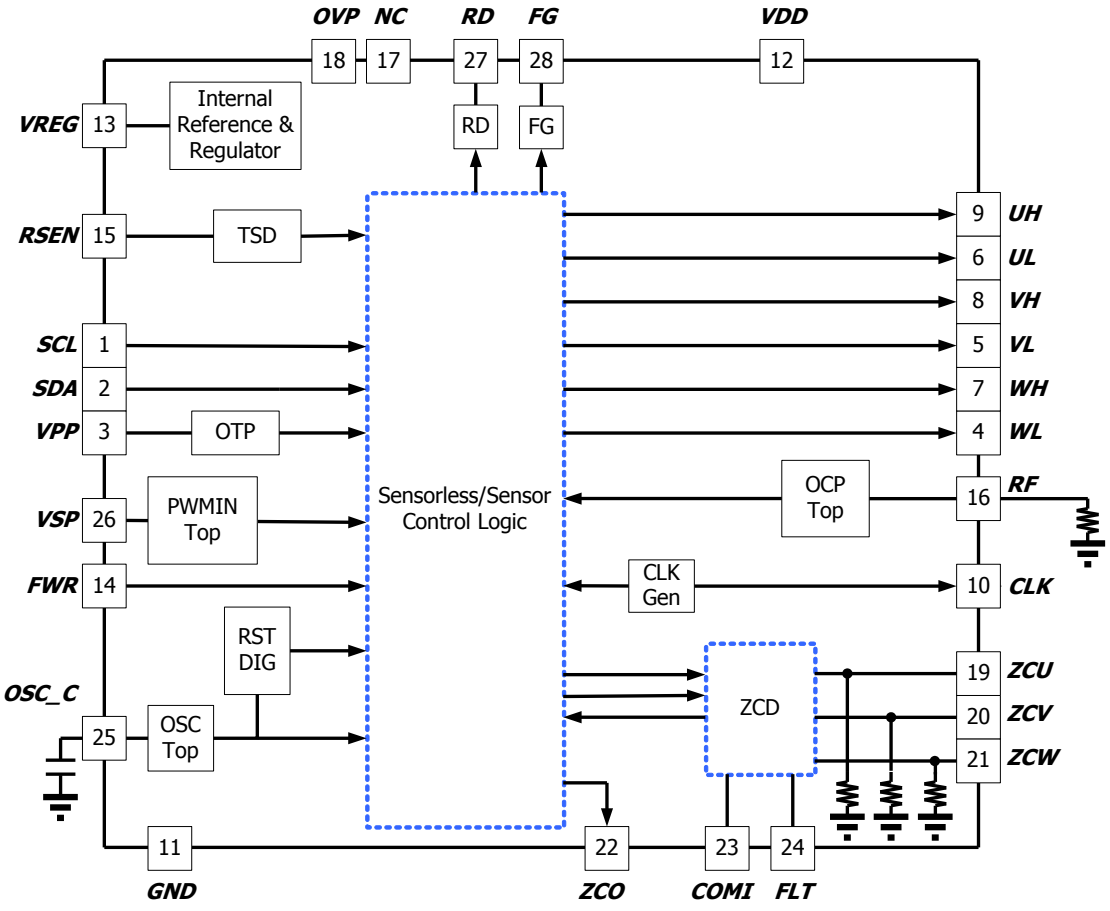
FEATURES

- 3-phase sensor-less BLDC control
- Internal +5V regulator and 5V – 24V power application
- Internal OTP write support for motor parameters
- I2C interface for parameter setting
- Over-current protection and over-voltage protection
- Thermal protection function with an external NTC resistor
- Lock protect function
- PWM or DC control input support for motor speed control
- FG output function

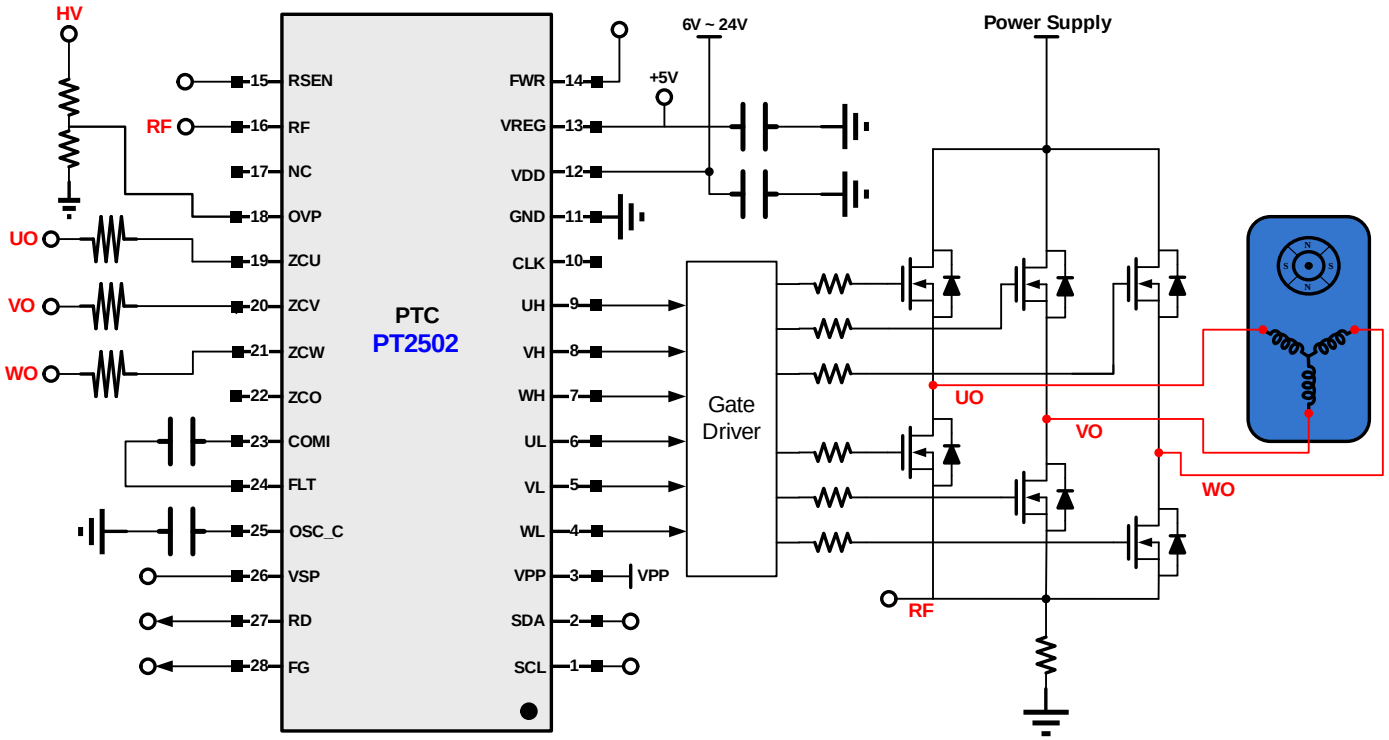
APPLICATIONS

- 3-phase sensor-less BLDC motor controller
- High speed fan
- Water pump

BLOCK DIAGRAM



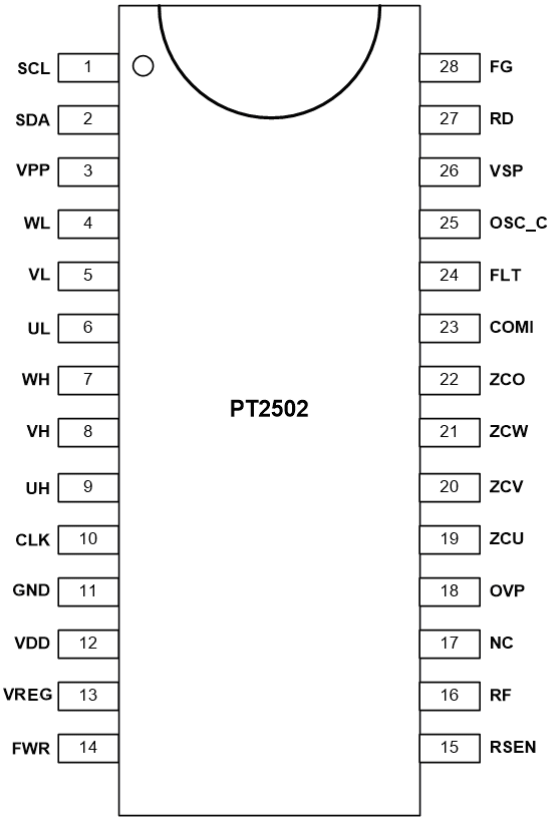
APPLICATION CIRCUIT



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2502-X	28 Pins, SSOP	PT2502-X

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SCL	I	Serial clock input – I2C control interface	1
SDA	I/O	Serial data input/output – I2C control interface	2
VPP	P	High voltage power supply (7.5V) for programming OTP	3
WL	O	W phase low side signal output	4
VL	O	V phase low side signal output	5
UL	O	U phase low side signal output	6
WH	O	W phase high side signal output	7
VH	O	V phase high side signal output	8
UH	O	U phase high side signal output	9
CLK	O	Clock output pin	10
GND	P	High and low voltage ground	11
VDD	P	High voltage power supply	12
VREG	P	5V regulator output	13
FWR	I	Forward or reverse select input	14
RSEN	O	External resistor connection for over temperature sensing	15
RF	O	Current limit voltage sensor	16
NC	-	-	17
OVP	I	Over voltage protection	18
ZCU	I	U phase BEMF zero crossing input	19
ZCV	I	V phase BEMF zero crossing input	20
ZCW	I	W phase BEMF zero crossing input	21
ZCO	O	Six-step commutation signal output	22
COMI	I	Motor pseudo middle point of the motor	23
FLT	I	Six-step commutation signal filter input	24
OSC_C	IO	External capacitor connection to generate PWM triangle waveform	25
VSP	I	Speed command control thru DC or PWM input	26
RD	O	Lock mode signal output (5V CMOS logic)	27
FG	O	Fan speed signal output (5V CMOS logic)	28

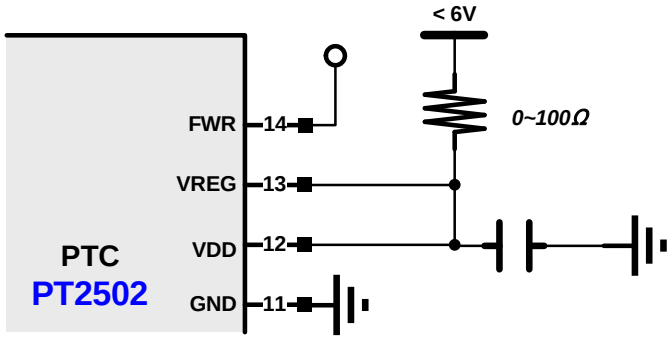
FUNCTION DESCRIPTION

POWER SUPPLY

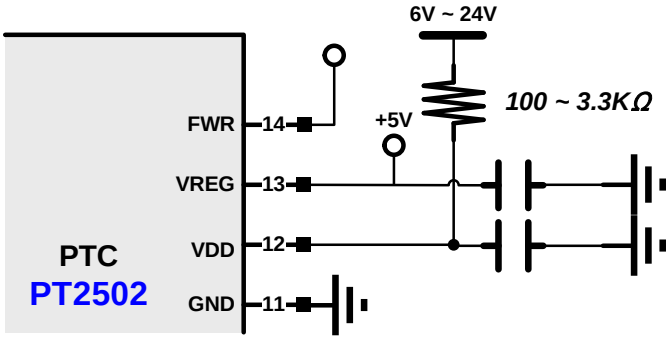
Since PT2502's current consumption is very low (<5 mA) and PT2502 has a built-in 24V to 5V linear regulator (LDO) to provide the power for logic and analog circuitry, for 6V to 24V motor applications, there is no need for an external 5V regulator device. In a high-voltage (<400V) motor system, the 15V power supply voltage may be used. For a 5V voltage operation, VDD and VREG pins should be shorted to each other.

In order to avoid interference or unstable power supply, PT2502 monitors the internal LDO voltage. When the LDO voltage exceeds 3.5V, the logic circuit will operate within 10ms. In the motor system the chip may easily be affected by the induced noise, so placement of a bypass capacitor as near as possible to the IC power pins is recommended.

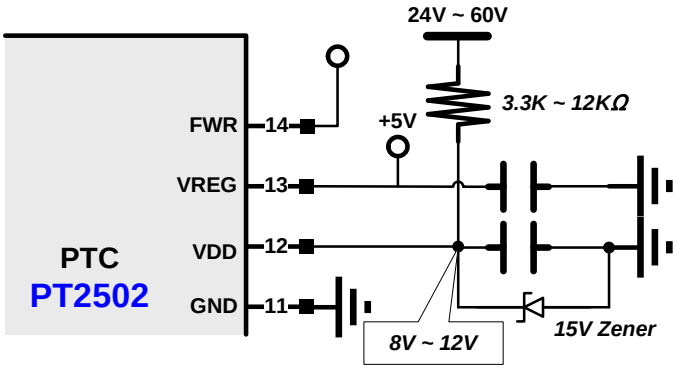
When the power supply is less than 6V or for the case of a 5V supply system, connect VDD to VREG as shown below.



When the power supply provides 6V – 24V or for a high-voltage system where VM is larger than 60V and there exists a 15V power supply regulator, the PT2502 power schematic connection is shown below.



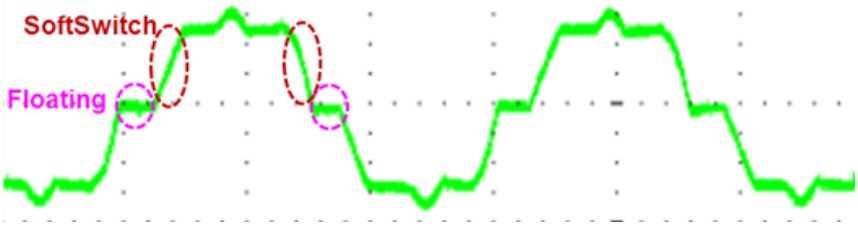
When the power supply provides 24V – 60V, the resistor may be used to drop supply voltage to below 8V – 12V and may be combined with 15V Zener diode for protection. The power schematic connection is shown below.



SENSORLESS CONTROL

The PT2502 control scheme is based on sensor-less (no Hall sensor required) trapezoidal wave. The primary benefit is to eliminate the need for the Hall sensor, reducing module cost as well as temperature variation issues. Feedback for sensor-less control is achieved mainly through measurement of the induced BEMF of motor wires while the motor is rotating. When the motor is being controlled, UVW coil endpoint voltage (phase voltage) is combined with the control signal and BEMF, making it difficult to separate the BEMF from the phase voltage. Floating the motor for a while (at a specific angle) when the motor is commutating is one method to obtain the BEMF signal. In general, the floating electrical angle is 60° for pure square wave control, 120° under commutation control, and 30° for trapezoidal wave control. There is also the 150° commutation control case.

The PT2502 senses UVW phase voltages by using voltage-divider resistors (10K resistors connected to ground) to lower the phase voltages to approximately 5V, allowing the analog circuitry to process the signals and generate the zero crossing (ZC) signal for commutation. Because of the many possible combinations of motors, operating voltages, speeds, and other factors, adjustment of the analog filter (an external capacitor) or digital filter (internal parameters) may be needed. Having system noise that is too large or a motor's BEMF signal that is too weak will affect the ZC signal accuracy and this may cause control failure. The PT2502's implementation of a soft-switching control function is helpful in reducing audible electro-current noise.



PT2502 commutation current waveform examples

CURRENT LIMIT

PT2502 implements a current limit function by using a sense resistor to obtain a voltage (at the RF pin) that is related to phase-to-phase current. PWM operation is turned off or PWM duty is decreased when the detected RF voltage exceeds 0.3V. The RF resistor is required to be a high-power, precision resistor in order to avoid burn-out phenomenon when the resistor is over-temperature. If the RF resistor is open due to the burn-out, it may damage the controller, Gate Driver and MOSFET components.

CAPACITANCE SELECTION BETWEEN COM AND FLT PINS

PT2502 detects the motor position by comparing the back electromotive force generated from the rotation of motor and the 3-phase virtual mid-point voltage. However, noise arising from the motor startup or rotation may interfere with the determination of the zero crossing point and this may result in startup failure or reduced motor efficiency at high speed. Adding a capacitor between the COM and FLT pins helps to mitigate the effects of the noise interference. The recommended range for capacitance values is from 1nF to 10nF. Because the filter will affect the detection of commutation delay, the higher the speed of the motor, the smaller the chosen capacitance value to minimize the impact of filter delay on efficiency. Alternatively, the internal parameters may be used to set the digital filter. Regardless of whether the digital filter or analog filter is selected, either will cause delay. The PT2502 provides various configurable parameters to compensate for a variety of delay and to allow the motor to maintain efficient operation.

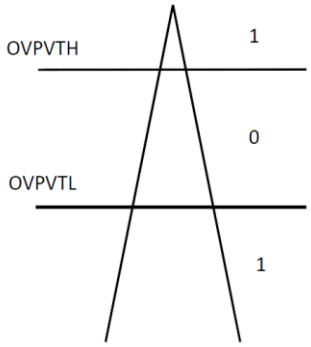
OVER TEMPERATURE PROTECTION

The PT2502 uses an external negative temperature coefficient (NTC) resistor to implement the detector for the over temperature protection function. At the RSEN pin, a normal resistor is connected to 5V and a NTC resistor is connected to ground. The NTC resistor should be physically placed near a device targeted for over temperature protection (OTP), such as a MOSFET. Once the temperature rises, the NTC resistance is reduced and the voltage level at the RSEN pin decreases. When the RSEN voltage is less than 0.6V, the PT2502 enters OTP mode and the logic level at the RD pin is pulled HIGH and the system enters shutdown mode. Once the temperature lowers and the voltage at the RSEN pin rises higher than 1.2V, the motor system will start again.

In shutdown mode of the PT2502, UH/UL/VH/VL/WH/WL output logic levels are LOW.

OVER VOLTAGE PROTECTION

The over voltage protection function of the PT2502 is designed to stop the motor rotation in order to prevent both motor burn out when the external voltage VM is too high as well as abnormal behavior of the overall system when VM is too low. The over voltage protection function diagram is as follows:



Over voltage protection function diagram

A warning signal is issued when the detected voltage at OVP pin (generated from VM through a resistor network) is higher than OVP_{VTH} or the detected voltage is lower than OVP_{VTL}. Only when the detected signal is within the safe range does the system operate normally. The over voltage protection feature is set OFF by default but its status may be read out thru the UI program. To enable over voltage protection, the register value may be set through the UI program. For detailed instructions, please refer to the UI application manual.

In PT2502, OVP_{VTH} and OVP_{VTL} may be set individually. The internal OVP comparators incorporate hysteresis circuitry to avoid unwanted instability when the detected OVP signal slightly changes.

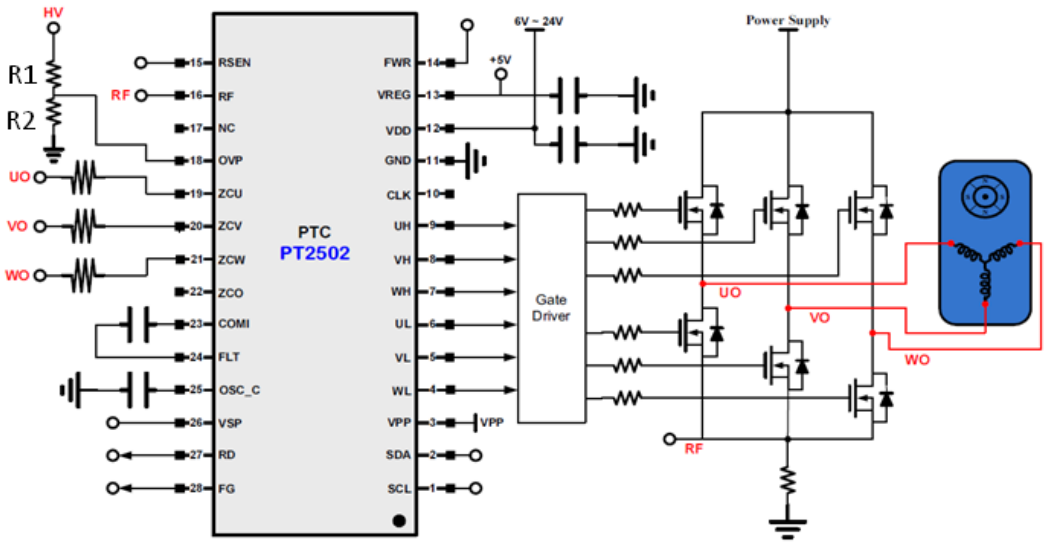
OVPVTH Code	OVP Voltage	Unit
0	2.125	V
1	2.250	V
2	2.375	V
3	2.500	V
4	2.625	V
5	2.750	V
6	2.875	V
7	3.000	V

OVPVTL Code	OVP Voltage	Unit
0	1.125	V
1	1.250	V
2	1.375	V
3	1.500	V
4	1.625	V
5	1.750	V
6	1.875	V
7	2.000	V

OVP_{VTH} and OVP_{VTL} codes vs. OVP value

The procedure to set-up the over voltage protection function for the PT2502 is discussed below.

1. According to customer requirements for the upper and lower operation limits (if an AC value is given, please convert to a DC value), sum the upper and lower limit values and divide by 4 to obtain a ratio value.
2. Divide the upper and lower limit values individually by the ratio value to obtain the OVP_{VTH} and OVP_{VTL} detection threshold values, respectively. Refer to the table above to determine the appropriate code which corresponds to each desired threshold value.
3. The resistor values are calculated according to the customer requirements as long as the relationship, [R2/(R1+R2)]*[upper threshold + lower threshold]/2 = 2, is satisfied.



Application Circuit

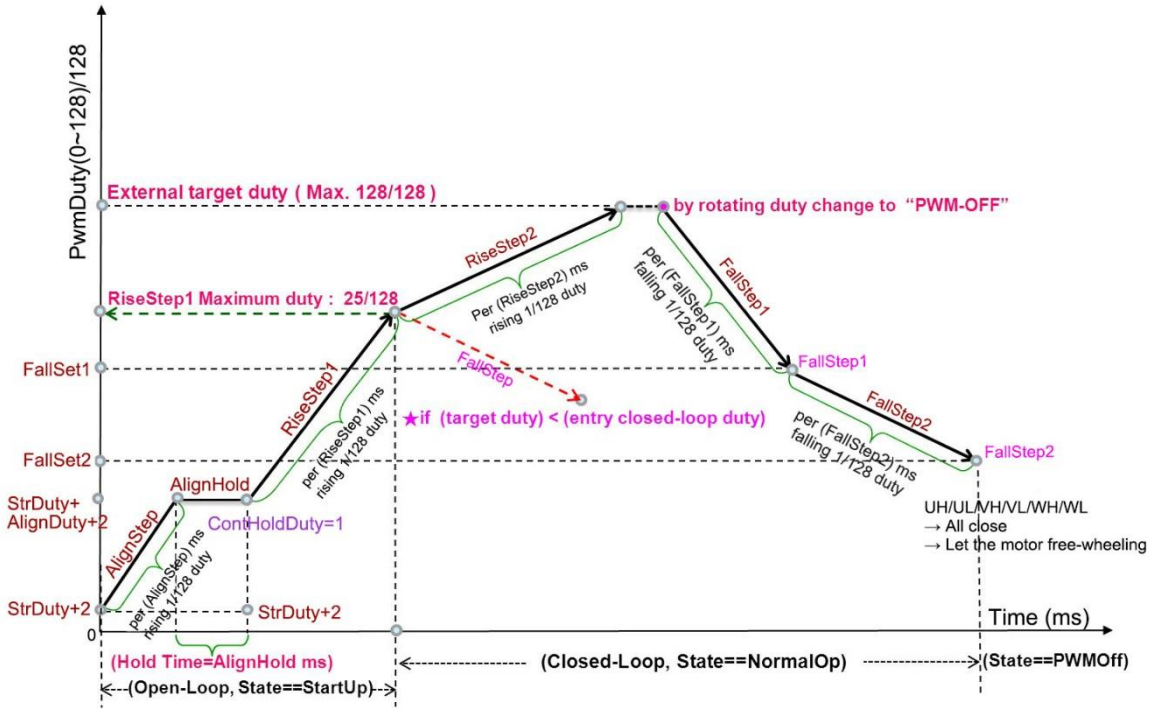
For example, in one application the required motor operation range from AC 80 V to AC 140 V.

1. Change AC value to DC value by multiplying by 1.414. Sum the upper and lower limit values and divide by 4: (80 + 140)*1.414/4 = 77.77.
2. The lower detection value, OVP_{VTL} = 80*1.414/77.77 = 1.454. The upper detection value, OVP_{VTH} = 140*1.414/77.77 = 2.545. From these two values, refer to the corresponding values in the table above to select the appropriate codes. In this example, the lower limit code is 3 and the upper limit code is 4.
3. Finally, the values for resistors, R1 and R2 (shown in the Application Circuit above), may be selected. If R2 is 40 kΩ, R1 is calculated to 3071 kΩ. R1 may be chosen to be 3000 kΩ.

PARAMETERS SETTING

In PT2502, voltage thresholds for the over temperature, over current protection, and zero-crossing signal filter functions are set by external resistors and capacitors. The other, such as startup process, acceleration and deceleration time, and voltage lag compensation parameters, are adjustable in real time and are written to internal OTP (One Time Programmable) memory thru I²C. A voltage of +7.5V needs to be applied to the VPP pin when writing to OTP memory.

Below is a diagram illustrating some parameters of the PT2502. For detailed parameter descriptions and adjustments, please refer to the PT2502_UI_Application_Note file.



PWM or DC input for speed control

The PT2502 offers an external DC or PWM control input to the VSP pin to adjust the motor speed. With PWM input, the high voltage potential needs to be greater than 3.5V and the low potential to be less than 0.3V. The recommended PWM frequency is between 15KHz – 25KHz.

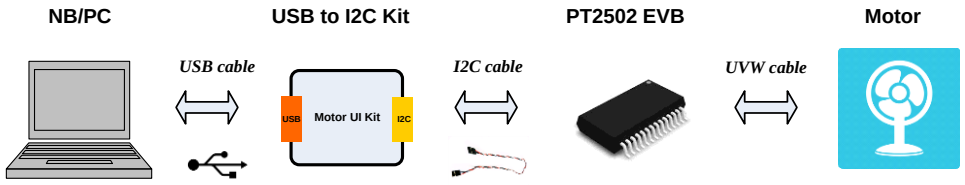
With an analog DC input, the voltage control ranges should be between 0.6V to 3.3V. When the VSP pin is floating, internal pull-HIGH logic will set the motor to run at full speed at 100% duty cycle. When using an external MCU to control the PT2502, FG can be used to obtain speed information to adjust speed.
In addition, PT2502 can accept input PWM duty command thru I2C and VSP pin is set to 0.3V or less.

FORWARD AND REVERSE SETTING

PT2502 may be set to forward or reverse mode via the FR pin and can be controlled through I²C. If the FR mode is changed, the motor will stop automatically and then rotate in the opposite direction.

I²C INTERFACE

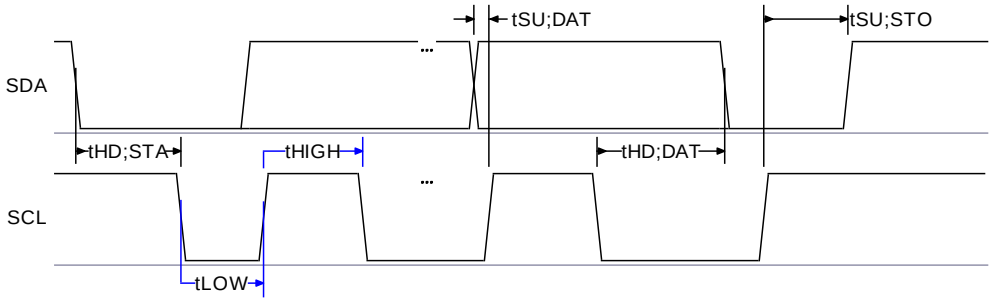
PT2502 may be controlled via I2C to set parameters or to write to OTP memory. The parameters are adjusted by I²C communication thru NB/PC USB and the schematic is shown below.



Using I2C is to adjust the parameters of the IC registers does not affect OTP memory and there is no limit to the number of times that the parameters of the IC registers may be changed. The adjusted parameters may be saved electronically or written into OTP memory through UI software. Please note that adjusting the register values of the IC thru the UI software does not write those parameters into the OTP memory. Hence, once the IC is powered-off and powered back on again, the IC register values will be reset and will no longer be the same as the parameter values shown in the UI software. There are three cases:

1. When OTP bank0 and bank1 are blank, the default register values will be loaded.
2. When OTP bank0 have values and bank1 is blank, the register values of bank0 will be loaded.
3. When OTP bank0 and bank1 both have values, the register values of bank1 will be loaded.

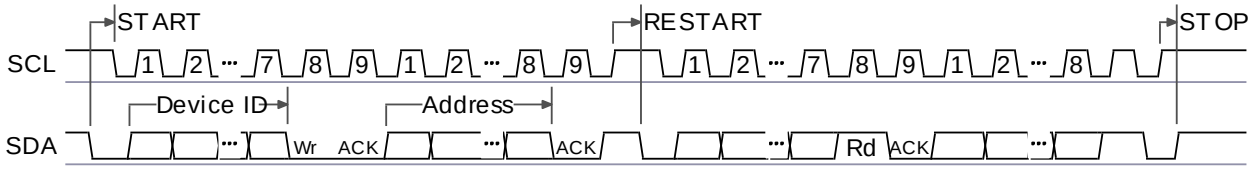
I²C CLOCK SPECIFICATIONS



Parameter	Symbol	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SCL}		0	50	KHz
Hold time START condition	$t_{HD;STA}$		4		μS
LOW period of the SCL clock	t_{LOW}		4.7		μS
HIGH period of the SCL clock	t_{HIGH}		4.0		μS
Data setup time	$t_{SU;DAT}$		250		nS
Data hold time	$t_{HD;DAT}$		5.0		μS
Setup time for STOP condition	$t_{SU;STO}$		4.0		μS

I²C DATA WRITE TIMING DIAGRAM

I²C DATA READ TIMING DIAGRAM



I²C READ / WRITE CONTROL

Read/Write Command Table

Register Map (Address: h00 – h04):

Bit								Address	Default
7	6	5	4	3	2	1	0	Hex	Hex
					PWMS_EN	FWRS1_EN	FWRS0	0	0x00
PWM_I2C								1	0x00
FG_I2C[7:0]								2	0x00
				FG_I2C[11:8]				3	0x00
Mstate[2:0]			RD	TSD	OVP	OCP		4	0x40

Address (Hex)	Bits	Register	Description	Default (Hex)	(R/W)
0x00	Bit[7:3]	Reserved		0x00	
	Bit[2]	PWMS_EN	1: select PWM duty cycle via I²C (PWM_I²C[7:0]) 0: select PWM duty cycle via external VSP input		W
	Bit[1]	FWRS1_EN	1: forward/reverse control by I²C 0: forward/reverse control via external FWR input pin		W
	Bit[0]	FWRS0	Forward/reverse control 1: forward (default) 0: reverse		W
0x01	Bit[7:0]	PWM_I2C[7:0]	PWM duty cycle select via I²C	0x00	W
0x02	Bit[7:0]	FG_I2C[7:0]	First byte of FG_I²C frequency count (read via I²C)	0x00	R
0x03	Bit[3:0]	FG_I2C[11:8]	4 MSBs of FG_I²C frequency count	0x00	R
0x04	Bit[7:5]	Mstate[2:0]	Motor System State : [000] : Start-Up State [001] : Normal Operation State [010] : PWM-Off State [011] : TSD or OVP State [100] : Lock-On State [101] : Dead-Lock State	0x40	R
	Bit[4]	RD	1: Into the Protection State 0: Normal		R
	Bit[3]	TSD	1: Over Temperature Protection 0: Normal		R
	Bit[2]	OVP	1: Over Voltage Protection 0: Normal		R
	Bit[1]	OCP	1: Over Current Protection 0: Normal		R
	Bit[0]	Reserved	-		-

I²C CONTROL PARAMETER

COMMON I2C CONTROL PARAMETERS:
Register Map (Address h21 – h49):

Bit								Address	Default
7	6	5	4	3	2	1	0	Hex	Hex
AlignStep[7:0]								21	0x64
AlignHold[7:0]								22	0x00
RiseStep1[7:0]								23	0x64
RiseStep2[7:0]								24	0x64
DutySel	SmoothSel[1:0]		RiseStep2[8]	RiseStep1[8]	AlignHold[9:8]		AlignStep[8]	25	0xC0
FallStep2[8]	FallStep1[8]	SSWDegree[2:0]			HMOS	ContHoldDuty	OCPSel	26	0x1E
FallStep1[7:0]								27	0x32
FallStep2[7:0]								28	0x64
EnOVP	BrakeEndSet[2:0]			DeadTime[3:0]				29	0x33
FallSet1[7:0]								2A	0x28
FallSet2[7:0]								2B	0x12
OCP BlankWidth[2:0]			ZCTarget[4:0]					2C	0x8F
ZCCntMn[7:0]								2D	0xC8
DigitalFilter[9:8]		ZCCntMn[13:8]						2E	0x00
DigitalFilter[7:0]								2F	0xC0
FilterDelay[7:0]								30	0xB8
FilterDelay[15:8]								31	0x0B
MinDuty[7:0]								32	0x05
StartTimeLimit[3:0]				LockStopTime[3:0]				33	0x55
DeadLock[7:0]								34	0x14
StartStep1[7:0]								35	0xE8
EnSpdCtrl	DeadLock[8]	StartStep1[13:8]						36	0x03
StartStep2[7:0]								37	0x20
ShortNum[1:0]		StartStep2[13:8]						38	0xC3
LowFreqthd[1:0]		WaitTime[9:8]		FrFloating[3:0]				39	0x41
WaitTime[7:0]								3A	0x0D
EnFreqSpd	StrDuty[6:0]							3B	0x03
PreMUXTime[1:0]		AlignDuty[5:0]						3C	0x86
MaxDuty[7:0]								3D	0x80
Div4	BrakeCountSet[6:0]							3E	0x7F
PreCheckTime[7:0]								3F	0x7C
FGLSel[1:0]		PreCheckTime[13:8]						40	0x41
BrakeClkSel[1:0]		**RevBrakeTime[5:0]**						41	0x7C
TrimA[7:0]								42	0x88
TrimB[7:0]								43	0x88
TrimC[7:0]								44	0xF0
ZcTooLong[7:0]								45	0xC8
ZcTooLong[11:8]				EnPreCheck	SpdSel[2:0]			46	0x0B
ZCIgnoreTime[7:0]								47	0x80
HysterSel[1:0]		ZCIgnoreTime[13:8]						48	0x42
				ZCIgnoreSelect	ZCIgnorePhase[2:0]			49	0x01

PARAMETER TABLE (ADDRESS H21 – H49):

Address (Hex)	Bits	Register	Description	Default (Hex)
0x21	Bit[7:0]	AlignStep [7:0]	During the alignment process, the force is gradually increased to avoid excessive swings. The incremental increase is 1/128 PWM duty at every time step (set by the AlignStep parameter).	0x64
0x22	Bit[7:0]	AlignHold [7:0]	Set the Align duration.	0x00
0x23	Bit[7:0]	RiseStep1 [7:0]	Set the accelerating slope before entering sensorless closed-loop control. Incremental step is 1/128 PWM duty for each RiseStep1 time step parameter. The maximum PWM duty is 25/128.	0x64
0x24	Bit[7:0]	RiseStep2 [7:0]	Set the accelerating slope after entering sensorless closed-loop control. Incremental step is 1/128 PWM duty for each RiseStep2 time step parameter. The maximum PWM duty is equal to the external setting speed or protected and clamped PWM duty by internal control.	0x64
0x25	Bit[7]	DutySelect	PWM duty processing selection 1 (default): The internal controller sets the PWM duty cycle change and the approximate rising and falling curves are achieved smoothly. 0: PWM duty cycle change is controlled via external command and is not adjusted by the internal controller.	0xC0
	Bit[6:5]	SmoothSel [1:0]	After the system has entered sensorless control mode, if the jitter of the ZC signal is too large, the system will consider this abnormal and will transition to the stall protection mode. SmoothSel [1:0] sets the ZC jitter range.	
	Bit[4]	RiseStep2 [8]	MSB of RiseStep2 (first byte is 0x24 Bit[7:0])	
	Bit[3]	RiseStep1 [8]	MSB of RiseStep1 (first byte is 0x23 Bit[7:0])	
	Bit[2:1]	AlignHold [9:8]	2 MSBs of AlignHold. The units of AlignHold are milliseconds. The default value is 0.	
	Bit[0]	AlignStep [8]	MSB of AlignStep (first byte is 0x21 Bit[7:0])	
0x26	Bit[7]	FallStep2 [8]	MSB of FallStep2 (first byte is 0x28 Bit[7:0])	0x1E
	Bit[6]	FallStep1 [8]	MSB of Fallstep1 (first byte is 0x27 Bit[7:0])	
	Bit[5:3]	SSWDegree [2:0]	Set the soft-switch angle parameter. The larger the SSWDegree value, the shorter the relative floating time angle will be.	
	Bit[2]	High-Side MOS	High side MOS polarity (default is 1). 1: positive logic 0: negative logic	
	Bit[1]	ContHoldDuty	Select whether to continue to use the old Align setting (strength setting) to start motor after the end of the AlignHold process. The default value is 1. 0: RiseStep1 duty begins from (StrDuty+2). 1: RiseStep1 duty begins from HoldTime duty after the end of the HoldTime process.	
	Bit[0]	OCPSel	PT2502 detects the current thru motors and MOS drives by sensing the voltage across the RF pin resistor. When the voltage exceeds a set value, PT2502 PWM duty will be reduced to avoid over-current or current limit protection will occur. OCPselect selects the reaction time during the periods of reducing PWM duty. The default value is 0. 1: reaction time is 20KHz (0.5us). The fast response setting may generate electrical noise. 0: If the reaction time is one electrical cycle (or ZC period), the reaction becomes slow and there is no electronic noise generated by OCP.	
0x27	Bit[7:0]	FallStep1 [7:0]	Reduce by 1/128 PWM duty for every FallStep1 millisecond in the first speed reducing slope section.	0x32
0x28	Bit[7:0]	FallStep2 [7:0]	Reduce by 1/128 PWM duty for every FallStep2 millisecond in the second speed reducing slope section.	0x64

Address (Hex)	Bits	Register	Description	Default (Hex)
0x29	Bit[7]	EnOVP	Enable OVP function. The default value is 0. 1: Over voltage protection enabled. The system enters Lock-On stage when the detected voltage is over the setting value. 0: Disable the over-voltage protection function.	0x33
	Bit[6:4]	BrakeEndSet [2:0]	Set ZC stop duration according to the stop phenomena for the headwind brake condition. The default value is 3. 0: 7.8ms 1: 15.6ms 2: 23.4ms 3: 31.2ms 4: 39ms 5: 46.8ms 6: 54.6ms 7: 70.2ms Follows the Alignment procedure after the start up.	
	Bit[3:0]	DeadTime [3:0]	The dead time unit is one clock-cycle (0.39μs) and the default value is 3.	
0x2A	Bit[7:0]	FallSet1 [7:0]	Use the second decreased slope from this segment set value connected to the two different slopes of the decreased PWM duty process.	0x28
0x2B	Bit[7:0]	FallSet2[7:0]	PWM duty will be changed to free wheeling duty setting (6 Power MOS off) if the PWMOFF or FWR reverse command is executed in the operation mode.	0x12
0x2C	Bit[7:5]	OCP_BlankWidth [2:0]	PWM switching may generate surge or jitter signals, and the use of the external low pass filter to filter those signals or internal control to avoid this switching time may be required to ensure the reading of the correct the OCP signal. The OCP_BlankWidth parameter specifies this switching signal avoidance time. The time period may be set from 0 to 4 clock-cycles (each clock-cycle is 0.39μs). When the time period is set to 0, the OCP blanking function is disabled. The default value is 4.	0x8F
	Bit[4:0]	ZCTarget [4:0]	Set the number of the read ZC signals to allow the system enter closed loop mode in the startup process. The recommended value is 10–15 and the default value is 15.	
0x2D	Bit[7:0]	ZCCntMn [7:0]	After entering sensorless mode, if ZC signal time is too short, the system determines the ZC is abnormal and the system enters stall protection mode. ZCCntMn is the shortest ZC time period (unit: clock-cycle = 0.39μs).	0xC8
0x2E	Bit[7:6]	DigitalFilter [9:8]	2 MSBs of DigitalFilter (first byte is 0x2F BIT[7:0])	0x00
	Bit[5:0]	ZCCntMn [13:8]	6 MSBs of ZCCntMn (first byte is 0x2D BIT[7:0])	
0x2F	Bit[7:0]	DigitalFilter [7:0]	Set the digital filter (de-glitch) duty width for ZC signal. The unit is one clock-cycle (0.39μs) and the default is 192.	0xC0
0x30	Bit[7:0]	FilterDelay [7:0]	This parameter is a corresponding delay time value caused by "external circuit filter capacitor" and "digital filter." Once the FilterDelay value is optimized, the current waveform is symmetrical, ZC will be more stable, and the controller's efficiency will be the best. The unit is one clock-cycle (0.39μs) and the default value is 3000.	0xB8
0x31	Bit[7:0]	FilterDelay [15:8]		0x0B
0x32	Bit[7:0]	MinDuty [7:0]	The minimum PWM duty is limited to 1/128 duty. The maximum setting value is 64/128. When the input PWM duty is less than MinDuty, this is equivalent to asserting the PWMOFF command. The default value is 5.	0x05
0x33	Bit[7:4]	StartTimeLimit [3:0]	This parameter specifies the time limitation to allow the control system to enter the sensorless loop in the motor startup process. The unit is seconds and the default value is 5. The limitation time range is from 1 to 15 seconds. If the control system does not enter sensorless mode in the limit time set by the parameter, the system will enter the stall protection (lock-on state).	0x55
	Bit[3:0]	LockStopTime [3:0]	Set the waiting time when the system goes into the stall protection state. The unit is seconds and the default value is 5. The waiting time range is from 1 to 15 seconds.	

Address (Hex)	Bits	Register	Description	Default (Hex)
0x34	Bit[7:0]	DeadLock [7:0]	Set how many times the lock-on state happens before the system enters dead lock status. The unit is lock-on count. After lock-on stall happens the number of times specified by DeadLock[7:0], the system will lock the motor. The motor must be un-plugged and then re-plugged to the power supply to release the lock-on state.	0x14
0x35	Bit[7:0]	StartStep1 [7:0]	Set the step change time to force the motor to rotate before the correct ZC happens in the startup process.	0xE8
0x36	Bit[7]	EnSpdCtrl	Enable PWM-Duty Speed Control (default value is 0). This function is active when EnFreqSpd is set to 0 first. 1: The set speed command PWMIN is controlled by duty cycle. 0: When EnFreqSpd is set to 0 first, PWMIN uses the original command.	0x03
	Bit[6]	DeadLock [8]	MSB of DeadLock (first byte is 0x34 Bit[7:0])	
	Bit[5:0]	StartStep1 [13:8]	6 MSBs of StartStep1 (first byte is 0x35 Bit[7:0])	
0x37	Bit[7:0]	StartStep2 [7:0]	Set the step change time for the forcing motor to rotate when there are ZC signals but they do not meet the sensorless closed-loop condition in the startup process.	0x20
0x38	Bit[7:6]	ShortNum [1:0]	Set the number of consecutive ZC signals in a short time to determine whether the motor is in stall state. If the frequency of the ZC signal is too high in a short time, the motor may sometimes be disturbed. 0: disable and do not judge 1: detect ZC signal once 2: detect two consecutive ZC signals 3: detect three consecutive ZC signals	0xC3
	Bit[5:0]	StartStep2 [13:8]	6 MSBs of StartStep2 (first byte is 0x37 Bit[7:0])	
0x39	Bit[7:6]	LowFreqthd	Low Frequency Threshold is the lowest frequency limit for the frequency speed control command input. When the input of control frequency is less than the LowFreqThd value, the Frequency is set to OFF. The default value is 1. 0: 1Hz 1: 5Hz 2: 10Hz 3: 20Hz	0x41
	Bit[5:4]	WaitTime [9:8]	2 MSBs of WaitTime (first byte is 0x3A Bit[7:0])	
	Bit[3:0]	FrFloating [3:0]	Set the buffer time for the system to be read to start the motor in the opposite direction when fans coast down to almost completely stopped and there is no ZC signal change in 0.3 sec after the FWR reverse command and Fallset2 are finished.	
0x3A	Bit[7:0]	WaitTime [7:0]	PT2502 uses square wave control (120 degree control) during start-up stage. This parameter is to set the delay time for the system control to enter the sensorless control of trapezoidal waveform and the purpose is to allow sensorless control to be more stable. The unit per step for WaitTime is 32ms and the default value is 13 (416ms).	0x0D
0x3B	Bit[7]	EnFreqSpd	Enable Frequency Speed Control and the default is 0. This is the highest priority control command. 1: Set input frequency for the speed control command 0: Set speed control or duty cycle command using original PWM Duty command	0x03
	Bit[6:0]	StrDuty [6:0]	Set the initial force in order to overcome the static friction of the motor. In the Alignment and Startup process this parameter will be used. The unit is 1/128 PWM duty and the default value is 3.	
0x3C	Bit[7:6]	PreMUXTime [1:0]	Set the period to check U, V, W-phase in turns and this parameter is used to determine the rotation direction of motor (clockwise or reverse). The default value is 2.	0x86
	Bit[5:0]	AlignDuty [5:0]	Set the maximum align force and the unit is 1/128 PWM duty. The maximum value is 31/128 PWM duty. The default is 6.	

Address (Hex)	Bits	Register	Description	Default (Hex)
0x3D	Bit[7:0]	MaxDuty [7:0]	Limit the maximum duty value of PWMIN and the unit is 1/128 PWM duty. The minimum setting is 64/128. When the input PWM duty is greater than the maxDuty, the output value is maxDuty. The default value is 128.	0x80
0x3E	Bit[7]	Div4	Input Frequency Divided by 4 and the default value is 0. 1: The input frequency is four times the FG output frequency 0: The input frequency is equal to the FG output frequency	0x7F
	Bit[6:0]	BrakeCountSet [6:0]	Set interval (floating state) between the motor brake points. The interval value is BrakeClkSel multiples (1 – 127) and the default value is 127.	
0x3F	Bit[7:0]	PreCheckTime [7:0]	Set maximum time for PreCheck program in the headwind and downwind.	0x7C
0x40	Bit[7:6]	FGLSel [1:0]	Set FG output frequency (units in Hz). The default value is 1. 0: FG output frequency is equal to FG divided by 1: The normal frequency output, i.e. if the motor has 8 poles, the rotational speed is (15 x FG frequency) RPM 2: FG output frequency is equal to 2 x FG 3: FG output frequency is equal to 3 x FG	0x41
	Bit[5:0]	PreCheckTime [13:8]	6 MSBs of PreCheckTime (first byte is 0x3F Bit[7:0])	
0x41	Bit[7:6]	BrakeClkSel [1:0]	When the system detects headwind condition, PT2502 will first brake and re-start. The braking method is by “pumping,” where each successive braking period is longer than the previous one, e.g. the first braking period is 1ms, the second is 2ms, the third time is 3ms, and so on until the motor stops. BrakeClKSel is set to the braking period unit time. The default value is 1 (500μs). 0: 100μs 1: 500μs 2: 1ms 3: 2ms	0x7C
	Bit[5:0]	Reserved	-	
0x42	Bit[7:0]	Reserved	-	0x88
0x43	Bit[7:0]	Reserved	-	0x88
0x44	Bit[7:0]	Reserved	-	0xF0
0x45	Bit[7:0]	ZcTooLong [7:0]	The system enters the stall protection mode if the ZC signal is too long and system has determined that the motor is not operating normally after the system has entered sensorless control loop. Set the maximum waiting time for ZC signal.	0xC8
0x46	Bit[7:4]	ZcTooLong [11:8]	4 MSBs of ZcTooLong (first byte is 0x45 Bit[7:0])	0x0B
	Bit[3]	EnPreCheck	The default value is 1. 1: Enable headwind/downwind detect program 0: Disable headwind/downwind detect program	
	Bit[2:0]	SpdSel [2:0]	FG frequency selection range in PWM-Duty control speed command (default value is 3). 0: 16Hz 1: 32Hz 2: 64Hz 3: 128Hz 4: 256Hz 5: 512Hz 6: 1024Hz 7: 2048Hz	
0x47	Bit[7:0]	ZCIgnoreTime [7:0]	The parameter is a fixed time value in ST1 and ST2 equations and the unit is one clock-cycle (0.39μs). The default value is 640.	0x80

Address (Hex)	Bits	Register	Description	Default (Hex)
0x48	Bit[7:6]	HysterSel [1:0]	PT2502 provides constant speed control (closed loop speed control) and command inputs may be frequency (also known as Clock), PWM duty, or VSP voltage. These inputs all need the delay hysteresis parameter. For frequency command or PWM-Duty command inputs while under constant speed control, the hysteresis angle selection options are below. The default value is 1. 0: No hysteresis 1: Hysteresis 0.23º 2: Hysteresis 0.47º 3: Hysteresis 0.94º	0x42
	Bit[5:0]	ZCIgnoreTime [13:8]	6 MSBs of the ZCIgnoreTime (first byte is 0x47 Bit[7:0])	
0x49	Bit[7:4]	Reserved		0x01
	Bit[3]	ZCIgnoreSelect	Reading the ZC signal in the interval (ST) when the motor commutation and ZC signal is unstable should be avoided. The time specified by the ST parameter should be changed for different fan speeds or different motors. If the ST time is set to be too short, the ZC judgment may be affected. If the ST time is too long, the ZC detection time may be shortened. PT2502 provides two options to set the ST time and the default value is 0.	
	Bit[2:0]	ZCIgnorePhase [2:0]	This parameter is the selection angle in ST2 equation. The default value is 1 (3.75º). 0: 1.875º 1: 3.75º 2: 7.5º 3: 11.25º 4: 15º 5: 18.75º 6: 20.625º 7: 22.5º	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max.	Unit
VDD supply voltage	V_M	5	28	V
Input pin withstand voltage	-	- 0.3	6	V
Operating temperature	T_A	- 40	+85	°C
Storage temperature	T_{STG}	- 40	+150	°C

ELECTRICAL CHARACTERISTIC

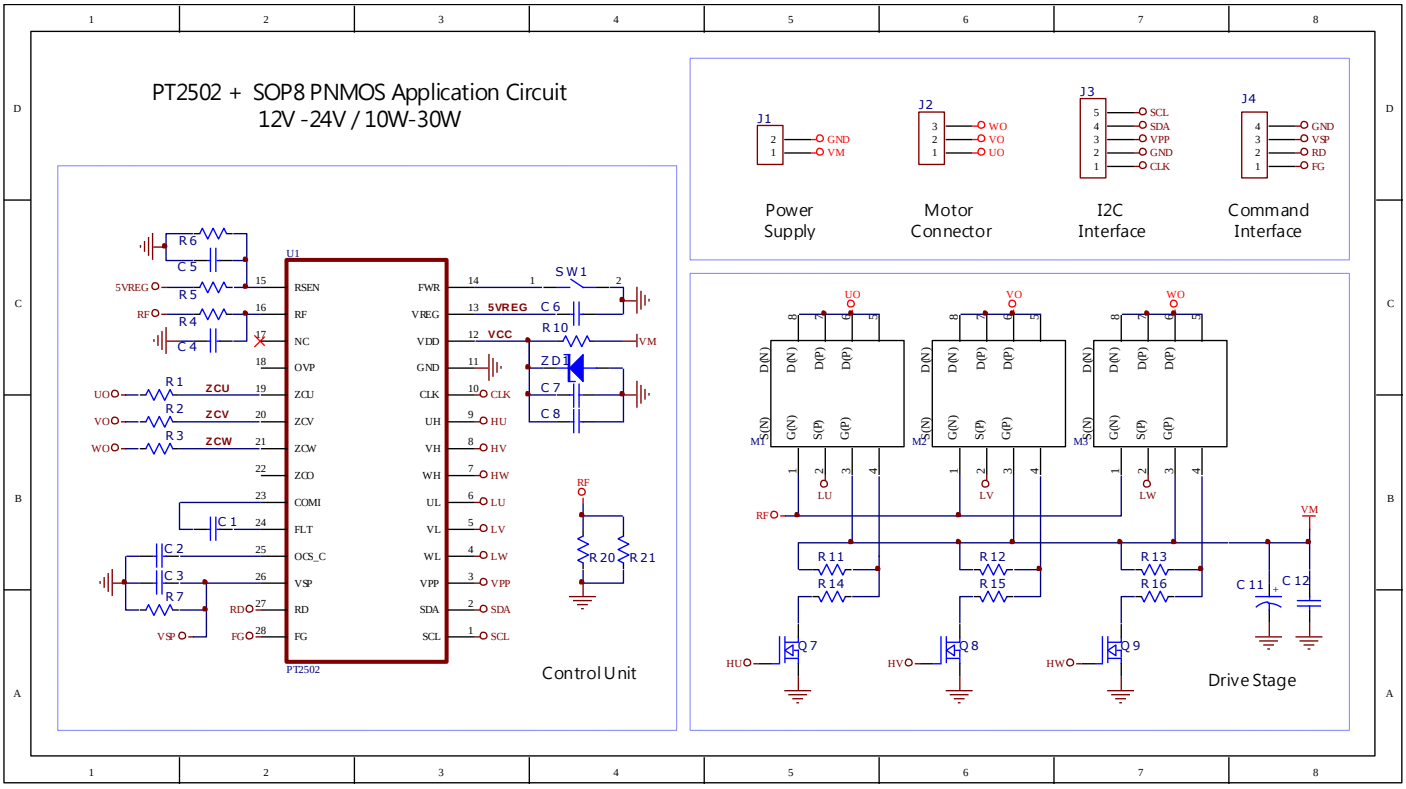
(V_{DD} = 12.0 V, SGND = V_{SS}, T = 27°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
General						
VDD supply voltage	V_{DD}	VDD input	6.0	12	24	V
Power supply current	I_{DD}	VDD = 12V	-	5	-	mA
Regulator output voltage	V_{REG}		4.75	5	5.25	V
Regulator output current	I_{REG}		-	20	-	mA
Pin parameter setting						
Over current protection voltage	V_{OCP}	RF pin	-	0.3	-	V
External oscillator	F_{OSC_1K}	OSC_C=470pF	-	1	-	KHz
External oscillator frequency range	F_{OSC_C}	OSC_C pin	0.1	-	10	KHz
Operation Characteristics						
PWM switching frequency	F_{SW}		-	20	-	KHz
I/O interface						
Logic output high level	V_{OH}	UVWL, UVWH, RD, FG	4.0	4.5	5.5	V
Logic output low level	V_{OL}	UVWL, UVWH, RD, FG	-	0	0.3	V
Logic input pull high current	I_{SOURCE}	FR	-	-	10	μA
RSEN internal pull high resistance	R_{SEN}	RSEN pin, Connect to V_{REG}	-	47	-	KΩ
VSP DC for control range	VSP_{DC}	DC input (VSP pin)	0.3		3.0	V
VSP input high level for PWM	VSP_H	PWM input (VSP pin)	3.3	-	-	V
VSP input low level for PWM	VSP_L	PWM input (VSP pin)	-	-	0.3	V
VSP input frequency range for PWM	VSP_F	PWM input (VSP pin)	15	-	25	KHz
Parameter setting						
Over temperature protection trigger voltage	V_{OTP}	RSEN pin	-	0.6	-	V
Over temperature protection release voltage	V_{REL}	RSEN pin	-	1.2	-	V
Over voltage protection HIGH voltage level*	OVP_{VTH}	OVP pin	-	3.0	-	V
Over voltage protection LOW voltage level*	OVP_{VTL}	OVP pin	-	1.125	-	V

*OVP_{VTH}, OVP_{VTL} are adjustable via I^2C interface. Parameter setting details are described in the *Over Voltage Protection* section.

APPLICATION EXAMPLES

12V-24V / 10W-30W

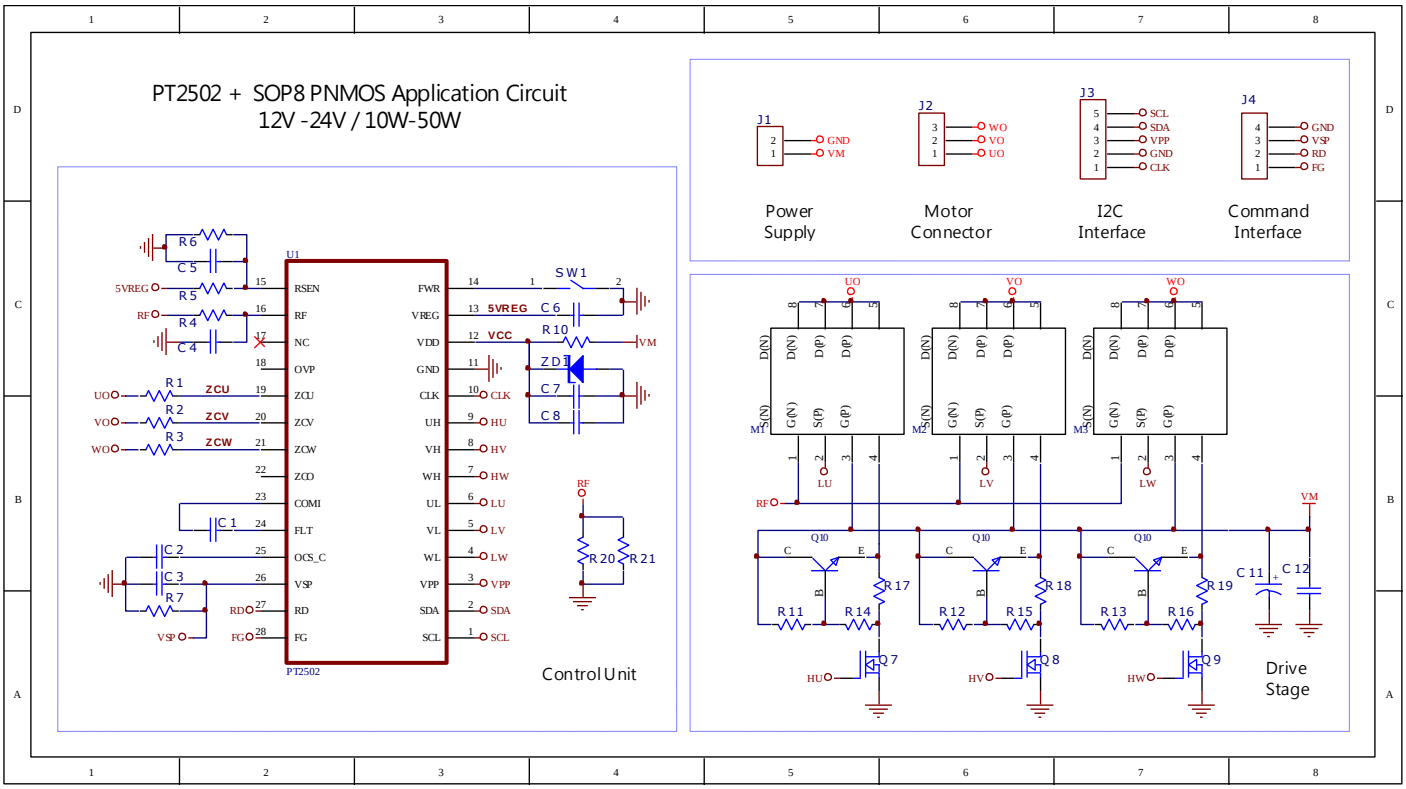


BOM of PT2502 + SOP8 PNMOS for 24V

Component	Size	Value	Note
U1	SSOP28_150	PT2502	
M1, M2, M3	SOP8	PNMOS	
Q7, Q8, Q9	SOT23	NMOS(2N7002)	
ZD1	D1206	ZD15V	
C1	0805	100pF – 10nF	
C2	0805	1nF	
C3, C4, C5	0805	1nF – 100nF	
C6	0805	1μF	
C7	0805	100nF / 25V	
C8	1206	1μF / 25V	
C10	1206	10μF / 25V (NC)	
C11	DIP	100μF / 25V	

Component	Size	Value	Note
R1, R2, R3	0805	33K – 68K	
R4	0805	10K	
R5	0805	100K	
R6	0805	NTC (TBD)	
R7	0805	100K	
R10	0805	100R – 2.2K	
R11, R12, R13	0805	390	
R14, R15, R16	0805	390	
R20, R21	1812	0.22	

12V-24V / 20W-50W

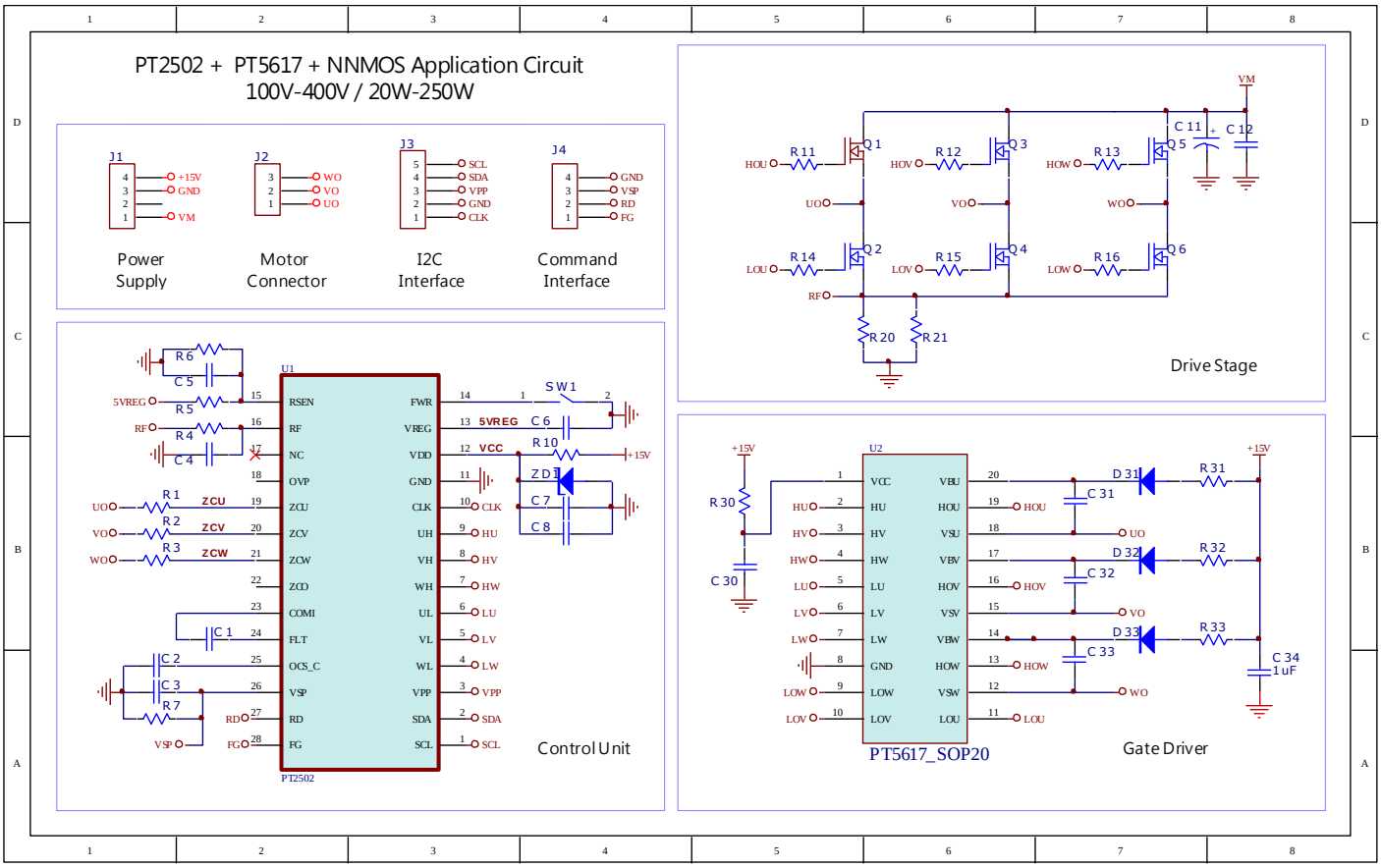


BOM of PT2502 + PMOS & NMOS for 24V

Component	Size	Value	Note
U1	SSOP28_150	PT2502	
Q1, Q3, Q5	TO252	PMOS	
Q2, Q4, Q6	TO252	NMOS	
Q7, Q8, Q9	SOT23	NMOS(2N7002)	
Q10, Q11, Q12	SOT23	NPN(3904)	
ZD1	D1206	ZD15V	
C1	0805	100pF – 10nF	
C2	0805	1nF	
C3, C4, C5	0805	1nF – 100nF	
C6	0805	1μF	
C7	0805	100nF / 25V	
C8	1206	1μF / 25V	
C10	1206	10μF / 25V (NC)	
C11	DIP	100μF / 25V	

Component	Size	Value	Note
R1, R2, R3	0805	33K – 68K	
R4	0805	10K	
R5	0805	100K	
R6	0805	NTC (TBD)	
R7	0805	100K	
R10	0805	100R – 2.2K	
R11, R12, R13	0805	10K	
R14, R15, R16	0805	10K	
R17, R18, R19	0805	1K	
R20, R21	1812	0.22	

100V-400V / 20W-250W



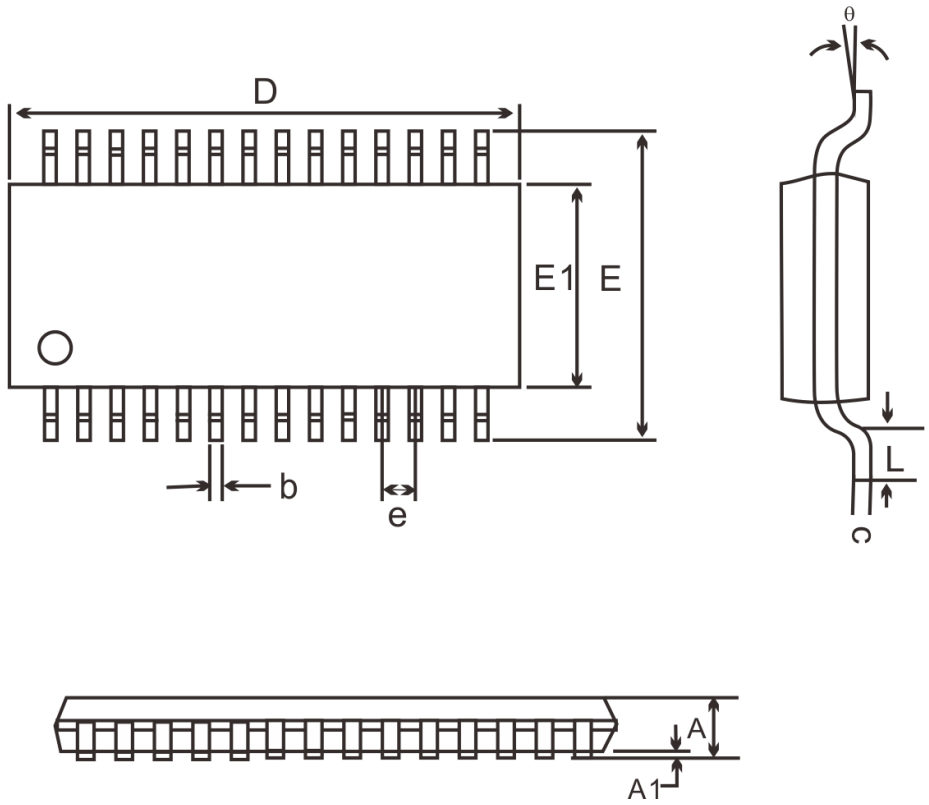
BOM of PT2502 + PT5617 + NMOS for 400V

Component	Size	Value	Note
U1	SSOP28_150	PT2502	
Q1 ~ Q6	TO252	NMOS/600V	
D31, D32, D33	1206	DHE1J	
ZD1	D1206	ZD15V	
C1	0805	100pF – 10nF	
C2	0805	1nF	
C3, C4, C5	0805	1nF – 100nF	
C6	0805	1μF	
C7	0805	100nF / 25V	
C8	1206	1μF / 25V	
C10	1206	10μF / 25V (NC)	
C11	DIP	100μF / 25V	
C30	1206	1μF / 25V	

Component	Size	Value	Note
C31, C32, C33	1206	2.2μF / 25V	
C34	1206	1μF / 25V	
R1, R2, R3	0805	33K – 68K	
R4	0805	10K	
R5	0805	100K	
R6	0805	NTC (TBD)	
R7	0805	100K	
R10	0805	100R – 2.2K	
R11 ~ R16	0805	100	
R20, R21	1812	2	
R30	0805	100	
R31, R32, R33	0805	100	

PACKAGE INFORMATION

28 Pins, SSOP, 150MIL



Symbol	Min.	Nom.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
b	0.20	-	0.30
c	0.10	-	0.25
D	9.80	9.90	10.00
e	0.635 BSC		
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
L	0.40	-	1.27
θ	0º	-	8º

Notes:
1. Refer to JEDEC MO-137 AF
2. Unit: mm

IMPORTANT NOTICE

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