HARRIS Semiconductor

RFP2N08, RFP2N10

2A, 80V and 100V, 1.05 Ohm, N-Channel Power MOSFETs

July 1998

Features

- **2A, 80V and 100V**
- **$r_{DS(ON)}$ 1.05Ω**
- **SOA is Power Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Majority Carrier Device**
- **Related Literature**
  - **TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”**

Description

These are N-channel enhancement mode silicon gate power field effect transistors designed for applications such as switching regulators, switching converters. motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

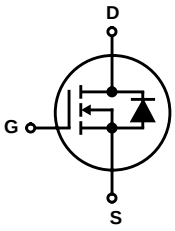
Formerly developmental type TA09282.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFP2N08	TO-220AB	RFP2N08
RFP2N10	TO-220AB	RFP2N10

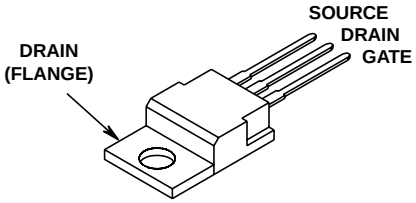
NOTE: When ordering, use entire part number.

Symbol



Packaging

JEDEC TO-220AB



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2883.1**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFP2N08	RFP2N10	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	80	100	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1)	V_{DGR}	80	100	V
Continuous Drain Current	I_D	2	2	A
Pulsed Drain Current (Note 3)	I_{DM}	5	5	A
Gate to Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation	P_D	25	25	W
Linear Derating Factor		0.2	0.2	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering				
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	ID = 250μA, VGS = 0				
RFP2N10			100	-	-	V
RFP2N08			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 8)	2	-	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $T_C = 25^oC$	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, $T_C = 125^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 2A, V_{GS} = 10V (Figures 6, 7)	-	-	1.05	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 2A, V_{GS} = 10V	-	-	2.1	V
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx$ 1A, V_{DD} = 50V, R_G = 50Ω, R_L = 25Ω, V_{GS} = 10V (Figures 10, 11, 12)	-	17	25	ns
Rise Time	t_r		-	30	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	30	45	ns
Fall Time	t_f		-	17	25	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f =1MHz (Figure 9)	-	-	200	pF
Output Capacitance	C_{OSS}		-	-	80	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	25	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	5	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 2A	-		1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 50A/μs	-	100	-	ns

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless otherwise Specified

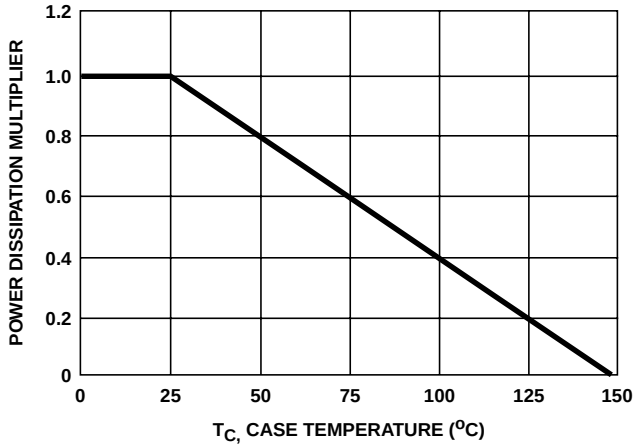


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

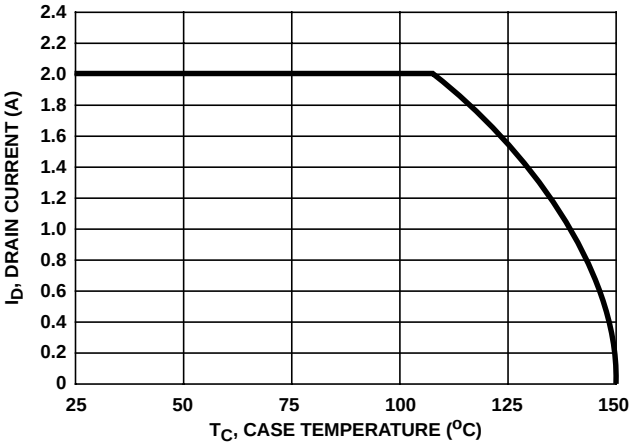


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

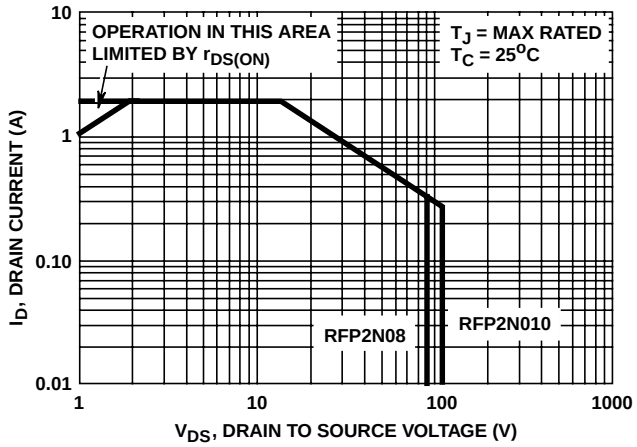


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

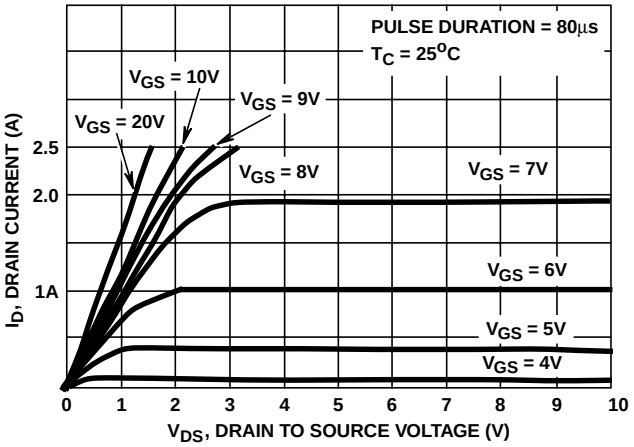


FIGURE 4. SATURATION CHARACTERISTICS

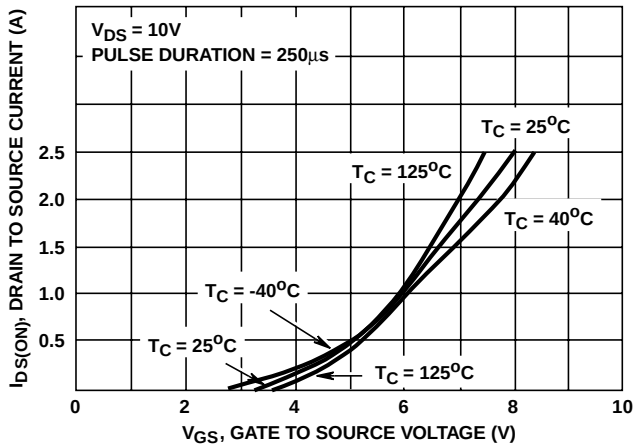


FIGURE 5. TRANSER CHARACTERISTICS

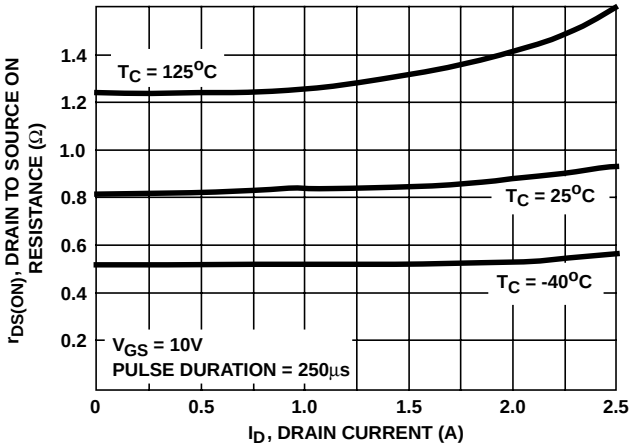


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless otherwise Specified (Continued)

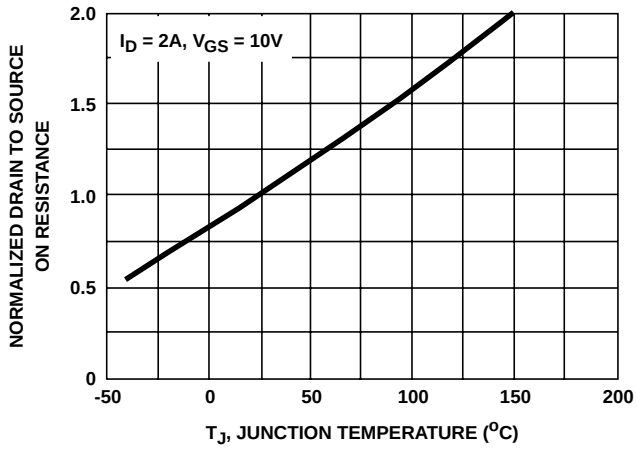


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

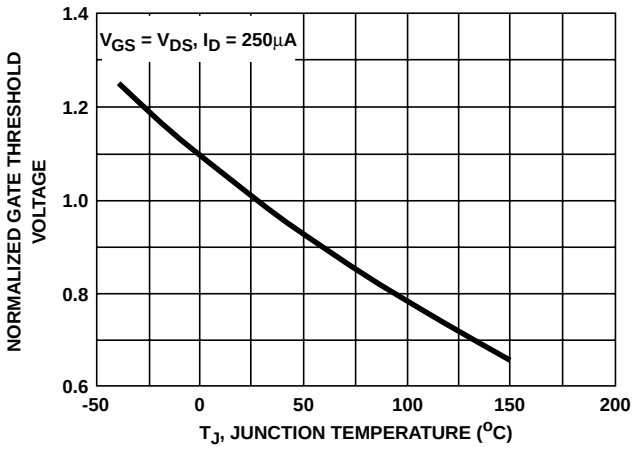


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

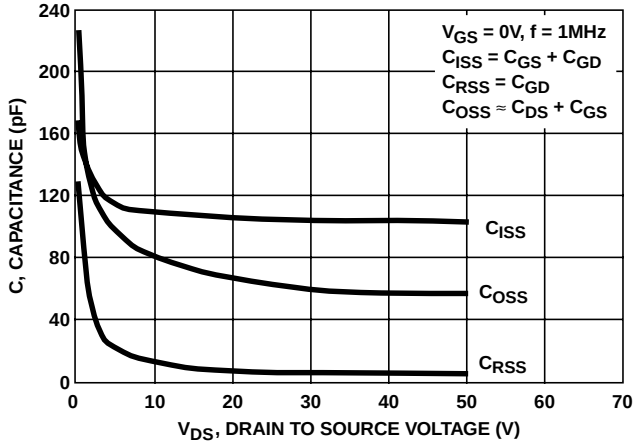
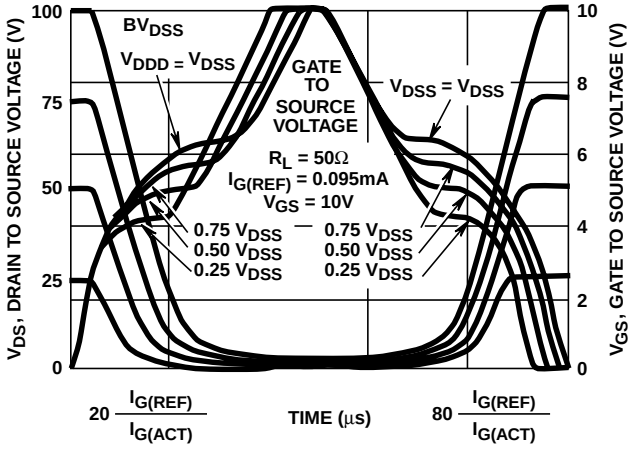


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

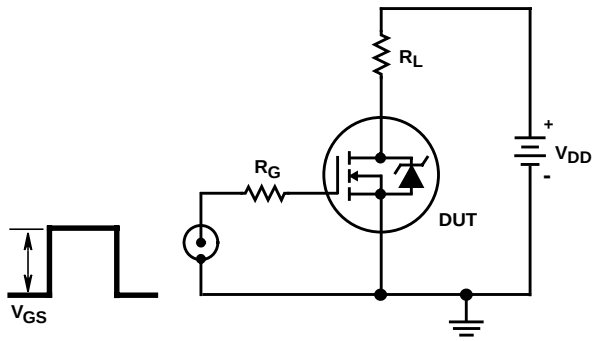


FIGURE 11. SWITCHING TIME TEST CIRCUIT

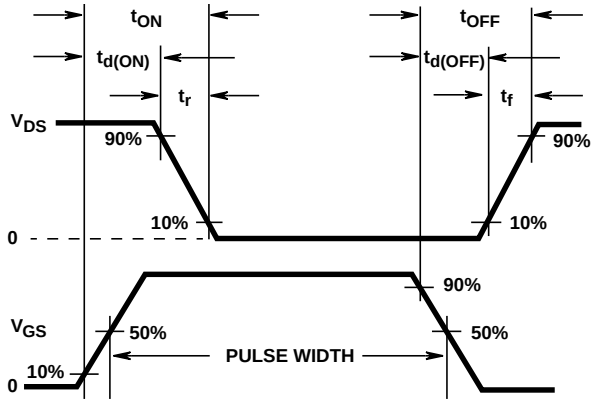


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS