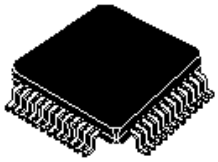
STB5610

GPS RF FRONT-END IC

PRELIMINARY DATA

- ONE CHIP SYSTEM TO INTERFACE GPS ANTENNA TO GPS MICRO CONTROLLER
- ABLE TO SUPPORT ACTIVE AND PASSIVE ANTENNA
- MINIMUM EXTERNAL COMPONENTS
- COMPATIBLE WITH GPS L1 SPS SIGNAL AND GALILEO FREQUENCIES
- CMOS OUTPUT LEVELS
- 2.7 V .. 3.6 V SUPPLY VOLTAGE
- EMBEDDED LOW PHASE NOISE PLL
- ACTIVE ANTENNA SENSOR
- SMART CHIP ENABLE FUNCTION FOR POWER CONSUMPTION OPTIMIZATION
- ESD PROTECTED



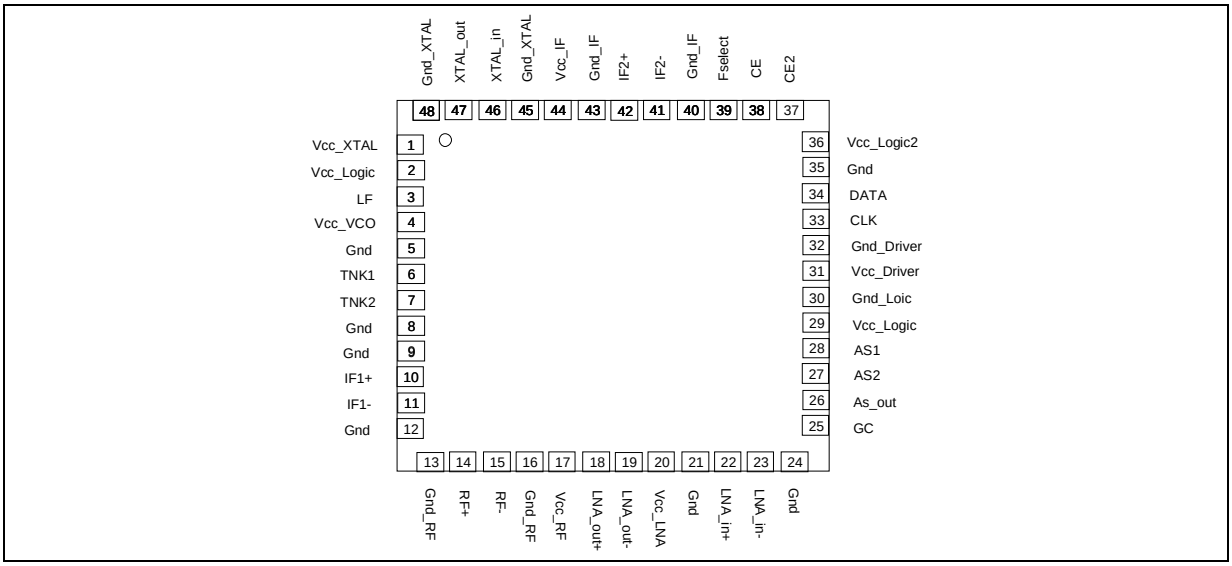
TQFP48

ORDER CODE	BRANDING
STB5610	STB5610

DESCRIPTION

The STB5610, using ST Microelectronics RF Bipolar technology, implements a Global Positioning System RF front-end. The chip provides down conversion from the 1575.42 MHz GPS (L1) signal to 4.092 MHz Output signal. The integrated PLL with on-chip reference oscillator uses a low cost 16.368 MHz crystal. No TCXO is required.

PIN CONNECTION



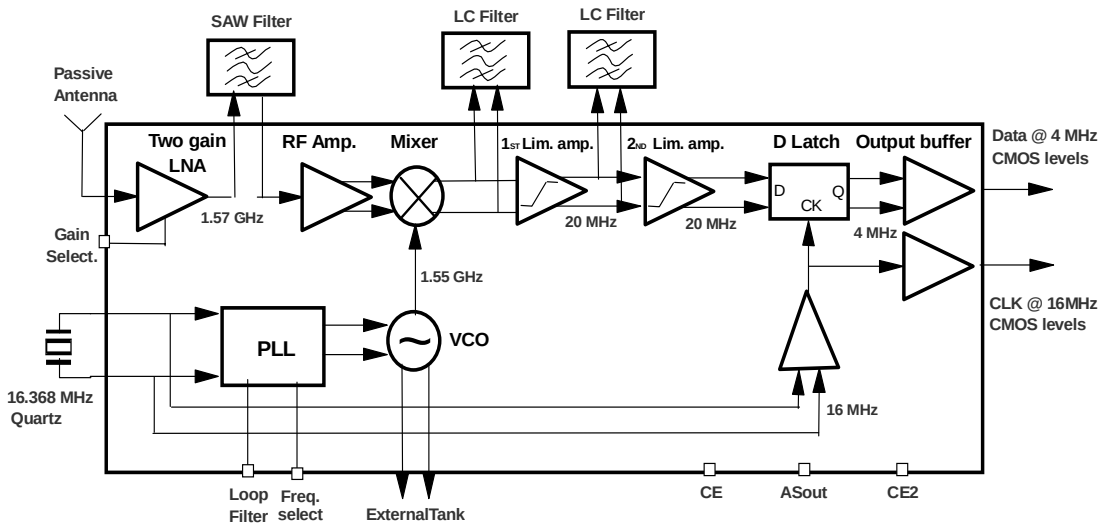
PIN CONFIGURATION

PIN	Symbol	Typ. DC Bias	Description	External Circuit
1	Vcc_XTAL		Power supply	
2	Vcc_Logic		Power supply	
3	LF		Loop filter	
4	Vcc_VCO		Power supply	
5	Gnd		Ground	
6	TNK1		Tank Input	
7	TNK2		Tank Input	
8	Gnd		Ground	
9	Gnd		Ground	
10	IF1+		Mixer Output	
11	IF1-		Mixer Output	
12	Gnd		Ground	
13	Gnd_RF		Ground	
14	RF+		RF amp. input	
15	RF-		RF amp. input	
16	Gnd_RF		Ground	
17	Vcc_ RF		Power supply	
18	LNA_Out+		LNA output	
19	LNA_Out-		LNA output	
20	Vcc_LNA		Power supply	
21	Gnd_LNA		Ground	
22	LNA_in+		LNA input	
23	LNA_in-		LNA input	
24	Gnd_LNA		Ground	

PIN CONFIGURATION

PIN	Symbol	Typ. DC Bias	Description	External Circuit
25	GC		LNA Gain control	
26	AS_Out		Antenna sensor output	
27	AS2		Antenna sensor input	
28	AS1		Vcc Antenna Supply	
29	Vcc_Logic		Power supply	
30	Gnd_Logic		Ground	
31	Vcc_Driver		Supply Voltage	
32	Gnd_Driver		Ground	
33	CLK		Clock	
34	DATA		Data	
35	Gnd		Ground	
36	Vcc_Logic2		Supply Voltage	
37	CE2		Chip Enable (no data)	
38	CE		Chip Enable	
39	Fselect		Frequency Selector	
40	Gnd_IF		Ground	
41	IF2-		Lim. Amp. Output	
42	IF2+		Lim. Amp. Output	
43	Gnd_IF		Ground	
44	Vcc_IF		Supply Voltage	
45	Gnd_XTAL		Ground	
46	XTAL_in		Crystal Input	
47	XTAL_out		Crystal Output	
48	Gnd_XTAL		Ground	

BLOCK DIAGRAM (GPS L1)



FUNCTIONAL DESCRIPTION

LNA section

The RF input signal is amplified by two gain levels LNA. Using gain control pin the LNA gain is set to 19 dB to support passive antenna or 10 dB to support active antenna. The LNA output signal is filtered by 1575.42 MHz SAW filter.

RF Amplifier plus mixer section

The 1575.42 MHz input signal, amplified by RF amp., is mixed with the VCO signal to generate a differential 20.46MHz IF signal

IF section

Two LC filters at mixer output and at first limiting output are used to suppress undesirable signals and mixer products. The second stage limiting amplifier is connected to a D-Type latch clocked by 16.368MHz crystal oscillator signal. The effect of sampling the 20.46MHz signal at 16.368MHz is to create sub-sampling alias at 4.092MHz. This is fed to the output level converter.

Output section

The output buffers perform level translation from the internal ECL levels to CMOS output levels referred to ground. The Data signal changes during the clock signal negative edge.

Power supplies

The STB5610, has been designed to support from 2.7 V to 3.6 V supply voltage.

VCO and PLL

Using external tank the VCO is able to provide very low phase noise signal. Through the freq. selector pin the VCO signal is set at 1554.96 MHz and at 1571.328 MHz. The on-chip reference oscillator uses a low cost 16.368 MHz crystal.

Antenna sensor circuitry

Integrated sensor circuitry is able to evaluate the antenna current consumption; the Asout pin output provides this info externally. Using external sensing resistor of 10 Ohm if the antenna current consumption is inside the range 10mA…40mA (active antennas typical current consumption) the Asout output logic level is High, if the antenna current consumption is outside the above reported range (passive antenna or problem on antenna connection) the Asout output logic level is low.

Chip enable

Using the CE pin it is possible to switch off all the chip (neither data nor clock available).

Using CE2 pin it is possible to disable the analog portion of the chip (no data available) maintaining the digital portion active (Clock available) optimizing the chip current consumption.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
Vcc	Supply voltage	5.9	V
Tj	Junction operating temperature	-40 to 125	^{o}C

THERMAL DATA

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case	TBD	^{o}C/W

ELECTRICAL CHARACTERISTICS (Vcc = 3+/-10%, Tcase= 25 ^{o}C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY						
Vcc	Supply voltage		2.7	3.3	3.6	V
Icc	Supply current			37		mA
AS1	Vcc Antenna Supply		2.7	3.3 / 5	5.5	V
LNA						
Gp	Power gain	Pin GC at GND Pin GC at Vcc		19 10		dB
NF	Noise figure	Pin GC at GND Pin GC at Vcc		3 10		dB
IIP3	Input IP3	Pin GC at GND Pin GC at Vcc		-20 -5		dBm
VSWRin	Voltage Stat. Wave Ratio	Z_L=50Ω			2.1	
RF AMPLIFIER AND MIXER CHAIN						
IIP3	Input IP3			-19		dBm
NF	Noise Figure			5.5		dB
Z_{IN}	Input impedance			50		Ω
Z_{OUT}	Differential output impedance			1.4		KΩ
fRF	Input signal RF			1.575		MHz
G	Voltage Convertion Gain			30		dB
FIRST LIMITING AMPLIFIER						
G	Voltage Gain			60		dB
Z_{OUT}	Differential output impedance			2.4		KΩ

ELECTRICAL CHARACTERISTICS (Vcc = 3+/-10%, Tcase= 25 ^{o}C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SECOND LIMITING AMPLIFIER						
G	Voltage Gain			30		dB
VCO *(GPS LO frequency 1555MHz)*						
VCO	Phase noise	Δf = 1KHz, SSB (10KHz PLL closed loop bandwith)		-60		dBc/Hz
OUTPUT BUFFER *(square wave CMOS level)*						
V_{OH}	High output voltage		Vcc-0.4		Vcc	V
V_{OL}	Low output voltage		0		0+0.4	V
PHASE LOCKED LOOP						
XTAL	Reference crystal			16.368		MHz

INPUT CONTROL PINS TABLE (The logic levels are TTL compatible)

GC Pin (lna gain control pin)

Logic level	Value
Low	Max Gain
High	Min Gain

CE Pin (Total chip enable pin)

Logic level	Value
Low	Switch-off
High	Switch-on

CE2 Pin (Analog portion enable pin)

Logic level	Value
Low	Switch-off
High	Switch-on

FSELECT (Frequencies Selector Pin)

Logic level	Value
Low	GPS frequency
High	Galileo frequency

OUTPUT CONTROL PINS TABLE

The Asout pin output provides information on Antenna current consumption

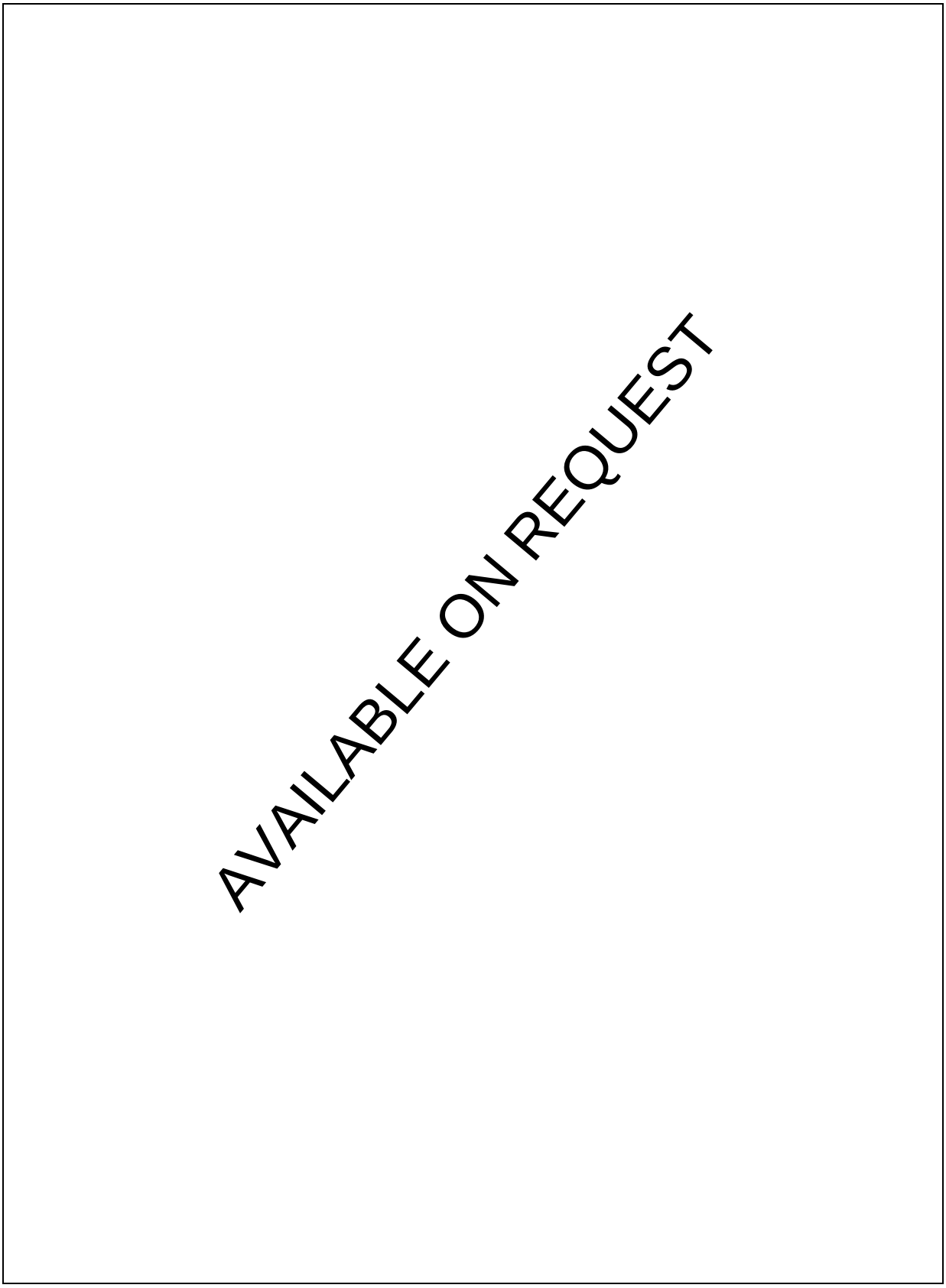
ASout Pin (Antenna sensor pin)*

Logic level	Value
Low**	Iant<10mA Iant.>40mA
High**	10mA<Iant<40mA

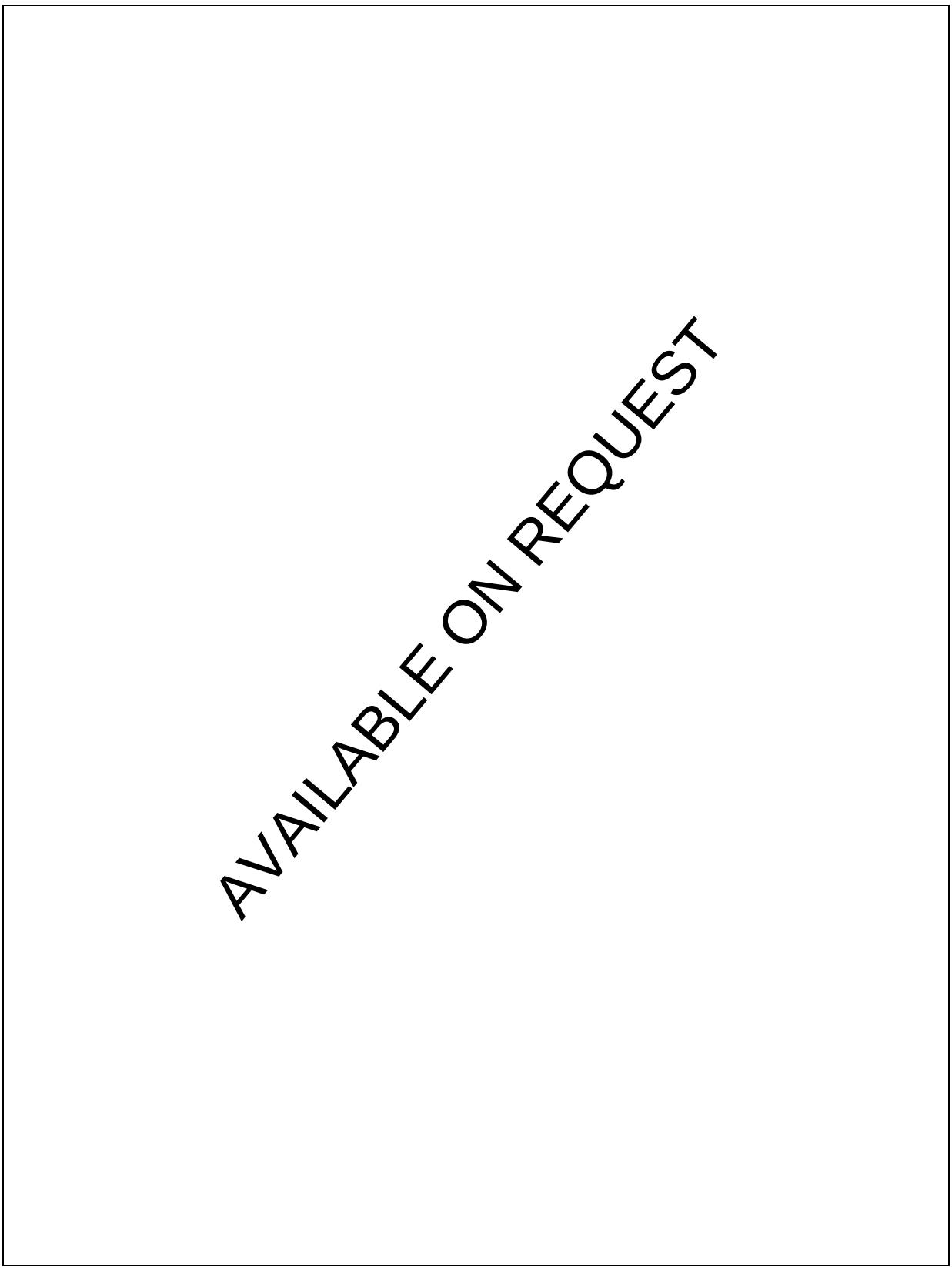
* It is referred to external sensing resistor of 10 OHm
Application requiring higher or lower current threshold should adjust the resistor value appropiately

** The logic levels are referred to STB5610 Supply Voltage

APPLICATION BOARD SCHEMATIC (ACTIVE ANTENNA)



APPLICATION BOARD LAYOUT (ACTIVE ANTENNA)



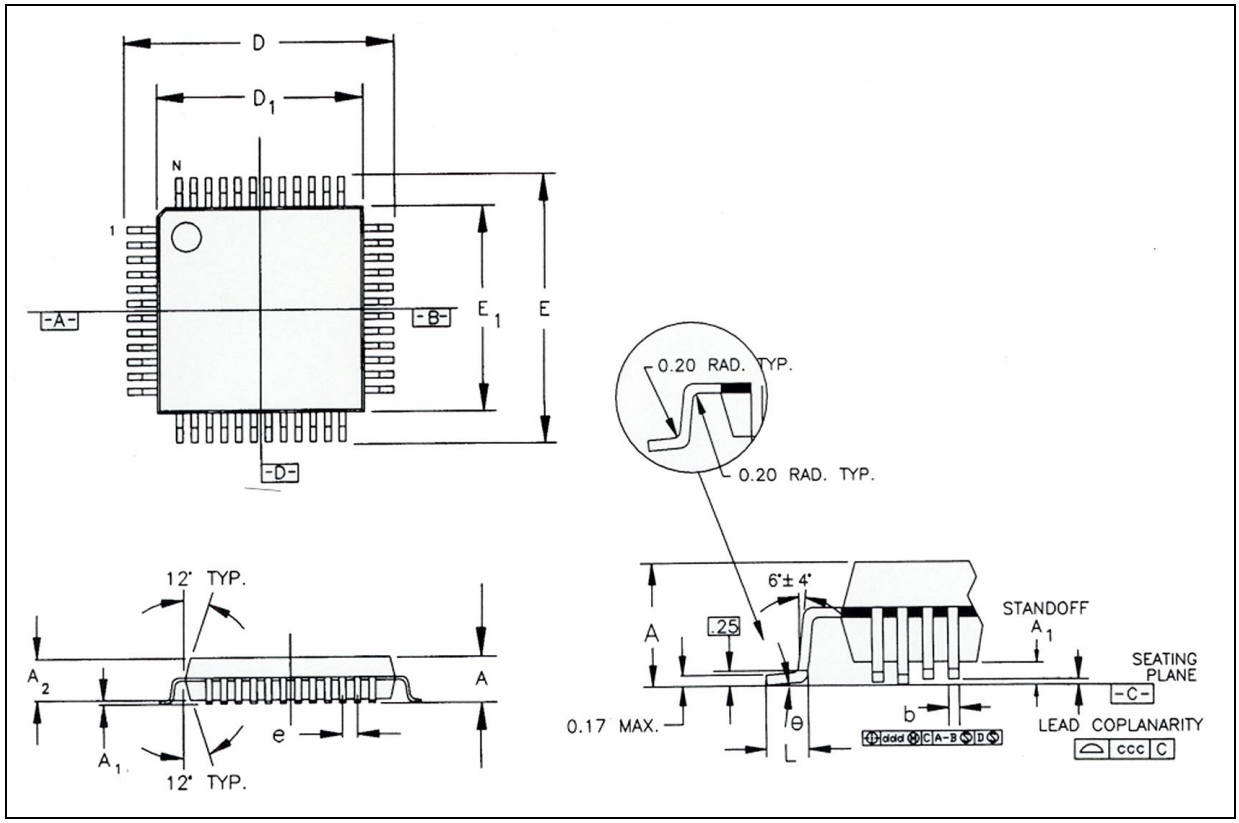
BILL OF MATERIALS

AVAILABLE ON REQUEST

MECHANICAL DATA

DIM.	mm		
	MIN.	TYP.	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
D	8.75	9.00	9.25
D1	6.9	7.00	7.1
E	8.75	9.00	9.25
E1	6.9	7.00	7.1
L	0.5	0.60	0.75
e		0.5	
b	0.17	0.22	0.27
ccc			0.08
ddd			0.08
TETA	0^o		7^o

Note: L is measured at gage plane (at 0.25 above the seating plane)



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