SONY

CXD2044Q

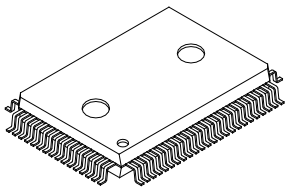
Digital Comb Filter (NTSC/PAL/PAL-M/PAL-N)

For the availability of this product, please contact the sales office.

Description

The CXD2044Q is an adaptive intra-field comb filter compatible with NTSC, PAL, PAL-M and PAL-N systems, and can provide high-precision Y/C separation with a single chip.

80 pin QFP (Plastic)



Features

- Intra-field Y/C separation by adaptive processing
- 8-bit A/D converter (1-channel)
- 8-bit D/A converter (2-channel)
- Four 1H delay lines
- Clock 4fsc

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

• Supply voltage	DV_{DD}	V_{SS} – 0.5 to +7.0	V
	AAVD	V_{SS} – 0.5 to +7.0	V
	ADVD	V_{SS} – 0.5 to +7.0	V
	YV_{DD}	V_{SS} – 0.5 to +7.0	V
	CV_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	DV_{DD}	5.0 ± 0.25	V
	AAVD	5.0 ± 0.25	V
	ADVD	5.0 ± 0.25	V
	YV_{DD}	5.0 ± 0.25	V
	CV_{DD}	5.0 ± 0.25	V
• Analog input	ADIN	1.8	Vp-p
• Operating temperature			
	Topr	–20 to +75	°C

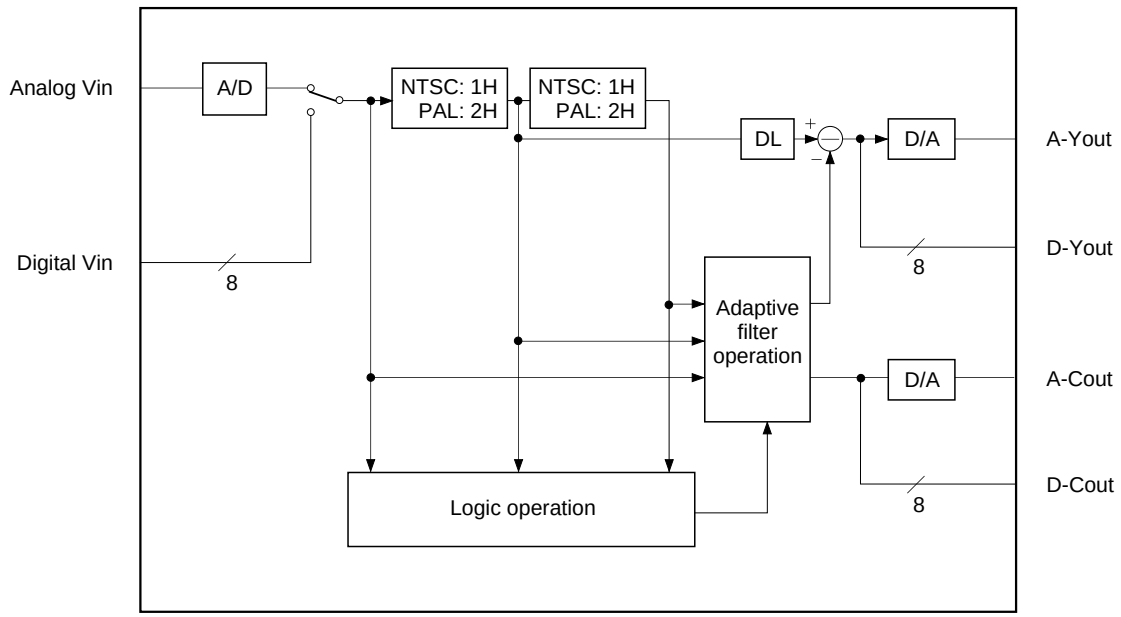
Applications

Y/C separation for color TVs and VCRs

Structure

Silicon gate CMOS IC

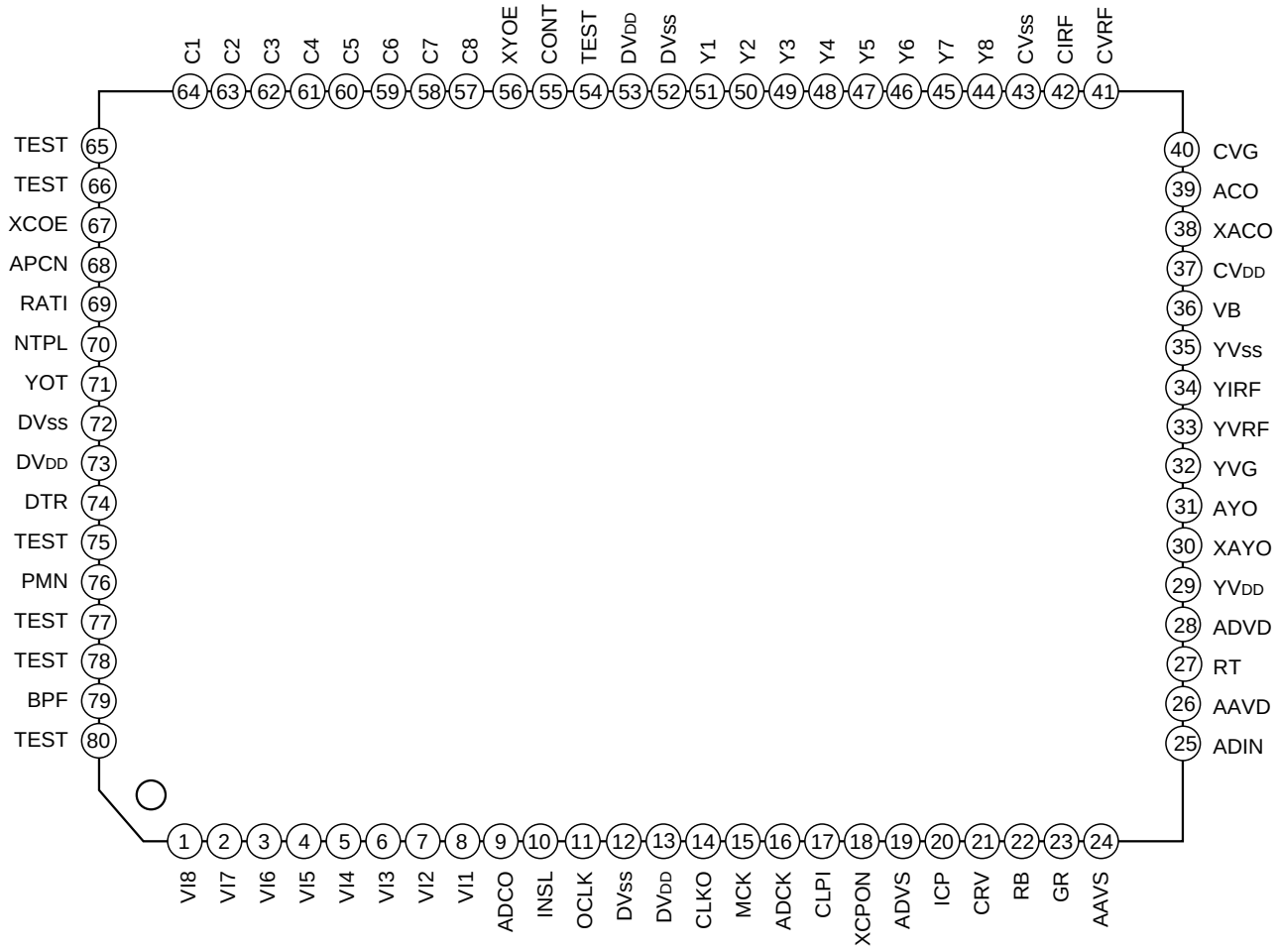
Block Diagram



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E95418-ST

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	VI8	I	Digital input (MSB). Connect to DV_{DD} or DVss when not in use.
2	VI7	I	Digital input. Connect to DV_{DD} or DVss when not in use.
3	VI6	I	Digital input. Connect to DV_{DD} or DVss when not in use.
4	VI5	I	Digital input. Connect to DV_{DD} or DVss when not in use.
5	VI4	I	Digital input. Connect to DV_{DD} or DVss when not in use.
6	VI3	I	Digital input. Connect to DV_{DD} or DVss when not in use.
7	VI2	I	Digital input. Connect to DV_{DD} or DVss when not in use.
8	VI1	I	Digital input (LSB). Connect to DV_{DD} or DVss when not in use.
9	ADCO	I	A/D converter output through mode. High: Video signals taken into the A/D converter (input pin: ADIN) are output without change from the Y output pins as 8-bit digital data with a 3.5 clock delay. Low: Standard mode
10	INSL	I	Input switching. Switches the input data fed to the comb filter. High: Digital input Low: Analog input
11	OCLK	I	Clock amplifier input. Input 0.8Vp-p or more, eliminating the DC components with a capacitor.

Pin No.	Symbol	I/O	Description
12	DV_{SS}	—	Digital ground.
13	DV_{DD}	—	Digital power supply. (5V)
14	CLKO	O	Clock amplifier output.
15	MCK	I	Master clock input. Input the 4fsc clock locked to the color burst. Normally, connect the clock amplifier output (CLKO: Pin 14).
16	ADCK	I	Clock input for the A/D converter. Input the same clock as the master clock (MCK: Pin 15). Normally, connect the clock amplifier output (CLKO: Pin 14).
17	CLPI	I	Clamp pulse input for the A/D converter. Clamps the signal voltage during the low period of the clamp pulse signal. When the clamp function is off, connect to the digital power supply (DV_{DD}).
18	XCPON	I	Clamp setting for the A/D converter. High: Clamp function is set to off, and the normal A/D converter function is only enabled. Low: Clamp function is enabled.
19	ADVS	—	Digital ground for the A/D converter.
20	ICP	I	Clamp control voltage integral pin. Connect a capacitor of approximately 0.01µF. When not using clamp, connect to the analog ground (AAVS).
21	CRV	I	Clamp reference voltage input. Operates to make the analog input voltage equal to the clamp reference voltage during the clamp period. When not using clamp, connect to the analog ground (AAVS).
22	RB	O	Reference voltage (bottom): 0.5V (typ.)
23	GR	—	Guard ring. Connect to the analog ground (AAVS).
24	AAVS	—	Analog ground for the A/D converter.
25	ADIN	I	Comb filter analog input (A/D converter input).
26	AAVD	—	Analog power supply for the A/D converter. (5V)
27	RT	O	Reference voltage (top): 2.6V (typ.)
28	ADVD	—	Digital power supply for the A/D converter. (5V)
29	YV_{DD}	—	Analog power supply for the Y D/A converter. (5V)
30	XAYO	O	AYO inverted current output. Connect to the analog ground (YVss).
31	AYO	O	Analog luminance signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
32	YVG	O	Connect a capacitor of approximately 0.1µF.
33	YVRF	I	Sets the full-scale value of the analog luminance output signal.
34	YIRF	O	Connect a resistor of “16R” (16 times the output resistor “R” of the AYO pin).
35	YVss	—	Analog ground for the Y D/A converter.
36	VB	O	Connect a capacitor of approximately 0.1µF.
37	CV_{DD}	—	Analog power supply for the C D/A converter. (5V)
38	XACO	O	ACO inverted current output. Connect to the analog ground (CVss).

Pin No.	Symbol	I/O	Description
39	ACO	O	Analog chroma signal output. Output can be obtained by connecting a resistor between this pin and the analog ground.
40	CVG	O	Connect a capacitor of approximately 0.1µF.
41	CVRF	I	Sets the full-scale value of the analog chroma output signal.
42	CIRF	O	Connect a resistor of “16R” (16 times the output resistor “R” of the ACO pin).
43	CVss	—	Analog ground for the C D/A converter.
44	Y8	O	Digital luminance signal output (MSB).
45	Y7	O	Digital luminance signal output.
46	Y6	O	Digital luminance signal output.
47	Y5	O	Digital luminance signal output.
48	Y4	O	Digital luminance signal output.
49	Y3	O	Digital luminance signal output.
50	Y2	O	Digital luminance signal output.
51	Y1	O	Digital luminance signal output (LSB).
52	DVss	—	Digital ground.
53	DV_{DD}	—	Digital power supply. (5V)
54	TEST	I	Test. Normally open or fix to “Low”.
55	CONT	I	Normally open or fix to “High”.
56	XYOE	I	Digital luminance signal output control. High: High impedance Low: Standard output However, during PAL-M/N mode (Pins 70 and 76 are both “High”), the digital chroma signal output is also controlled simultaneously. See Table 1.
57	C8	O	Digital chroma signal output (MSB).
58	C7	O	Digital chroma signal output.
59	C6	O	Digital chroma signal output.
60	C5	O	Digital chroma signal output.
61	C4	O	Digital chroma signal output.
62	C3	O	Digital chroma signal output.
63	C2	O	Digital chroma signal output.
64	C1	O	Digital chroma signal output (LSB).
65	TEST	I	Test. Normally open or fix to “Low”.
66	TEST	I	Test. Normally open or fix to “Low”.
67	XCOE	I	Digital chroma signal output control. See Table 1. High: High impedance Low: Standard output
68	APCN	I	Aperture compensation circuit setting. High: Compensates for the aperture-induced frequency response characteristics degradation. Even in through mode (YOT: H), aperture compensation is performed for the Y output. Low: Standard mode

Pin No.	Symbol	I/O	Description
69	RATI	I	Ratio setting. High: PAL/PAL-M/PAL-N: When DTR: H, compulsively fixed to “Low” internally. Low: NTSC
70	NTPL	I	NTSC/PAL/PAL-M/PAL-N mode setting. See Table 1. High: PAL/PAL-M/PAL-N Low: NTSC
71	YOT	I	Y output through mode. High: Outputs the input composite video signal from the Y output. At this time, there is 1H + 15 clock delay from the digital input for NTSC, and 2H + 15 clock delay from the digital input for PAL/PAL-M/PAL-N. For C output, the Y/C separated chroma signal is output. Low: Y/C separation mode
72	DVss	—	Digital ground.
73	DV_{DD}	—	Digital power supply. (5V)
74	DTR	I	PAL/PAL-M/PAL-N: High: Dot interference reduction mode Low: Before dot interference reduction NTSC: Fix to “Low”.
75	TEST	I	Test. Normally fix to “Low”.
76	PMN	I	NTSC/PAL/PAL-M/PAL-N mode selection. See Table 1.
77	TEST	I	Test. Normally fix to “Low”.
78	TEST	I	Test. Normally fix to “Low”.
79	BPF	I	Y/C separation processing mode setting. High: Fixed to BPF separation mode Low: Adaptive processing mode
80	TEST	I	Test. Normally fix to “Low”.

Table 1. NTSC/PAL/PAL-M/PAL-N mode selection

(Numbers in parentheses indicate the Pin No.)

Mode	NTPL (70)	PMN (76)	XCOE (67)*
NTSC	0	0	0
PAL	1	0	0
PAL-M	1	1	0
PAL-N	1	1	1

* Digital Y output enable and digital C output enable are simultaneously controlled by XYOE (Pin 56) during PAL-M/PAL-N mode.

Electrical Characteristics

DC Characteristics

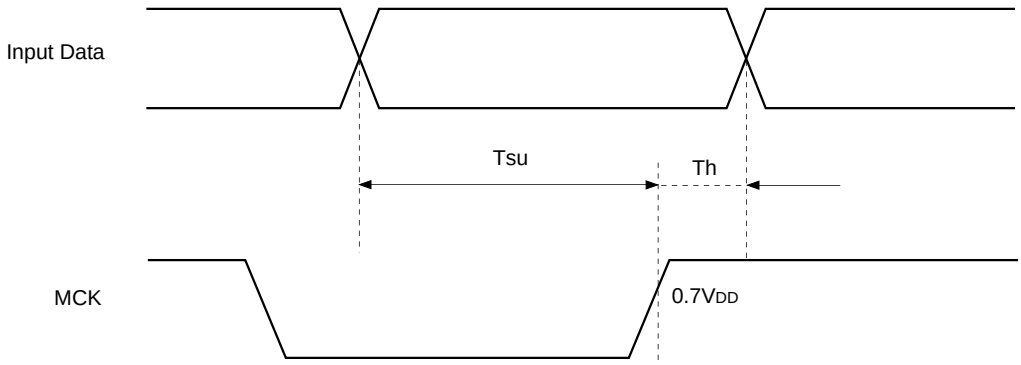
(V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to +75°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V_{DD}	—	4.75	5.0	5.25	V	*1
	AAVD						
	ADVD						
	YV_{DD}						
	CV_{DD}						
Operating temperature	Topr	—	–20		+75	°C	
Input/output voltage	V_I, V_O	—	Vss		V_{DD}	V	*2
Input voltage	V_{IH}	CMOS level input	0.7V_{DD}			V	*3
	V_{IL}				0.3V_{DD}		
Input rise/fall time	tr, tf	—	0		500	ns	*1
Output voltage	V_{OH}	I_{OH} = –2mA	V_{DD}–0.8			V	*4
		I_{OH} = –4mA					*5
	V_{OL}	I_{OL} = 4mA			0.4		*4
		I_{OL} = 8mA					*5
Logical Vth	LVth	—		V_{DD}/2		V	*6
Input voltage	V_{IH}		0.7V_{DD}			V	
	V_{IL}				0.3V_{DD}		
Input amplitude	V_{IN}	fmax = 50MHz sine wave	0.8			Vp-p	
Feedback resistance value	R_{FB}	V_{IN} = Vss or V_{DD}	250k	1M	2.5M	Ω	
Input leak current	I_{IL}, I_{IH}	V_{IN} = V_{SS} or V_{DD}	–10		10	µA	*7
	I_{IH}	V_{IH} = V_{DD}	40	100	240		*8
	I_{IL}	V_{IL} = V_{SS}	–40	–100	–240		*9
Clock amplifier output delay	—	—	3.0	9.0	18.0	ns	*5

*1 All pins
*2 All pins other than *6
*3 All input pins other than *6
*4 All output pins other than *5
*5 CLKO (Pin 14)
*6 OCLK (Pin 11)
*7 All pins other than *8 and *9
*8 Pins 54, 65, 66 and 75 to 80
*9 Pin 55

AC Characteristics

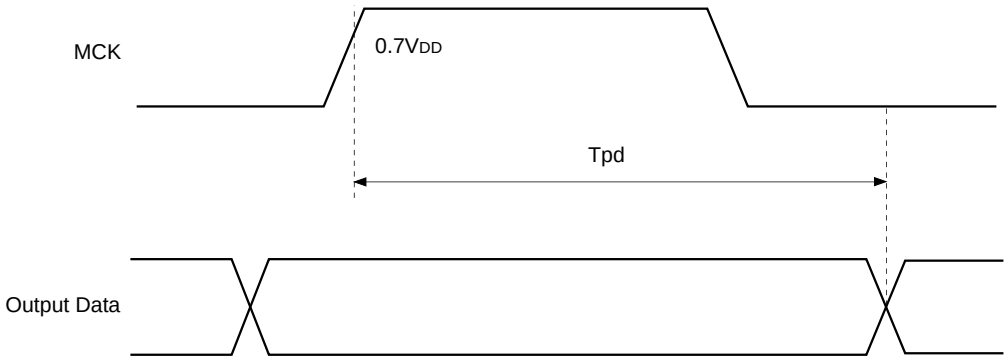
Input Interface Timing



Input Characteristics (V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to +75°C)

Input pin	Pin No.	Min.		Unit	Remarks
		Tsu	Th		
VI8 to VI1	1 to 8	20.00	10.00	ns	Rising edge of MCK is used as a reference.

Output Interface Timing



Output Characteristics (V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to +75°C)

Output pin	Pin No.	Tpd (output load capacitance 20 [pF])		Unit	Remarks
Y8 to Y1	44 to 51	Max.	25.0	ns	Rising edge of MCK is used as a reference.
		Min.	5.00		
C8 to C1	57 to 64	Max.	25.00	ns	Rising edge of MCK is used as a reference.
		Min.	5.00		

Clock Frequency (V_{DD} = 4.75 to 5.25V, V_{SS} = 0V, Ta = –20 to +75°C)

Input pin	Pin No.	Symbol	Min.	Typ.	Max.	Unit
OCLK, MCK, ADCK	11, 15, 16	f	—	4fsc*1	—	MHz

*1 fsc = 3.58MHz (NTSC), 4.43MHz (PAL)

I/O Pin Capacitance (Ta = 25°C, f = 1MHz, V_{IN} = V_{OUT} = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}	—	—	9	pF
Output pin capacitance	C_{OUT}	—	—	11	

Internal 8-bit ADC Characteristics (V_{DD} = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		18	—	—	MSPS
Analog input bandwidth	BW	–3dB	—	18	—	MHz
Self bias	VRB		0.48	0.52	0.56	V
	VRT–VRB		1.96	2.08	2.22	V
Output data delay	tpd		—	—	45	ns
Differential linearity error	E_D		–1.0	—	+1.0	LSB
Integral linearity error	E_L		–3.0	—	+3.0	LSB
Clamp offset voltage	E_{OC}	V_{REF} = VRB	–20	0	+20	mV
		V_{REF} = VRT	–30	–10	+10	mV

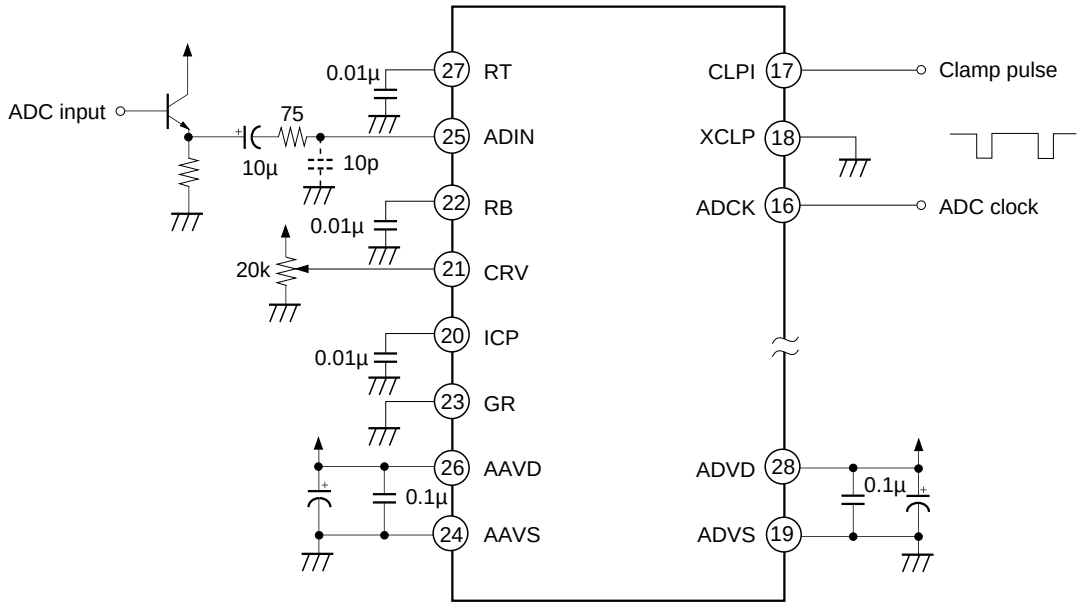
Internal 8-bit DAC Characteristics (V_{DD} = 5V, V_{RF} = 2V, R_{IRF} = 3.3kΩ, R = 200Ω, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		18	—	—	MSPS
Differential linearity error	E_D		–0.8	—	+0.8	LSB
Integral linearity error	E_L		–2.0	—	+2.0	LSB
Output full-scale voltage	V_{FS}		1.805	1.90	1.995	V
Output full-scale current	I_{FS}		—	9.5	15	mA
Output offset voltage	V_{OS}		—	—	1.0	mV
Glitch energy	G_E	*2	—	30	—	pV-s

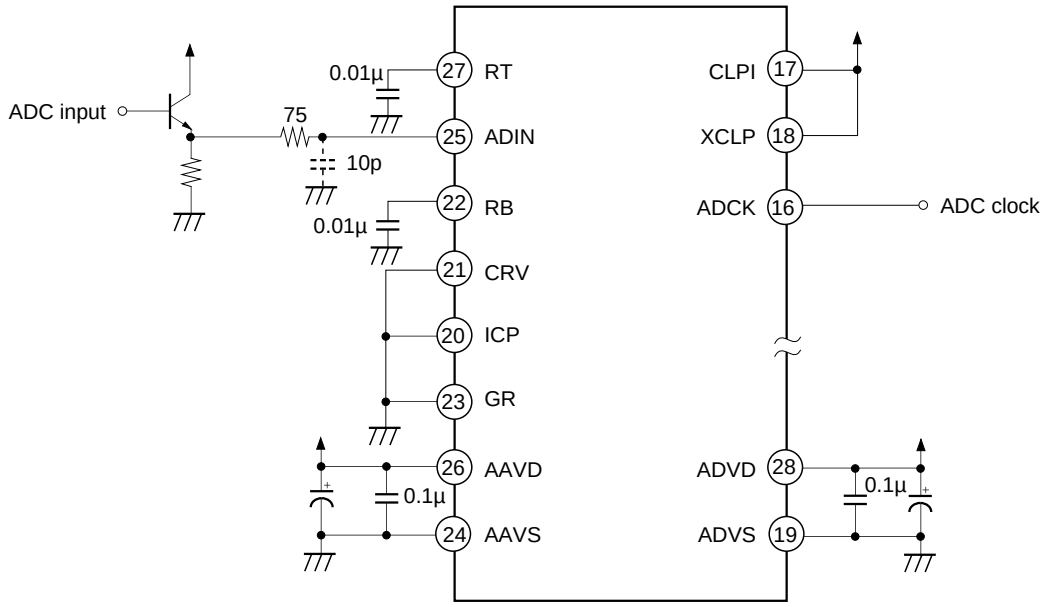
*2 R = 75Ω, 1Vp-p output

Application Circuit for the A/D Converter Block

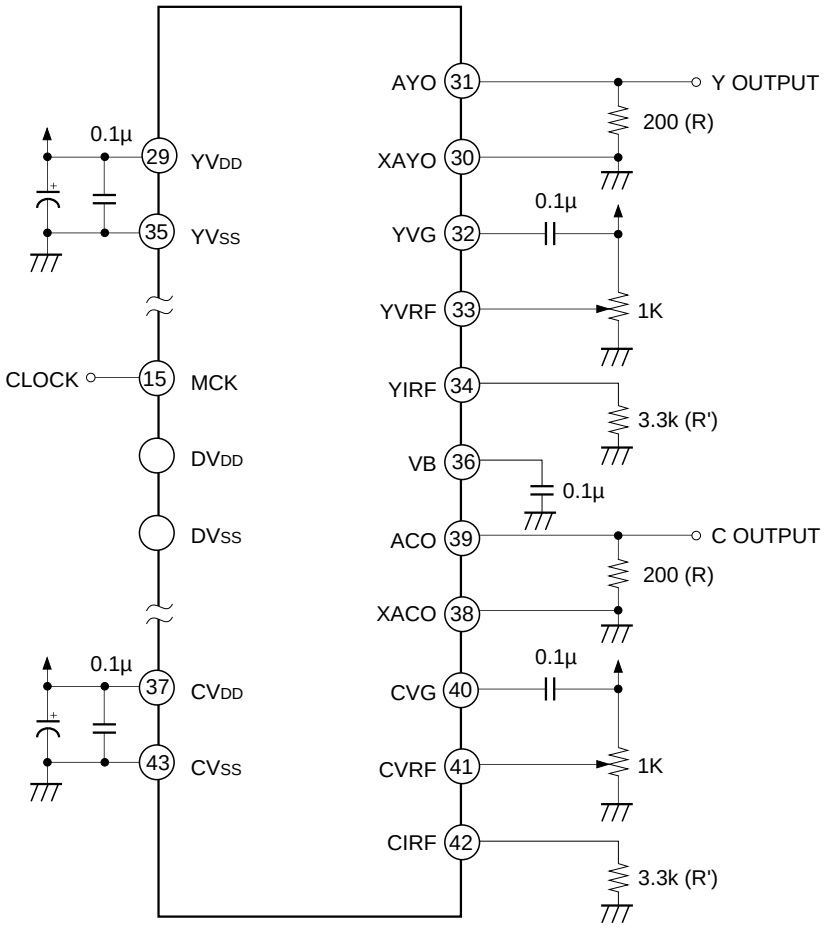
(1) When inputting the clamp pulse directly



(2) When not using the internal clamp circuit



Application Circuit for the D/A Converter Block



• Method of selecting the output resistor

The CXD2044Q has a built-in current output type D/A converter. To obtain the output voltages, connect resistors to the AYO and ACO pins.

The specs are as follows: output full-scale voltage V_{FS} = 0.5 to 2.0 [V], output full-scale current I_{FS} = 0 to 15 [mA].

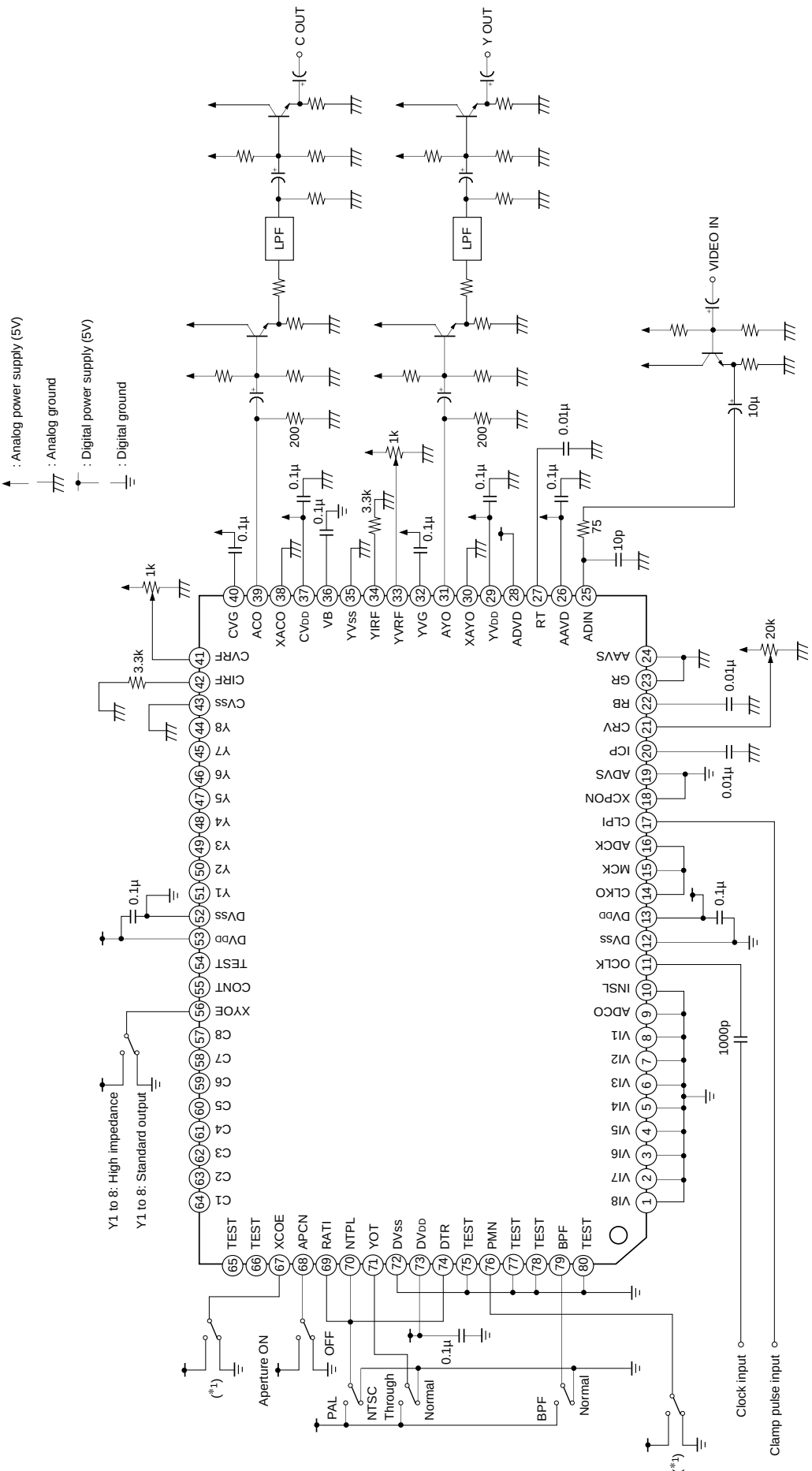
Calculate the output resistance value using the relationship $V_{FS} = I_{FS} \times R$. In addition, connect a resistor of 16 times the output resistor to the reference current pin (YIRF, CIRF). In case this results in a non-existent value, use a resistance value as close to the calculated value as possible.

Note that, at this time, $V_{FS} = V_{RF} \times 16R/R'$ (V_{RF}: Pin voltage of YVRF and CVRF). Here, R is the resistor connected to AYO/ACO, and R' is the resistor connected to YIRF/CIRF. Power consumption can be reduced by using higher resistance values for the R, but the glitch energy and data settling time increase contrastingly. Set the optimum values according to the system applications.

• V_{DD}, Vss

Separate the analog and digital systems around the device to reduce the effects of noise. YV_{DD} and CV_{DD} are by-passed to YVss and CVss, respectively, as close to each other as possible through ceramic capacitors of approximately 0.1µF.

Application Circuit

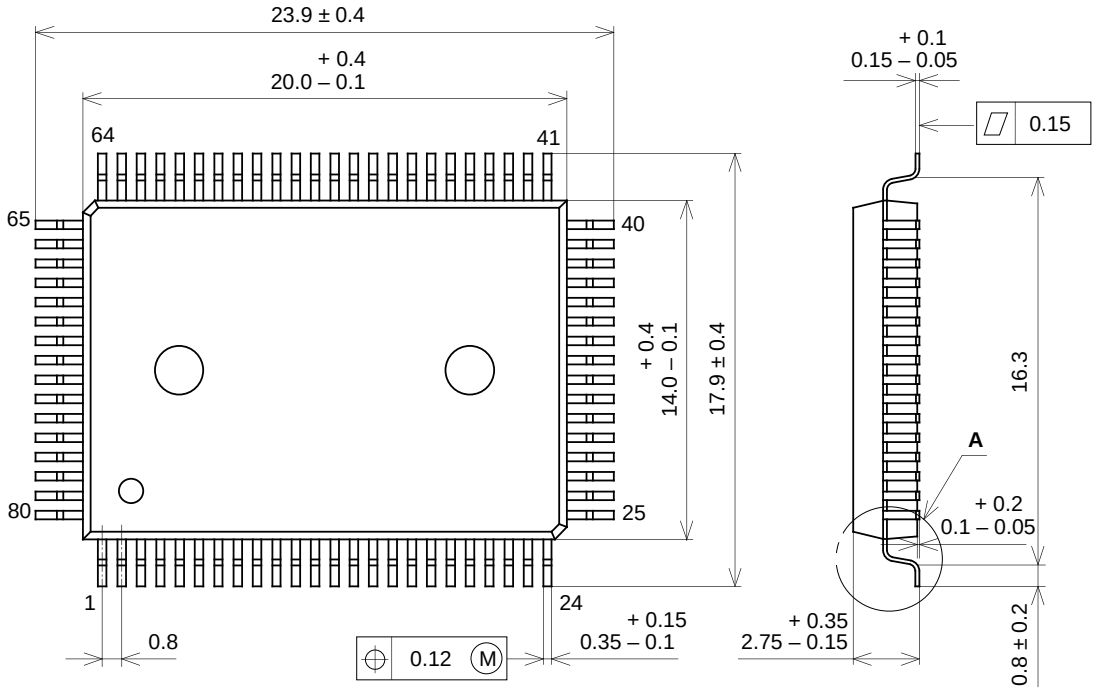


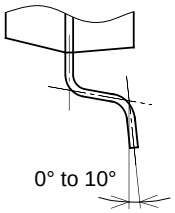
PMN (pin76) / XCOE (pin67)	Digital power supply (5V)	Digital ground
Digital power supply (5V)	PAL-N	C1 to 8: High Impedance
Digital ground	PAL-M	C1 to 8: Standard output

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	∗QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g