ICS671-01
Zero Delay, Low Skew Buffer and Multipler

Description

The ICS671-01 is a low phase noise, high speed PLL based, 8 output, low skew zero delay buffer and multiplier. Based on ICS's proprietary low jitter Phase Locked Loop (PLL) techniques, the device provides eight low skew outputs at speeds up to 160 MHz at 3.3 V. The ICS671-01 includes a bank of six outputs running at either x2 or x4 mode, one output running at either x2, x4, or x5 mode, and one more output running at either x1, x2, or x4 mode. For normal operation, output clock CLK8 is tied to the FBIN pin.

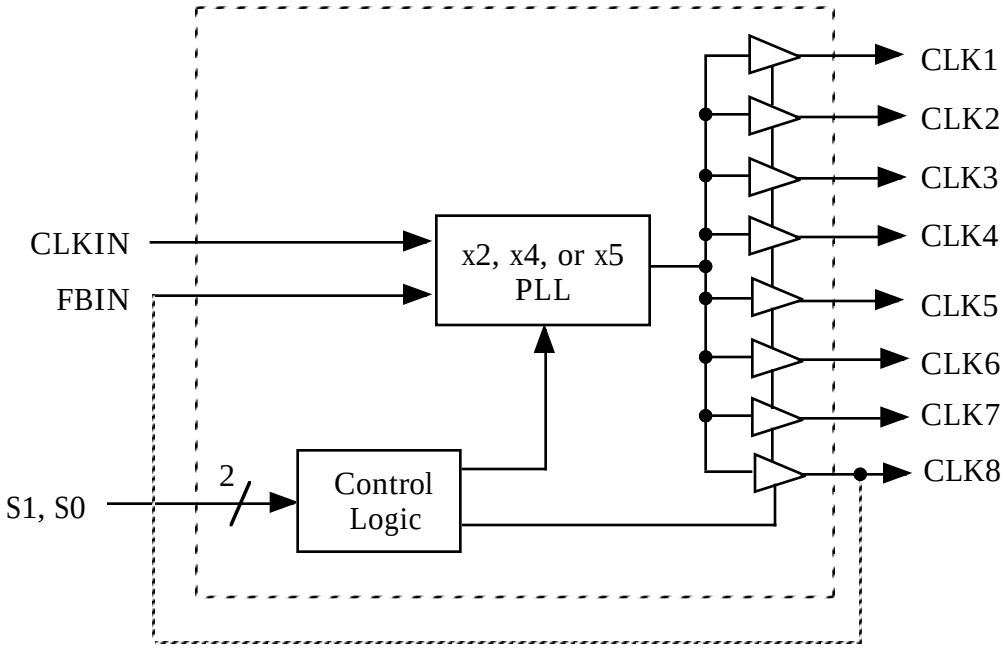
ICS manufactures the largest variety of clock generators and buffers, and is the largest clock supplier in the world.

Features



- Packaged in 16 pin narrow SOIC
- Clock outputs from 5 to 160 MHz
- Zero input-output delay
- Integrated x2 or x4 selections, and x5 for CLK7
- Eight low-skew (<250 ps) outputs
- Full CMOS outputs with 25 mA output drive capability at TTL levels
- Tri-state mode for board-level testing
- Advanced, low power, sub-micron CMOS process
- 3.3 V to 5 V operating voltage

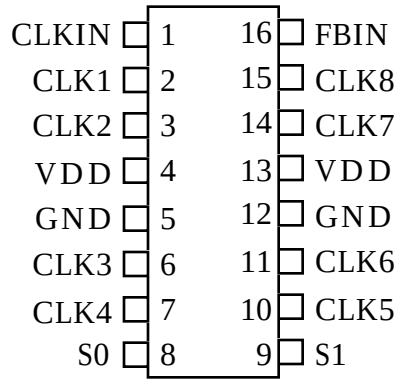
Block Diagram



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Pin Assignment

ICS671-01



16 pin narrow (150 mil) SOIC

Output Clock Mode Select Table

S1	S0	CLK1:6	CLK7	CLK8	Input range
0	0	Tri-state (high impedance)	Tri-state (high impedance)	Tri-state (high impedance)	-
0	1	x2	x5	x1	5 to 30 MHz
1	0	x2	x2	x2	15 to 80 MHz
1	1	x4	x4	x4	7.5 to 40 MHz

Pin Descriptions

Number	Name	Type	Description
1	CLKIN	I	Clock Input.
2, 3, 6, 7, 10, 11	CLK1:6	O	Clock Outputs 1:6. See above table.
4, 13	VDD	P	Power supply. Connect both pins to same voltage (either 3.3 V or 5 V).
5, 12	GND	P	Connect to ground.
8	S0	I	Select input 0. See table above.
9	S1	I	Select input 1. See table above.
14	CLK7	I	Clock Output 7. See table above.
15	CLK8	I	Clock Output 8. See table above. Normally use this clock as feedback.
16	FBIN	I	Feedback Input. Connect to CLK8 under normal operations.

Key: I = Input; O = output; P = power supply connection.

External Components

The ICS671-01 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between VDD and GND on pins 4 and 5, and VDD and GND on pins 13 and 12, as close to the device as possible. A series termination resistor of 33 Ω may be used close to each clock output pin to reduce reflections.

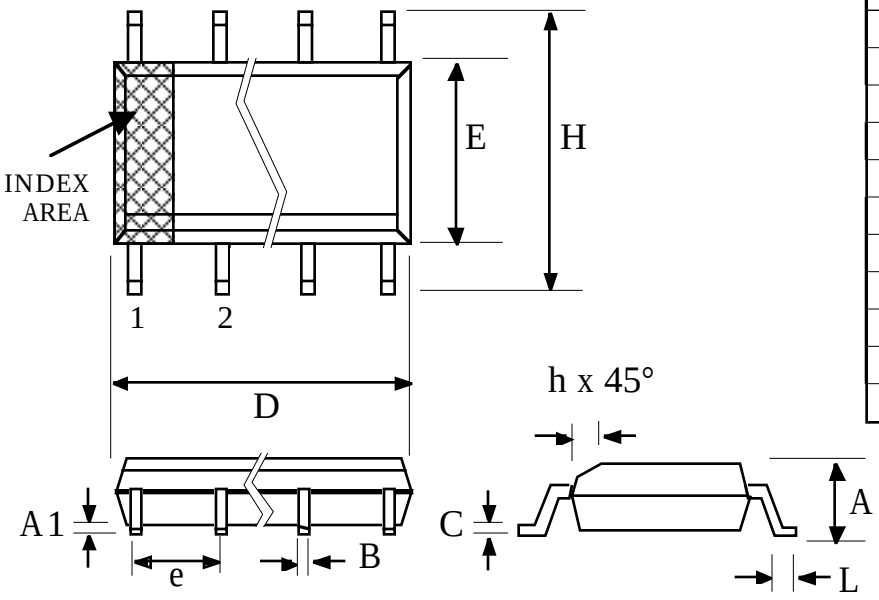
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND	-0.5		7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Electrostatic Discharge	MIL-STD-883	2000			V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Junction temperature				150	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless specified otherwise)					
Operating Voltage, VDD		3.13		5.50	V
Input High Voltage, VIH, CLKIN pin only		VDD/2+1	VDD/2		V
Input Low Voltage, VIL, CLKIN pin only			VDD/2	VDD/2-1	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Suppl Current, IDD (Note 2)	No Load, S1=1, S0=0		25		mA
Operating Suppl Current, IDD (Note 3)	No Load, S1=1, S0=0		74		mA
Short Circuit Current	Each output		±50		mA
Input Capacitance	S0, S1, FBIN		7		pF
AC CHARACTERISTICS (VDD = 3.3 V unless specified otherwise)					
Input Clock Frequency	See table on page 2	5		80	MHz
Output Clock Frequency	See table on page 2	5		160	MHz
Output Clock Rise Time, CL=30pF	0.8 to 2.0V			1.5	ns
Output Clock Fall Time, CL=30pF	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle, VDD=3.3V	At VDD/2	40	50	60	%
Device to Device Skew, equally loaded	rising edges at VDD/2			700	ps
Output to Output Skew, equally loaded	rising edges at VDD/2			250	ps
Input to Output Skew, FBIN to CLK8	rising edges at VDD/2			±350	ps
Maximum Absolute Jitter			300		ps
Cycle to Cycle Jitter, 30pF loads				500	ps

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With CLKIN = 20 MHz, FBIN to CLK8, all outputs at 40 MHz.
3. With CLKIN = 80 MHz, FBIN to CLK8, all outputs at 160 MHz.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



16 pin SOIC narrow

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
ICS671M-01	ICS671M-01	tubes	16 pin SOIC	0-70 °C
ICS671M-01T	ICS671M-01	tape and reel	16 pin SOIC	0-70 °C

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