

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
 - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
 - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
 - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

M65761FP

QM-Coder

REJ03F0234-0200
Rev.2.00
Sep 14, 2007

Description

The M65761FP is a compression and decompression LSI conforming to the high efficiency encoding system (QM-Coder) in the International Standard, the JBIG/JPEG (ITU-T Recommendations T.81 and T.82) for coding still images.

It also conforms to the International Standard (ITU-T Recommendation T.85) for facsimile.

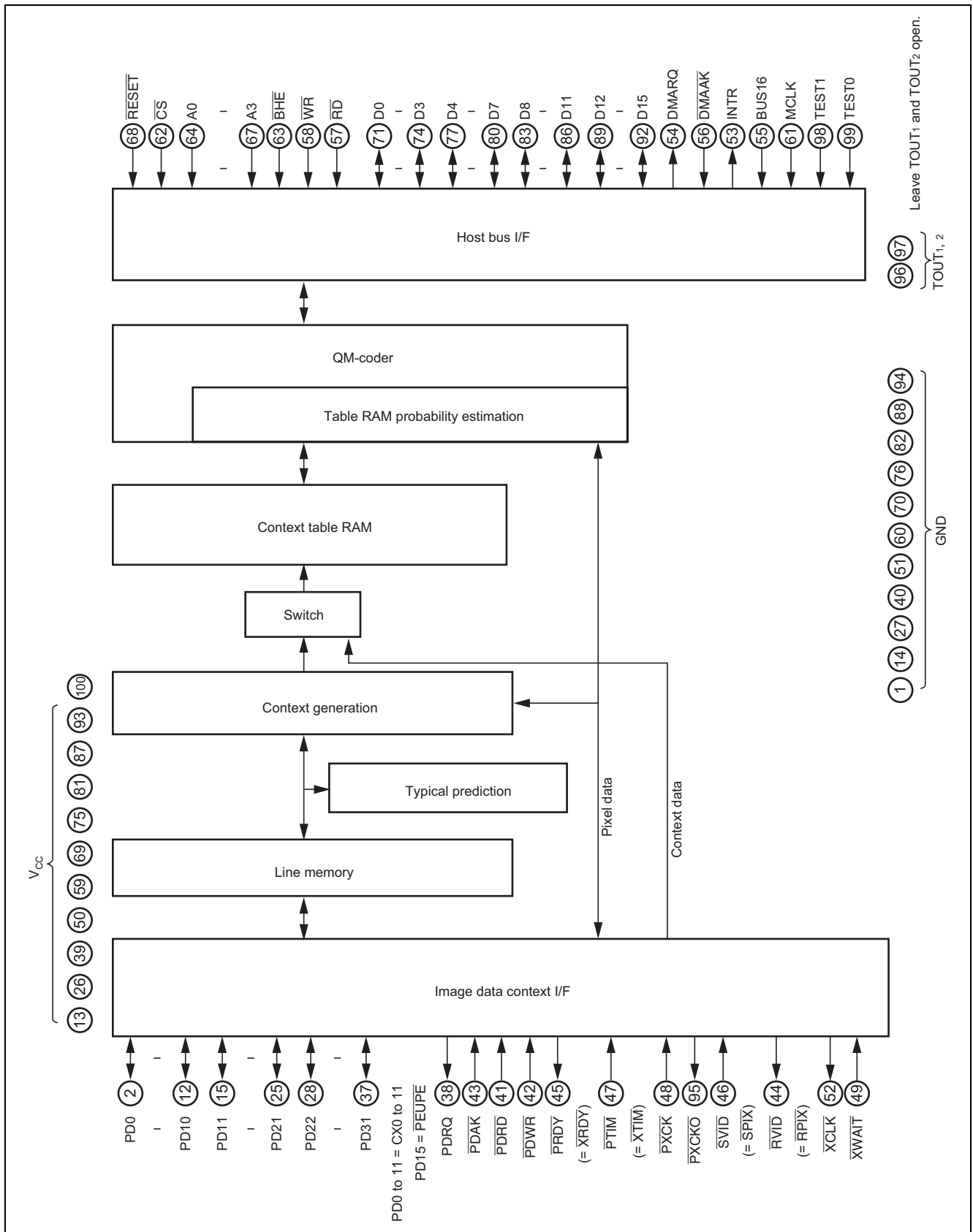
Features

- 100 pin plastic molded quad flat package (fine pitch): PRQP0100JB-A (100P6S-A)

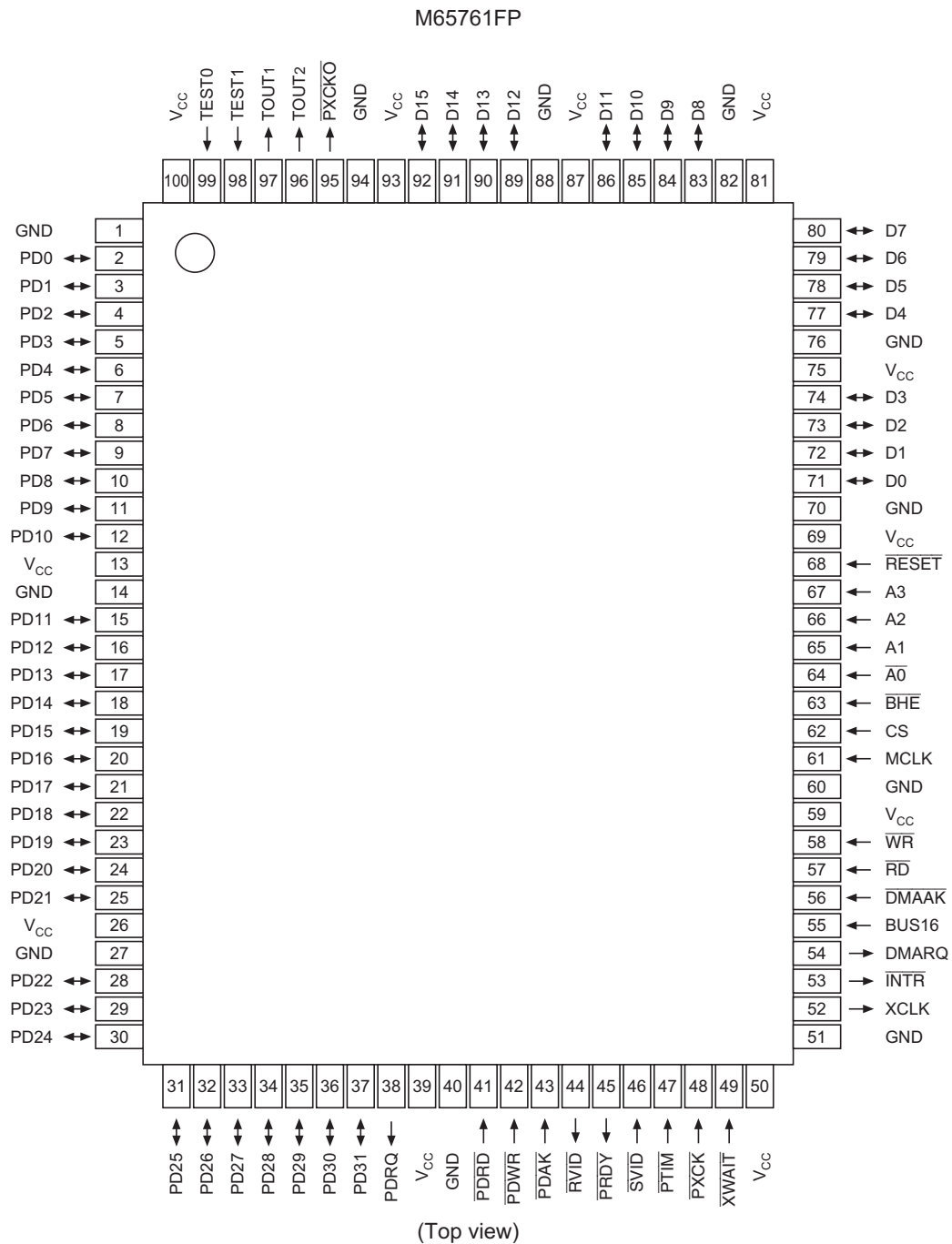
Application

- OA equipment including facsimile, copier and printer

Block Diagram



Pin Arrangement



Outline: PRQP0100JB-A (100P6S-A)

Pin Description

Classification		Pin Name	I/O	BUF	Function
Host bus I/F		$\overline{\text{RESET}}$	I	S	H/W reset signal
		$\overline{\text{CS}}$	I		Chip select signal
		A0 to 3	I		Internal register address select signal
		$\overline{\text{BHE}}$	I		High-order (D8 to 15) access signal
		$\overline{\text{WR}}$	I	S	Write strobe signal
		$\overline{\text{RD}}$	I	S	Read strobe signal
		D0 to 15	IO	8	I/O data signal (D0 to 7 used on 8-bit bus)
		DMARQ	O	2	Code data DMA request signal
		$\overline{\text{DMAAK}}$	I	US	Code data DMA acknowledge signal
		INTR	O	2	Interrupt request signal
		BUS16	I	U	8-bit bus (D0 to 7) and 16-bit bus (D0 to 15) function select bus
Image data I/F	Parallel	PD0 to 31	IO	U2	Parallel image I/O bus (PD0 to 15 used on 16-bit bus)
		PDRQ	O	2	Image data DMA request signal
		$\overline{\text{PDAK}}$	I	US	Image data DMA acknowledge signal
		$\overline{\text{PDRD}}$	I	US	Image data read strobe signal
		$\overline{\text{PDWR}}$	I	US	Image data write strobe signal
	Serial	$\overline{\text{PRDY}}$	O	2	Image data 1-line I/O start ready signal
		$\overline{\text{PTIM}}$	I	US	Image data 1-line transfer section signal
		$\overline{\text{PXCK}}$	I	US	Image data transfer clock signal
		$\overline{\text{PXCKO}}$	O	4	Image data transfer sync clock signal
		$\overline{\text{SVID}}$	I	U	Image data input signal
		$\overline{\text{RVID}}$	O	2	Image data output signal
		Context I/F	CX0 to 11	I	U
$\overline{\text{PEUPE}}$	I		U	PE RAM up date enable (learning function ON/OFF) (= PD15)	
$\overline{\text{SPIX}}$	I		U	Coded image data input signal (= SVID)	
$\overline{\text{RPIX}}$	O		2	Decoded image data output signal (= RVID)	
$\overline{\text{XCLK}}$	O		4	Context data transfer clock signal	
$\overline{\text{XWAIT}}$	I		US	Context data transfer wait signal	
$\overline{\text{XRDY}}$	O		2	Context data 1-stripe I/O start ready signal (= PRDY)	
$\overline{\text{XTIM}}$	I		US	Context data 1-stripe transfer section signal (= PTIM)	
Others		MCLK	I		Master clock input signal
		TEST0, 1	I	DS	Test signal (should be connected to GND when normally used)
		V _{CC} /GND	—	—	Power supply (+5 V)/ground

Note: Most of the context I/F signals are used in conjunction with the image data I/F signals.

The input buffers of the input terminals (I and IO) are at TTL level.

Options are as follows.

(U: with pull-up resistors, D: with pull-down resistors, S: Schmitt trigger)

Numbers (2, 4, 8) of the BUF column of the output terminals (O and IO) indicate current value. (one of 2, 4, or 8 mA)

Absolute Maximum Ratings

(Ta = -20 to +70 °C unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.3 to +7.0	V	
Input voltage	V _I	-0.3 to V _{CC} + 0.3	V	
Output voltage	V _O	0 to V _{CC}	V	
Storage temperature	T _{stg}	-65 to +150	°C	
Power dissipation	P _d	1380	mW	Ta = 25 °C, when single IC is used

Note: All of the voltage is reference the GND terminal of the circuit.

Maximum value and minimum value are expression of absolute value.

Recommend Operating Conditions

Item	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Supply voltage	V _{CC}	4.5	5.0	5.5	V	
GND voltage	GND	—	0	—	V	
Input voltage	V _I	0	—	V _{CC}	V	
Operating temperature range	T _{opr}	-20	—	+70	°C	
Output capacitance (against IC)	C _L	—	50	—	pF	

Electrical Characteristics

(Ta = -20 to +70°C, V_{CC} = 5 V ± 10% unless otherwise noted)

Item		Symbol	Limits			Unit	Test Conditions
			Min	Typ	Max		
"H" input voltage	PD<31:0>, A<3:0>, D<15:0>	V _{IH}	2.0	—	—	V	
"L" input voltage	SVID, BUS16, $\overline{\text{CS}}$, BHE	V _{IL}	—	—	0.8	V	
"H" input voltage	MCLK, PXCK	V _{IH}	4.5	—	—	V	
"L" input voltage		V _{IL}	—	—	0.0	V	
Positive threshold voltage	PDRD, $\overline{\text{DMAAK}}$, PDAK, PTIM,	V _{T+}	—	—	2.4	V	
Negative threshold voltage	XWAIT, PDWR, TEST1, TEST0,	V _{T-}	0.6	—	—	V	
Hysteresis width	$\overline{\text{RD}}$, $\overline{\text{WR}}$, RESET	V _H	—	0.2	—	V	
"H" output voltage	D<15:0>	V _{OH}	V _{CC} - 0.8	—	—	V	I _{OH} = -8 mA
"L" output voltage		V _{OL}	—	—	0.55	V	I _{OH} = 8 mA
"H" output voltage	XCLK, PXCKO	V _{OH}	V _{CC} - 0.8	—	—	V	I _{OH} = -4 mA
"L" output voltage		V _{OL}	—	—	0.55	V	I _{OH} = 4 mA
"H" output voltage	PD<31:0>, INTR, DMARQ, PDRQ,	V _{OH}	V _{CC} - 0.8	—	—	V	I _{OH} = -2 mA
"L" output voltage	$\overline{\text{PRDY}}$, RVID	V _{OL}	—	—	0.55	V	I _{OH} = 2 mA
"H" input current	A<3:0>, D<15:0>, $\overline{\text{RD}}$, $\overline{\text{WR}}$, MCLK,	I _{IH}	—	—	-1.0	μA	V _{CC} = 5.5 V, V _I = 5.5 V
"L" input current	BHE, RESET, $\overline{\text{CS}}$	I _{IL}	—	—	1.0	μA	V _{CC} = 5.5 V, V _I = 0 V
"H" output current in OFF state	D<15:0>	I _{OZH}	—	—	-5.0	μA	V _{CC} = 5.5 V, V _I = 5.5 V
"L" output current in OFF state		I _{OZL}	—	—	5.0	μA	V _{CC} = 5.5 V, V _I = 0 V
Pull up resistor	PD<31:0>, PDRD, PDWR, PDAK, SVID, PTIM, PXCK, XWAIT, BUS16, $\overline{\text{DMAAK}}$	R _U	25	—	100	kΩ	V _{CC} = 5.5 V, V _I = 0 V
Pull down resistor	TEST1, TEST0	R _D	21	—	100	kΩ	V _{CC} = 5.5 V, V _I = 5 V
Dynamic consumption		I _{CCA}	—	100	—	mA	V _{CC} = 5.5 V, V _I = V _{CC} , GND

Note: The value of resistor is 50 kΩ buffer's value.

Coding Specification

(1) Coding Algorithm

- QM-Coder
(JBIG standard arithmetic coding system)

(2) Context

(i) Built-in context mode

a) Template model

- 2 or 3 line 10 pixel template (see figure 1)
(This agrees with the template used with the minimum resolution of JBIG)
Note: The coding efficiency of the 3-line template is better than that of the 2-line template by several %.

b) Adaptive template (AT)

- It is possible to move up to 127 pixels on the coding line.
(The position of AT given instruction by the MPU)
Note: It is possible to improve the coding efficiency against the dither image by the use of AT.
- It is possible to change the position of AT line by line in the middle of coding and decoding.
Note: It is not possible to change the template at the time when change the position of the AT pixels.

(ii) External context mode

- It is possible to input any context up to 12 bits.
(It is possible to interface with JBIG Progressive Coding and the Arithmetic Coding of JPEG Option Function)

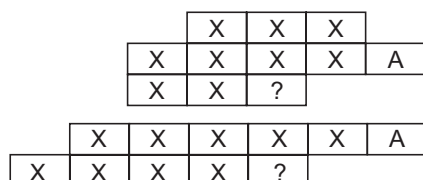


Figure 1 Template (X, A) (Top: 3-line, Bottom: 2-line)

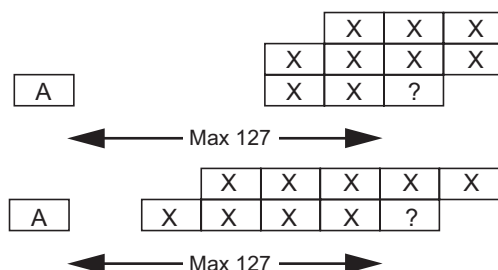


Figure 2 Adaptive Template (A)

(3) Typical Prediction

- Agreement with the Typical Prediction of the lowest resolution of JBIG.
The pseudo-pixel (SLNTP) is generated by the symbol LNTP which shows whether the coding/decoding process agree with the directly before line. If they agree, the line is not coding/decoding.
This makes it possible to shorten the time of process and rejection of the code data.

$$SLNTP_y \neq (LNTP_y \oplus LNTP_{y-1} - 1) \quad (y: \text{line number, } LNTP_y = 1; LNTP_{y-1} = 1)$$

(4) Deterministic Prediction

- This LSI is not equipped with the Typical Prediction. However, the DP function is realized when the DP pixels are identified and eliminated by the external circuits during the external context mode.

(5) Coding Data Format

- The Stripe Data Entity (SDE) (= Stripe coded data with byte stuffing (PSCD) + end marker (SDNORM / SDRST)) Coding/decoding of one stripe portion as performed. In case of the multi-striped (construct the multi stripes) stripes are activated one at a time.

(6) Marker Code

- The SDE end marker is supported. (SDNORM = 02h, SDRST = 03h, ABORT = 04h)
(During coding the marker code previously set in the register is outputted. During decoding, the marker code detected by requesting an interrupt to MPU when the marker is detected is read out of register.)

(7) Rough Estimate of Coding and Decoding Time**(T1: M65761FP as a Whole, T2: Processing Time of the Arithmetic Coding Section Alone)**

- The total number of clocks needed for coding and decoding 1 page (stripe) is calculates roughly using the following equations.

$T1 \approx (p \cdot Lp) + (9/8 \cdot C) + (Lp)$	p:	Number of pixels/line	: about 0.3
$-S \cdot ((1 -) \cdot p \cdot Ltp - Lp) \text{ [clock]}$	Lp:	Number of lines/page	
$T2 \approx (p \cdot Lp) + (9/8 \cdot C)$	Ltp:	Number of TP line/page	
$-S \cdot ((p \cdot Ltp) - Lp) \text{ [clock]}$	C:	Number of coded data bits/page	
	S = 1:	TP exists	0: No TP : about 10

Register Configuration

List of Registers

Address	Register Name	R/W	Description
0	System setting	R/W	- LSI H/W reset - Coding/decoding/image data through mode selection - Context selection (internal context/external context) - Byte swap ON/OFF of coded/image data on host bus - Bit swap ON/OFF of coded/image data on host bus - Image data I/O I/F (parallel I/F, serial I/F) - Image data bus bit width selection (32 bits/16 bits)
1	Parameter setting	R/W	- Template selection (2-line/3-line template) - Setting of AT pixel position (up to 127) (If 0 is set, AT becomes non-existent (default position)) - Latch input/through input selection in external context input mode
2	Command	W	- Context table RAM initialization command - Coding (decoding, through) start/end command - Start/stop command for R/W of context table RAM - Selection of temporary stop and terminating end
2	Status	R	- Processing status (in process/end of processing) - Coded data read/write ready (ready/busy) - Marker code detection (SDNORM, SDRST, ABORT, others) - Interrupt request status - SC counter overflow - Processing mode (stop temporary/terminating end)
3	Interrupt enable setting	R/W	Interrupt enable setting correspondence to each of bits positions of status register
4, 5	Pixel count setting	R/W	Setting the number of pixels on one line (in multiples of 16 or 32, up to 10240 pixels)
6, 7	Line count setting	R/W	Setting the number of lines to be coded/decoded (up to 65535 lines)
8, 9	Processed line count	R	Setting the number of coded/decoded lines (up to 65535 lines)
A, B	Data write buffer	W	Buffer for writing coded data/image data/context table RAM data from MPU into LSI (DMA transferable) (RAM address is automatically incremented each time data is written.)
A, B	Data read buffer	R	Buffer for reading coded data/image data/context table RAM data from LSI into MPU (DMA transferable) (RAM address is automatically incremented each time data is read).
C	Marker code setting	W	Setting a terminal marker code in coding (SDNORM/SDRST)
C	Marker code read	R	Reading a marker code in decoding (SDNORM, SDRST, ABORT, others)
D	Scaling	R/W	- Reduction in coding (1/2 reduction in horizontal and vertical directions, horizontal OR processing) - Magnification during decoding (×2 lengthwise and width) - Select throwing away the leading 1-byte of the coded data read when decoding - Selecting the typical prediction - Selection of prohibiting line memory initialization

Note: When the 8-bit bus is used for the data read/write buffer, use address A only.

In case of the 16-bit buffer, only the word access is possible.

(The byte access is not possible.)

Description of Registers

(1) System set up register (W/R)

(Address: 0)	d7 (MSB)						d0
SYS_REG:	PB	PI	BX	BS	CX	MOD	HR

d0 (HR): H/W reset (0: Active, 1: Reset state)

To make a H/W reset, set this bit to 1 then to 0.

Reset initializes the entire LSI including the group of register and line memory. However, the context table RAM is not initialized.

d1, d2 (MOD): This sets up the operating modes.

(d2 = 0, d1 = 0: coding, d2 = 1, d1 = 0: lage data through (lage data I/F Host I/F),

d2 = 0, d1 = 1: decoding, d2 = 1, d1 = 1: lage data through (Host I/F lage data I/F))

d3 (CX): Context select (0: internal context, 1: Image data through)

Note: The internal context should be selected when the image data through mode is used.
When initializing or processing R/W of the context table RAM and coding/decoding.
This bit must be set the same. (Because RAM configuration changes depending on internal/external modes.)

d4 (BS): Select data bit swap of the host bus. (0: MSB (d7) first, 1: LSB (d0) first)

d5 (BX): Select data byte swap of the host bus. (0: Lower byte (A) first, 1: Upper byte (B) first)

Note: BX is valid only when the host bus is 16 bits. (BUS16 = HIGH)

Table 1 The Coed Data and Image Data Lineup on the Host Bus

Bus Width BUS16	Swap		Upper Address (B)			Lower Address (A)		
	BX	BS	d15	•••••	d8	d7	•••••	d0
1	0	0	b8	•••••	b15	b0	•••••	b7
16-bit	0	1	b15	•••••	b8	b7	•••••	b0
	1	0	b0	•••••	b7	b8	•••••	b15
	1	1	b7	•••••	b0	b15	•••••	b8
0	—	0	—			b0	•••••	b7
8-bit	—	1	—			b7	•••••	b0

Note: b0 is the first coded data on the time series/the left-hand side image data on the screen.
b15 is the last coded data on the time series/the right-hand image data on the screen.

b6 (PI): Selects the image data I/O I/F (0: Serial I/F, 1: Parallel I/F)

b7 (PB): Selects the bit width of the image data bus (0: 32-bit bus (PD0 to 31), 1: 16-bit bus (PD0 to 15))

Table 2 The Image Data Lineup on the Image Data Parallel Bus

Bit Width	PD31	•••••	PD16	PD15	•••••	PD0
PB = 0	p0	•••••	p15	p16	•••••	p31
PB = 1	—			p0	•••••	p15

Note: p0 is the image data on the left-hand on the screen.
p31 is the image data on the right-hand on the screen.

(2) Parameter setup register (WR)

1) External context mode

(Address: 1)	d7		d4		d0
PARAM_REG:	C0	LC	0	0	

d6 (LC): Condition of taking in the input from the external context are selected.

(0: through output, 1: latch input)

When this bit is set to 1, the CX0 to CX11 of the context input is latched once using the transfer clock. ("XCLK")

d7 (C0): When this bit is set to 1, CX0 is selected.

(0: CX0 external input, 1: CX0 internal feedback)

2) Internal context mode

(Address: 1)	d7	d6	d5	d4		d0
PARAM_REG:	AT		TM	AT		

d0 to 4 (AT<0> to AT<4>): AT pixel position lower 5 bits. (see figure 2)

d5 (TM): Template select (0: 3-line template, 1: 2-line template)

d6, d7 (AT<5>, AT<6>): AT pixel position upper 2 bits (the 6th and 7th bits)

Example:	d7		d4		d0
3-line template, AT = 4:	0	0	0	0	0
	d7		d4		d0
2-line template, AT = 48:	0	1	1	1	0

Note: The AT pixel position at time of the internal context mode is set up by using all the AT<6:0> (0 to 127).

When the default position (when the AT pixels are not used) is used, AT is set to 0.

When the 2-line template is used, AT should not be set to 1 to 4. In case of the 3-line template, AT = 1 to 2 is not allowed.

(3) Command register (W)

(Address: 2)	d7		d3		d0
CMD_REG:	0		JP	RC	JC

d0 (IC): This command starts initialization of context table RAM (1: start initialization)

When this bit goes 1, the context table RAM initialization starts. This bit returns to 0 automatically when the initialization is completed.

d1 (JC): Processing (coding/decoding/through) start/end command (1: start processing, 0: end processing)

When this bit goes 1, processing (coding/decoding/through) starts.

This bit returns to 0 automatically when processing of the number of set lines is finished during the selection of end of termination.

And if this JC bit is made 0 and inputting the image data is stopped during the coding process, the coding is stopped (flushed) even if the set lines are not filled. Moreover, if this bit made 0 during decoding and no more coded data is coming in, it is assumed that the "00" of the coded data came in and the preset lines have been processed. However, in case of the multi-striped coding, processing should not end by making this bit "0" except in case of last stripe.

d2 (RC): This command starts and stops R/W of context table RAM. (1: R/W start, 0: R/W end)

The context table RAM is read out or written in by making this bit to "1".

When reading/writing is finished, this bit must have "0" on it.

d3 (JP): This selected temporary stop and the end of termination of coding/decoding/through processing.

(1: Temporary stop selected, 0: End of processing selected)

When the process start command d1 (JC) is issued by making this JP bit to 1, the processing stops temporarily when the set number of lines have been processed. Then, if the process start command d1 (JC) is issued, processing restarts. (See " Sequence of Setting Up Registers " (3))

(4) Status register (R)

(Address: 2)	d7	d5					d0
STAT_REG:	0	PS	SC	IS	MS	DS	JS

d0 (JS): This register indicates the status of processing in initialization, coding, decoding and through.

(0: Processing in progress (being initialized), 1: End of processing)

This JS bit goes to "1" when the initialization is completed as RAM initialization command is issued.

(IC = 1) This JS bit goes to "1" when all coded data has been read out during coding in case when the process start command of the processing end is issued. (JC = 1, JP = 0) This JS bit goes to "1" when reading all the image data has been completed during the image data through and decoding. Moreover, this JS bit stays "0" even when the set number of lines have been processed when the command to start processing the process which has been stopped temporarily has been issued (JC = 1, JP = 1). (However, interrupts are issued during the temporary stops.)

d1 (DS): This is used for read and write ready of coded data. (In case of the through mode, this is used for the image data.) (1: Ready, 0: Reading no possible)

It is possible to do R/W of data by the way of the data write/read buffer when this bit is 1.

d2 (MS): This detects the marker code during decoding. (0: not detected, 1: detected)

This bit goes to "1" if any marker is detected during decoding.

d3 (IS): This indicates the status of the interrupt request. (0: No request, 1: Request exists)

d4 (SC): This shows the SC count over error during coding. (0: Normal, 1: There is a SC counter overflow)

Note: The SC counter counts the "FF" data bytes which occur during coding. Coding continues even when the SC counter overflows, this means correct coding data will not be outputted. (Coding error)

d5 (PS): Processing modes (Stopped temporary/End of trailer) (1: Process temporarily stopped, 0: End of processing)

This PS bit corresponds to the temporary stop and end of processing of d3 bit (JP) processing of the command register.

(5) Interrupt enable register (W/R)

(Address: 3)	d7	d3				d0
IENB_REG	MP	0	SE	ME	DE	JE

d0 (JE): Temporary stop/end of trailer interrupt of initialization/coding/decoding/through.

(0: interrupt mask, 1: interrupt enable)

d1 (DE): Coded data (image data) read out/write in ready interrupt.

(0: interrupt mask, 1: interrupt enable)

d2 (ME): Marker code detection interrupt during decoding. (0: interrupt mask, 1: interrupt enable)

d3 (SE): SC count over error interrupt during coding. (0: interrupt mask, 1: interrupt enable)

This bit sets to 1 beforehand, it occurs the interruption when the SC counter is overflow during coding. Processing of coding continues, but the correct coded data is not output.

Note: Bits, d0 to d3, are for interrupt enable of bits d0 to d2 and d4 of the status register.

The interrupt request signal (INTR) is asserted when any one of the status bit set in the interrupt enable (D0 (JE) generates interrupts even during the temporary stop), the status goes to "0" due to H/W reset or the INTR signal is negated when the interrupt mask causes factors for interrupt to be lost. Moreover, the status register will not be cleared by the generation of interrupts or the R/W of the interrupt enable register.

d7 (MP): This specified the marker code detection time halt. (0: continue/restart, 1: temporary halt)

Decoding will stop temporarily when the marker code is detected if this MP bit is preset to "1" during decoding. (It occurs interruption when the marker code is detected, if the ME bit preset to "1".)

If decoding is not completed during the temporary halt, it is possible to reset the line number setup register. Next, if this MP bit is set to "0", decoding is restarted. (Decoding continues to the line number set.)

(6) Register used to set the number of pixels (W/R)

(Address: 4)	d7		d0
PEL_REG_L:	PEL_L		
(Address: 5)	d7	d5	d0
PEL_REG_H:	0	PEL_H	

d0 to 7 (PEL_L): Number of pixels/line is set (Lower byte)

d0 to 5 (PEL_H): Number of pixels/line is set (Upper byte)

It is possible to set up 8192 pixels maximum when 3-line template is used. It is used to set up 10240 pixels maximum when 2-line template is used. The number of pixels actually coded (or decoded) should be set when reducing (or expanding). When the image bus uses 16 bits (or 32 bits) in parallel I/F, multiples of 16 (or 32) should be set. In case of serial I/F, multiples of 8 should be used.

(7) Line number setting register (W/R)

(Address: 6)	d7	d0
LSET_REG_L:	LSET_L	
(Address: 7)		
LSET_REG_H:	LSET_H	

d0 to 7 (LSET_L): This sets the number of lines to be processed. (Lower bytes)

(1 to 65535, 0 line not used)

d0 to 7 (LSET_H): This sets the number of lines to be processed. (Upper bytes)

When reducing (magnification) the actual number of lines to be coded (decoded) should be set. The number of lines (relative number of lines) from the process start command to be issued from now the immediately following temporary stop/end of trailer should be set. This register should be set to the value specified before the process start command is issued. Moreover, this register can be rewritten during processing as long as the following conditions are met:

- If the maximum value, (65535), is set before the process start command is issued, it can be reset once during processing.
- If a value other than maximum value (65535) is set before the process start command is issued and if resetting becomes necessary during processing, the maximum value (65535) has to be reset once and desired value should be reset.

(8) Number of lines to be processed specified (R)

(Address: 8)	d7	d0
LIN_REG_L:	LINE_L	
(Address: 9)		
LIN_REG_H:	LINE_H	

d0 to 7 (LINE_L): The number of lines actually processed is read out (Lower bytes) (0 to 65535)

d0 to 7 (LINE_H): The number of lines actually processed is read out (Upper bytes)

When the number of lines processed number of lines set, coding/decoding/through stops temporarily/end of processing.

Note: The number of lines to be processed by this processing is cleared to 0 by the issuance of process start command.

(9) Data write in buffer (W) (See note 1)

(Address: A)	d7	d0
DWR_BUF_L:	DWR_L	
(Address: B)		
DWR_BUF_H:	DWR_H	

d0 to 7 (DWR_L): This writes in the coded data/image data/context table RAM data (Lower bytes)

d0 to 7 (DWR_H): This writes in the coded data/image data/context table RAM data (Upper bytes)

(10) Data read out buffer (R) (See note 1)

(Address: A)	d7	d0
DRD_BUF_L:	DRD_L	
(Address: B)		
DRD_BUF_H:	DRD_H	

d0 to 7 (DRD_L): This read out the coded data/image data/context table RAM data. (Lower bytes)

d0 to 7 (DRD_H): This read out the coded data/image data/context table RAM data. (Upper bytes)

Note: 1. Address A is used with 8-bit bus. In case of the 16-bit bus, only the word access is possible. (Not byte access) If the number of coded data bytes is an odd number during coding, an one byte pad ("00") is attached after the end marker is issued in order to use it as a word boundary.

See table 1 for the bit arrangement used during the coded data/image data. In case of the context table RAM data, only the lower byte becomes valid data regardless of the bus width of the host bus (BUS16).

Table 3 Context Data Lineup

Host I/F Bus Width	Upper Address (B)			Lower Address (A)		
	d15	• • • • •	d8	d7	d6 • • • • •	d0
8-bit		—		mps	s6 • • • • •	s0
16-bit		—		mps	s6 • • • • •	s0

Note: mps: Superior symbol MPS (expected value 0/1)

s6 to 0: Status number ST (0 to 112)

(11) Marker code set up register (W)

(Address: C)	d7	d0
MSET_REG:	MSET	

d0 to 7 (MSET): The end marker code used during coding is set. (SDNORM = 02h, SDRST = 03h)

The byte set to this register is outputted as the end marker during coding.

(12) Marker code read out register (R)

(Address: C)	d7	d0
MDET_REG:	MDET	

d0 to 7 (MDET): The marker codes detected during decoding are read out.

(SDNORM = 02h, SDRST = 03h, ABORT = 04h, etc.)

The marker codes detected during decoding read out as is.

(13) This register sets up various functions (W/R)

(Address: D)	d7								d0
CONV_REG:	TP	LI	OB	HO	HR	VR	HE	VE	

d0 (VE): Selects expansion in lengthwise direction during decoding. (0: Equal dimension, 1: 2 expansion)

d1 (HE): Selects expansion sideways during decoding. (0: Equal dimension, 1: 2 expansion)

d0 and d1 are possible only during decoding.

d2 (VR): Selects reduction in lengthwise direction during coding. (0: Equal dimension, 1: 1/2 reduction)

d3 (HR): Selects sideways reduction during coding. (0: Equal dimension, 1: 1/2 reduction)

d2 and d3 are possible only during coding.

d4 (HO): Selects thinning in sideways direction during coding. (0: Simple thinning, 1: OR processing)

This reduction is valid only during coding.

Notes: 1. This lengthwise 1/2 reduction during coding is used for the simple thinning. (Odd lines are skipped)

2. The number of lines for image data to be inputs when VR = 1 for coding must be twice the value set by the register which sets the number of lines.

3. The number of lines for image data to be outputs when VE = 1 for decoding must be twice the value set by the register which sets the number of lines.

d5 (OB): This selects if the leading 1 byte is discarded during decoding. (0: Normal processing (No discarding), 1: The leading 1 byte is discarded)

If a command to start processing the first the stripe decoding is issued during decoding while OB is set to "1", the leading 1 byte of the input data is discarded. (Not used for decoding) If OB = 0, the one of byte discarding process is not used. (Normal decoding used) For example, this function is used by the Host 16 bits bus when the leading 1 byte of the input data word is an invalid data.

Note: Selecting this function is valid in case of the host 8 bits bus and the external context mode also.

d6 (LI): Line memory initialization is prohibited. (0: Initialization specified, 1: Initialization prohibited)

When a command to start processing coding/decoding of the first stripe is issued, if LI = 1, the initialization of the internal line memory is prohibited. (The last image data of the immediately prior coding/decoding left in the line memory is used as the leading reference line data of the next coding/decoding.) When LI = 0, the internal line memory is initialized. (All white (0) data is used as the leading reference line data of the next coding/decoding.) In case when the previous stripe ended with SDNORM during coding/decoding of multi-stripe by setting this bit in the initialization prohibit (1).

Note: Even when LI = 1 is set, this LI bit is cleared (0) and the internal line memory *will be initialized the same line* due to the fact that the H/W reset is written into the external reset terminal or the system set up register.

d7 (TP): This selects the typical prediction when coding and decoding. (0: Typical prediction OFF, 1: Typical prediction ON)

Initialization of Register

Each register is initialized as shown in the table below by writing H/W reset to the external RESET terminals or the system set up registers.

Table 4 Initialization Values for Registers

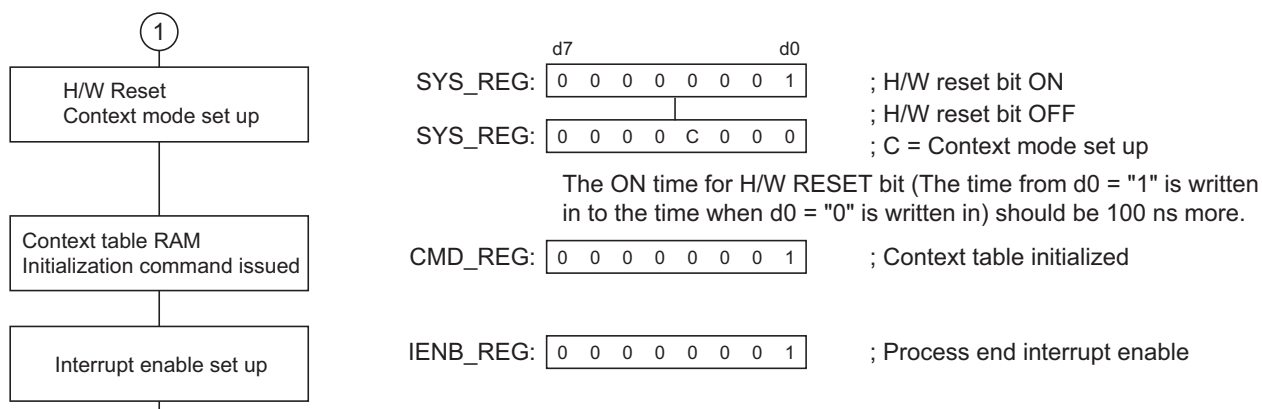
Registers	Initialization Values
System set up	00h ^{Note}
Parameter set up	00h
Command	00h
Status	00h
Interrupt enable	00h
Number of pixels set up	00h
Set up number of lines	00h
Number of lines processed	00h
Data buffer	Indefinite
Marker code set up	00h
Marker code read out	00h
Various functions set up	00h

Note: When writing H/W RESET into the System Setup Register, the value written into is set up in the System Setup Register.

Sequence of Setting Up Registers

(1) Initialization sequence of the internal line memory and context table RAM

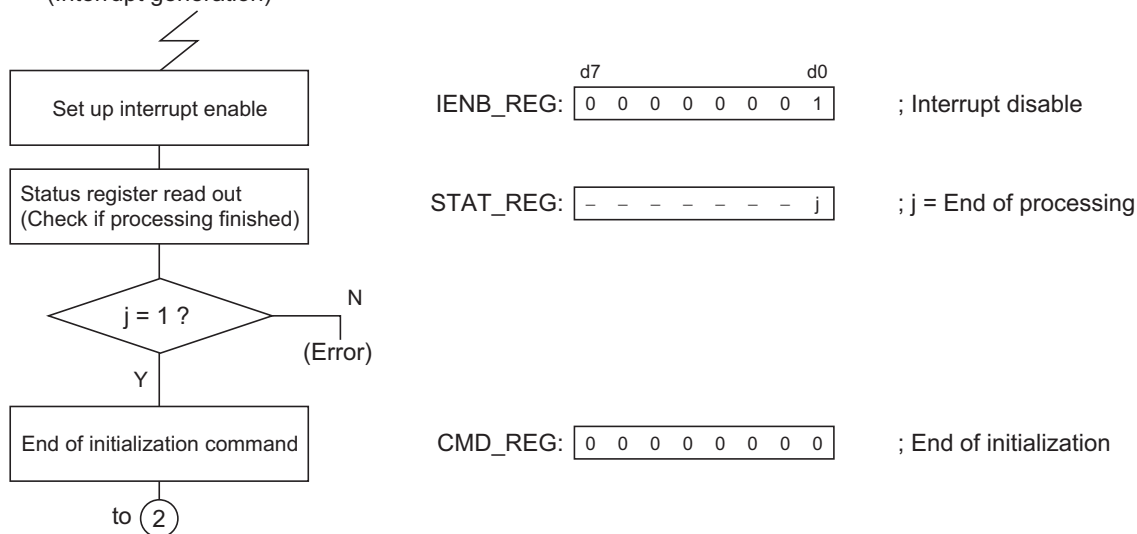
This sequence starts with the initialization set up (see note) of internal line memory by the H/W RESET. It is followed by the initialization of the context table RAM. (Clear)



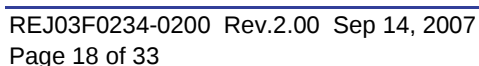
[During this time, the context table RAM is initialized.]

The number of clocks needed for initialization is as follows,
 When the internal text mode is used. 1024 + [clocks]
 When the external text mode is used. 4096 + [clocks]

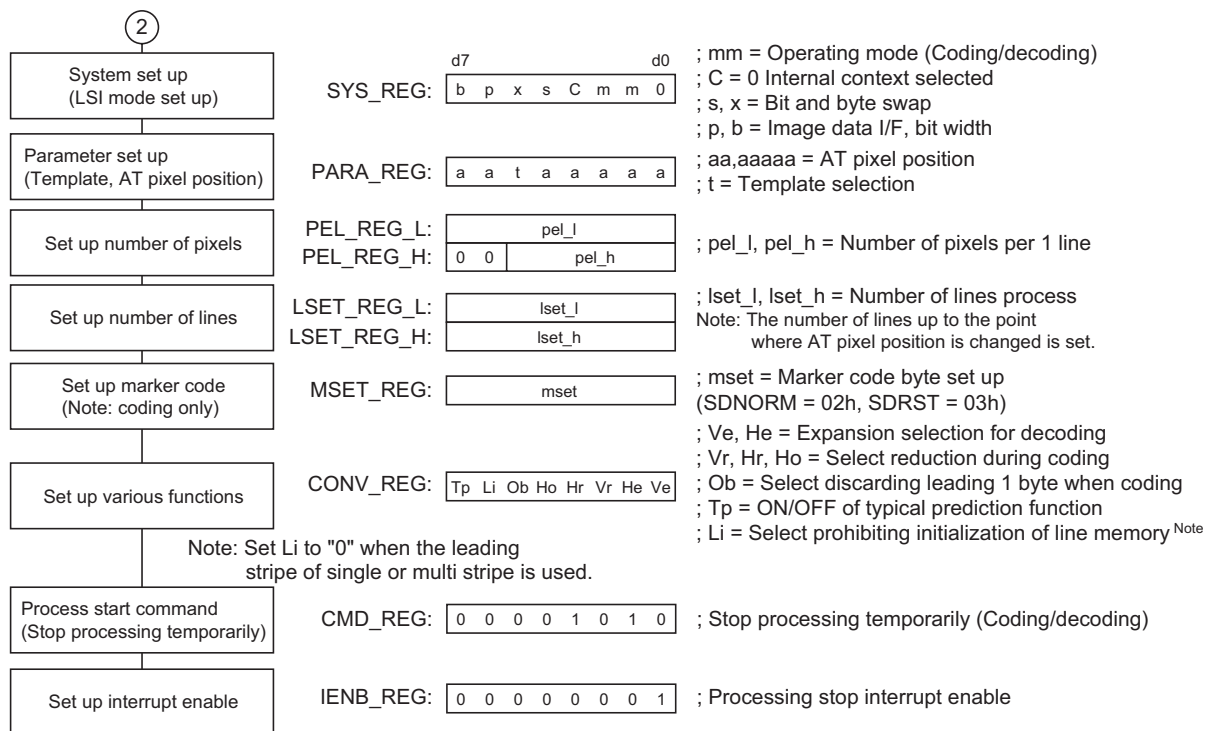
(Interrupt generation)



Note: Initialization of the line memory by H/W RESET is provided for the start of coding and decoding by preparing the all white (0) data as a reference line. At the same time, it initializes the LNTP bit to LNTP = 1 for the Typical Prediction.



(3) Processing sequence of coding/decoding of stripes (internal context mode and AT pixel position may change)

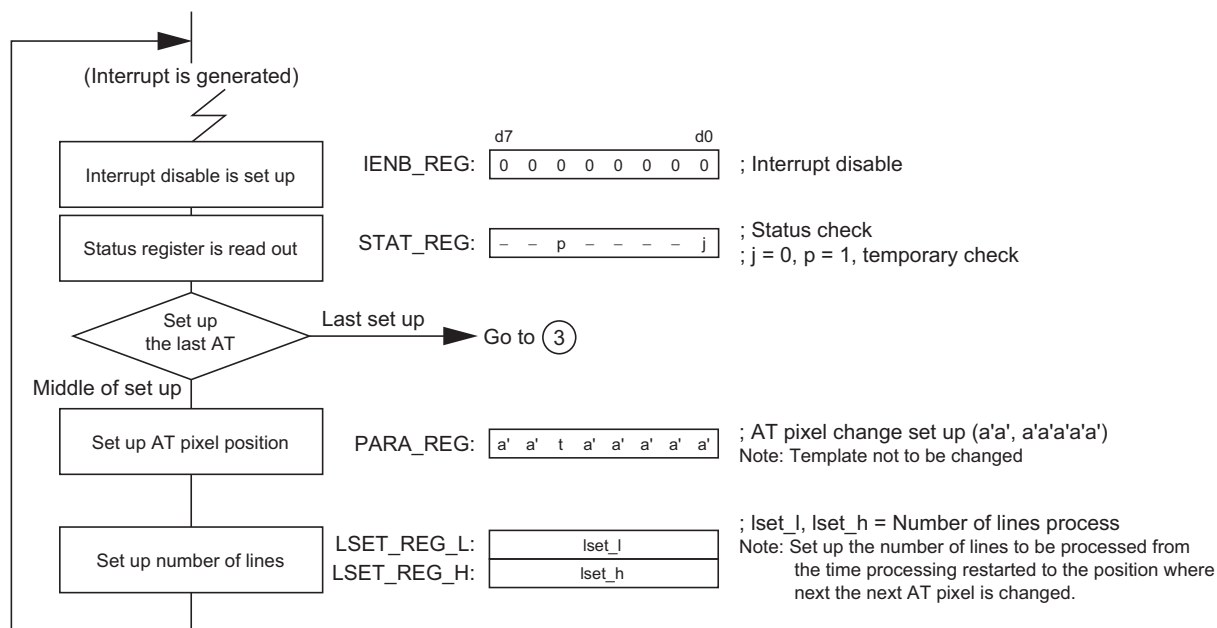


[Coding/decoding go on during this time]—I/O of the first image data and code data take place.

Note: During the first processing, if it is coding, (the number of lines of the input image data) =

(the value set in the register which sets the number of lines) + 1

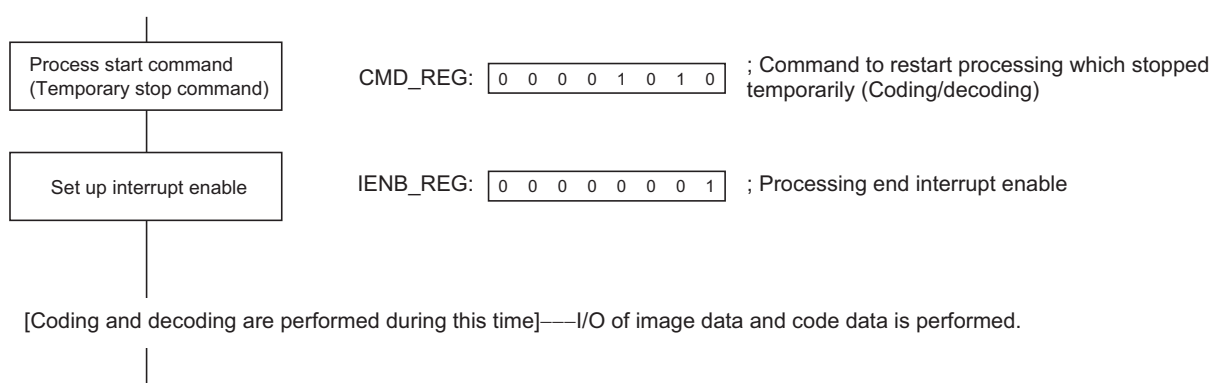
During decoding, (number of lines of the output image data) = (the value set in the register which sets the number of lines) – 1



to Next page

(To previous page)

This routine is repeated the (AT move - 1) times



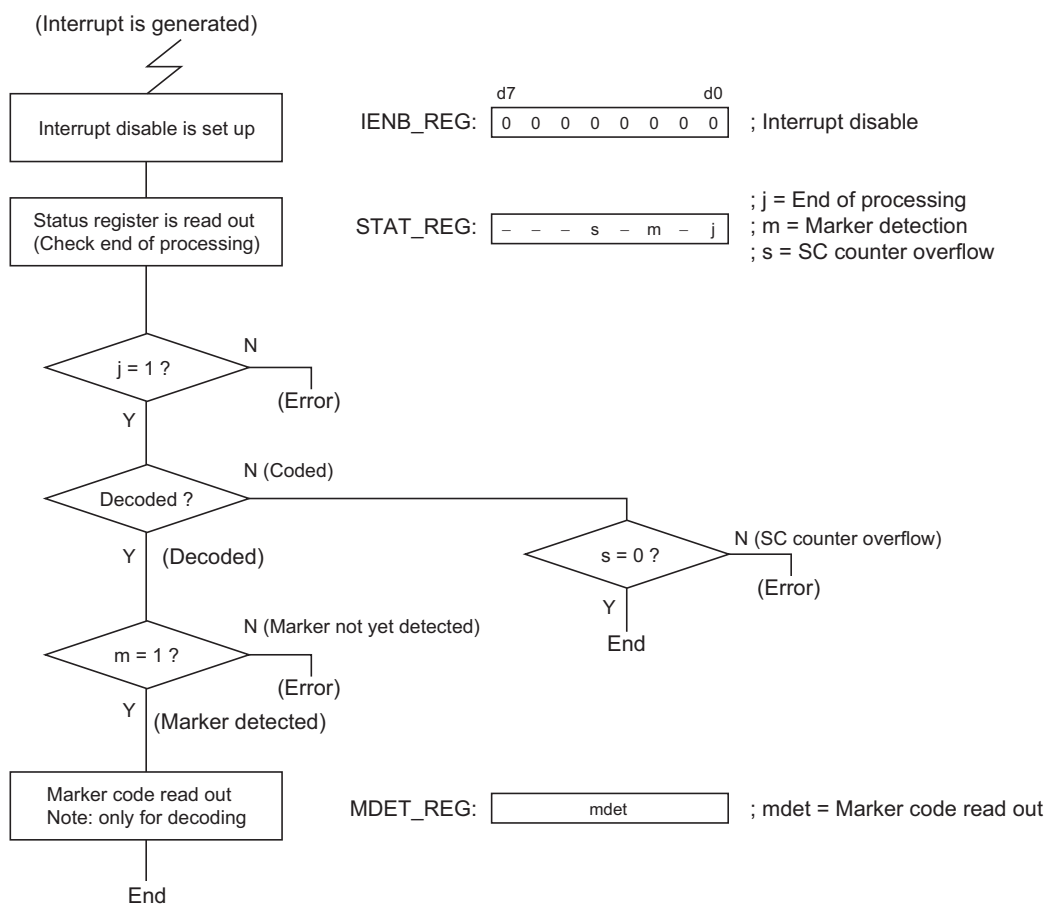
Note: During the above processing the following is true.

During coding,

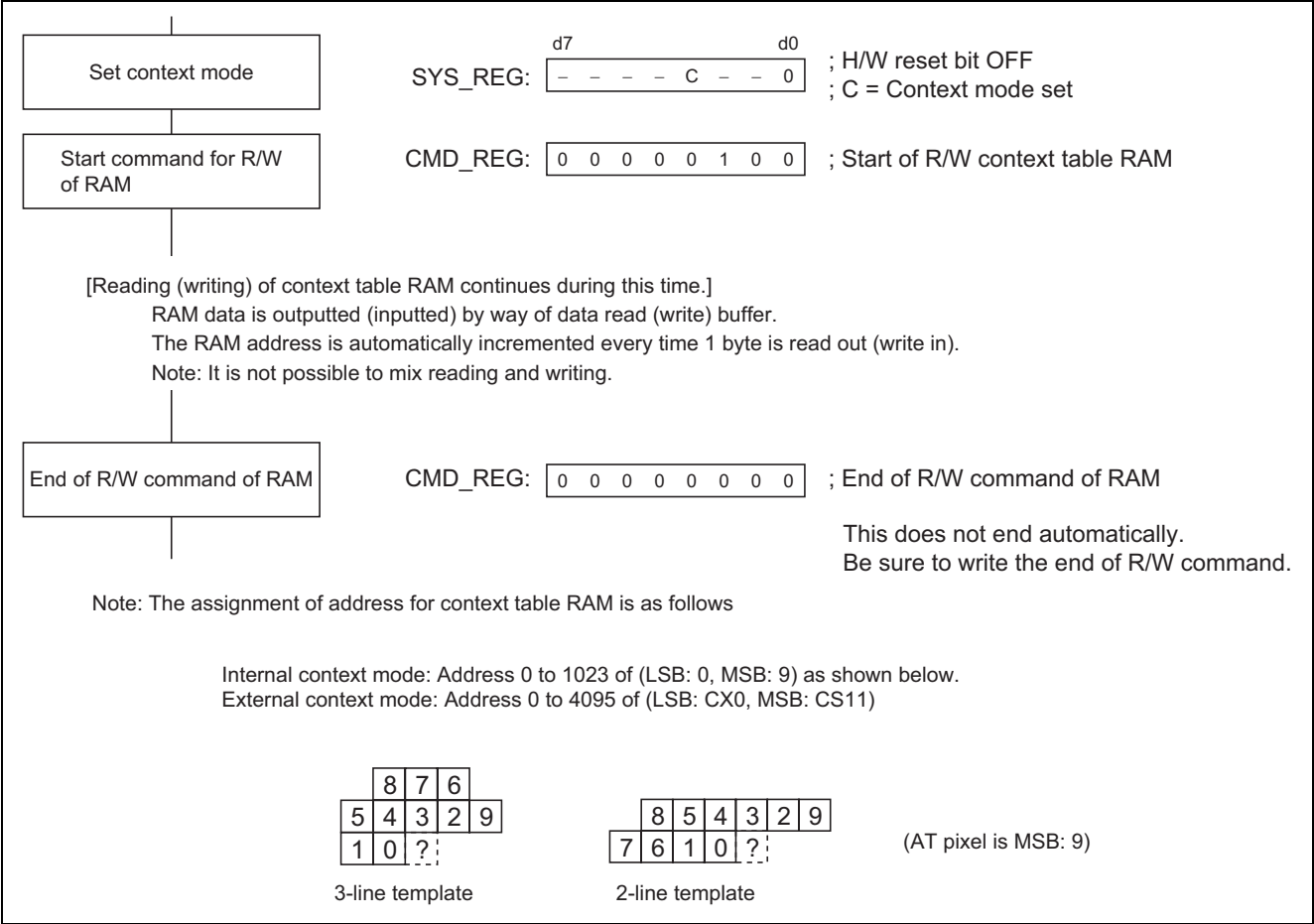
(The number of lines of the input image data) = (Number of lines set in the line number setting register)

During decoding,

(Number of lines of the output image data) = (Number of lines set in the line number setting register)

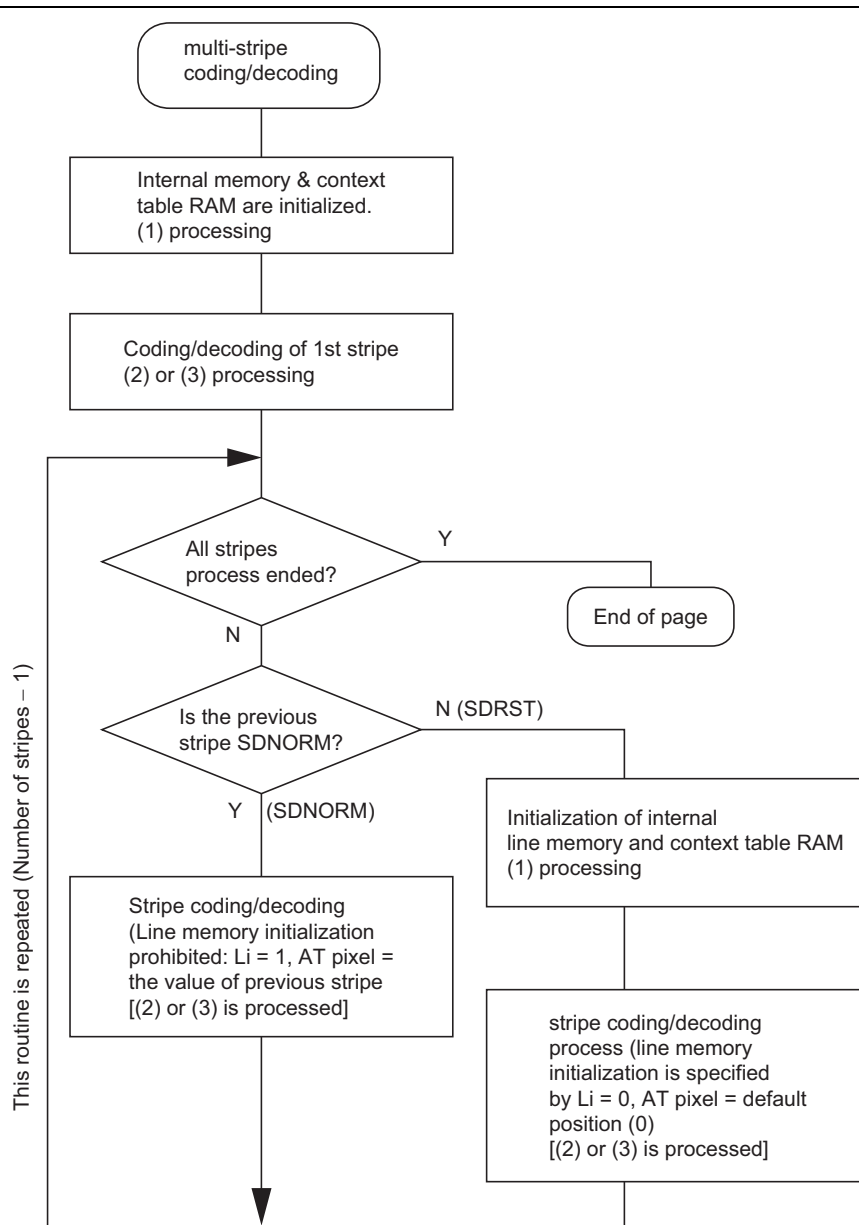


(4) Read out/write in sequence of context table RAM
This sequence dies R/W of context table RAM.



(5) Overall sequence of multi-stripe coding/decoding

The image whose 1 page is composed of multiple stripes must perform (2) or (3) by stripes after the initialization of (1).



- Notes:
1. When 16-bit bus is used for the host-bus during coding, in order to use the word boundary, the pad byte ("00") 1 byte long tends to follow behind the end marker code of each stripe. This must be eliminated externally.
 2. When starting decoding of each stripe (during decoding), inputting must start from the leading coded data of SDE (stripe data entity). If necessary, the leading 1 byte is discarded. (In case when the leading portion of coded data of the next stripe is already inputted in LSI (FIFO) or when it is not lined up with the lead boundary during decoding of each stripe ends, external management is needed.)
 3. Management of marker codes (AT MOVE, NEWLEN, etc.) processing (insertion at the time of coding and detection/removing at the time of decoding) should be done externally.

Description

If the end marker of the stripe one before is SDNORM, do not initialize the line memory nor the context table RAM. The AT pixel position will use the last value of the previous stripe and starts processing next stripe. In case of SDRST, initialization takes place first and then the AT pixel position is returned to the default position. Then the processing of the next stripe begins.

Timing Characteristics 1

(Ta = -20 to +70°C, V_{CC} = 5 V ± 10% unless otherwise noted)

1) Host Bus I/F

Item	Symbol	Limits			Unit	Test Circuit	Test Conditions
		Min	Typ	Max			
D0 to 15 output define time for $\overline{\text{RD}}$ assert	t _{PZL} (RD-D0 to 15)	0	—	30	ns	1	C _L = 50 pF
	t _{PZH} (RD-D0 to 15)	0	—	30	ns		
D0 to 15 output hold time for $\overline{\text{RD}}$ assert	t _{PLZ} (RD-D0 to 15)	0	—	30	ns		
	t _{PHZ} (RD-D0 to 15)	0	—	30	ns		
DMARQ negate time for $\overline{\text{DMAAK}}$ assert	t _{PHL} (DMAAK-DMARQ)	—	—	20	ns		

2) Image Data I/F

Item	Symbol	Limits			Unit	Test Circuit	Test Conditions
		Min	Typ	Max			
$\overline{\text{PRDY}}$ negate time for $\overline{\text{PTIM}}$ assert	t _{PLH} (PTIM-PRDY)	—	—	30	ns	1	C _L = 50 pF
$\overline{\text{RVID}}$ output define time for the fall of $\overline{\text{PXCK}}$	t _{PHL} (PXCK-RVID)	—	—	25	ns		
	t _{PLH} (PXCK-RVID)	—	—	25	ns		
PXCKO delay time for $\overline{\text{PXCK}}$	t _{PHL} (PXCK-PXCKO)	—	—	15	ns		
	t _{PLH} (PXCK-PXCKO)	—	—	15	ns		
$\overline{\text{RVID}}$ output define time for the fall of $\overline{\text{PXCKO}}$	t _{PHL} (PXCKO-RVID)	—	—	10	ns		
	t _{PLH} (PXCKO-RVID)	—	—	10	ns		
$\overline{\text{RVID}}$ negate time for $\overline{\text{PTIM}}$ negate	t _{PLH} (PTIM-RVID)	0	—	—	ns		
$\overline{\text{PDRQ}}$ negate time for $\overline{\text{PDAK}}$ assert	t _{PHL} (PDAK-PDRQ)	—	—	20	ns		
PD0 to 31 output define time for $\overline{\text{PDRD}}$ assert	t _{PZL} (PDRD-PD0 to 31)	0	—	30	ns		
	t _{PZH} (PDRD-PD0 to 31)	0	—	30	ns		
PD0 to 31 hold time for $\overline{\text{PDRD}}$ negate	t _{PLZ} (PDRD-PD0 to 31)	0	—	30	ns		
	t _{PHZ} (PDRD-PD0 to 31)	0	—	30	ns		

3) Context I/F

Item	Symbol	Limits			Unit	Test Circuit	Test Conditions
		Min	Typ	Max			
$\overline{\text{XRDY}}$ negate time for $\overline{\text{XTIM}}$ assert time	t_{PLH} ($\overline{\text{XTIM}}\text{-}\overline{\text{XRDY}}$)	—	—	30	ns	1	$C_L = 50 \text{ pF}$
$\overline{\text{RPIX}}$ output define time for the fall of $\overline{\text{XCLK}}$	t_{PLH} ($\overline{\text{XCLK}}\text{-}\overline{\text{RPIX}}$)	0	—	30	ns		
	t_{PHL} ($\overline{\text{XCLK}}\text{-}\overline{\text{RPIX}}$)	0	—	30	ns		
$\overline{\text{XCLK}}$ delay time for $\overline{\text{MCLK}}$	t_{PLH} ($\overline{\text{MCLK}}\text{-}\overline{\text{XCLK}}$)	—	—	30	ns		
	t_{PHL} ($\overline{\text{MCLK}}\text{-}\overline{\text{XCLK}}$)	—	—	30	ns		

Timing Characteristics 2

(Ta = -20 to +70°C, V_{CC} = 5 V ± 10% unless otherwise noted)

1) Host Bus I/F

Item	Symbol	Limits			Unit	Test Circuit	Test Conditions
		Min	Typ	Max			
RESET assert time	t _w (RESET)	100	—	—	ns	1	C _L = 50 pF
CS set up time for RD assert	t _{su} (RD-CS)	20	—	—	ns		
CS hold time for RD negate	t _h (RD-CS)	20	—	—	ns		
A0 to 3 set up time for RD assert	t _{su} (RD-A0 to 3)	20	—	—	ns		
BHE set up time for RD assert	t _{su} (RD-BHE)	20	—	—	ns		
RD assert time	t _w (RD)	30	—	—	ns		
A0 to 3 hold time for RD negate	t _h (RD-A0 to 3)	20	—	—	ns		
BHE hold time for RD negate	t _h (RD-BHE)	20	—	—	ns		
CS set up time for WR assert	t _{su} (WR-CS)	20	—	—	ns		
CS hold time for WR negate	t _h (WR-CS)	20	—	—	ns		
A0 to 3 set up time for WR assert	t _{su} (WR-A0 to 3)	20	—	—	ns		
BHE set up time for WR assert	t _{su} (WR-BHE)	20	—	—	ns		
WR assert time	t _w (WR)	30	—	—	ns		
A0 to 3 hold time for WR negate	t _h (WR-A0 to 3)	20	—	—	ns		
BHE hold time for WR negate	t _h (WR-BHE)	20	—	—	ns		
D0 to 15 input set up time for WR negate	t _{su} (WR-D0 to 15)	20	—	—	ns		
D0 to 15 input hold time for WR negate	t _h (WR-D0 to 15)	20	—	—	ns		
DMAAK set up time for RD assert	t _{su} (RD-DMAAK)	20	—	—	ns		
DMAAK hold time for RD negate	t _h (RD-DMAAK)	20	—	—	ns		
DMAAK set up time for WR assert	t _{su} (WR-DMAAK)	20	—	—	ns		
DMAAK hold time for WR negate	t _h (WR-DMAAK)	20	—	—	ns		

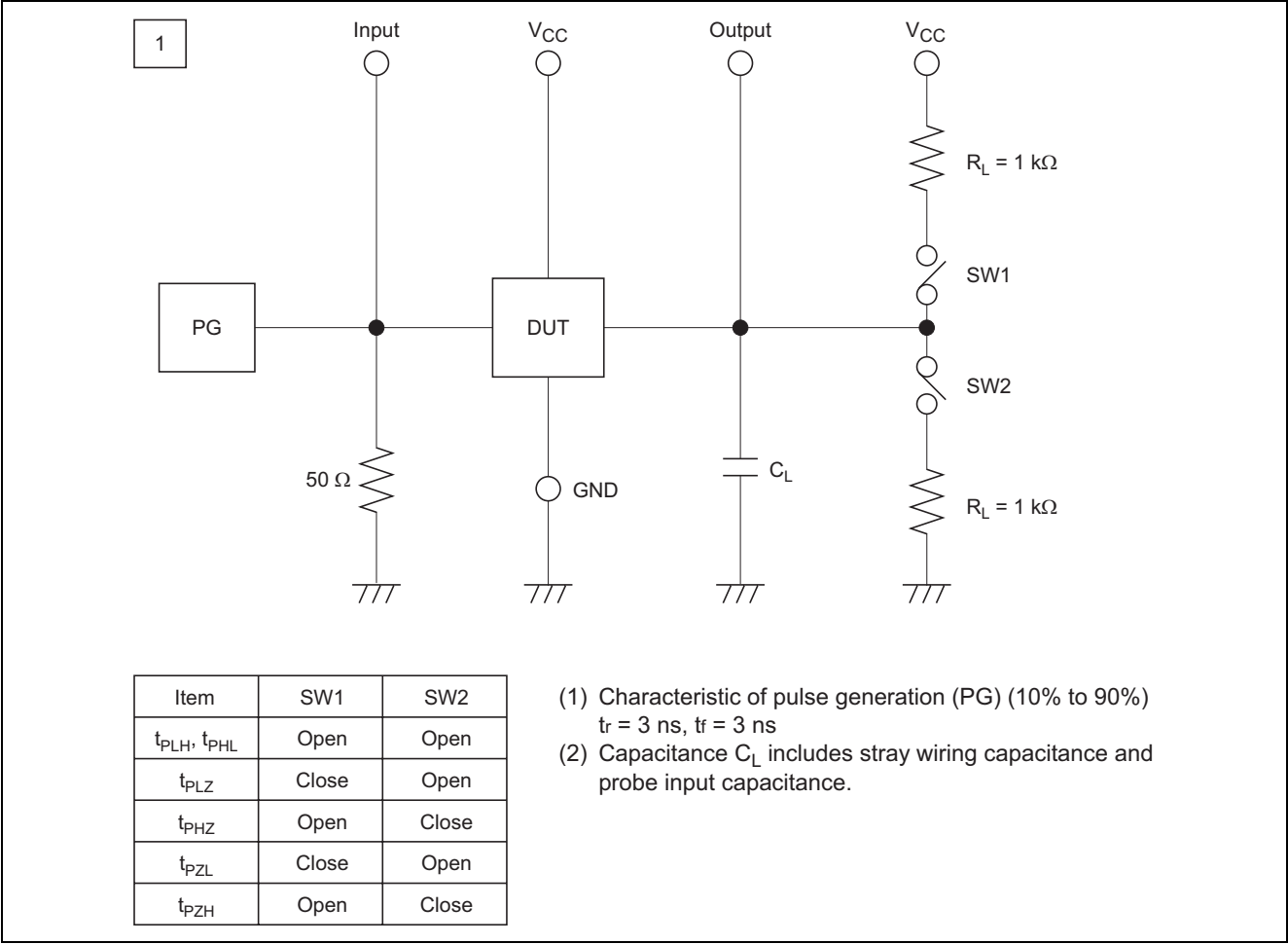
2) Image Data I/F

Item	Symbol	Limits			Unit	Test Circuit	Test Conditions
		Min	Typ	Max			
MCLK period (Mx) when used image data I/F	t_{ci} (MCLK)	50	—	—	ns	1	$C_L = 50 \text{ pF}$
MCLK high level time (Mh) when used image data I/F	t_{wi+} (MCLK)	20	—	—	ns		
MCLK low level time (Ml) when used image data I/F	t_{wi-} (MCLK)	20	—	—	ns		
MCLK rising time when used image data I/F	t_{ri} (MCLK)	—	—	20	ns		
MCLK falling time when used image data I/F	t_{fi} (MCLK)	—	—	20	ns		
PTIM set up time for the fall of $\overline{PXCK}$	t_{su} ($\overline{PXCK}$ -PTIM)	20	—	—	ns		
PTIM hold time for the rise of $\overline{PXCK}$	t_h ($\overline{PXCK}$ -PTIM)	20	—	—	ns		
$\overline{PXCK}$ high time	t_{w+} ($\overline{PXCK}$)	20	—	—	ns		
$\overline{PXCK}$ low time	t_{w-} ($\overline{PXCK}$)	20	—	—	ns		
$\overline{PXCK}$ period	t_c ($\overline{PXCK}$)	50	—	—	ns		
SVID set up time for the fall of $\overline{PXCK}$	t_{su} ($\overline{PXCK}$ -SVID)	10	—	—	ns		
SVID hold time for the rise of $\overline{PXCK}$	t_h ($\overline{PXCK}$ -SVID)	10	—	—	ns		
PDAK set up time for PDRD assert	t_{su} (PDRD-PDAK)	20	—	—	ns		
PDAK hold time for $\overline{PDRD}$ negate	t_h ($\overline{PDRD}$ -PDAK)	20	—	—	ns		
$\overline{PDRD}$ assert time	t_w ($\overline{PDRD}$)	30	—	—	ns		
PDAK set up time for PDWR assert	t_{su} (PDWR-PDAK)	20	—	—	ns		
PDAK hold time for PDWR negate	t_h (PDWR-PDAK)	20	—	—	ns		
$\overline{PDWR}$ assert time	t_w ($\overline{PDWR}$)	20	—	—	ns		
PD0 to $\overline{31}$ input set up time for $\overline{PDWR}$ negate	t_{su} ($\overline{PDWR}$ -PD0 to 31)	20	—	—	ns		
PD0 to $\overline{31}$ input hold time for $\overline{PDWR}$ negate	t_h ($\overline{PDWR}$ -PD0 to 31)	20	—	—	ns		

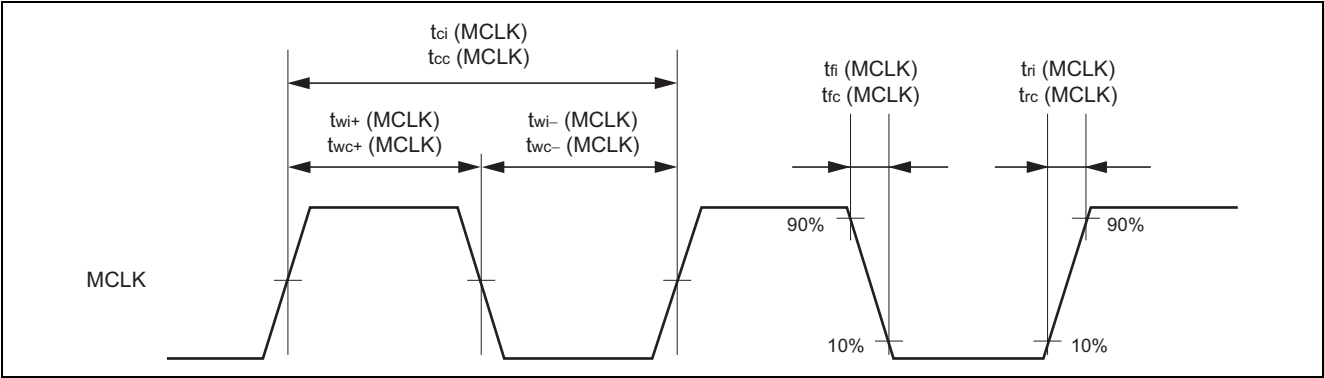
3) Context I/F

Item	Symbol	Limits			Unit	Test Circuit	Test Conditions
		Min	Typ	Max			
MCLK period (Mx) when used context I/F	t_{cc} (MCLK)	100	—	—	ns	1	$C_L = 50 \text{ pF}$
MCLK high level time (Mh) when used context I/F	t_{wc+} (MCLK)	40	—	—	ns		
MCLK low level time (Ml) when used context I/F	t_{wc-} (MCLK)	40	—	—	ns		
MCLK rising time when used context I/F	t_{rc} (MCLK)	—	—	20	ns		
MCLK falling time when used context I/F	t_{fc} (MCLK)	—	—	20	ns		
$\overline{XTIM}$ assert time for the rise of MCLK	t_{su} (MCLK- $\overline{XTIM}$)	20	—	—	ns		
$\overline{XTIM}$ negate time for the rise of XCLK	t_{h} (XCLK- $\overline{XTIM}$)	—	—	20	ns		
XCLK high time	t_{w+} (XCLK)	—	Mh	—	ns		
XCLK low time	t_{w-} (XCLK)	—	MI	—	ns		
$\overline{XCLK}$ period	t_c (XCLK)	—	Mx	—	ns		
$\overline{XWAIT}$ negate time for the rise of XCLK	t_{h} (XCLK- $\overline{XWAIT}$)	0	—	10	ns		
$\overline{CX0}$ to $\overline{11}$ set up time for the rise of XCLK	t_{sul} (XCLK-CX0 to 11)	20	—	—	ns		
PEUPE set up time for the rise of XCLK	t_{sul} (XCLK-PEUPE)	20	—	—	ns		
SPIX set up time for the rise of XCLK	t_{sul} (XCLK-SPIX)	20	—	—	ns		
$\overline{CX0}$ to $\overline{11}$ hold time for the rise of XCLK	t_{hl} (XCLK-CX0 to 11)	20	—	—	ns		
PEUPE hold time for the rise of XCLK	t_{hl} (XCLK-PEUPE)	20	—	—	ns		
SPIX hold time for the rise of XCLK	t_{hl} (XCLK-SPIX)	20	—	—	ns		
$\overline{CX0}$ to $\overline{11}$ set up time for the rise of $\overline{XCLK}$	t_{sut} (XCLK-CX0 to 11)	70	—	—	ns		
SPIX set up time for the rise of $\overline{XCLK}$	t_{sut} (XCLK-SPIX)	70	—	—	ns		
$\overline{CX0}$ to $\overline{11}$ hold time for the rise of $\overline{XCLK}$	t_{ht} (XCLK-CX0 to 11)	20	—	—	ns		
SPIX hold time for the rise of $\overline{XCLK}$	t_{ht} (XCLK-SPIX)	20	—	—	ns		
PEUPE input define time for the rise of $\overline{XCLK}$	t_k (XCLK-PEUPE)	—	—	20	ns		

Test Circuit

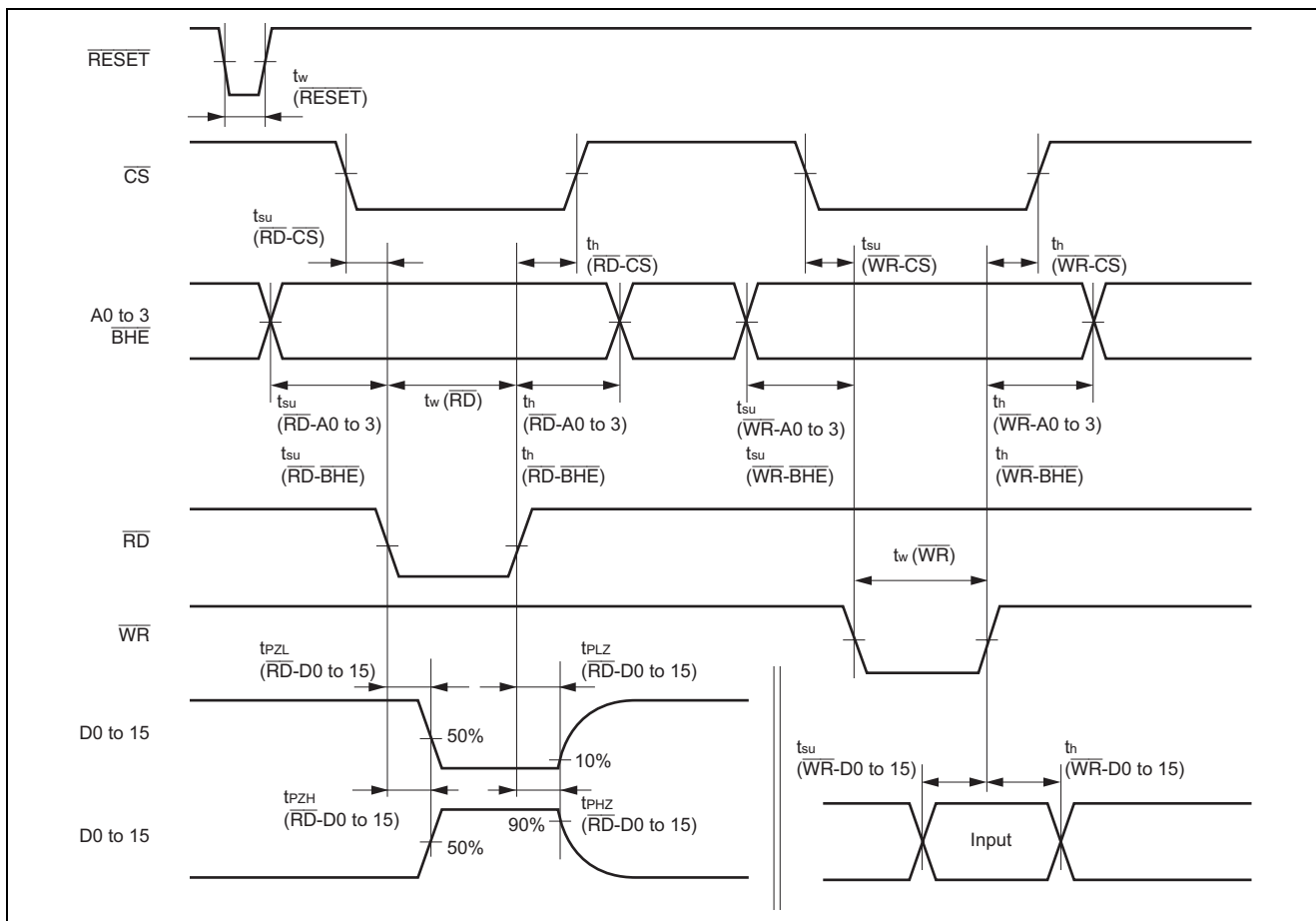


Master Clock



Host Bus I/F

(1) MPU Access



(2) DMA Access

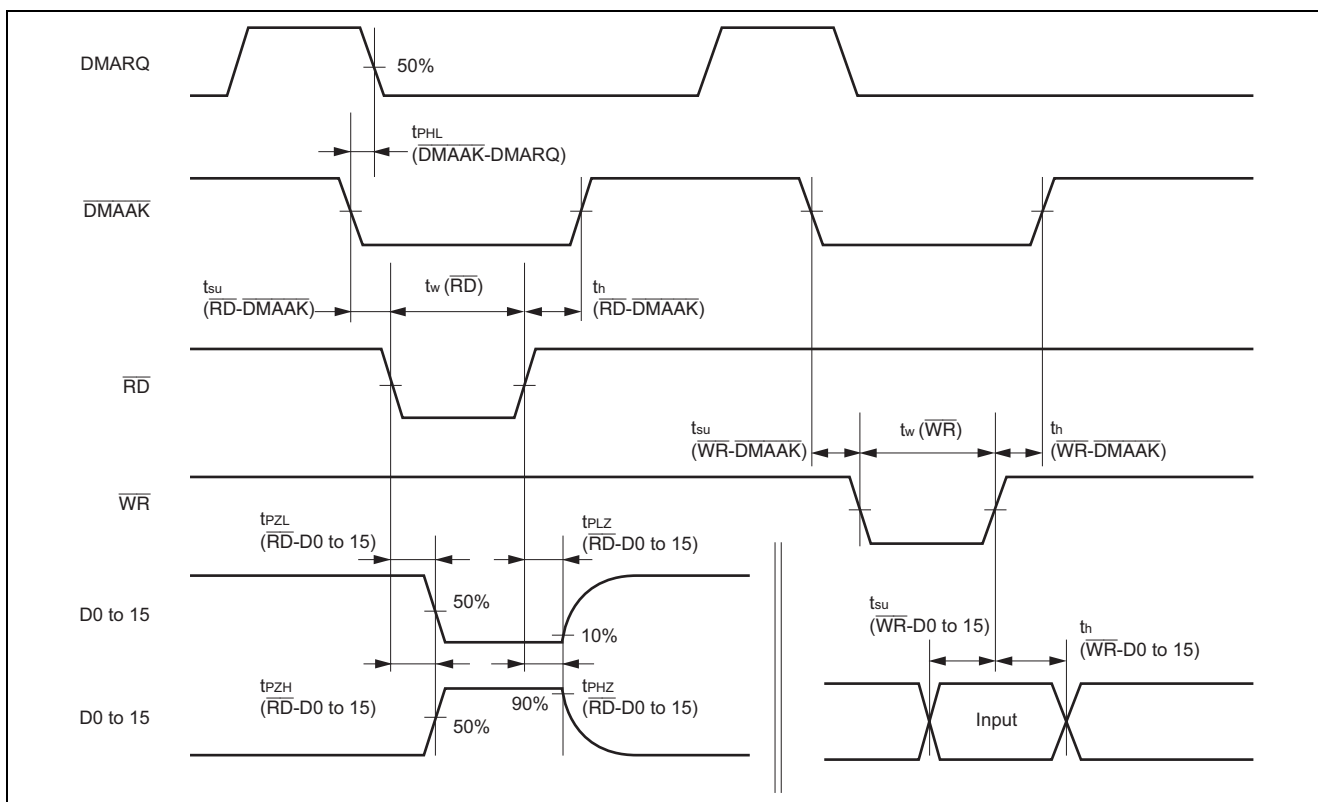
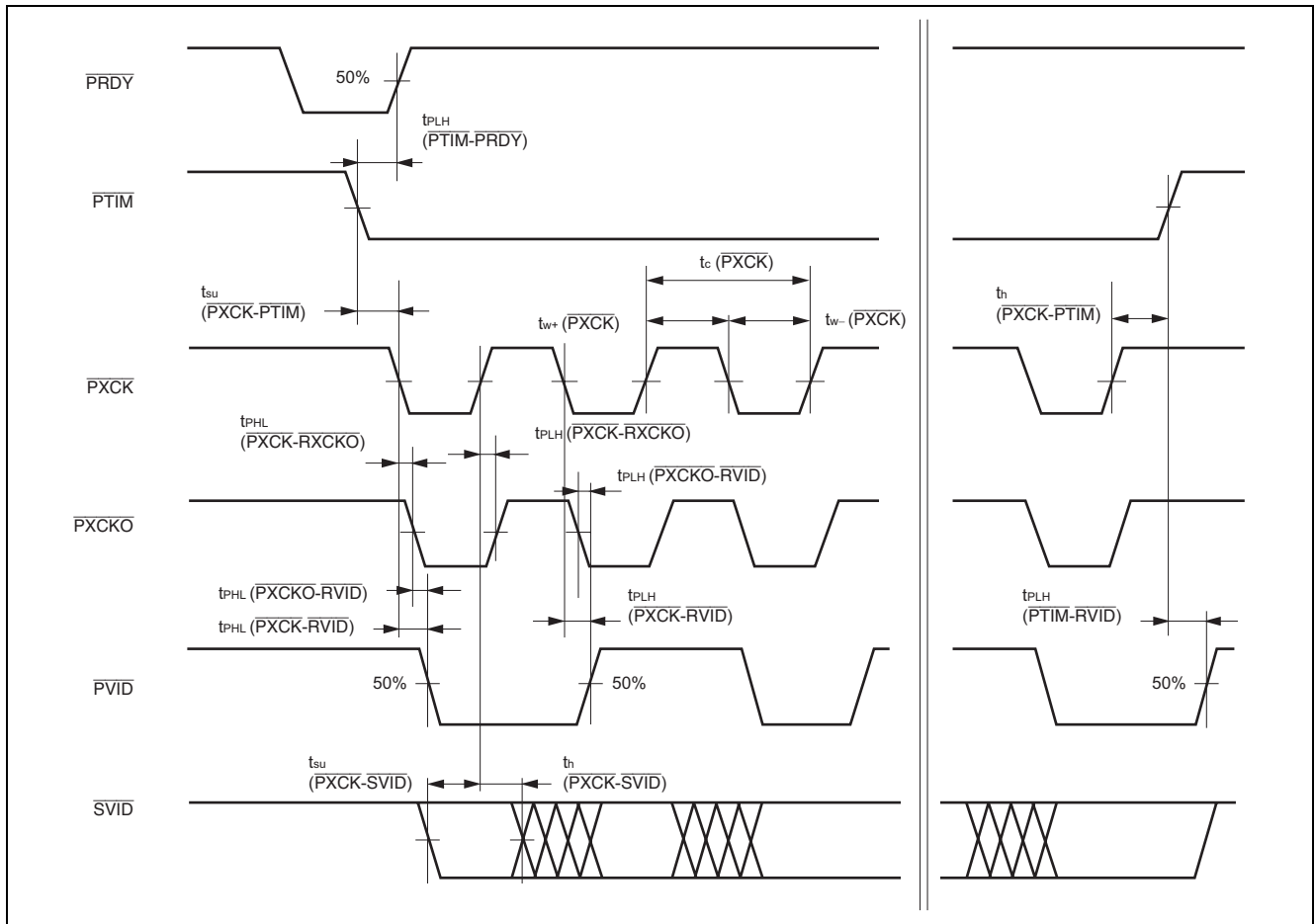
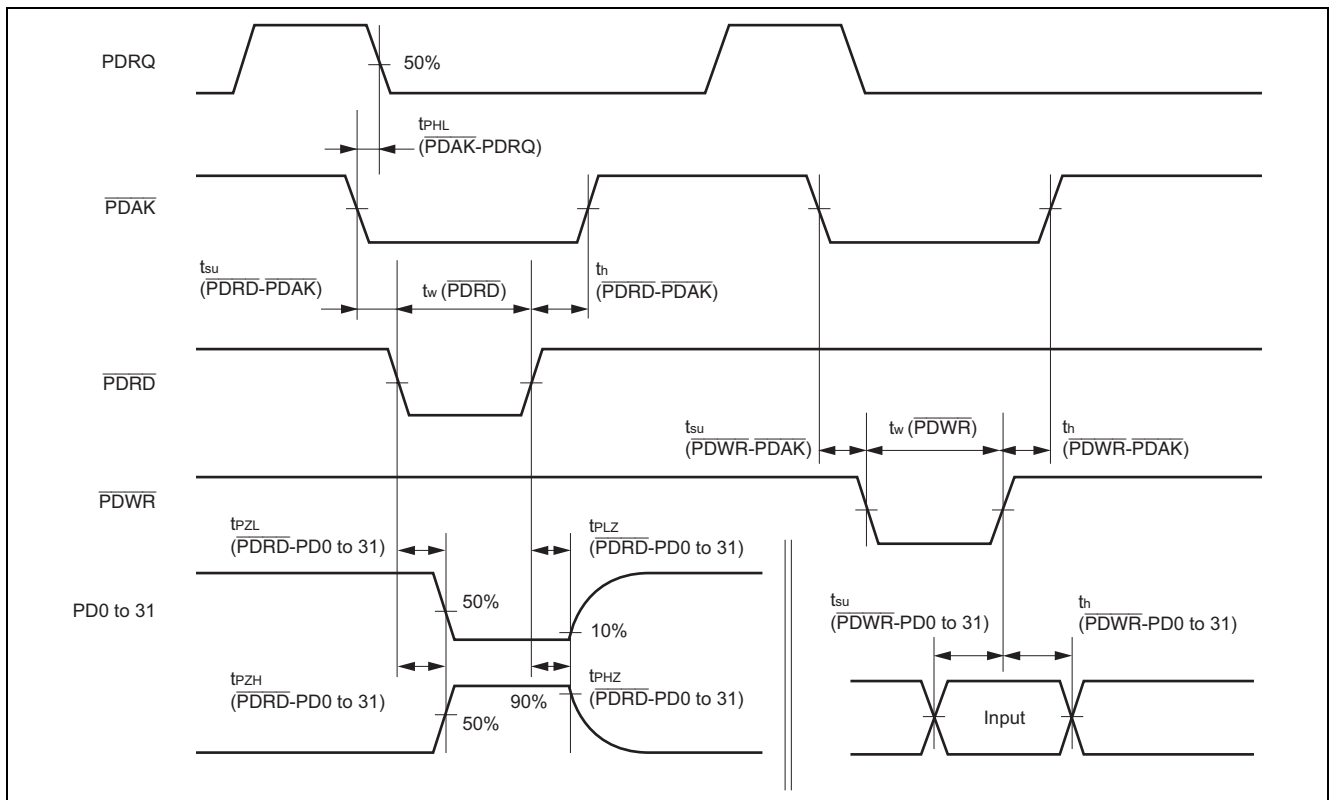


Image Data I/F

(1) Serial Image Data I/F

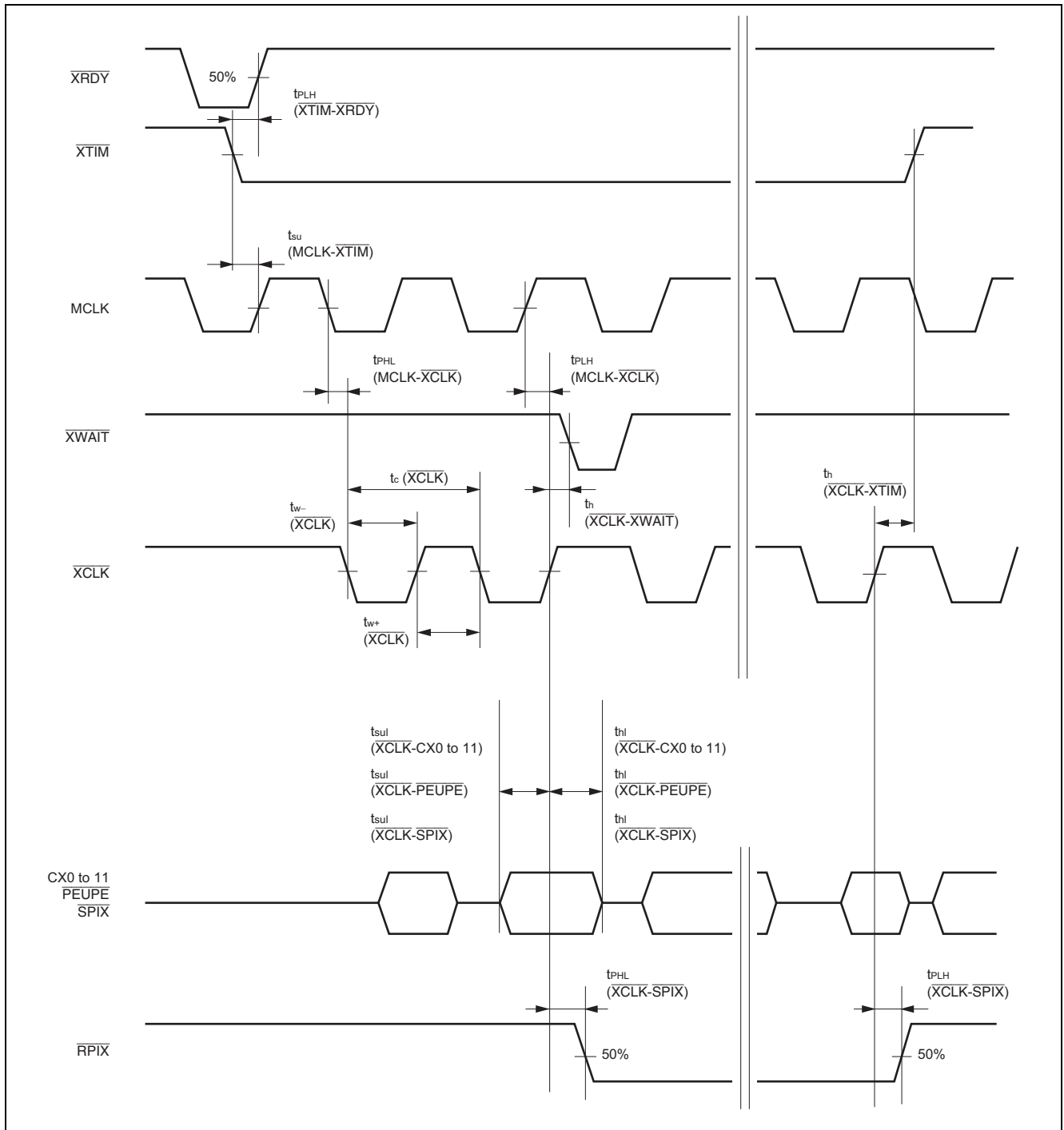


(2) Parallel Image Data

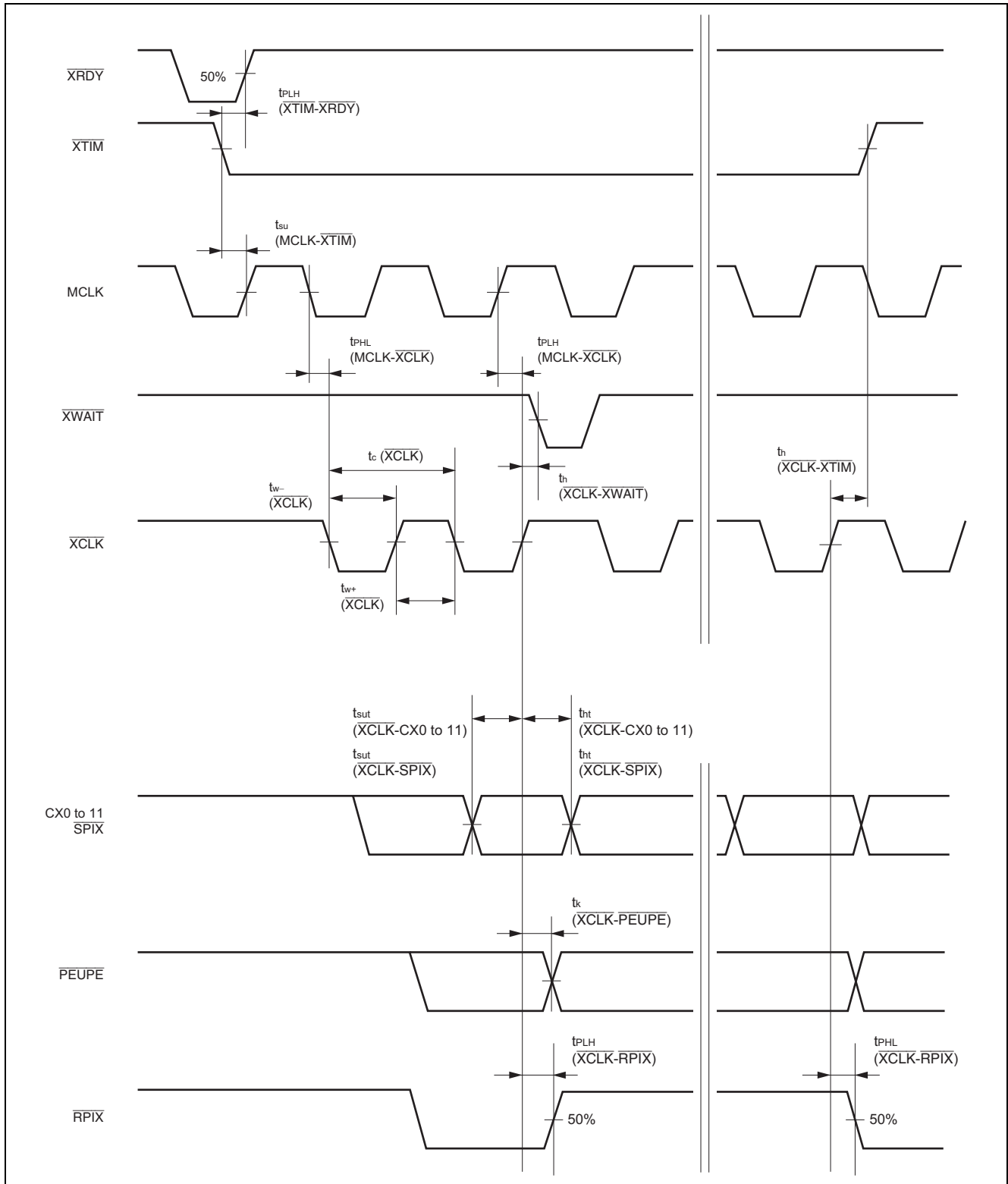


Context I/F

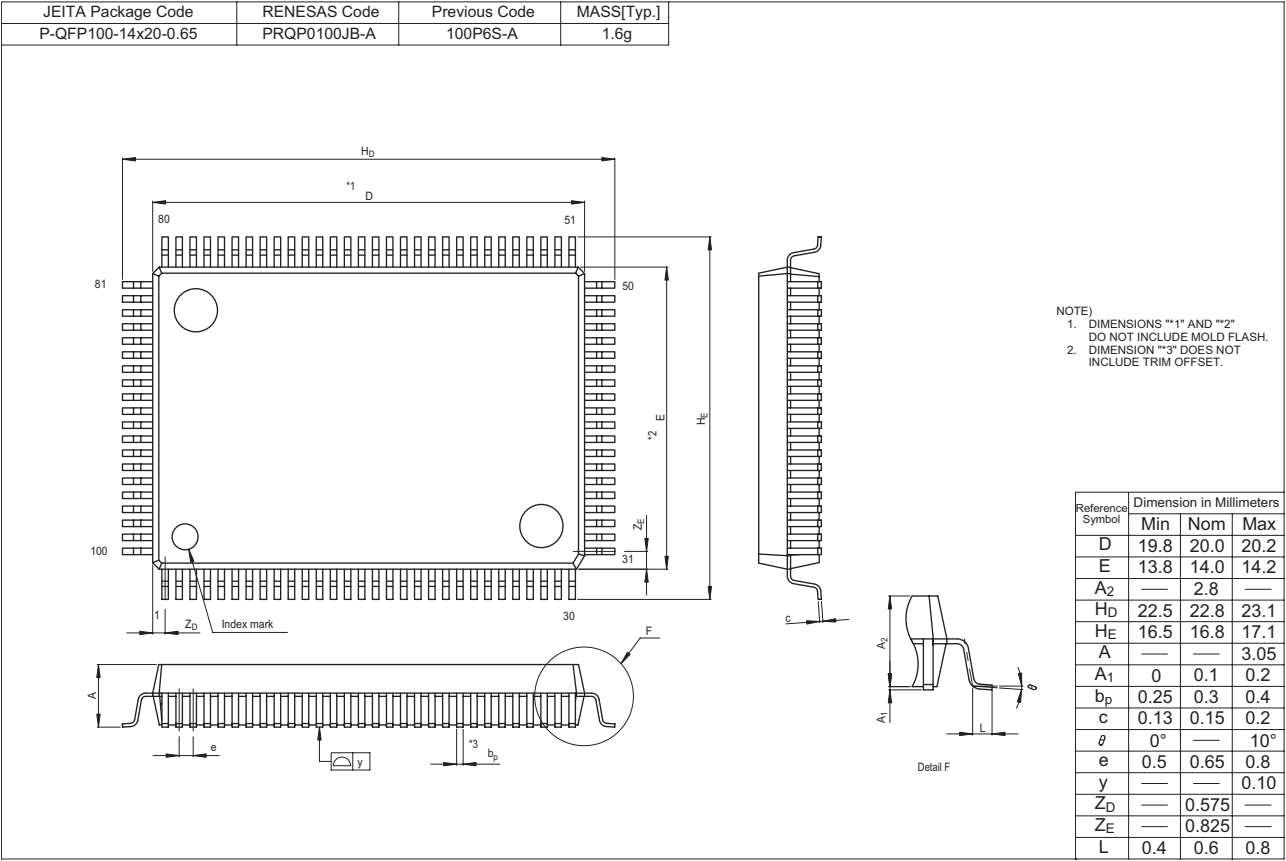
(1) Latch Input Mode



(2) Through Input Mode



Package Dimensions



Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510