**KK4052B**

# Analog Multiplexer Demultiplexer
## High-Performance Silicon-Gate CMOS

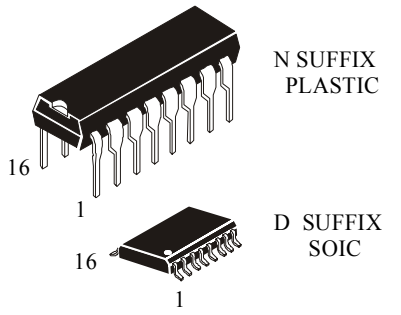
The KK4052B analog multiplexer/demultiplexer is digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20V (if $V_{CC}$ - GND = 3V, a $V_{CC}$ - $V_{EE}$ of up to 13 V can be controlled; for $V_{CC}$ - $V_{EE}$ level differences above 13V a $V_{CC}$ - GND of at least 4.5V is required).

These multiplexer circuits dissipate extremely low quiescent power over the full $V_{CC}$ -GND and $V_{CC}$ - $V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1"is present at the ENABLE input terminal all channels are off.

The IW4052 is a differential 4-channel multiplexer having two binary control inputs. A and B, and an enable input. The two binary input signals select 1 of 4 pairs of channels to turned on and connect the analog inputs to the outputs.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1μA at 18 V over full package-temperature
- range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):

1.0 V min @ 5.0 V supply
2.0 V min @ 10.0 V supply
2.5 V min @ 15.0 V supply




N SUFFIX
PLASTIC

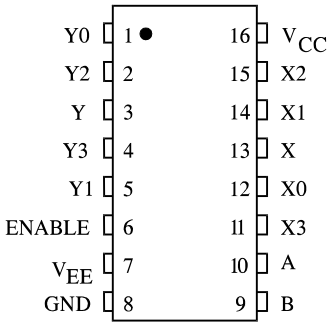
D SUFFIX
SOIC

**ORDERING INFORMATION**

| | |
|---|---|
| **KK4052BN** | Plastic DIP |
| **KK4052BD** | SOIC |

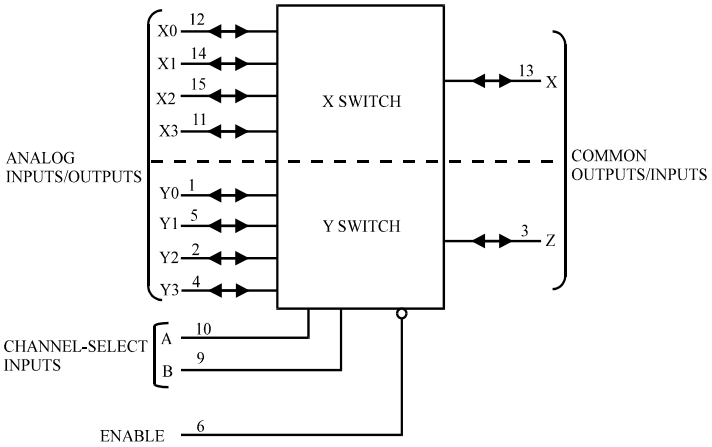
$T_A$ = -55° to 125° C for all packages

## PIN ASSIGNMENT




## LOGIC DIAGRAM

Double-Pole, 4-Position
Plus Common Off




PIN 16 =$V_{CC}$
PIN 7 = $V_{EE}$
PIN 8 = GND

## FUNCTION TABLE

| Control Inputs | | | ON Channels | |
|---|---|---|---|---|
| Enable | Select | | | |
| | B | A | | |
| L | L | L | Y0 | X0 |
| L | L | H | Y1 | X1 |
| L | H | L | Y2 | X2 |
| L | H | H | Y3 | X3 |
| H | X | X | None | |

H = high level
L = low level
X = don't care

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | -0.5 to +20 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC}$ +0.5 | V |
| $I_{IN}$ | DC Input Current, per Pin | ±10 | mA |
| $P_D$ | Power Dissipation in Still Air | 500*[1] | mW |
| $P_{tot}$ | Power Dissipation per Output Transistor | 100 | mW |
| Tstg | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SO Package) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*[1] - for Plastic DIP from -55° to +100°C, for SO Package from -55° to +65°C.
+Derating - Plastic DIP: - 12 mW/°C from 100° to 125°C
SO Package: - 7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 3.0 | 18 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | -55 | +125 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND≤($V_{IN}$ or $V_{OUT}$)≤$V_{CC}$.

Unused digital pins must be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused Analog I/O pins may be left open or terminated.

## DC ELECTRICAL CHARACTERISTICS Digital Section

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | ≥ -55 °C | ≤ 25 °C | ≤ 125 °C | |
| $V_{IH}$ | Minimum High-Level Input Voltage, Channel-Select or Enable Inputs | $V_{IS}$=$V_{CC}$ thru 1kΩ<br>$V_{EE}$=GND=0<br>$I_{IS}$<2μA on all OFF Chanels<br>$R_L$=1kΩ to GND | 5<br>10<br>15 | 3.5<br>7<br>11 | 3.5<br>7<br>11 | 3.5<br>7<br>11 | V |
| $V_{IL}$ | Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs | $V_{IS}$=$V_{CC}$ thru 1kΩ<br>$V_{EE}$=GND=0<br>$I_{IS}$<2μA on all OFF Chanels<br>$R_L$=1kΩ to GND | 5<br>10<br>15 | 1.5<br>3<br>4 | 1.5<br>3<br>4 | 1.5<br>3<br>4 | V |
| $I_{IN}$ | Maximum Input Leakage Current, Channel-Select or Enable Inputs | $V_{IN}$=$V_{CC}$ or GND<br>$V_{EE}$=GND=0 | 18 | ±0.1 | ±0.1 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | Channel Select = $V_{CC}$ or GND<br>$V_{EE}$=GND=0 | 5<br>10<br>15<br>20 | 5<br>10<br>20<br>100 | 5<br>10<br>20<br>100 | 150<br>300<br>600<br>3000 | μA |

## DC ELECTRICAL CHARACTERISTICS Analog Section

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | ≥ -55 °C | ≤ 25 °C | ≤ 125 °C | |
| $R_{ON}$ | Maximum "ON" Resistance | $V_{EE}$=GND=0<br>$V_{IS}$ = GND to $V_{CC}$ | 5<br>10<br>15 | 800<br>310<br>200 | 1050<br>400<br>240 | 1150<br>550<br>320 | Ω |
| $\Delta R_{ON}$ | Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package | $V_{EE}$=GND=0 | 5<br>10<br>15 | -<br>-<br>- | 10*<br>15*<br>5* | -<br>-<br>- | Ω |
| $I_{OFF}$ | Maximum Off- Channel Leakage Current, Any One Channel | $V_{EE}$=GND=0 | 18 | ±100 | ±100 | ±1000 | nA |
| | Maximum Off- Channel Leakage Current, Common Channel | $V_{EE}$=GND=0 | 18 | ±100 | ±100 | ±1000 | |

* - Typical Value

## AC ELECTRICAL CHARACTERISTICS ($C_L$=50pF,Input $t_r$=$t_f$=20.0 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit ≥ -55 °C | Guaranteed Limit ≤ 25 °C | Guaranteed Limit ≤ 125 °C | Unit |
|---|---|---|---|---|---|---|
| $t_{PHL}$($t_{PLH}$) | Maximum Propagation Delay , Analog Input to Analog Output (Figure 1)<br>$R_L$=200kΩ, $V_{EE}$=GND=0 | 5<br>10<br>15 | 60<br>30<br>20 | 60<br>30<br>20 | 70<br>40<br>30 | ns |
| $t_{PHL1}$($t_{PLH1}$) | Maximum Propagation Delay , Channel-Select Input to Analog Output (Figure 1)<br>$R_L$=200 kΩ, $V_{EE}$=GND=0 | 5<br>10<br>15 | 350<br>200<br>160 | 350<br>200<br>160 | 400<br>250<br>200 | ns |
| $t_{PZL1}$($t_{PZH1}$) | Maximum Propagation Delay , Channel-Select Input to Analog Output<br>(Figure 2) $R_L$=10 kΩ<br>$V_{EE}$=GND=0 | 5<br>10<br>15 | 720<br>320<br>240 | 720<br>320<br>240 | 720<br>320<br>240 | ns |
| | $V_{EE}$=-5B, GND=0 | 5 | 450 | 450 | 450 | |
| $t_{PZL2}$($t_{PZH2}$) | Maximum Propagation Delay , Enable to Analog Output<br>(Figure 2) $R_L$=10 kΩ<br>$V_{EE}$=GND=0 | 5<br>10<br>15 | 720<br>320<br>240 | 720<br>320<br>240 | 720<br>320<br>240 | ns |
| | $V_{EE}$=-10B, GND=0 | 5 | 400 | 400 | 400 | |
| $t_{PLZ1}$($t_{PHZ1}$) | Maximum Propagation Delay , Channel-Select Input to Analog Output<br>(Figure 2) $R_L$=10 kΩ<br>$V_{EE}$=GND=0 | 5<br>10<br>15 | 720<br>320<br>240 | 720<br>320<br>240 | 720<br>320<br>240 | ns |
| | $V_{EE}$=-5B, GND=0 | 5 | 450 | 450 | 450 | |
| $t_{PLZ2}$($t_{PHZ2}$) | Maximum Propagation Delay , Enable to Analog Output<br>(Figure 2) $R_L$=1,0 kΩ<br>$V_{EE}$=GND=0 | 5<br>10<br>15 | 450<br>210<br>160 | 450<br>210<br>160 | 450<br>210<br>160 | ns |
| | $V_{EE}$=-10B, GND=0 | 5 | 300 | 300 | 600 | |
| $C_{IN}$ | Maximum Input Capacitance, Channel-Select or Enable Inputs | - | - | 7.5 | - | pF |
| $C_{I/O}$ | Maximum Capacitance<br>$V_{EE}$=GND=-5V<br>$C_{IS}$ | 5 | - | 5* | - | pF |
| | $C_{OS}$ | 5 | - | 18* | - | |
| | Feedthrough $C_{IOS}$ | 5 | - | 0.2* | - | |

## ADDITIONAL APPLICATION CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | $V_{IS}$** V | Limits Typical Value 25 °C | Unit |
|---|---|---|---|---|---|---|
| $B_W$ | Maximum On-Channel Bandwidth or Minimum Frequency Response (-3db) | $V_{EE}$=GND=0<br>$R_L$=1kΩ<br>20 log($V_{OS}$/$V_{IS}$)=-3db<br>$V_{OS}$ at Common OUT/IN | 10 | 2,5 | 20 | MHz |
| | | $V_{OS}$ at Any Channel | 10 | 2,5 | 60 | |
| $f_1$ | (-40db) Feedthrough Frequency (All Channels OFF) | $V_{EE}$=GND=0<br>$R_L$=1kΩ<br>20 log($V_{OS}$/$V_{IS}$)=-40db<br>$V_{OS}$ at Common OUT/IN | 10 | 2,5 | 12 | MHz |
| | | $V_{OS}$ at Any Channel | 10 | 2,5 | 8 | |
| $f_2$ | (-40db) Signal Crosstalk Frequency | $V_{EE}$=GND=0<br>$R_L$=1kΩ<br>20 log($V_{OS}$/$V_{IS}$)=-40db<br>Between Sections :<br>Measured on Common<br>Measured on Any Chanel | <br><br><br><br>10<br>10 | <br><br><br><br>2,5<br>2,5 | <br><br><br><br>6<br>10 | MHz |
| THD | Total Harmonic Distortion | $V_{EE}$=GND=0<br>$f_{IS}$=1kHz sine wave | 5<br>10<br>15 | 1<br>1,5<br>2,5 | 0.3<br>0.2<br>0.12 | % |
| $V_{AO/I}$ | Address-or Enable to Signal Crosstalk | $V_{EE}$=GND=0, $R_L$=10kΩ***<br>$t_r$,$t_f$=20ns<br>Square Wave | 10 | - | 65 | mV (Peak) |

** Peak-to-peak voltage symmetrical about ($V_{CC}$-$V_{EE}$)/2.

*** Both ends of channel.

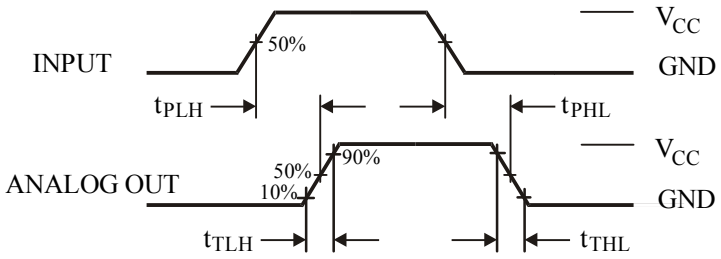



**Figure 1. Switching Waveforms**

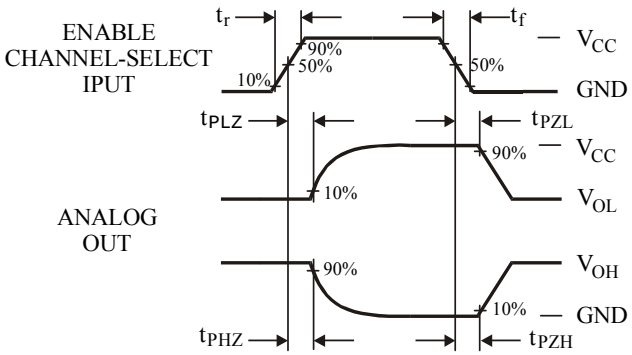
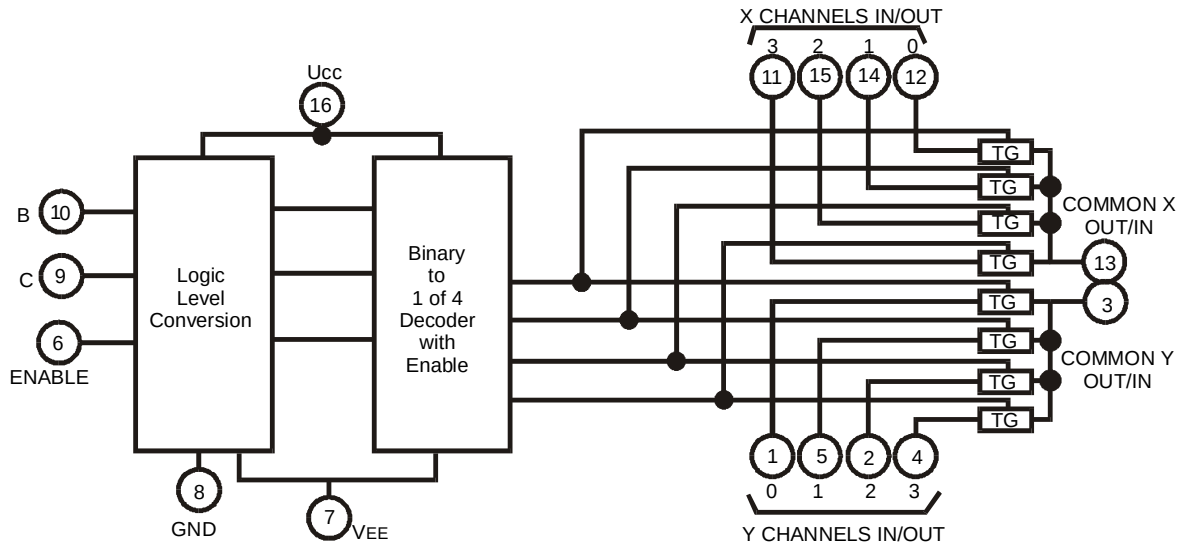
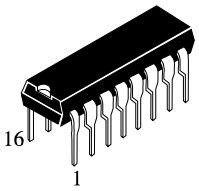


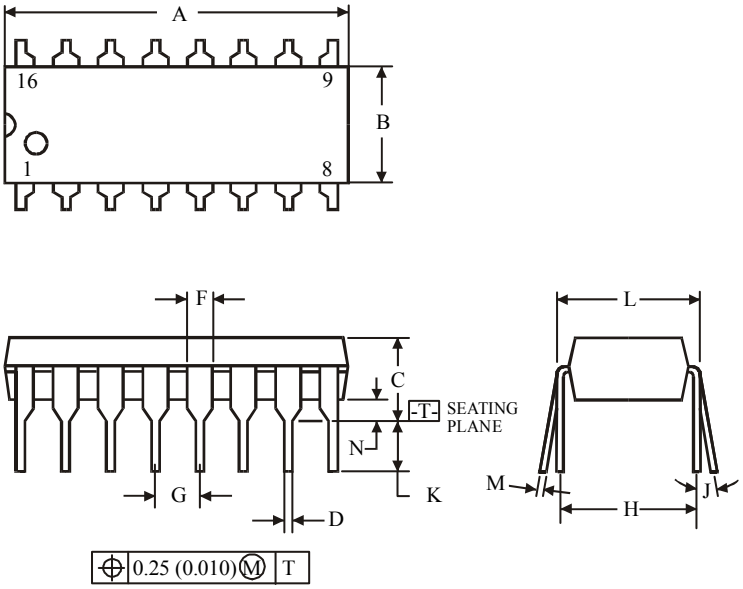

**Figure 2. Switching Waveforms**

## EXPANDED LOGIC DIAGRAM



## N SUFFIX PLASTIC
## (MS - 001BB)



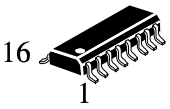



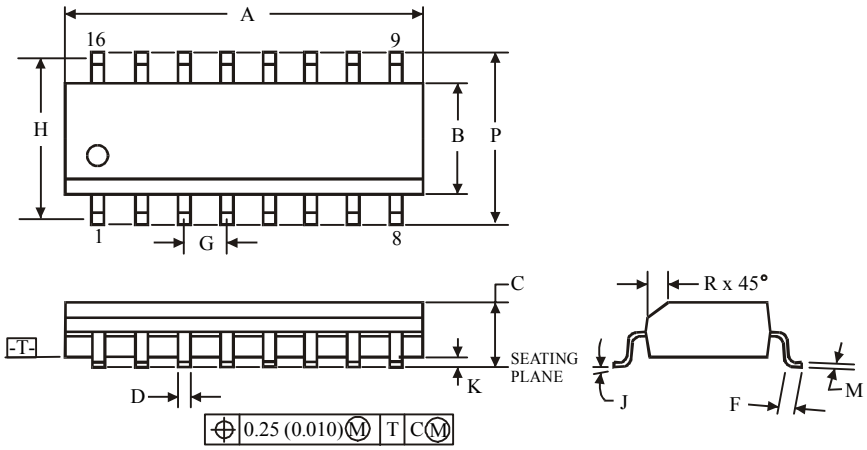

| Symbol | Dimensions, mm | |
|---|---|---|
| | MIN | MAX |
| A | 18.67 | 19.69 |
| B | 6.10 | 7.11 |
| C | | 5.33 |
| D | 0.36 | 0.56 |
| F | 1.14 | 1.78 |
| G | 2.54 | |
| H | 7.62 | |
| J | 0° | 10° |
| K | 2.92 | 3.81 |
| L | 7.62 | 8.26 |
| M | 0.20 | 0.36 |
| N | 0.38 | |

**NOTES:**

1. imensions “A”, “B” do not include mold flash or protrusions. Maximum mold flash or protrusions 0.25 mm (0.010) per side.

## D SUFFIX SOIC
## (MS - 012AC)




| Symbol | Dimensions, mm | |
|---|---|---|
| | MIN | MAX |
| A | 9.80 | 10.0 |
| B | 3.80 | 4.00 |
| C | 1.35 | 1.75 |
| D | 0.33 | 0.51 |
| F | 0.40 | 1.27 |
| G | 1.27 | |
| H | 5.72 | |
| J | 0° | 8° |
| K | 0.10 | 0.25 |
| M | 0.19 | 0.25 |
| P | 5.80 | 6.20 |
| R | 0.25 | 0.50 |

**NOTES:**

1.Dimensions A and B do not include mold flash or protrusion.
2.Maximum mold flash or protrusion 0.15 mm (0.006) per side for A, for B - 0.25 mm (0.010) per side.