

# THS1408-EP

## 14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE AND PGA

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

### Features

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance up to –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **14-Bit Resolution**
- **3- and 8-MSPS Speed Grade**
- **Differential Nonlinearity (DNL) ±0.6 LSB Typ**

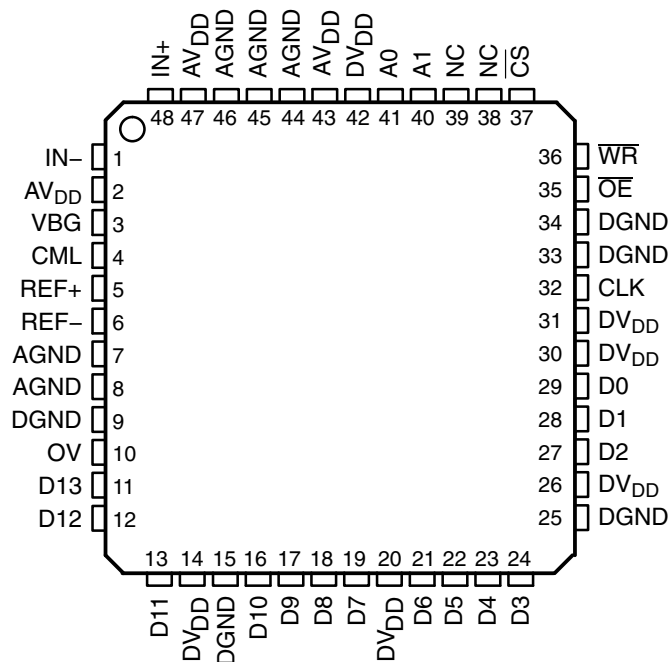
- **Integral Nonlinearity (INL) ±1.5 LSB Typ**
- **Internal Reference**
- **Differential Inputs**
- **Programmable Gain Amplifier**
- **μP-Compatible Parallel Interface**
- **Timing Compatible With TMS320C6000 DSP**
- **3.3-V Single Supply**
- **Power-Down Mode**
- **Monolithic CMOS Design**

### Applications

- **xDSL Front Ends**
- **Communication**
- **Industrial Control**
- **Instrumentation**
- **Automotive and Selected Military**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**PHP PACKAGE  
(TOP VIEW)**



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2010, Texas Instruments Incorporated

# THS1408-EP

## 14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE AND PGA

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

### description

The THS1408 is a 14-bit, 3/8-MSPS single-supply analog-to-digital converter (ADC), with an internal reference, differential inputs, programmable input gain, and an on-chip sample and hold amplifier.

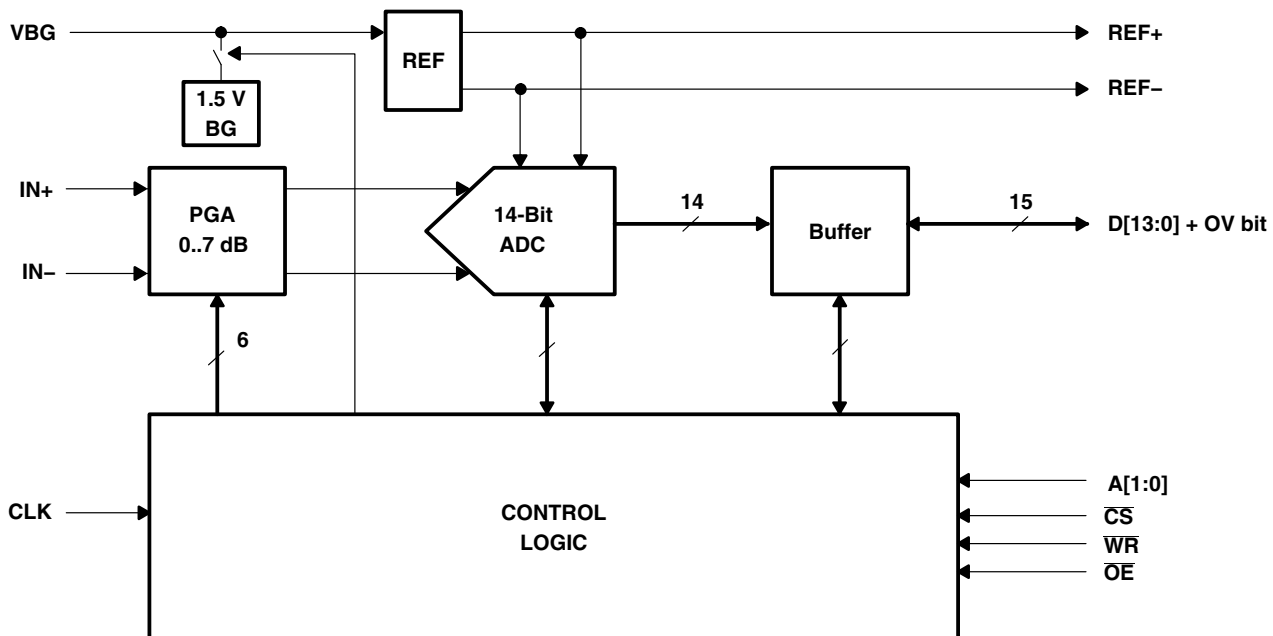
Implemented with a CMOS process, the device has outstanding price/performance and power/speed ratios. The THS1408 is designed for use with 3.3-V systems, and with a high-speed  $\mu$ P-compatible parallel interface, making it the first choice for solutions based on high-performance DSPs like the TI TMS320C6000 series.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PQFP – PHP	THS1408MPHPEP	THS1408ME

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### functional block diagram



**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**Terminal Functions**

TERMINAL NAME NO.		I/O	DESCRIPTION
A[1:0]	40, 41	I	Address input
AGND	7, 8, 44, 45, 46		Analog ground
AV <sub>DD</sub>	2, 43, 47		Analog power supply
CLK	32	I	Clock input
CML	4		Reference midpoint. This pin requires a 0.1- $\mu$ F capacitor to AGND.
$\overline{CS}$	37	I	Chip select input. Active low
DGND	9, 15, 25, 33, 34		Digital ground
DV <sub>DD</sub>	14, 20, 26, 30, 31, 42		Digital power supply
D[13:0]	11, 12, 13, 16, 17, 18, 19, 21, 22, 23, 24, 27, 28, 29	I/O	Data inputs/outputs
NC	38, 39		No connection, do not use. Reserved
IN+	48	I	Positive differential analog input
IN-	1	I	Negative differential analog input
$\overline{OE}$	35	I	Output enable. Active low
OV	10	O	Out of range output
REF+	5	O	Positive reference output. This pin requires a 0.1- $\mu$ F capacitor to AGND.
REF-	6	O	Negative reference output. This pin requires a 0.1- $\mu$ F capacitor to AGND.
VBG	3	I	Reference input. This pin requires a 1- $\mu$ F capacitor to AGND.
$\overline{WR}$	36	I	Write signal. Active low



**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, ( $AV_{DD}$ to AGND)	4 V
Supply voltage, ( $DV_{DD}$ to DGND)	4 V
Reference input voltage range, VBG	-0.3 V to $AV_{DD} + 0.3$ V
Analog input voltage range	-0.3 V to $AV_{DD} + 0.3$ V
Digital input voltage range	-0.3 V to $DV_{DD} + 0.3$ V
Operating free-air temperature range, $T_A$ : Q suffix	-40°C to 125°C
M suffix	-55°C to 125°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**THERMAL CHARACTERISTICS**

	TYP	UNIT
Thermal resistance, junction-to-ambient, $\Theta_{JA}$	28.8	°C/W
Thermal resistance, junction-to-case, $\Theta_{JC}$	0.79	°C/W

† Thermal resistance is modeled data, is not production tested, and is given for informational purposes only.

**recommended operating conditions**

	MIN	NOM	MAX	UNIT	
Supply voltage, $AV_{DD}$ , $DV_{DD}$	3	3.3	3.6	V	
High level digital input, $V_{IH}$	2	3.3		V	
Low level digital input, $V_{IL}$		0	0.8	V	
Load capacitance, $C_L$		5	15	pF	
Clock frequency, $f_{CLK}$	0.1	8	8	MHz	
Clock duty cycle	45%	50%	55%		
Operating free-air temperature	Q suffix	-40	25	125	°C
	M suffix	-55	25	125	



**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

electrical characteristics over recommended operating free-air temperature range,  
 $AV_{DD} = DV_{DD} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power Supply</b>						
$I_{DDA}$	Analog supply current	$AV_{DD} = 3.6\text{ V}$		81	90	mA
$I_{DDD}$	Digital supply current	$DV_{DD} = 3.6\text{ V}$		5	10	mA
	Power	$AV_{DD} = DV_{DD} = 3.6\text{ V}$		270	360	mW
	Power down current			20		$\mu\text{A}$
<b>DC Characteristics</b>						
	Resolution			14		Bits
DNL	Differential nonlinearity			$\pm 0.6$	$\pm 1$	LSB
INL	Integral nonlinearity	THS1408 at 3 MSPS	Best fit	$\pm 2$	$\pm 4$	LSB
		THS1408 at 8 MSPS	Best fit	$\pm 3.5$	$\pm 10.5$	
	Offset error	$IN+ = IN-$ , PGA = 0 dB			0.3	%FSR
	Gain error	PGA = 0 dB			1.75	%FSR
<b>AC Characteristics</b>						
ENOB	Effective number of bits			11.2	11.5	Bits
THD	Total harmonic distortion	$f_i = 100\text{ kHz}$		-81		dB
		$f_i = 1\text{ MHz}$		-78		
		$f_i = 4\text{ MHz}$		-77		
SNR	Signal-to-noise ratio	$f_i = 100\text{ kHz}$		72		dB
		$f_i = 1\text{ MHz}$	70	72		
		$f_i = 4\text{ MHz}$		71		
SINAD	Signal-to-noise ratio + distortion	$f_i = 100\text{ kHz}$		70		dB
		$f_i = 1\text{ MHz}$	69	70		
		$f_i = 4\text{ MHz}$		70		
SFDR	Spurious free dynamic range	$f_i = 100\text{ kHz}$		80		dB
		$f_i = 1\text{ MHz}$	71	80		
		$f_i = 4\text{ MHz}$		80		
	Analog input bandwidth			140		MHz



# THS1408-EP

## 14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE AND PGA

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

electrical characteristics over recommended operating free-air temperature range,  
 $AV_{DD} = DV_{DD} = 3.3\text{ V}$  (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Reference Voltage</b>						
V <sub>BG</sub>	Bandgap voltage, internal mode		1.425	1.5	1.575	V
	Input impedance			40		k $\Omega$
	Positive reference voltage, REF+			2.5		V
	Negative reference voltage, REF-			0.5		V
	Reference difference, $\Delta_{REF}$ , REF+ – REF-			2		V
	Accuracy, internal reference			5%		
	Temperature coefficient			40		ppm/ $^{\circ}$ C
	Voltage coefficient			200		ppm/V
<b>Analog Inputs</b>						
	Positive analog input, IN+		0		$AV_{DD}$	V
	Negative analog input, IN-		0		$AV_{DD}$	V
	Analog input voltage difference	$\Delta A_{in} = IN+ - IN-$ , $V_{ref} = REF+ - REF-$	$-V_{ref}$		$V_{ref}$	V
	Input impedance			25		k $\Omega$
	PGA range		0		7	dB
	PGA step size			1		dB
	PGA gain error				$\pm 0.25$	dB
<b>Digital Inputs</b>						
V <sub>IH</sub>	High-level digital input		2			V
V <sub>IL</sub>	Low-level digital input				0.8	V
	Input capacitance			5		pF
	Input current				$\pm 1$	$\mu$ A
<b>Digital Outputs</b>						
V <sub>OH</sub>	High-level digital output	$I_{OH} = 50\ \mu$ A	2.6			V
V <sub>OL</sub>	Low-level digital output	$I_{OL} = 50\ \mu$ A			0.4	V
I <sub>OZ</sub>	Output current, high impedance				$\pm 10$	$\mu$ A
<b>Clock Timing (CS low)</b>						
f <sub>CLK</sub>	Clock frequency		0.1 <sup>†</sup>	8	8	MHz
t <sub>d</sub>	Output delay time				25	ns
	Latency			9.5		Cycles

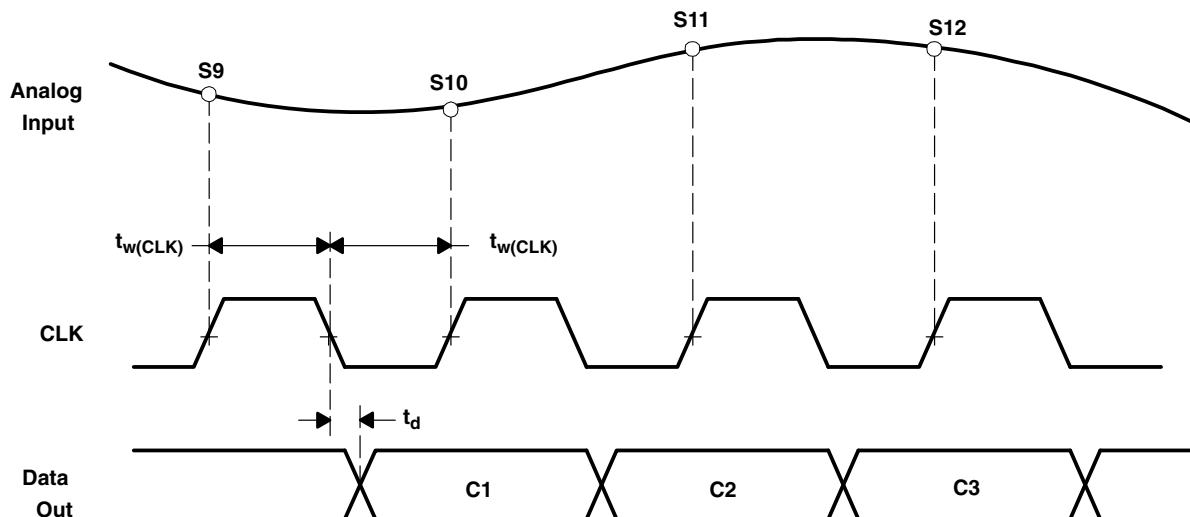
<sup>†</sup> This parameter is not production tested.



**PARAMETER MEASUREMENT INFORMATION**

**sample timing**

The core is based on a pipeline architecture with a latency of 9.5 samples. The conversion results appear on the digital output 9.5 clock cycles after the input signal was sampled.



**Figure 1. Sample Timing**

The parallel interface of the ADC features 3-state buffers, making it possible to directly connect it to a data bus. The output buffers are enabled by driving the OE input low.

Besides the sample results, it is also possible to read back the values of the control register, the PGA register, and the offset register. Which register is read is determined by the address inputs A[1,0]. The ADC results are available at address 0.

The timing of the control signals is described in the following sections.

**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

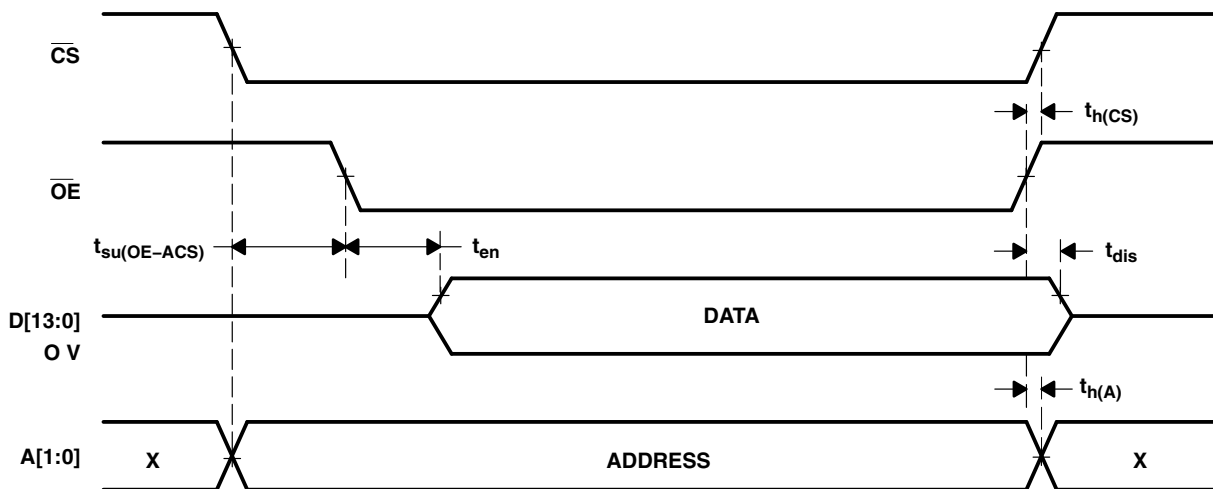
SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**PARAMETER MEASUREMENT INFORMATION**

**read timing (15-pF load)**

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(OE-ACS)}$	Address and chip select setup time	4			ns
$t_{en}$	Output enable			15	ns
$t_{dis}$	Output disable		10		ns
$t_{h(A)}$	Address hold time	1			ns
$t_{h(CS)}$	Chip select hold time	0			ns

NOTE: All timing parameters refer to a 50% level.



**Figure 2. Read Timing**



**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

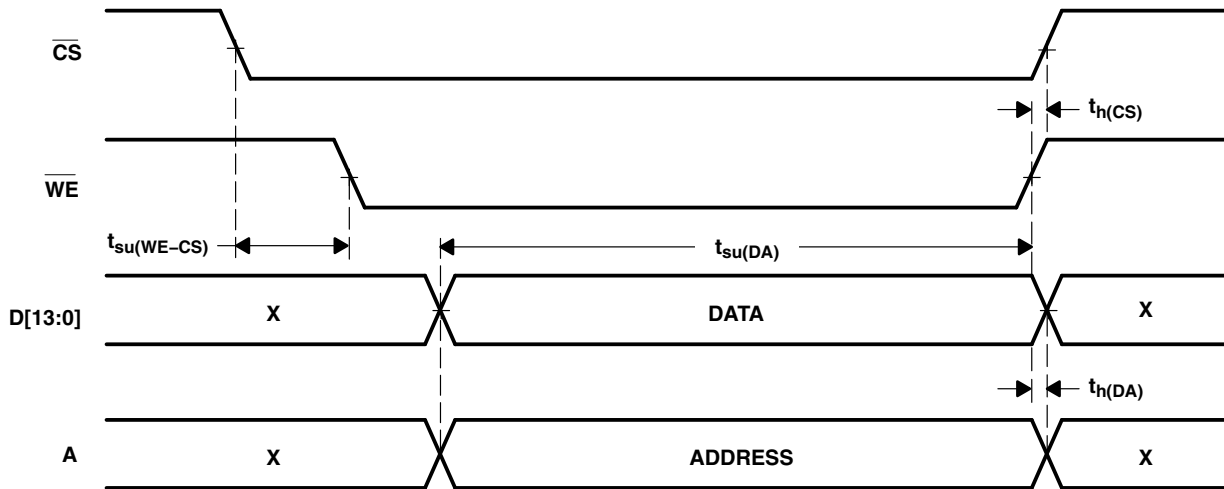
SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**PARAMETER MEASUREMENT INFORMATION**

**write timing (15-pF load)**

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(WE-CS)}$	Chip select setup time	4			ns
$t_{su(DA)}$	Data and address setup time	29			ns
$t_h(DA)$	Data and address hold time	0			ns
$t_h(CS)$	Chip select hold time	0			ns
$t_{wH(WE)}$	Write pulse duration high	15			ns

NOTE: All timing parameters refer to a 50% level.



**Figure 3. Write Timing**

# THS1408-EP 14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE AND PGA

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

## TYPICAL CHARACTERISTICS

POWER  
VS  
FREQUENCY

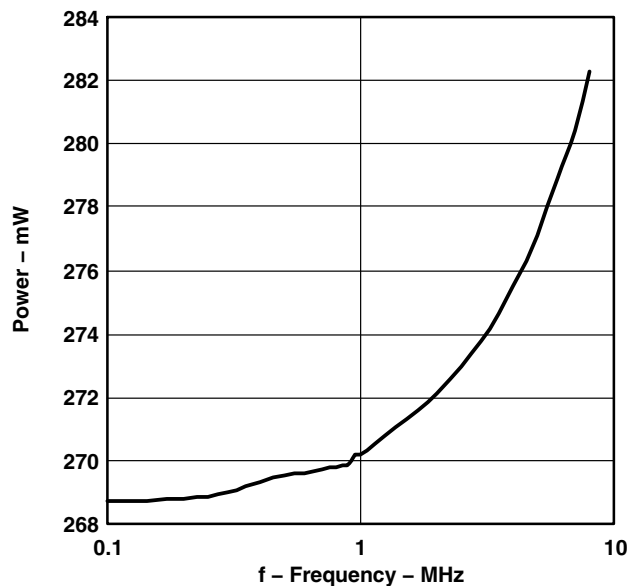


Figure 4

SUPPLY CURRENT  
VS  
TIME

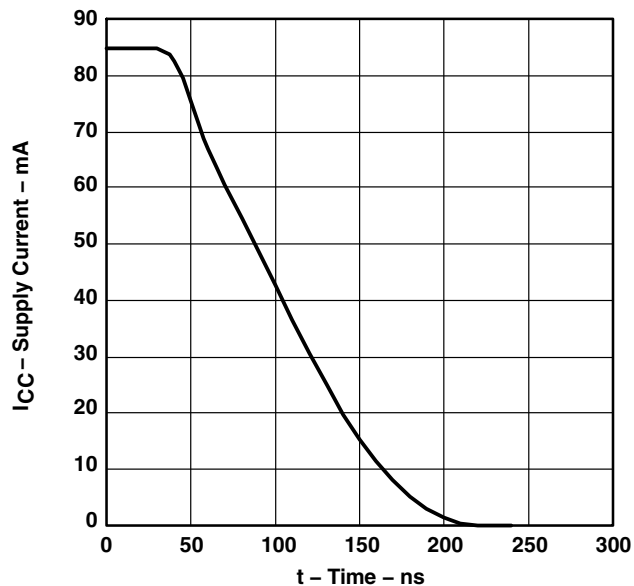


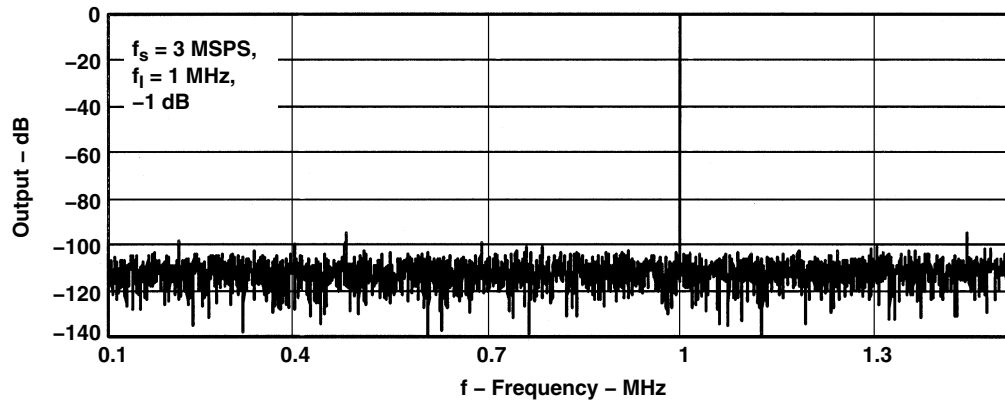
Figure 5

**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

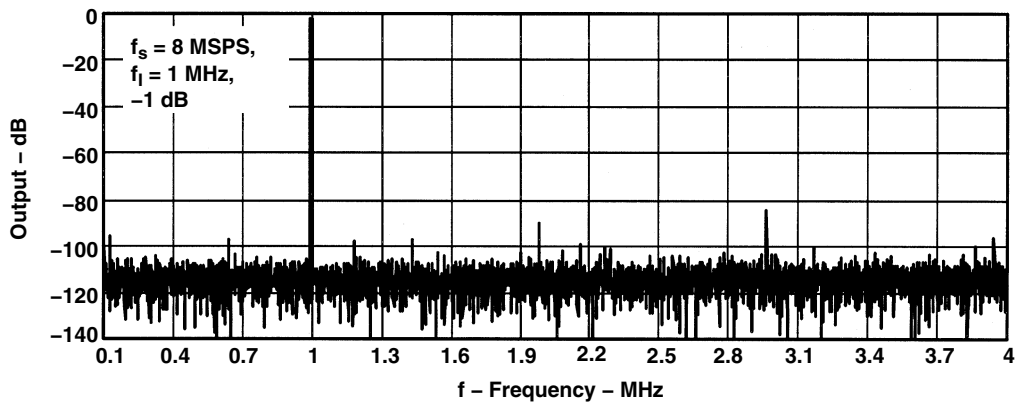
**TYPICAL CHARACTERISTICS**

**FAST FOURIER TRANSFORM**



**Figure 6**

**FAST FOURIER TRANSFORM**

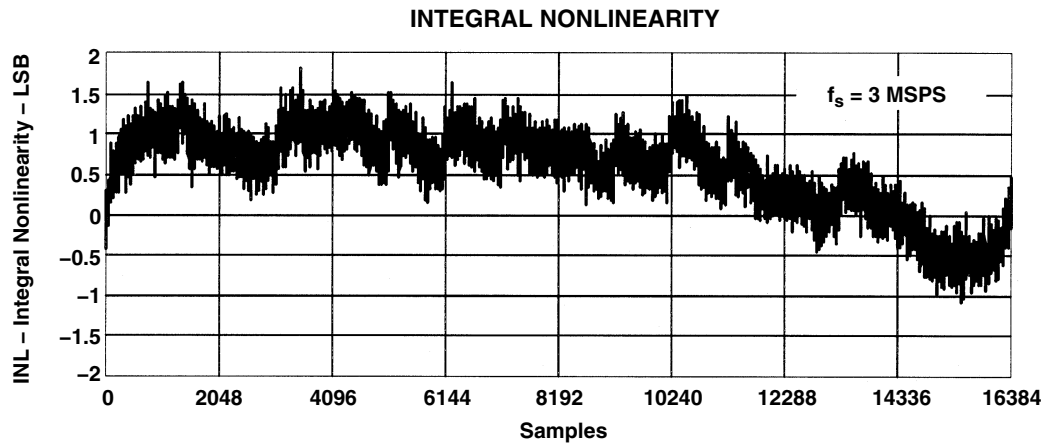


**Figure 7**

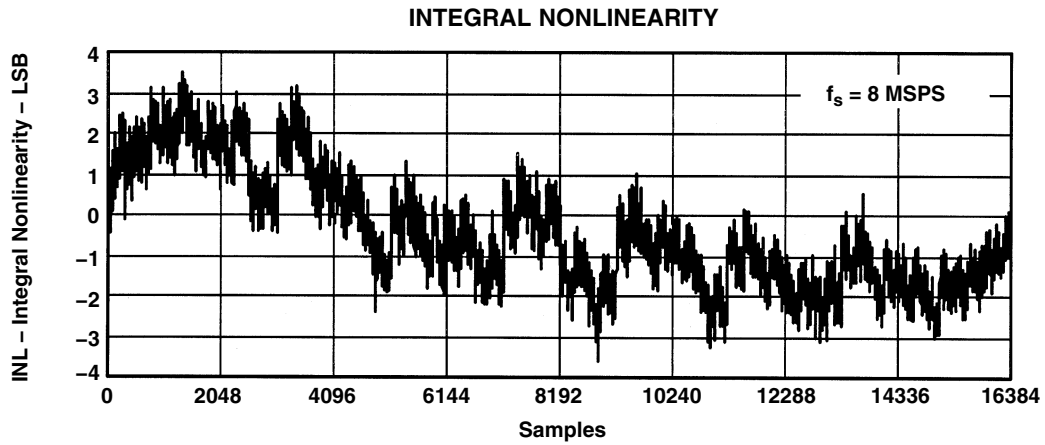
**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**TYPICAL CHARACTERISTICS**



**Figure 8**



**Figure 9**

TYPICAL CHARACTERISTICS

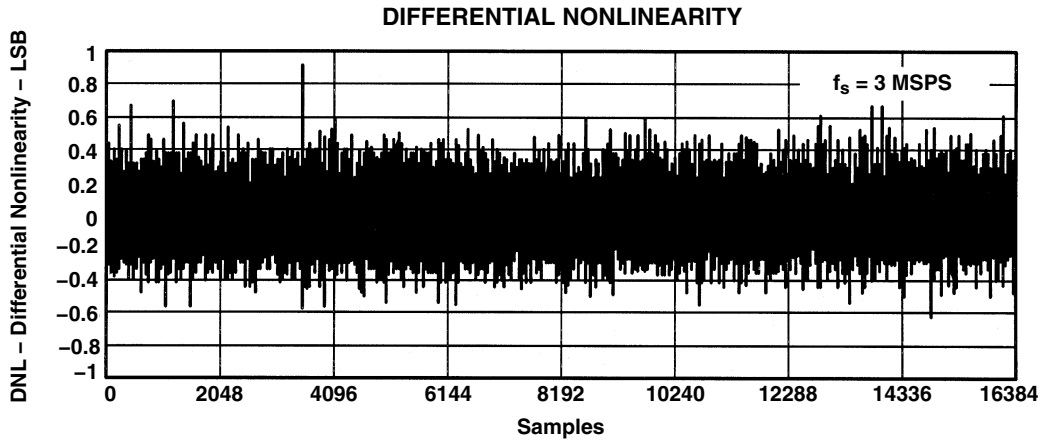


Figure 10

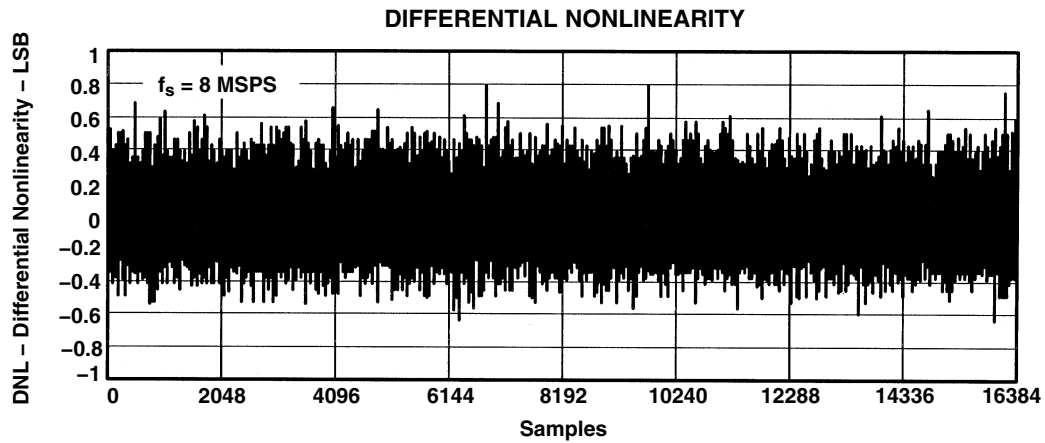


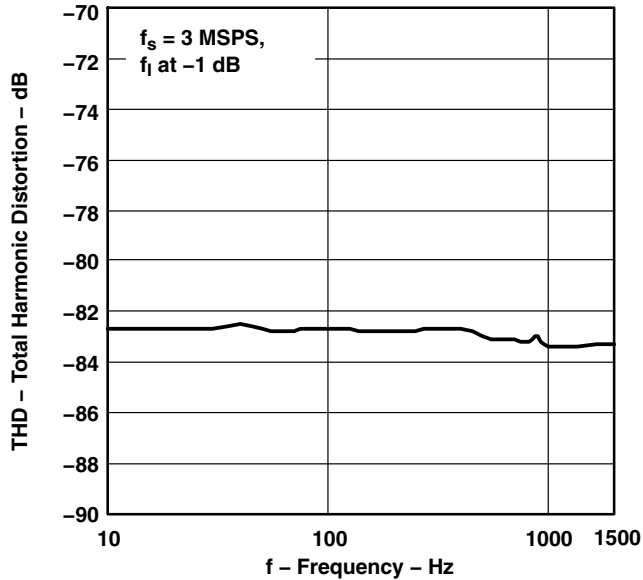
Figure 11

**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

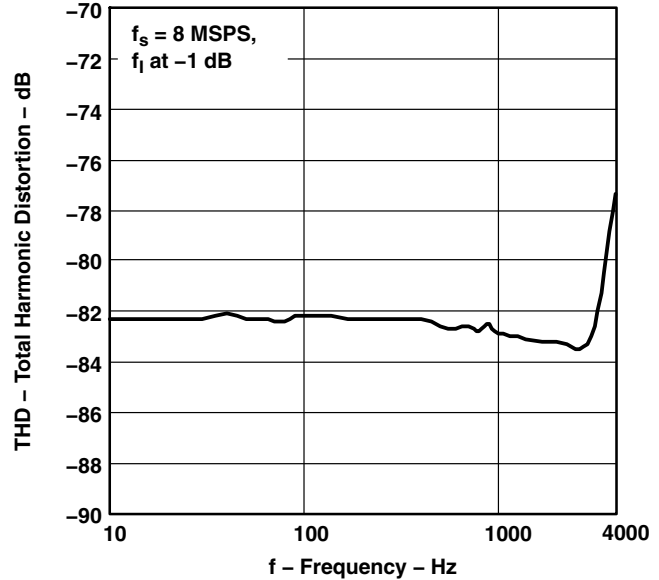
**TYPICAL CHARACTERISTICS**

**TOTAL HARMONIC DISTORTION  
 vs  
 FREQUENCY**



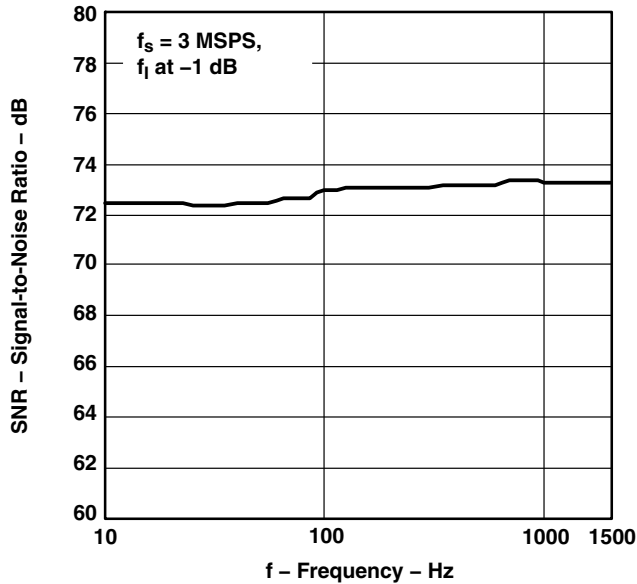
**Figure 12**

**TOTAL HARMONIC DISTORTION  
 vs  
 FREQUENCY**



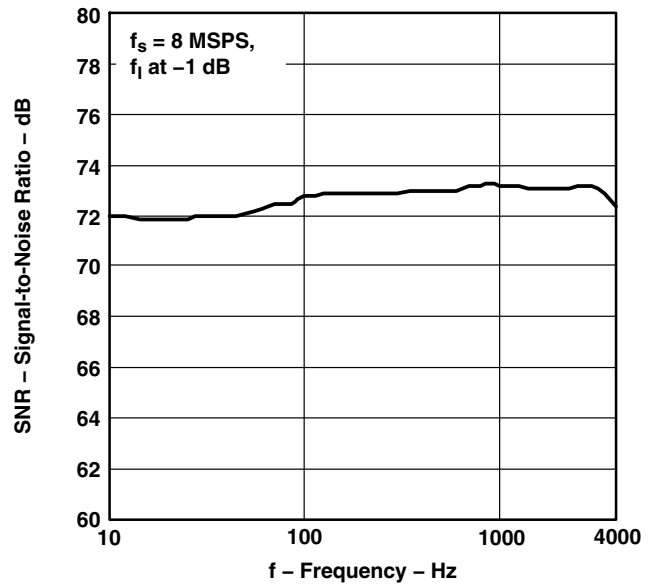
**Figure 13**

**SIGNAL-TO-NOISE RATIO  
 vs  
 FREQUENCY**



**Figure 14**

**SIGNAL-TO-NOISE RATIO  
 vs  
 FREQUENCY**



**Figure 15**



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**PRINCIPLES OF OPERATION**

**registers**

The device contains several registers. The A register is selected by the values of bits A1 and A0:

A1	A0	Register
0	0	Conversion result
0	1	PGA
1	0	Offset
1	1	Control

Tables 1 and 2 describe how to read the conversion results and how to configure the data converter. The default values (where applicable) show the state after a power-on reset.

**Table 1. Conversion Result Register, Address 0, Read**

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	MSB	...	...	...	...	...	...	...	...	...	...	...	...	LSB

The output can be configured for two's complement or straight binary format (see D11/control register).

The output code is given by:

2s complement:

–8192 at  $\Delta IN = -\Delta REF$

0 at  $\Delta IN = 0$

8191  $\Delta IN = -\Delta REF - 1 \text{ LSB}$

Straight binary:

0 at  $\Delta IN = -\Delta REF$

8192 at  $\Delta IN = 0$

16383 at  $\Delta IN = -\Delta REF - 1 \text{ LSB}$

$$1 \text{ LSB} = \frac{2\Delta REF}{16384}$$

**Table 2. PGA Gain Register, Address 1, Read/Write**

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	X	X	X	X	X	G2	G1	G0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The PGA gain is determined by writing to G2–0.

Gain (dB) = 1dB × G2–0. max = 7dB. The range of G2–0 is 0 to 7.

**Table 3. Offset Register, Address 2, Read/Write**

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	MSB	...	...	...	...	...	...	LSB
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The offset correction range is from –128 to 127 LSB. This value is added to the conversion results from the ADC.



**PRINCIPLES OF OPERATION**

**Table 4. Control Register, Address 3, Read**

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF	RES	RES	RES	RES	RES	RES	RES

**Table 5. Control Register, Address 3, Write**

BIT	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF	RES	RES	RES	RES	RES	RES	RES
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**PWD:** Power down                    0 = normal operation                    1 = power down  
**REF:** Reference select            0 = internal reference                1 = external reference  
**FOR:** Output format                0 = straight binary                    1 = 2s complement  
**TM2–0:** Test mode                    000 = normal operation  
     001 = both inputs = REF–  
     010 = IN+ at  $V_{ref}/2$ , IN– at REF–  
     011 = IN+ at REF+, IN– at REF–  
     100 = normal operation  
     101 = both inputs = REF+  
     110 = IN+ at REF–, IN– at  $V_{ref}/2$   
     111 = IN+ at REF–, IN– at REF+  
**OF:** Offset correction            0 = enable                                1 = disable  
**RES**    Reserved                        Must be set to 0.



## APPLICATION INFORMATION

### driving the analog input

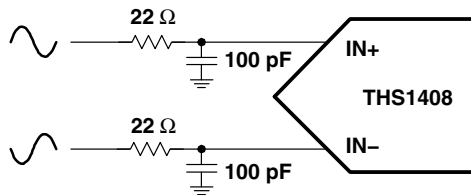
The ADC has a fully differential input. A differential input is advantageous with respect to SNR, SFDR, and THD performance because the signal peak-to-peak level is 50% of a comparable single-ended input.

There are three basic input configurations:

- Fully differential
- Transformer coupled single-ended to differential
- Single-ended

### fully differential configuration

In this configuration, the ADC converts the difference ( $\Delta IN$ ) of the two input signals on IN+ and IN–.



**Figure 16. Differential Input**

The resistors and capacitors on the inputs decouple the driving source output from the ADC input and also serve as first order low pass filters to attenuate out of band noise.

The input range on both inputs is 0 V to  $AV_{DD}$ . The full-scale value is determined by the voltage reference. The positive full-scale output is reached, if  $\Delta IN$  equals  $\Delta REF$ , the negative full-scale output is reached, if  $\Delta IN$  equals  $-\Delta REF$ .

$\Delta IN$ [V]	OUTPUT
$-\Delta REF$	– full scale
0	0
$\Delta REF$	+ full scale

**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

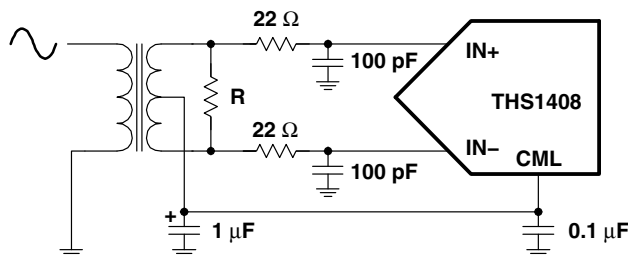
SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**APPLICATION INFORMATION**

**transformer coupled single-ended to differential configuration**

If the application requires the best SNR, SFDR, and THD performance, the input should be transformer coupled.

The signal amplitude on both inputs of the ADC is one half as high as in a single-ended configuration thus increasing the ADC ac performance.



**Figure 17. Transformer Coupled**

The following table shows the input voltages for negative full-scale output, zero output, and positive full-scale output:

IN [V <sub>PEAK</sub> ]	OUTPUT [PEAK]
-ΔREF	- full scale <sup>†</sup>
0	0
ΔREF	+ full scale <sup>†</sup>

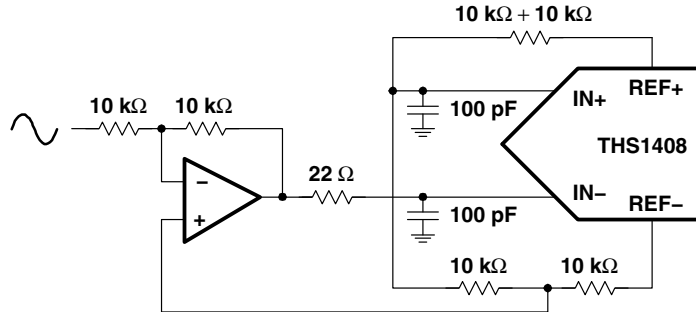
<sup>†</sup> n = 1 (winding ratio)

The resistor R of the transformer coupled input configuration must be set to match the signal source impedance  $R = n^2 R_s$ , where  $R_s$  is the source impedance and n is the transformer winding ratio.

**APPLICATION INFORMATION**

**single-ended configuration**

In this configuration, the input signal is level shifted by  $\Delta\text{REF}/2$ .



**Figure 18. Single-Ended With Level Shift**

The following table shows the input voltages for negative full-scale output, zero output, and positive full-scale output:

$\Delta\text{IN+ [V]}$	OUTPUT
$-\Delta\text{REF}$	- full scale
0	0
$\Delta\text{REF}$	+ full scale

Note that the resistors of the op-amp and the op-amp all introduce gain and offset errors. Those errors can be trimmed by varying the values of the resistors.

Because of the added offset, the op-amp does not necessarily operate in the best region of its transfer curve (best linearity around zero) and, therefore, may introduce unacceptable distortion. For ac signals, an alternative is described in the following section.

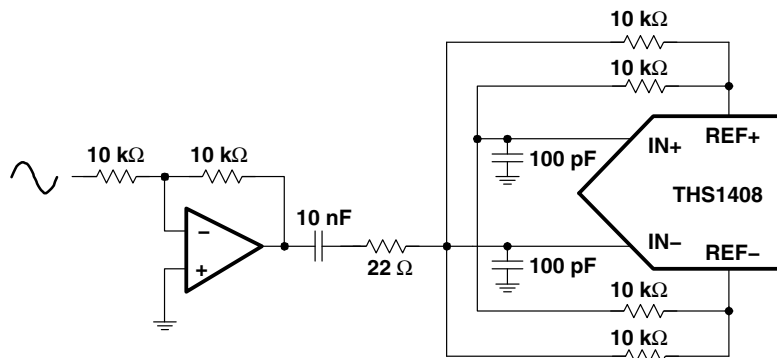
**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

**APPLICATION INFORMATION**

**AC-coupled single-ended configuration**

If the application does not require the signal bandwidth to include dc, the level shift shown in Figure 4 is not necessary.



**Figure 19. Single-Ended With Level Shift**

Because the signal swing on the op-amp is centered around ground, it is more likely that the signal stays within the linear region of the op-amp transfer function, thus increasing the overall ac performance.

IN [V <sub>PEAK</sub> ]	OUTPUT [PEAK]
-ΔREF	- full scale
0	0
ΔREF	+ full scale

Compared to the transformer-coupled configuration, the swing on IN- is twice as big, which can decrease the ac performance (SNR, SFD, and THD).

**THS1408-EP**  
**14-BIT, 3/8 MSPS DSP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER**  
**WITH INTERNAL REFERENCE AND PGA**

SGLS129B – JULY 2002 – REVISED FEBRUARY 2010

---

**APPLICATION INFORMATION**

### **internal/external reference operation**

The THS1408 ADC can either be operated using the built-in band gap reference or using an external precision reference in case very high dc accuracy is needed.

The REF+ and REF- outputs are given by:

$$\text{REF} + = \text{VBG} \left( 1 + \frac{2}{3} \right) \text{ and } \text{REF} - = \text{VBG} \left( 1 - \frac{2}{3} \right)$$

If the built-in reference is used, VBG equals 1.5 V, which results in REF+ = 2.5 V, REF- = 0.5 V and ΔREF = 2 V.

The internal reference can be disabled by writing 1 to D12 (REF) in the control register (address 3). The band gap reference is then disconnected and can be substituted by a voltage on the VBG pin.

### **programmable gain amplifier**

The on-chip programmable gain amplifier (PGA) has eight gain settings. The gain can be changed by writing to the PGA gain register (address 1). The range is 0 to 7 dB in steps of one dB.

### **out of range indication**

The OV output of the ADC indicates an out of range condition. Every time the difference on the analog inputs exceeds the differential reference, this signal is asserted. This signal is updated the same way as the digital data outputs and therefore subject to the same pipeline delay.

### **offset compensation**

With the offset register it is possible to automatically compensate system offset errors, including errors caused by additional signal conditioning circuitry. If the offset compensation is enabled (D7 (OFF) in the control register), the value in the offset register (address 2) is automatically subtracted from the output of the ADC.

In order to set the correct value of the offset compensation register, the ADC result when the input signal is 0 must be read by the host processor and written to the offset register (address 2).

### **test modes**

The ADC core operation can be tested by selecting one of the available test modes (see control register description). The test modes apply various voltages to the differential input depending on the setting in the control register.

### **digital I/O**

The digital inputs and outputs of the THS1408 ADC are 3-V CMOS compatible. In order to avoid current feed back errors, the capacitive load on the digital outputs should be as low as possible (50 pF max). Series resistors (100 Ω) on the digital outputs can improve the performance by limiting the current during output transitions.

The parallel interface of the THS1408 ADC features 3-state buffers, making it possible to directly connect it to a data bus. The output buffers are enabled by driving the  $\overline{\text{OE}}$  input low.

Refer to the read and write timing diagrams in the parameter measurement information section for information on read and write access.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS1408MPHPEP	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	THS1408ME	<a href="#">Samples</a>
V62/03608-03XE	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	THS1408ME	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF THS1408-EP :**

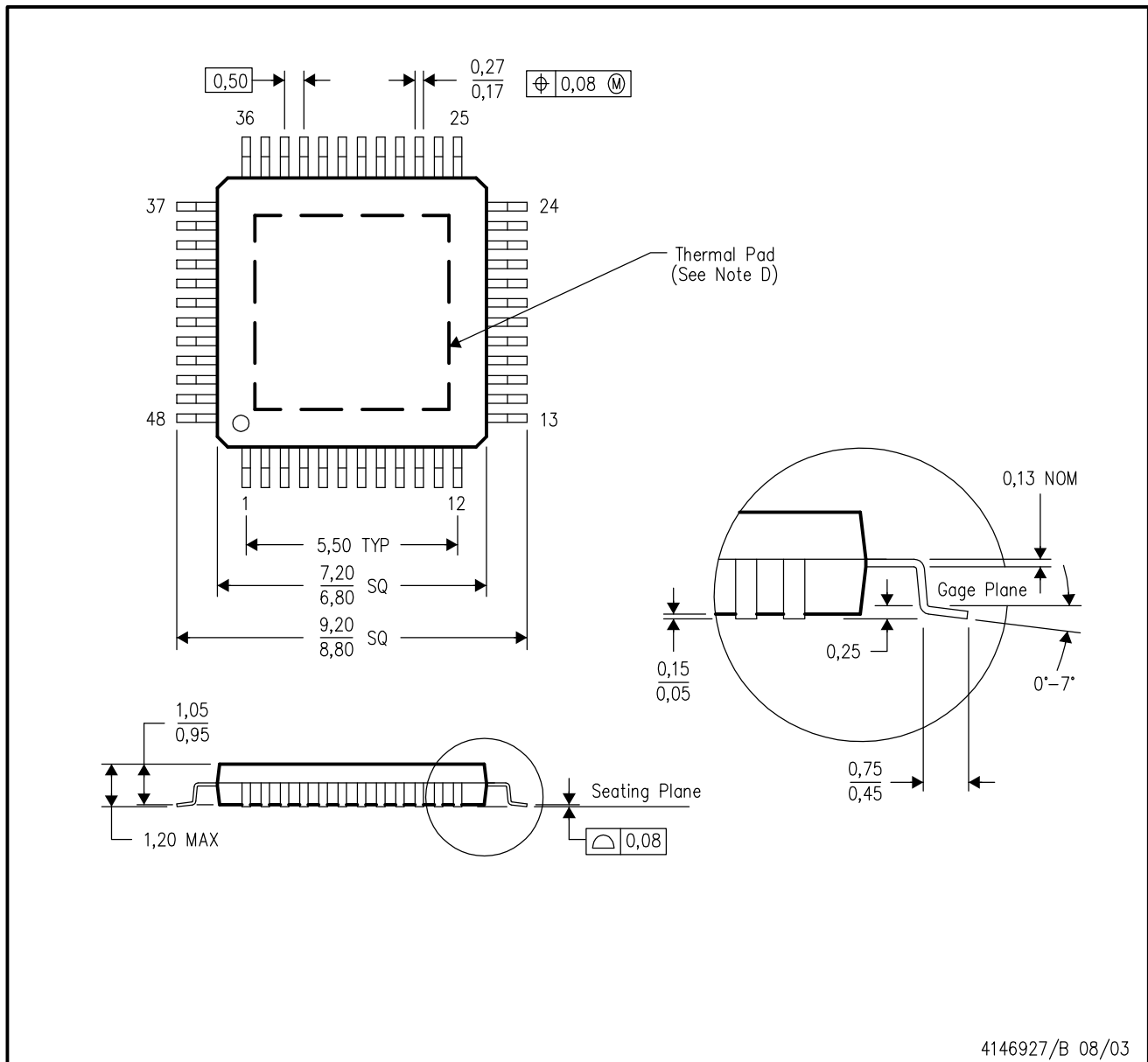
- Catalog: [THS1408](#)
- Military: [THS1408M](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.



# THERMAL PAD MECHANICAL DATA

PHP (S-PQFP-G48)

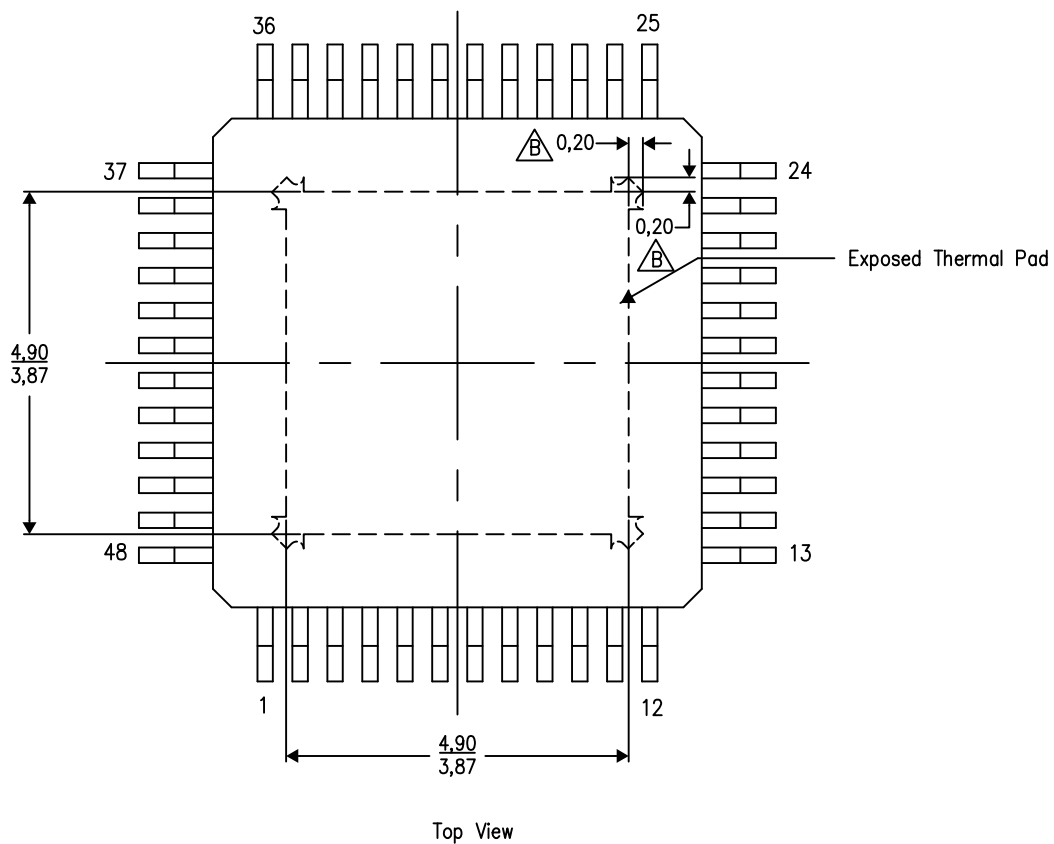
PowerPAD™ PLASTIC QUAD FLATPACK

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).


The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206329-4/0 05/14

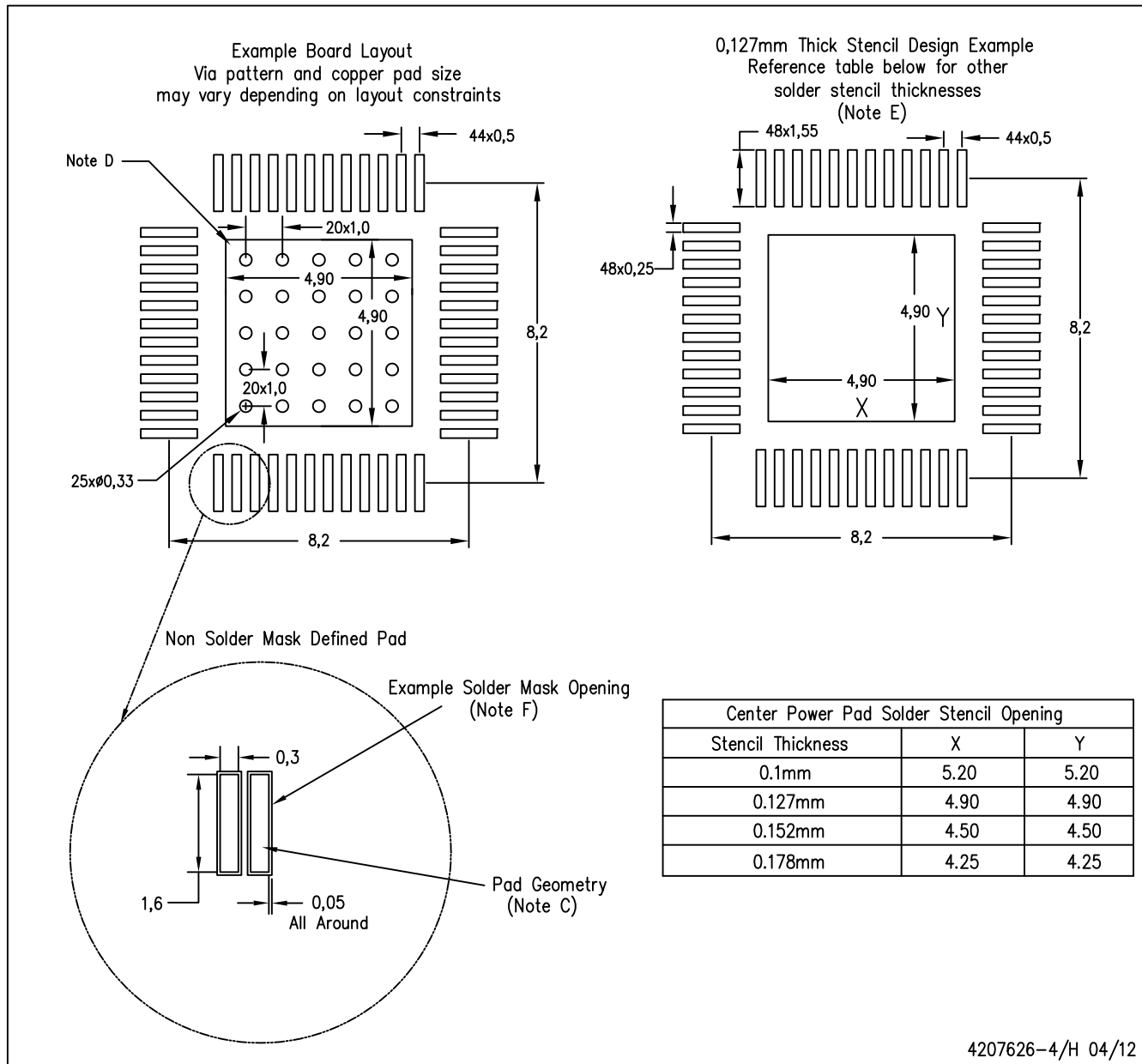
NOTE: A. All linear dimensions are in millimeters

 Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PHP (S-PQFP-G48)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

PowerPAD is a trademark of Texas Instruments

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Texas Instruments:](#)

[THS1408MPHPEP](#) [V62/03608-03XE](#)