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DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT

GENERAL DESCRIPTION

The MMC 4015 (G and H types) and MMC 4015 (E and F types) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.
The MMC 4015 consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA inputs is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one MMC 4015 package, or to more than 8 stages using additional MMC 4015's is possible.

FEATURES

- Medium speed operation: 12 MHz (typ.) clock rate at $V_{DD}-V_{SS} = 10$ V.
- Fully static operation.
- 8 master-slave flip-flops plus input and output buffering
- High noise immunity

ABSOLUTE MAXIMUM RATINGS

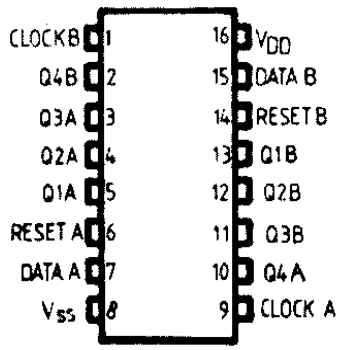
V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_i	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_A = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

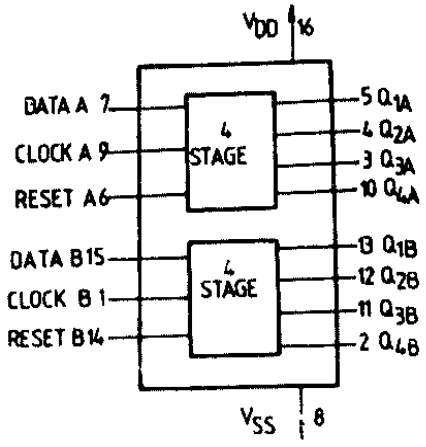
V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_i	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C

CONNECTION DIAGRAM



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FUNCTIONAL DIAGRAM

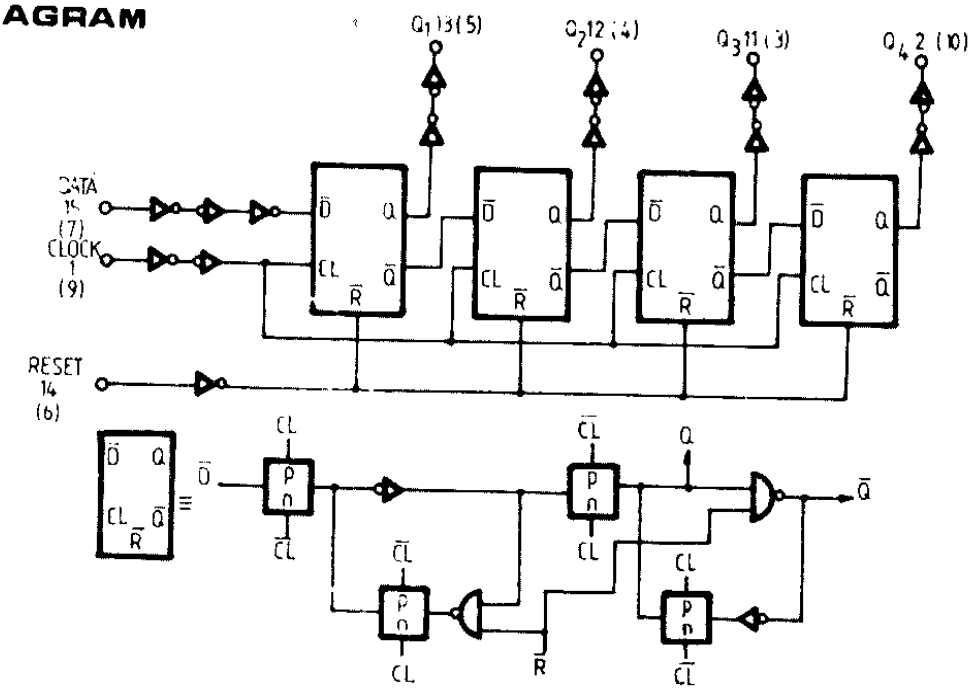


TRUTH TABLE

CL	D	R	Q_1	Q_n
⌐‾	0	0	0	Q_n-1
_/‾	1	0	1	Q_n-1
‾_	X	0	Q_1	Q_n
X	X	1	0	0

No change

LOGIC DIAGRAM



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STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES						UN
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μ
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		m
			0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
			0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
			0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
		E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
			0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
			0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
			0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
		E, F types	0/15			15		±0.3		$±10^{-5}$	±0.3		+1	
C	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

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DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times= 20 ns)

PARAMETER		TEST CONDITIONS V_{DD} (V)	VALUES min.	VALUES typ.	VALUES max.	UNIT
Clocked operation						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decoded out Lines)	5		160	320	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH}	Transition time (Carry Out or Decoded Out Lines)	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	3	6		MHz
		10	6	12		
		15	8.5	17		
t_W	Clock pulse width	5	180	90		ns
		10	80	40		
		15	50	25		
t_r, t_f*	Clock input rise or fall time	5			15	μs
		10			15	
		15			15	
t_{setup}	Data setup time	5	70	35		ns
		10	40	20		
		15	30	15		
Reset operation						
t_{PLH}, t_{PHL}	Propagation delay time	5		200	400	ns
		10		100	200	
		15		80	160	
t_W	Reset pulse width	5	200	100		ns
		10	80	40		
		15	60	30		

* If more than one unit is cascaded t_r CL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.