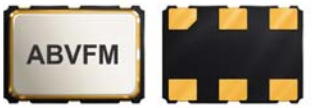
CERAMIC SMD CRYSTAL CLOCK OSCILLATOR WITH VOLTAGE CONTROL



5.0 x 7.0 x 1.8mm

ABVFM SERIES : PRELIMINARY

FEATURES:

- Based on a proprietary analog multiplier
- Tri-State Output
- Ultra low Phase Jitter
- 155.52MHz, 311.04MHz, 622.08MHz applications
- 2.5V to 3.3V +/- 10% operation
- Ceramic SMD, low profile package

APPLICATIONS:

- xDSL, Cable Modems
- Customer Premise Equipment (CPE)
- ATM, SONET, SDH, STB
- LAN / WAN Data Communications Equip.

STANDARD SPECIFICATIONS:

PARAMETERS	
Frequency Range	60 MHz to 320 MHz
Operating Temperature	0°C to + 70°C (see options)
Storage Temperature	- 55°C to + 125°C
Overall Frequency Stability	± 100 ppm max. (see options)
Supply Voltage (Vdd)	2.5V - 3.3 Vdc ± 10%
Jitter (12KHz - 20MHz)	RMS phase jitter < 0.6pS period jitter < 20pS peak to peak
Low Phase Noise	-130 dBc/Hz @ 1kHz Offset from 212.5MHz -140 dBc/Hz @ 10kHz Offset from 212.5MHz -145 dBc/Hz @ 100kHz Offset from 212.5MHz
Aging (PPM/year)	TBD Per Crystal
Pullability	+/- 50ppm
PECL	
Supply Current (I_{DD})[Fout = 212.50MHz]	58mA min, 65mA typical, 75mA max.
Output Clock Duty Cycle @ V_{DD}-1.3V	45% min, 50% typical, 55% max.
Output High Voltage	V_{OH} = VDD-2V (VDD-1.025V min)
Output Low Voltage	V_{OL} = VDD-2V (VDD-1.620V max)
Clock Rise time (t_r) @ 20/80%	0.7ns max, 0.4ns typical
Clock Fall time (t_f) @ 80/20%	0.7ns max, 0.4ns typical
CMOS	
Output Clock Rise/ Fall Time [10%~90% VDD with 10pF load]	1.6ns max, 1.2ns typical
Output Clock Duty Cycle [Measured @ 50% VDD]	45% min, 50% typical, 55% max
LVDS	
Supply Current (I_{DD}) [Fout = 212.50MHz]	60mA max, 55mA typical.
Output Clock Duty Cycle @ 1.25V	45% min, 50% typical, 55% max
Output Differential Voltage (V_{OD})	247mV min, 355mV typical, 454mV max
VDD Magnitude Change (ΔV_{OD})	-50mV min, 50mV max
Output High Voltage	V_{OH} = 1.6V max, 1.4V typical
Output Low Voltage	V_{OL} = 0.9V min, 1.1V typical
Offset Voltage [R_L = 100Ω]	V_{OS} = 1.125V min, 1.1V typical, 1.375V max
Offset Magnitude Voltage[RL = 100Ω]	ΔV_{OS} = 0mV min, 3mV typical, 25mV max
Power-off Leakage (I_{OXD}) [Vout=VDD or GND, VDD=0V]	±10µA max, ±1µA typical
Differential Clock Rise Time (t_r) [R_L=100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max
Differential Clock Fall Time (t_f) [R_L=100Ω, CL=10pF]	0.2ns min, 0.5ns typical, 0.7ns max

ABRACON CORPORATION

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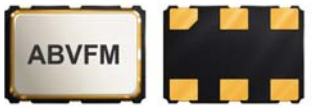
ABVFM SERIES : PRELIMINARY



5.0 x 7.0 x 1.8mm

PIN ASSIGNMENTS:

PIN #	NAME	DESCRIPTION
1	VCON	VCON
2	Tri-state	Tri-state
3	GND	Ground
4	Q	PECL, LVDS, or CMOS Output
5	Q	Complimentary PECL,LVDS, or NC
6	V_{DD}	VDD Connection

TRI-STATE PIN OPERATION:

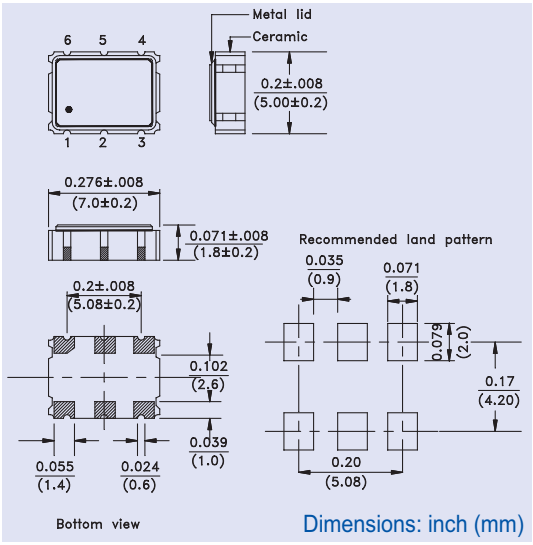
OUTPUT TYPE	PIN 2 LOGIC LEVEL*	OUTPUT STATE
PECL	0 (Default)	Enabled
	1	Tri-state
LVDS & CMOS	0	Tri-state
	1(Default)	Enabled

*Connect to VDD from logic level "1", connect to ground for logic level "0".

MARKING:

- TUH (Frequency: T=First “”10” digit of frequency, U=First “unit” of frequency, H=First “tenth” of frequency, Ex: 100 for 10.0MHz)
- ABFM ZY (Z: Month, A to L; Y: Year, 5 for 2005

OUTLINE DRAWING:



OPTIONS AND PART IDENTIFICATION (Left blank if standard):

ABFM - Frequency - Temperature - Frequency Stability - Output - Packaging

Temperature:
D for -10°C to +60°C
E for -20°C to +70°C
F for -30°C to +70°C
N for -30°C to +85°C
L for -40°C to +85°C

Stability options:
R for ± 25 ppm
C for ± 50 ppm

Output options:
P = PECL
L = LVDS
C = CMOS

Packaging option: T for Tape and Reel (1,000pcs/reel)

Availability limited to application specific application frequencies.
Please contact factory for available frequencies.

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