Dual N-CHANNEL ENHANCEMENT MODE POWER MOSFET

MTDN9971Q8

Description

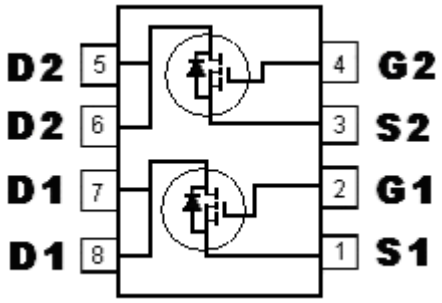
The MTDN9971Q8 provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Features

• $R_{DS(ON)}$=60mΩ@V_{GS}=4.5V, I_D=2.5A
• Simple drive requirement
• Low on-resistance
• Fast switching speed
• Dual N-ch MOSFET package
• Pb-free package

Equivalent Circuit

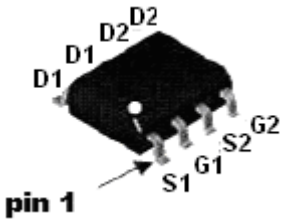
MTDN9971Q8



G：Gate
S：Source
D：Drain

Outline

SOP-8



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	60	V
Gate-Source Voltage	V_{GS}	±25	V
Continuous Drain Current @T_A=25 °C (Note 1)	I_D	5	A
Continuous Drain Current @T_A=70 °C (Note 1)	I_D	3.2	A
Pulsed Drain Current (Note 2, 3)	I_{DM}	30	A
Total Power Dissipation @ T_A=25 °C	Pd	2	W
Linear Derating Factor		0.016	W / °C
Operating Junction and Storage Temperature	Tj, Tstg	-55~+150	°C
Thermal Resistance, Junction-to-Ambient (Note 1)	Rth,ja	62.5	°C/W

Note : 1.Surface mounted on 1 in² copper pad of FR-4 board, 135°C/W when mounted on minimum copper pad.
2.Pulse width ≤300μs, duty cycle≤2%.
3.Pulse width limited by maximum junction temperature.

Electrical Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	60	-	-	V	V_{GS}=0, I_D=250μA
$\Delta BV_{DSS}/\Delta Tj$	-	0.06	-	V/°C	Reference to 25°C, I_D=1mA
$V_{GS(th)}$	1	-	3	V	V_{DS}=V_{GS}, I_D=250μA
*G_{FS}	-	7	-	S	V_{DS}=10V, I_D=5A
I_{GSS}	-	-	±100	nA	V_{GS}=±25V, V_{DS}=0
I_{DSS}	-	-	1	μA	V_{DS}=60V, V_{GS}=0
	-	-	25	μA	V_{DS}=48V, V_{GS}=0, Tj=70°C
*$R_{DS(ON)}$	-	-	50	mΩ	V_{GS}=10V, I_D=5A
	-	-	60		V_{GS}=4.5V, I_D=2.5A
Dynamic					
Ciss	-	1658	-	pF	V_{DS}=25V, V_{GS}=0V, f=1MHz
Coss	-	156	-		
Crss	-	109	-		
*$t_{d(ON)}$	-	9.6	-	ns	V_{DS}=30V, I_D=5A, V_{GS}=10V, R_G=3.3Ω, R_D=6Ω
*t_r	-	10	-	ns	
*$t_{d(OFF)}$	-	30	-	ns	
*t_f	-	5.5	-	ns	
*Qg	-	32.5	-	nC	V_{DS}=48V, I_D=5A, V_{GS}=10V
*Qgs	-	4.9	-	nC	
*Qgd	-	8.8	-	nC	
Source-Drain Diode					
*V_{SD}	-	-	1.2	V	V_{GS}=0V, I_S=1.6A
*trr	-	29.2	-	ns	I_S=5A, V_{GS}=0V, dI/dt=100A/μs
*Qrr	-	48	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Characteristic Curves

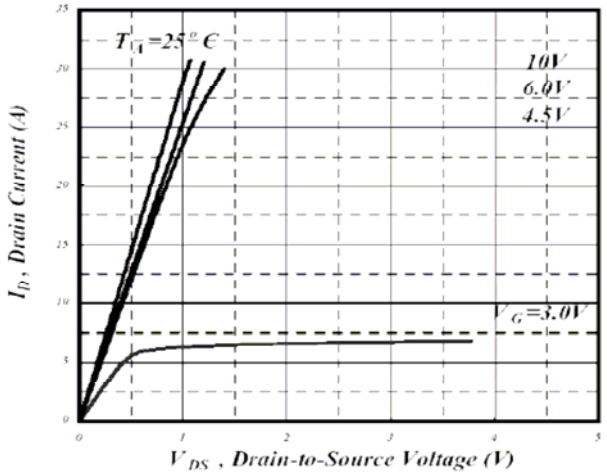


Fig 1. Typical Output Characteristics

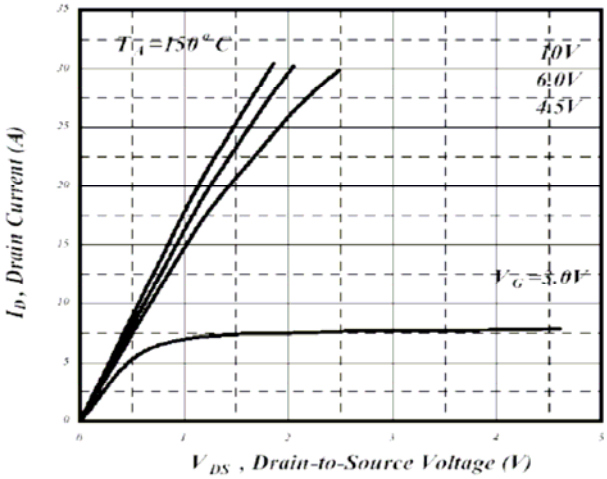


Fig 2. Typical Output Characteristics

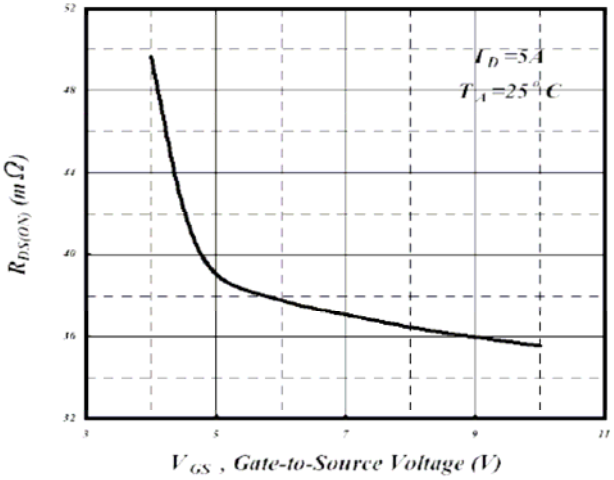


Fig 3. On-Resistance v.s. Gate Voltage

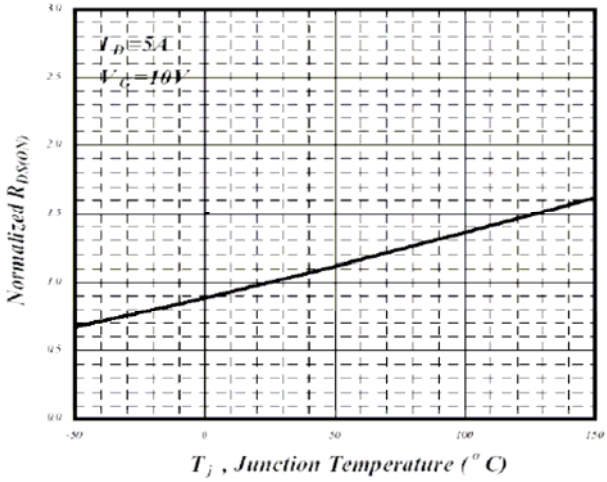


Fig 4. Normalized On-Resistance v.s. Junction Temperature

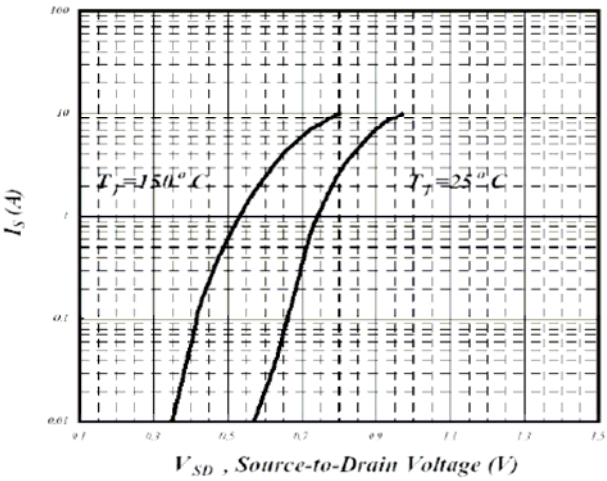


Fig 5. Forward Characteristics of Reverse Diode

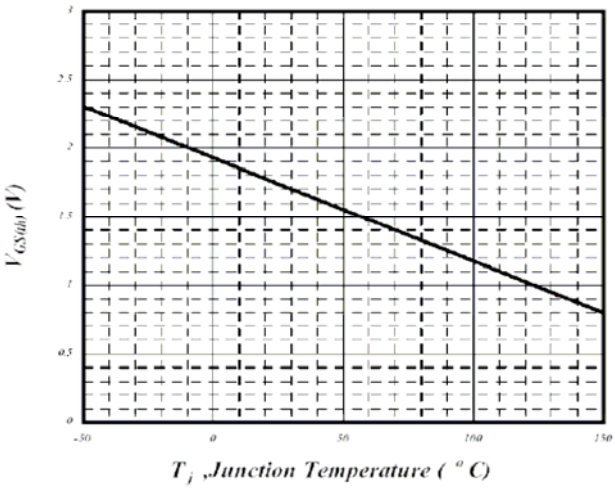


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Characteristic Curves(Cont.)

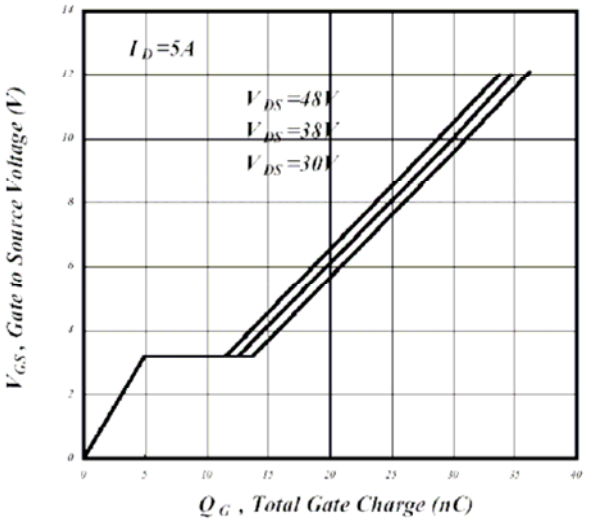


Fig 7. Gate Charge Characteristics

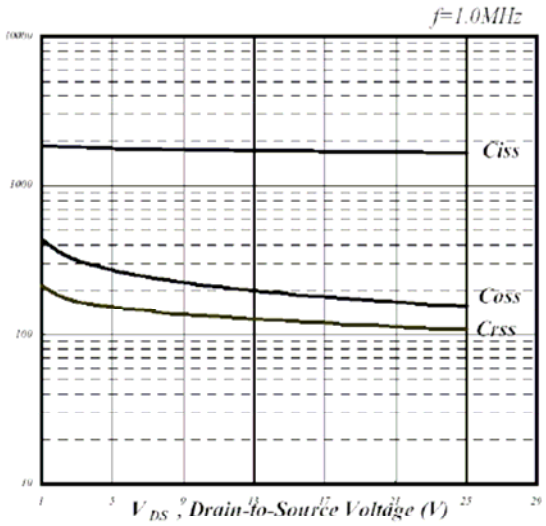


Fig 8. Typical Capacitance Characteristics

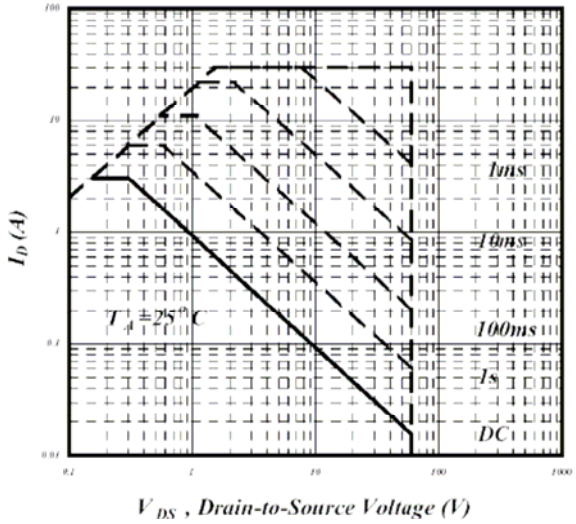


Fig 9. Maximum Safe Operating Area

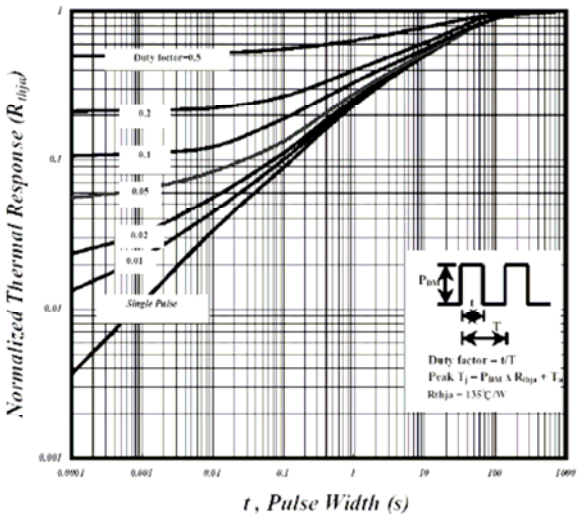


Fig 10. Effective Transient Thermal Impedance

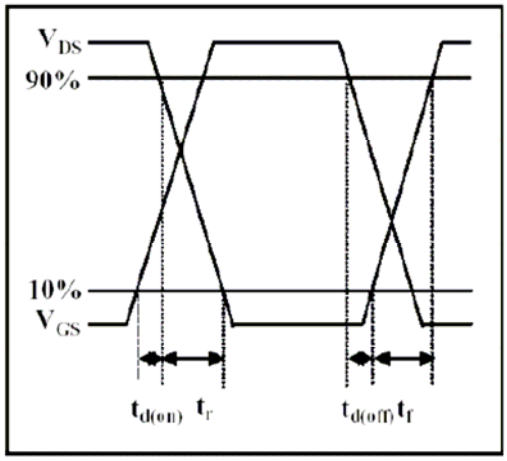


Fig 11. Switching Time Waveform

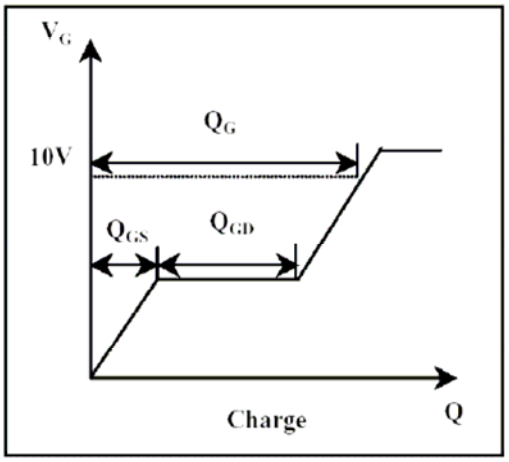
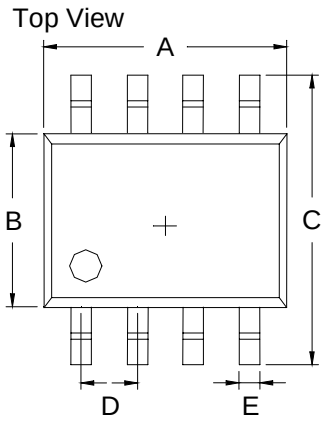
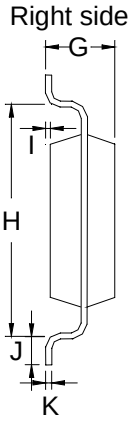
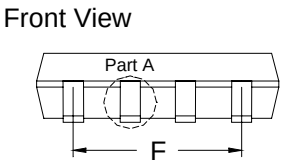


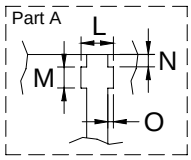
Fig 12. Gate Charge Waveform

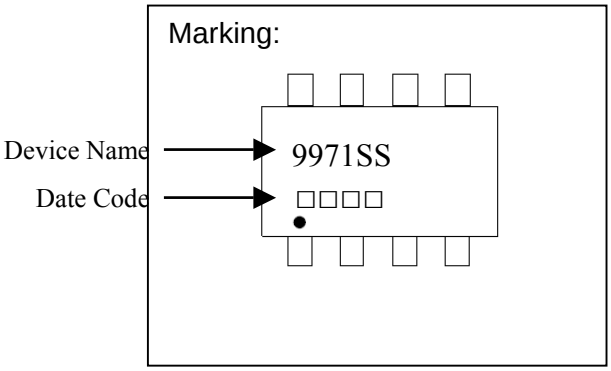
SOP-8 Dimension











8-Lead SOP-8 Plastic Package
CYStek Package Code: Q8

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1909	0.2007	4.85	5.10	I	0.0019	0.0078	0.05	0.20
B	0.1515	0.1555	3.85	3.95	J	0.0118	0.0275	0.30	0.70
C	0.2283	0.2441	5.80	6.20	K	0.0074	0.0098	0.19	0.25
D	0.0480	0.0519	1.22	1.32	L	0.0145	0.0204	0.37	0.52
E	0.0145	0.0185	0.37	0.47	M	0.0118	0.0197	0.30	0.50
F	0.1472	0.1527	3.74	3.88	N	0.0031	0.0051	0.08	0.13
G	0.0570	0.0649	1.45	1.65	O	0.0000	0.0059	0.00	0.15
H	0.1889	0.2007	4.80	5.10					

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.