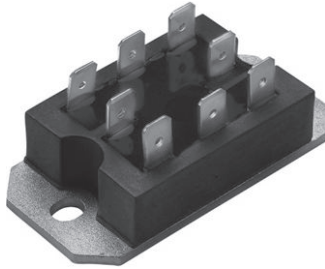


Power Modules, Passivated Assembled Circuit Elements, 40 A



PACE-PAK (D-19)

FEATURES

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200 V_{RRM}/V_{DRM}
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRIMARY CHARACTERISTICS

| | |
|---------|-------------------------------|
| I_o | 40 A |
| Type | Modules - thyristor, standard |
| Package | PACE-PAK (D-19) |

DESCRIPTION

The VS-P400 series of integrated power circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

MAJOR RATINGS AND CHARACTERISTICS

| SYMBOL | CHARACTERISTICS | VALUES | UNITS |
|--------------------------|-----------------|-------------|-------------------|
| I_o | 80 °C | 40 | A |
| I_{TSM} , I_{FSM} | 50 Hz | 385 | A |
| | 60 Hz | 400 | |
| I^2t | 50 Hz | 745 | A ² s |
| | 60 Hz | 680 | |
| $I^2\sqrt{t}$ | | 7450 | A ² √s |
| V_{RRM} | Range | 400 to 1200 | V |
| V_{ISOL} | | 2500 | V |
| T_J | | -40 to +125 | °C |
| T_{Stg} | | | |

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

| TYPE NUMBER | V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V | V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V | I_{RRM} MAXIMUM AT T_J MAXIMUM mA |
|---------------------------|---|--|---|
| VS-P401, VS-P421, VS-P431 | 400 | 500 | 10 |
| VS-P402, VS-P422, VS-P432 | 600 | 700 | |
| VS-P403, VS-P423, VS-P433 | 800 | 900 | |
| VS-P404, VS-P424, VS-P434 | 1000 | 1100 | |
| VS-P405, VS-P425, VS-P435 | 1200 | 1300 | |



| ON-STATE CONDUCTION | | | | | |
|--|-------------------------------------|--|----------------------------------|--------|-------------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | VALUES | UNITS |
| Maximum DC output current at case temperature | I _O | Full bridge circuits | | 40 | A |
| | | | | 80 | °C |
| Maximum peak, one-cycle non-repetitive on-state or forward current | I _{TSM} , I _{FSM} | t = 10 ms | No voltage reapplied | 385 | A |
| | | t = 8.3 ms | | | |
| | | t = 10 ms | 100 % V _{RRM} reapplied | 325 | |
| | | t = 8.3 ms | | | |
| Maximum I ² t for fusing | I ² t | t = 10 ms | No voltage reapplied | 745 | A ² s |
| | | t = 8.3 ms | | | |
| | | t = 10 ms | 100 % V _{RRM} reapplied | 530 | |
| | | t = 8.3 ms | | | |
| Maximum I ² √t for fusing | I ² √t | t = 0.1 ms to 10 ms, no voltage reapplied I ² t for time tx = I ² √t · √tx | | 7450 | A ² √s |
| Low level value of threshold voltage | V _{T(TO)1} | (16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J = T _J maximum | | 0.83 | V |
| High level value of threshold voltage | V _{T(TO)2} | (I > π × I _{T(AV)}), T _J = T _J maximum | | 1.03 | |
| Low level value of on-state slope resistance | r _{t1} | (16.7 % × π × I _{T(AV)} < I < π × I _{T(AV)}), T _J = T _J maximum | | 9.61 | mΩ |
| High level value of on-state slope resistance | r _{t2} | (I > π × I _{T(AV)}), T _J = T _J maximum | | 7.01 | |
| Maximum on-state voltage drop | V _{TM} | I _{TM} = π × I _{T(AV)} | T _J = 25 °C | 1.4 | V |
| Maximum forward voltage drop | V _{FM} | I _{FM} = π × I _{F(AV)} | T _J = 25 °C | 1.4 | V |
| Maximum non-repetitive rate of rise of turned-on current | di/dt | T _J = 125 °C from 0.67 V _{DRM} I _{TM} = π × I _{T(AV)} , I _g = 500 mA, t _r < 0.5 μs, t _p > 6 μs | | 200 | A/μs |
| Maximum holding current | I _H | T _J = 25 °C anode supply = 6 V, resistive load | | 130 | mA |
| Maximum latching current | I _L | | | 250 | |

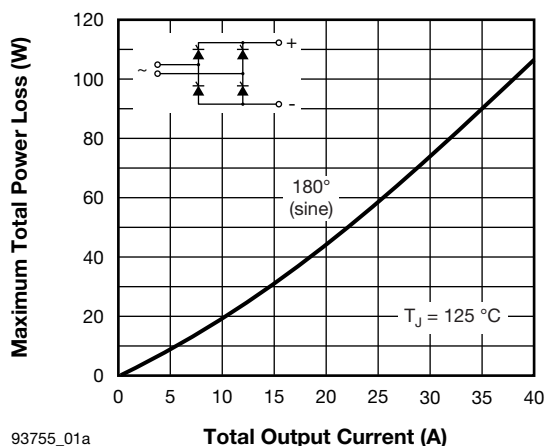
| BLOCKING | | | | | |
|---|-------------------------------------|--|--|--------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | VALUES | UNITS |
| Maximum critical rate of rise of off-state voltage | dV/dt | T _J = 125 °C, exponential to 0.67 V _{DRM} gate open | | 200 | V/μs |
| Maximum peak reverse and off-state leakage current at V _{RRM} , V _{DRM} | I _{RRM} , I _{DRM} | T _J = 125 °C, gate open circuit | | 10 | mA |
| Maximum peak reverse leakage current | I _{RRM} | T _J = 25 °C | | 100 | μA |
| RMS isolation voltage | V _{ISOL} | 50 Hz, circuit to base, all terminals shorted, T _J = 25 °C, t = 1 s | | 2500 | V |

| TRIGGERING | | | | | |
|--|--------------------|---|--|--------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | VALUES | UNITS |
| Maximum peak gate power | P _{GM} | | | 8 | W |
| Maximum average gate power | P _{G(AV)} | | | 2 | |
| Maximum peak gate current | I _{GM} | | | 2 | A |
| Maximum peak negative gate voltage | -V _{GM} | | | 10 | V |
| Maximum gate voltage required to trigger | V _{GT} | T _J = - 40 °C | | 3 | V |
| | | T _J = 25 °C | | 2 | |
| | | T _J = 125 °C | | 1 | |
| Maximum gate current required to trigger | I _{GT} | T _J = - 40 °C | | 90 | mA |
| | | T _J = 25 °C | | 60 | |
| | | T _J = 125 °C | | 35 | |
| Maximum gate voltage that will not trigger | V _{GD} | T _J = 125 °C, rated V _{DRM} applied | | 0.2 | V |
| Maximum gate current that will not trigger | I _{GD} | | | 2 | mA |

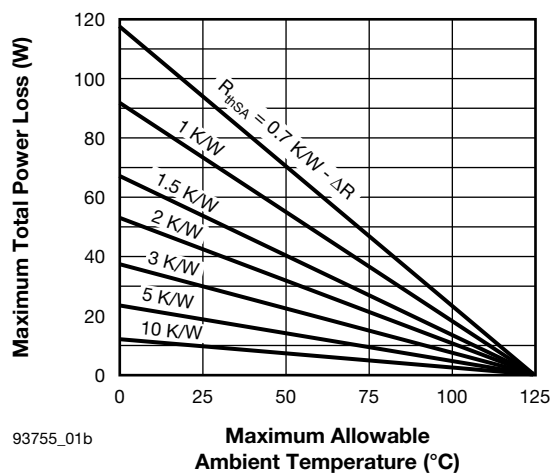
| THERMAL AND MECHANICAL SPECIFICATIONS | | | | |
|---|----------------|--------------------------------------|-----------------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | VALUES | UNITS |
| Maximum junction operating and storage temperature range | T_J, T_{Stg} | | -40 to +125 | °C |
| Maximum thermal resistance, junction to case per junction | R_{thJC} | DC operation | 1.05 | K/W |
| Maximum thermal resistance, case to heatsink | R_{thCS} | Mounting surface, smooth and greased | 0.10 | |
| Mounting torque, base to heatsink ⁽¹⁾ | | | 4 | Nm |
| Approximate weight | | | 58 | g |
| | | | 2.0 | oz. |
| Case style | | | PACE-PAK (D-19) | |

Note

(1) A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound

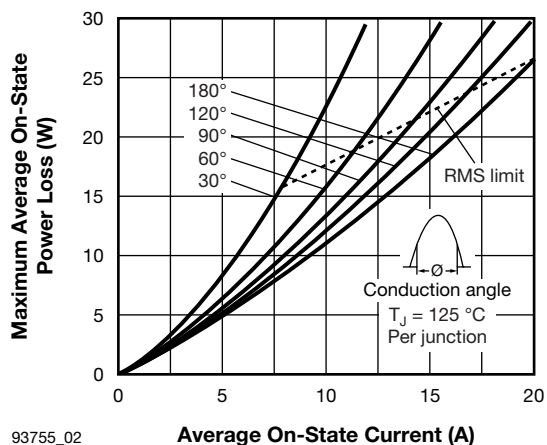


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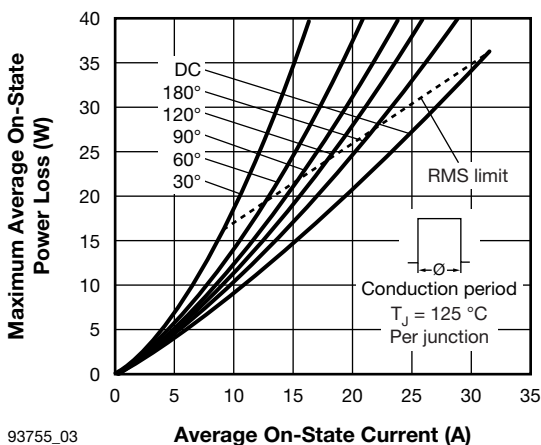
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Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)



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Fig. 2 - On-State Power Loss Characteristics



93755_03

Fig. 3 - On-State Power Loss Characteristics

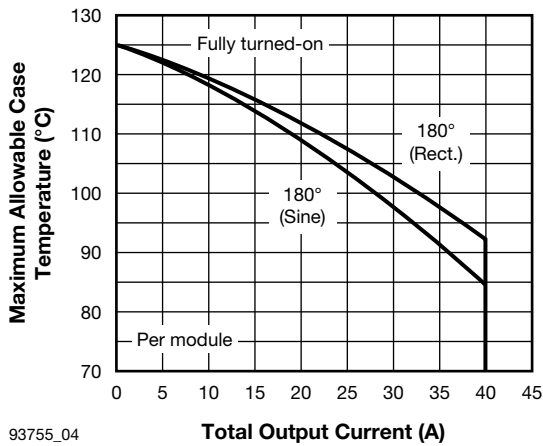


Fig. 4 - Current Ratings Characteristics

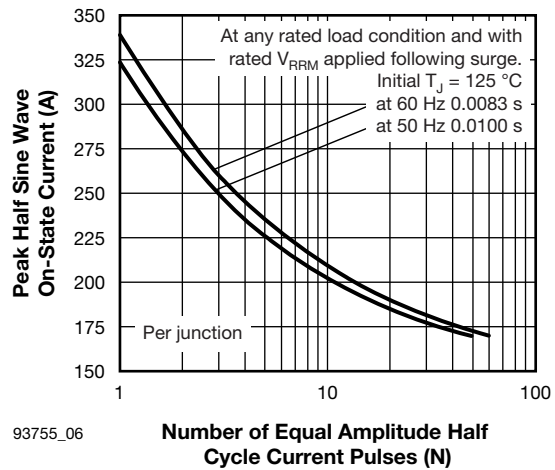


Fig. 6 - Maximum Non-Repetitive Surge Current

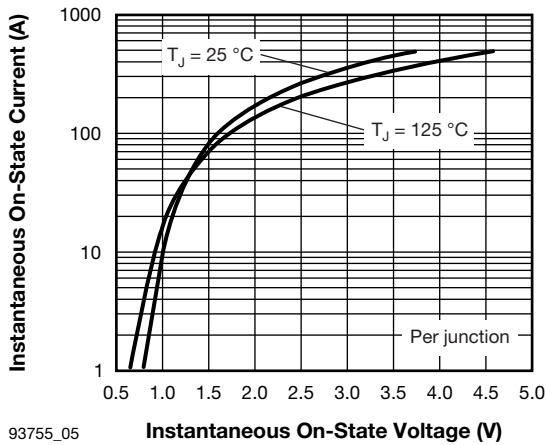


Fig. 5 - On-State Voltage Drop Characteristics

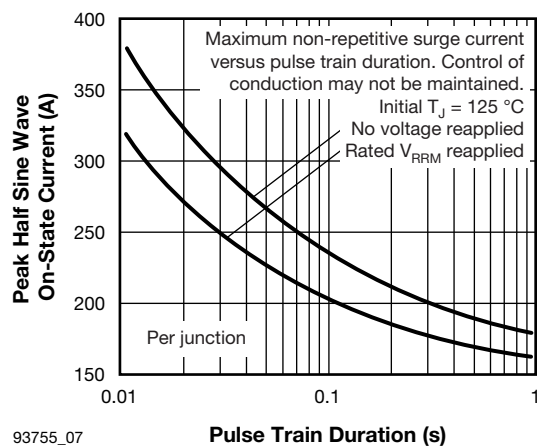


Fig. 7 - Maximum Non-Repetitive Surge Current

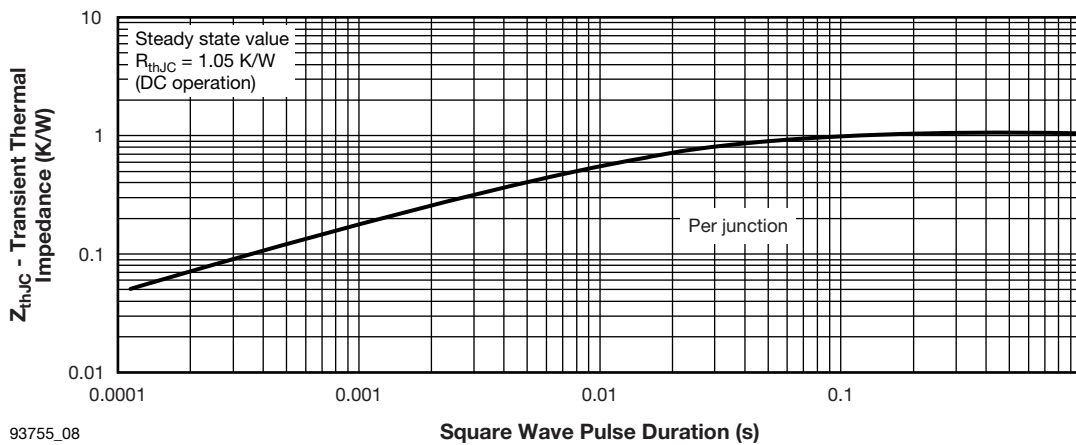


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

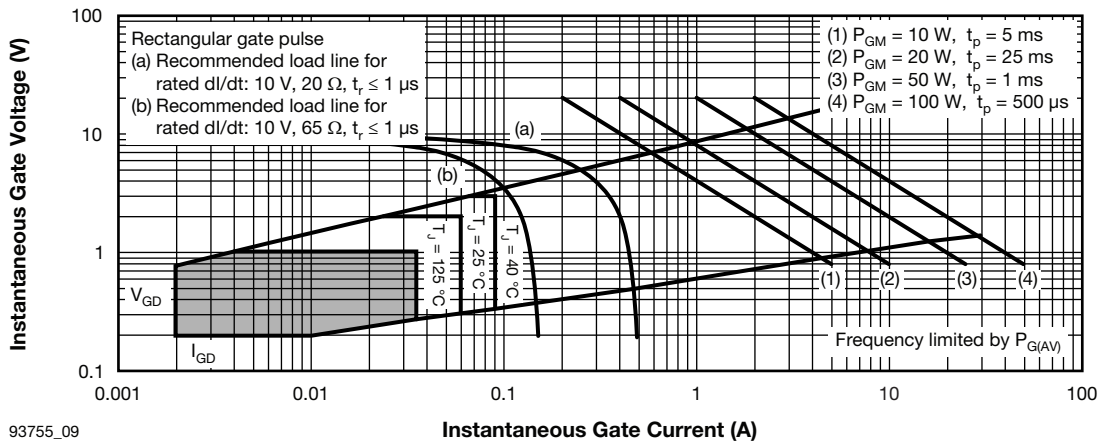


Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

| | | | | | | | |
|-------------|------------|----------|----------|----------|----------|----------|----------|
| Device code | VS- | P | 4 | 0 | 2 | K | W |
| | (1) | (2) | (3) | (4) | (5) | (6) | (7) |

- 1** - Vishay Semiconductors product
- 2** - Module type
- 3** - Current rating
 1 = 25 A DC (P100 series)
 4 = 40 A DC (P400 series)
- 4** - Circuit configuration
 0 = single phase, hybrid bridge common cathode
 2 = single phase, hybrid bridge doubler connection
 3 = single phase, all SCR bridge
- 5** - Voltage code
 1 = 400 V
 2 = 600 V
 3 = 800 V
 4 = 1000 V
 5 = 1200 V
- 6** - K = optional voltage suppression
- 7** - W = optional freewheeling diode

| CIRCUIT CONFIGURATION | | | |
|--|----------------------------|-------------------|--------------------|
| CIRCUIT DESCRIPTION | CIRCUIT CONFIGURATION CODE | SCHEMATIC DIAGRAM | TERMINAL POSITIONS |
| Single phase, hybrid bridge common cathode | 0 | | |
| Single phase, hybrid bridge doubler connection | 2 | | |
| Single phase, all SCR bridge | 3 | | |

| CODING (1) | | | | | |
|--|----------------------------|--------------|--------------------------|-------------------------|--|
| CIRCUIT DESCRIPTION | CIRCUIT CONFIGURATION CODE | BASIC SERIES | WITH VOLTAGE SUPPRESSION | WITH FREEWHEELING DIODE | WITH BOTH VOLTAGE SUPPRESSION AND FREEWHEELING DIODE |
| Single phase, hybrid bridge common cathode | 0 | P40. | P40.K | P40.W | P40.KW |
| Single phase, hybrid bridge doubler connection | 2 | P42. | P42.K | - | - |
| Single phase, all SCR bridge | 3 | P43. | P43.K | - | - |

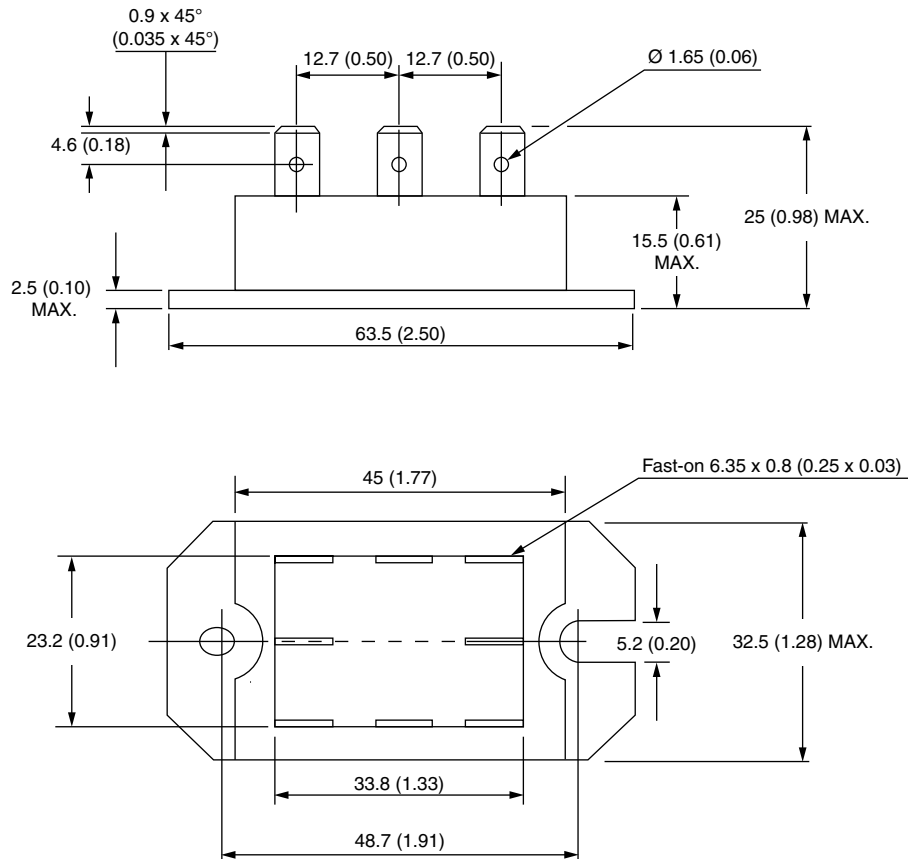
Note

(1) To complete code refer to Voltage Ratings table, i.e.: for 600 V P40.W complete code is P402W

| LINKS TO RELATED DOCUMENTS | |
|----------------------------|--|
| Dimensions | www.vishay.com/doc?95335 |

D-19 PACE-PAK

DIMENSIONS in millimeters (inches)





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