INA234 28-V, 12-Bit, Current, Voltage, and Power Monitor With an I²C Interface

1 Features

- High-side or low-side current sensing
- Operates from a 1.7-V to 5.5-V power supply
- Reports current, voltage and power
- Programmable full scale range: 20mV / 80mV
- Input common mode range: –0.3 V to 28 V
- Current monitoring accuracy:
  - 12-bit ADC resolution
  - 0.5% gain error (maximum)
  - 100-µV offset (maximum)
- Low input bias current: 10 nA (maximum)
- Configurable averaging options
- General call addressing allows conversion synchronization among devices
- Alert limits for over and under current events
- 1.2-V compliant I²C, SMBus interface
- 4-pin selectable addresses
- DSBGA-8 Package (0.745 mm × 1.508 mm)

2 Applications

- Mobile phones
- Smart speakers
- Wearables
- Battery chargers
- Power management
- Battery cell monitors and balancers
- Rack servers

3 Description

The INA234 device is a 12-bit digital current monitor with an I²C/SMBus-compatible interface that is compliant with a wide range of digital bus voltages such as 1.2 V, 1.8 V, 3.3 V, and 5.0 V. The device monitors the voltage across an external sense resistor and reports values for current, bus voltage, and power.

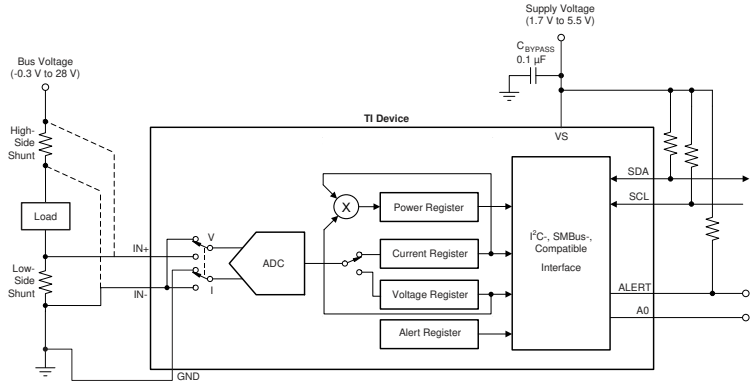
The INA234 features programmable ADC conversion times and averaging. The device also has a programmable calibration value with an internal multiplier that enables direct readouts of current in amperes and power in watts. The device monitors the bus voltage present on the IN- pin and can alert on over/under current as well as over/under voltage conditions. High input impedance while in current measurement mode allows use of larger current sense resistors needed to measure small value system currents.

The INA234 senses current on common-mode bus voltages that can vary from –0.3 V to 28 V, independent of the supply voltage. The device operates from a single 1.7-V to 5.5-V supply, drawing a typical supply current of 300 µA in normal operation. The device can be placed in a low-power standby mode where the typical operating current is 2.2 µA. The device is specified over the operating temperature range between –40°C and +125°C and features up to 4 programmable addresses.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA234	DSBGA (8)	0.745 mm × 1.508 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



High-Side or Low-Side Sensing Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision * (May 2021) to Revision A (August 2021)	Page
• Changed data sheet status from Advanced Information to Production Data	1

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5 Pin Configuration and Functions

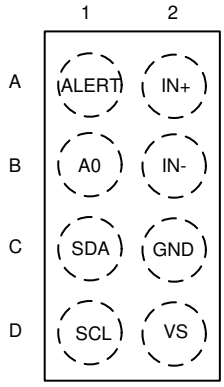


Figure 5-1. YBJ Package 8-Bump DSBGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	B1	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 7-1 lists the pin settings and corresponding addresses.
ALERT	A1	Digital output	Multifunctional alert, open-drain output. This pin alerts to report fault conditions or can be configured to notify host when a conversion is complete.
GND	C2	Ground	Ground for both analog and digital.
IN–	B2	Analog input	Current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor. Bus voltage measurements are made with respect to this pin.
IN+	A2	Analog input	Current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
SCL	D1	Digital input	Serial bus clock line, open-drain input.
SDA	C1	Digital input/output	Serial bus data line, open-drain input/output
VS	D2	Power Supply	Power supply, 1.7 V to 5.5 V

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply Voltage		6	V
V_{IN+}, V_{IN-}	Differential (V_{IN+}) - (V_{IN-})	–26	26	V
	Common - mode	GND – 0.3	30	V
V_{IO}	SDA, SCL, ALERT, A0	GND – 0.3	6	V
	Input current into any pin		5	mA
	Open-drain digital output current (SDA, ALERT)		10	mA
T_A	Operating Temperature	–55	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input range	GND – 0.3		28	V
V_S	Operating supply range	1.7		5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA234 YBJ (DSBGA) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

at T_A = 25°C, V_S = 3.3 V, V_{SENSE} = V_{IN+} - V_{IN-} = 0 mV, V_{IN-} = V_{BUS} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
CMRR	Common-mode rejection	V_{CM} = –0.3 V to 28 V, T_A = –40°C to 125°C	100	120		dB
	Shunt voltage input range	ADCRANGE = 0	–81.9175		81.92	mV
		ADCRANGE = 1	–20.4794		20.48	mV
V_{os}	Shunt offset voltage	V_{CM} = 12 V			±100	µV
dV_{os}/dT	Shunt offset voltage drift	T_A = –40°C to +125°C			±0.5	µV/°C
V_{os_b}	IN- bus offset Voltage				±15	mV
dV_{os_b}/dT	IN- bus offset voltage drift	T_A = –40°C to +125°C			±100	µV/°C
$PSRR_{SHUNT}$	Power supply rejection ratio (Current measurements)	V_S = 1.7 V to 5.5 V, T_A = –40°C to 125°C		±0.5	±2.5	µV/V
$PSRR_{BUS}$	Power supply rejection ratio (Voltage measurements)	V_S = 1.7 V to 5.5 V, T_A = –40°C to 125°C, V_{IN-} = 105 mV		±0.5	±2.5	mV/V
Z_{IN-}	IN- input impedance	Bus Voltage Measurement Mode		1.05		MΩ
I_{B_SHDWN}	Input Leakage	IN+, IN-, Shutdown Mode		0.1	5	nA
I_B	Input bias current	IN+, IN-, Current Measurement Mode		0.1	10	nA
DC ACCURACY						
R_{DIFF}	Differential Input Impedance (IN+ to IN-)	Shunt or Current Measurement Modes, V_{IN+} - V_{IN-} < 82 mV		140		kΩ
	ADC Resolution	T_A = –40°C to 125°C		12		Bits
	1 LSB step size	Shunt Voltage, ADCRANGE = 0		40		µV
		Shunt Voltage, ADCRANGE = 1		10		µV
		Bus Voltage		25.6		mV
	ADC Conversion-time (T_A = –40°C to 125°C)	CT bit = 000	133	140	147	µs
		CT bit = 001	194	204	214	µs
		CT bit = 010	315	332	349	µs
		CT bit = 011	559	588	617	µs
		CT bit = 100	1.045	1.100	1.155	ms
		CT bit = 101	2.01	2.116	2.222	ms
		CT bit = 110	3.948	4.156	4.364	ms
		CT bit = 111	7.832	8.244	8.656	ms
G_{SERR}	Shunt voltage gain error				±0.5	%
G_{S_DRFT}	Shunt voltage gain error drift	T_A = –40°C to +125°C			50	ppm/°C
G_{BERR}	V_{IN-} voltage gain error				±0.5	%
G_{B_DRFT}	V_{IN-} voltage gain error drift	T_A = –40°C to +125°C			50	ppm/°C
INL	Integral Non-Linearity			±2		m%
DNL	Differential Non-Linearity			±0.1		LSB
POWER SUPPLY						
I_Q	Quiescent current	V_{SENSE} = 0 mV		300	380	µA
		I_Q vs. temperature, T_A = –40°C to +125°C			500	µA
		Shutdown		2.2	3	µA
V_{POR}	Power-on reset threshold	V_S falling		0.95		V

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at T_A = 25°C, V_S = 3.3 V, V_{SENSE} = V_{IN+} - V_{IN-} = 0 mV, V_{IN-} = V_{BUS} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SMBUS						
	SMBUS timeout			28	35	ms
DIGITAL INPUT / OUTPUT						
	Input capacitance			3		pF
V_{IH}	Logic input level, high	V_S = 1.7 V to 5.5 V, T_A = –40°C to +125°C	0.9		5.5	V
V_{IL}	Logic input level, low	V_S = 1.7 V to 5.5 V, T_A = –40°C to +125°C	0		0.4	V
V_{HYS}	Hysteresis			130		mV
V_{OL}	Logic output level, low	I_{OL} = 3 mA, V_S = 1.7 V to 5.5 V, T_A = –40°C to +125°C	0		0.3	V
	Digital leakage input current	0 ≤ V_{INPUT} ≤ V_S	–1		1	µA

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6.6 Timing Requirements (I^2C)

		MIN	NOM	MAX	UNIT
I^2C BUS (FAST MODE)					
$F_{(SCL)}$	I^2C clock frequency	1		400	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	600			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		900	ns
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1300			ns
$t_{(HIGH)}$	SCL clock high period	600			ns
t_F	Data fall time			300	ns
t_F	Clock fall time			300	ns
t_R	Clock rise time			300	ns
t_R	Clock rise time (SCLK ≤ 100 kHz)			1000	ns
I^2C BUS (HIGH-SPEED MODE)					
$F_{(SCL)}$	I^2C clock frequency	10		2940	kHz
$t_{(BUF)}$	Bus free time between STOP and START conditions	160			ns
$t_{(HDSTA)}$	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
$t_{(SUSTA)}$	Repeated START condition setup time	100			ns
$t_{(SUSTO)}$	STOP condition setup time	100			ns
$t_{(HDDAT)}$	Data hold time	10		125	ns
$t_{(SUDAT)}$	Data setup time	20			ns
$t_{(LOW)}$	SCL clock low period	200			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
t_F	Data fall time			80	ns
t_F	Clock fall time			40	ns
t_R	Clock rise time			40	ns

6.7 Timing Diagram

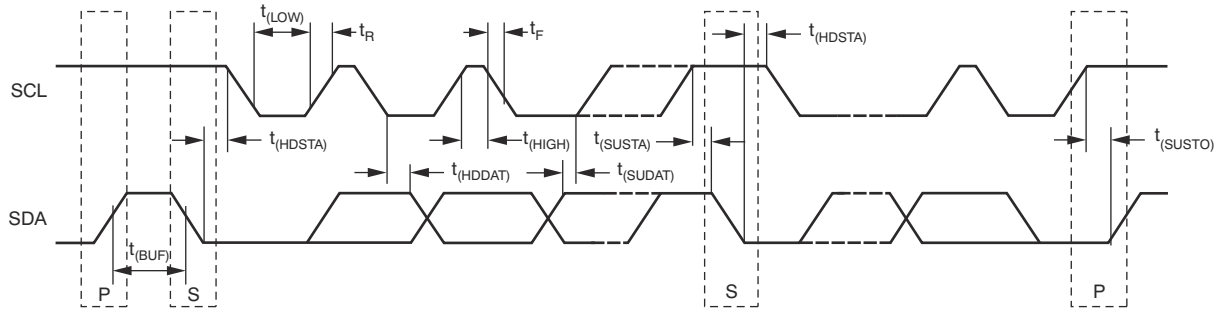


Figure 6-1. I^2C Timing Diagram

6.8 Typical Characteristics

at T_A = 25°C, V_{VS} = 3.3 V, V_{CM} = 12 V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV (unless otherwise noted)

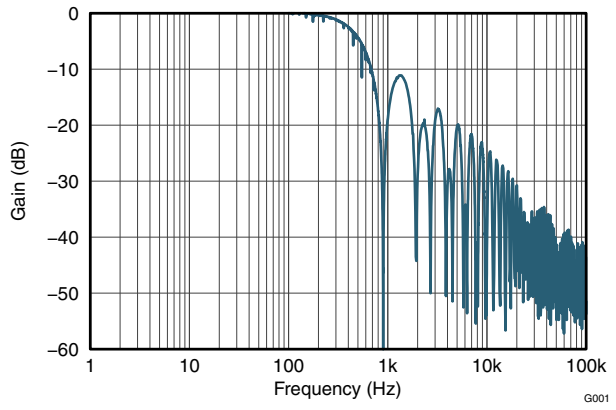


Figure 6-2. Frequency Response

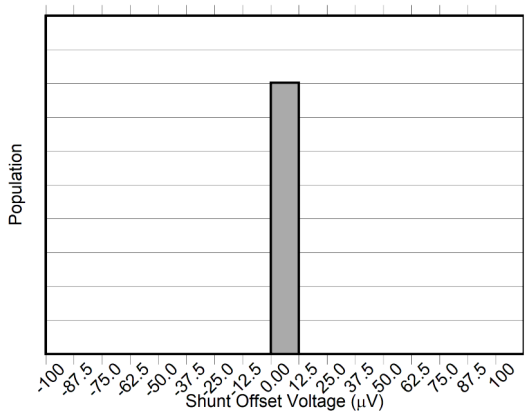


Figure 6-3. Shunt Input Offset Voltage Production Distribution

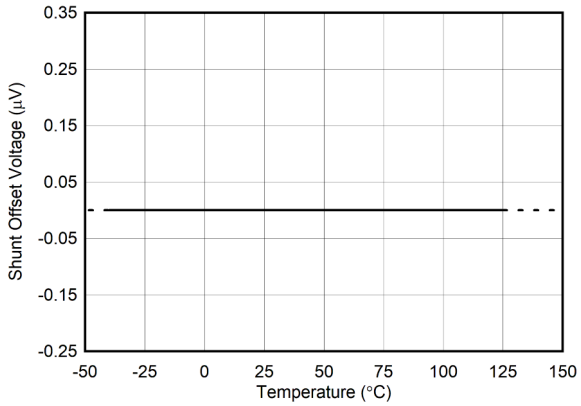


Figure 6-4. Shunt Input Offset Voltage vs. Temperature

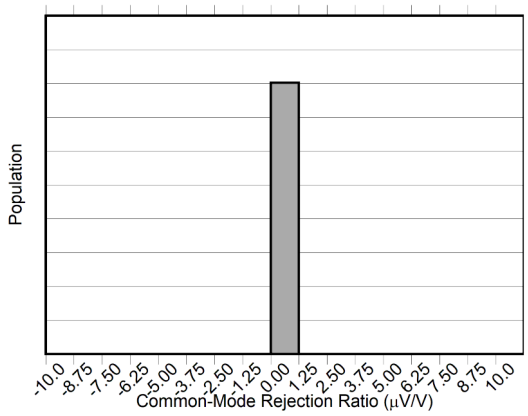


Figure 6-5. CMRR Production Distribution

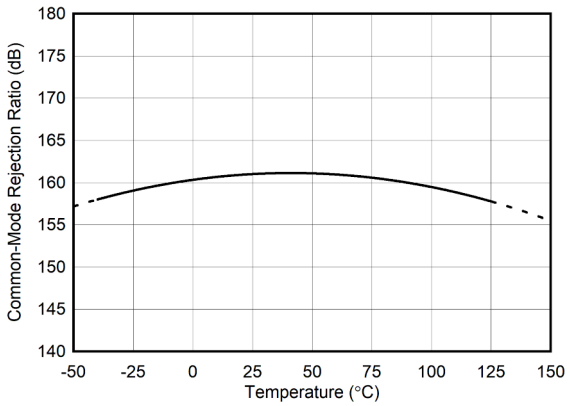


Figure 6-6. Shunt Input CMRR vs. Temperature

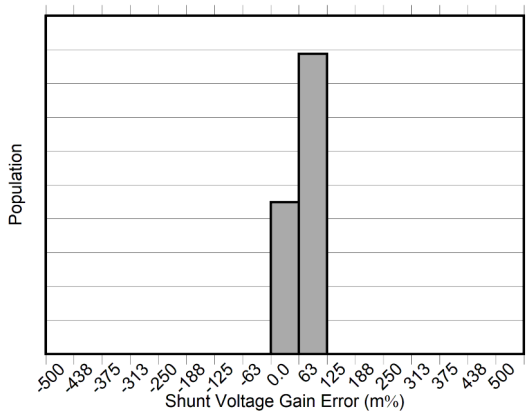


Figure 6-7. Shunt Voltage Gain Error Production Distribution

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3 V, V_{CM} = 12 V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV (unless otherwise noted)

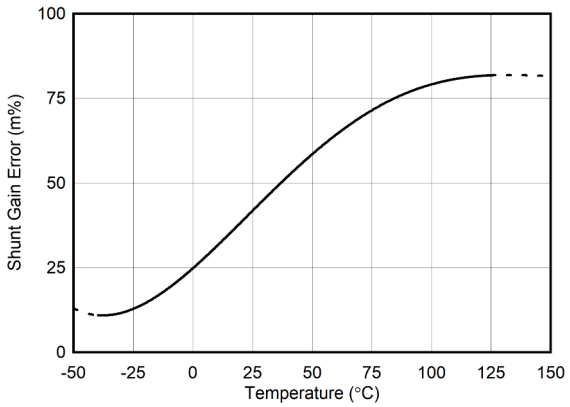


Figure 6-8. Shunt Gain Error vs. Temperature

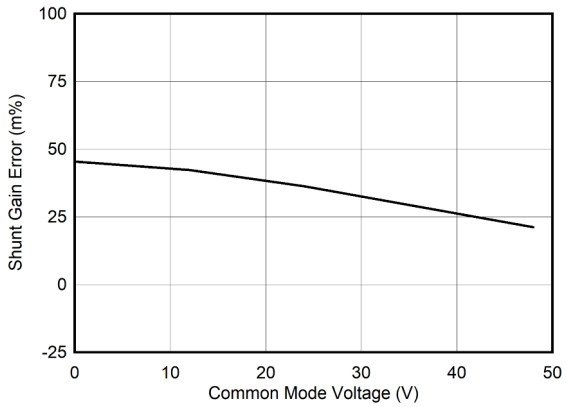


Figure 6-9. Shunt Gain Error vs. Common-Mode Voltage

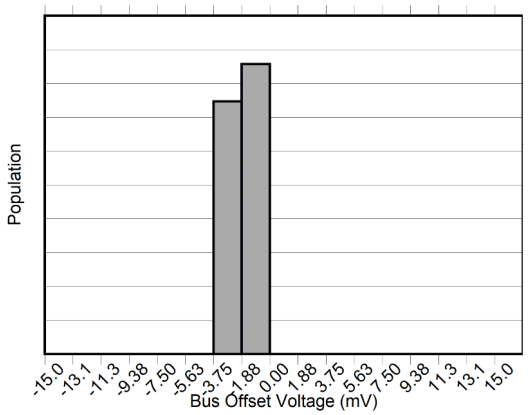


Figure 6-10. Bus Offset Voltage (V_{IN-}) Production Distribution

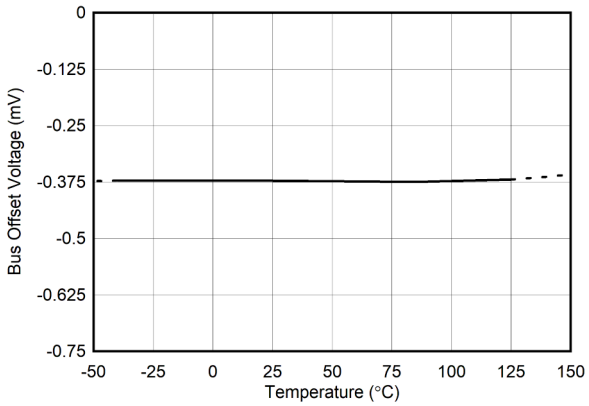


Figure 6-11. Bus Offset Voltage (V_{IN-}) vs. Temperature

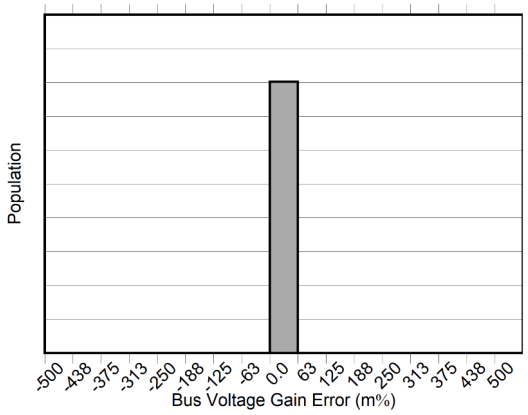


Figure 6-12. Bus Voltage (V_{IN-}) Gain Error Production Distribution

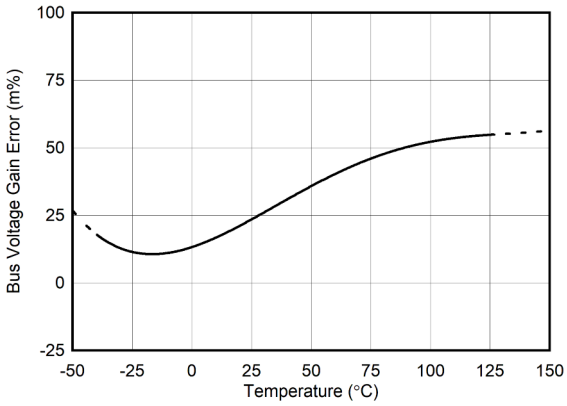


Figure 6-13. Bus Voltage (V_{IN-}) Gain Error vs. Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3 V, V_{CM} = 12 V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV (unless otherwise noted)

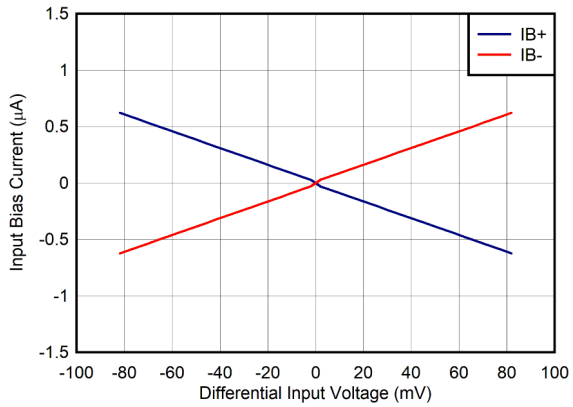


Figure 6-14. Input Bias Current vs. Differential Voltage

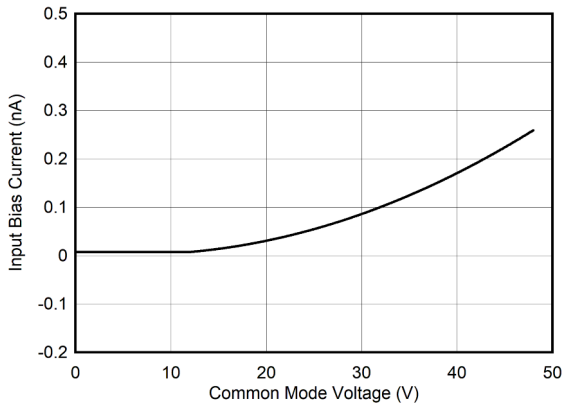


Figure 6-15. Input Bias Current vs. Common-Mode Voltage (IB+, IB-)

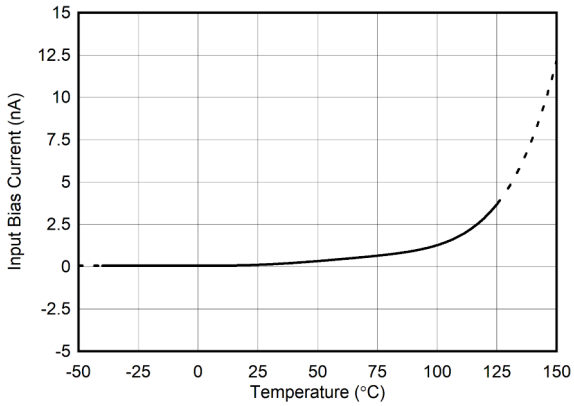


Figure 6-16. Input Bias Current vs. Temperature

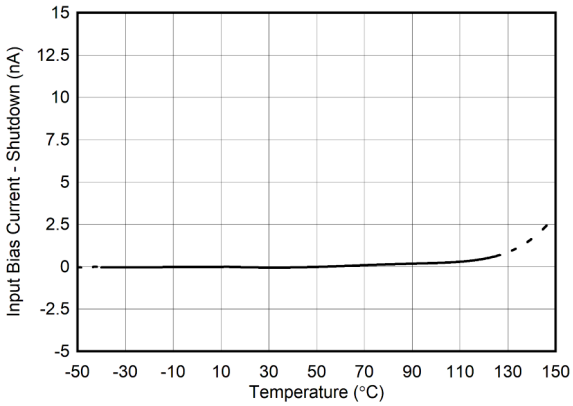


Figure 6-17. Input Bias Current vs. Temperature (Shutdown)

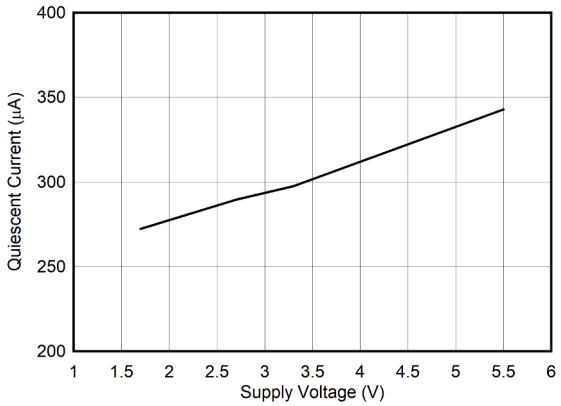


Figure 6-18. Quiescent Current vs. Temperature

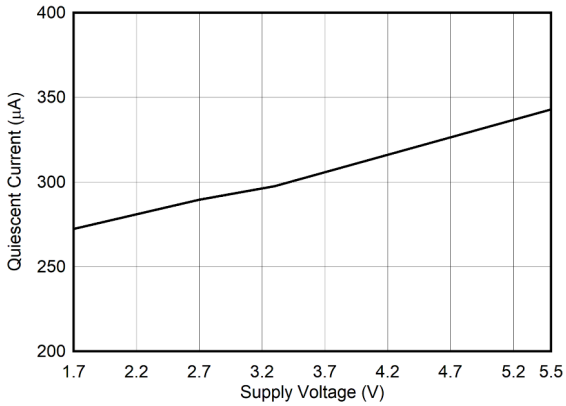


Figure 6-19. Quiescent Current vs. Supply Voltage

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3 V, V_{CM} = 12 V, and V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV (unless otherwise noted)

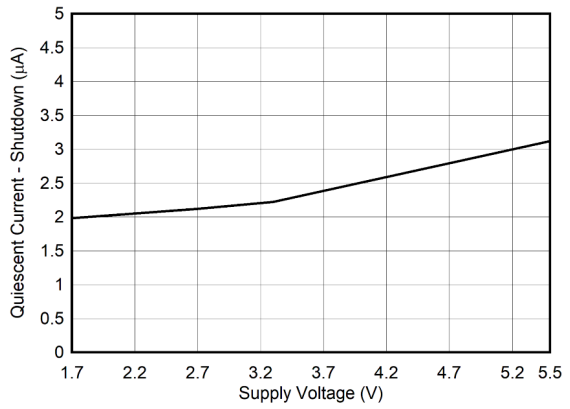


Figure 6-20. Quiescent Current - Shutdown vs. Supply Voltage

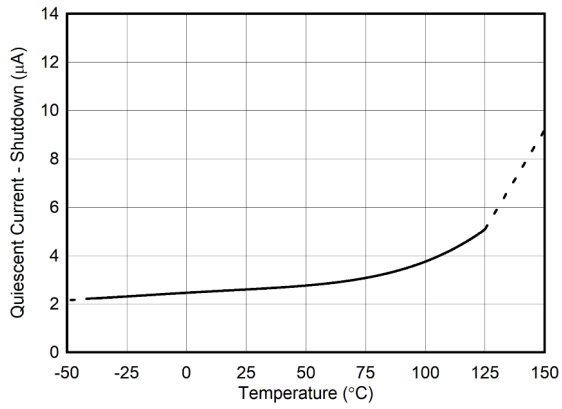


Figure 6-21. Quiescent Current - Shutdown vs. Temperature

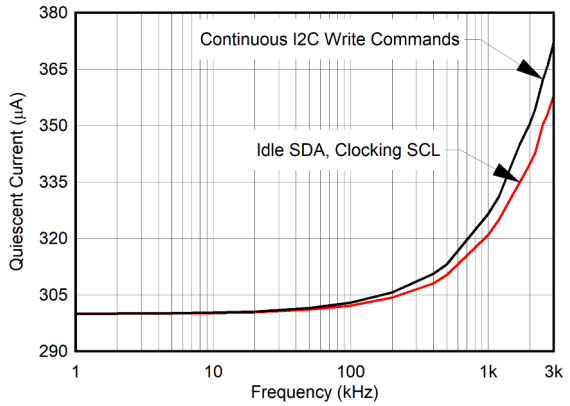


Figure 6-22. Quiescent Current vs. Clock(SCL) Frequency

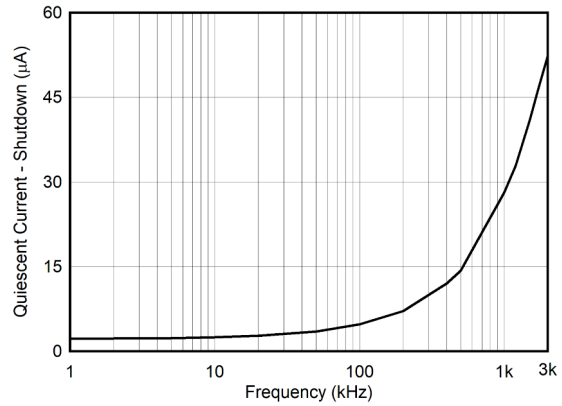


Figure 6-23. Quiescent Current - Shutdown vs. SCL Frequency

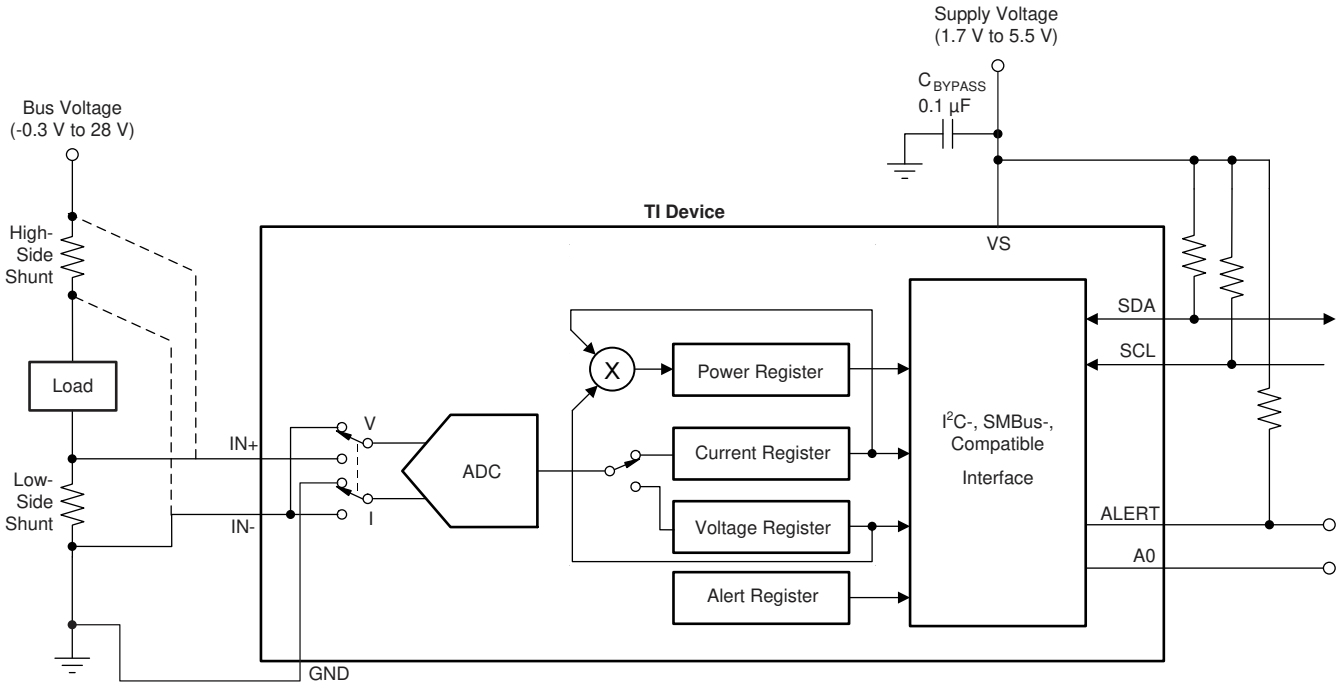
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7 Detailed Description

7.1 Overview

The INA234 is a digital current-sense amplifier with an I²C- and SMBus-compatible interface. The device reports the sensed current and features programmable out-of-range limits to issue alerts when the current is outside the normal range of operation. The integrated analog-to-digital converter (ADC) can be set to different averaging modes and configured for continuous-versus-triggered operation. *Device Registers* provides detailed register information for the INA234.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated Analog-to-Digital Convertor (ADC)

The INA234 integrates a low offset 12-bit delta-sigma (ΔΣ) ADC. This ADC is multiplexed to process both the shunt voltage and bus voltage measurements. Bus voltage measurements are made with respect to IN- and GND. The shunt voltage measurement is a differential measurement of the voltage developed when the load current flows through a shunt resistor as measured between the IN+ and IN– pins. The shunt voltage measurement has an maximum offset voltage of only 100 µV and a maximum gain error of 0.5%. The low offset voltage of the shunt voltage measurement allows for increased accuracy at light load conditions for a given shunt resistor value. Another advantage of low offset is the ability to sense a lower voltage drop across the sense resistor accurately, thus allowing for a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current-sense circuit and help improve the power efficiency of the end application.

There are no special considerations for power-supply sequencing because the bus common-mode at the IN+ and IN- pins and power-supply voltage at the vs. pin are independent of each other; therefore, the bus common-mode voltage can be present with the supply voltage off, and vice-versa.

7.3.2 Power Calculation

Figure 7-1 shows that the current and power are calculated after a shunt voltage and bus voltage measurement. Power is calculated based on the previous current calculation and the latest bus voltage measurement. If the value loaded into the calibration register is zero, the power value reported is also zero. The current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged. After all

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of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers where they can then be read. These calculations are performed in the background and do not add to the overall conversion time.

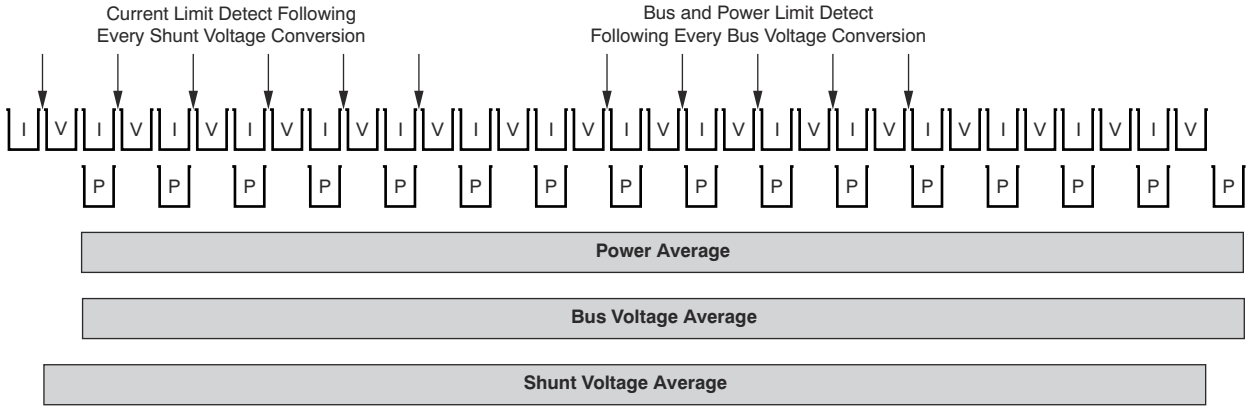


Figure 7-1. Power Calculation Scheme

7.3.3 Low Bias Current

When performing a current measurement, the INA234 features very low input bias current which provides several benefits. The low input bias current of the INA234 reduces the current consumed by the device in both active and shutdown state. Another benefit of low bias current is that it allows the use of input filters to reject high-frequency noise before the signal is converted to digital data. In traditional digital current-sense monitors, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias current, the reduction in accuracy due to input filters is minimized. An additional benefit of low bias current is the ability to use a larger shunt resistor to accurately sense smaller currents. Use of a larger value for the shunt resistor allows the device to accurately monitor currents in the sub-mA range.

The bias current in the INA234 is the smallest when the sensed current is zero. As the current starts to increase, the differential voltage drop across the shunt resistor increases which results in an increase in the bias current (see Figure 6-14).

The INA234 has low bias current only when making a current measurement, when bus voltage measurements are made the impedance of the IN- will decrease. During bus voltage measurements the IN- pin will be connected to an internal resistor divider with an impedance of approximately 1 MΩ. Configuring the ADC to perform only current measurements will allow the device to always have low bias current.

7.3.4 Low Voltage Supply and Wide Common-Mode Voltage Range

The supply voltage range of the INA234 is 1.7 V to 5.5 V. The ability to operate at 1.7 V enables the device to be used in 1.8-V supply rails. Even with a supply voltage of 1.7 V, the device can monitor currents on voltage rails as high as 28 V. This wide common-mode range of operation allows the device to be used in many applications where the common-mode voltage exceeds the supply voltage rail.

7.3.5 ALERT Pin

The INA234 has a single Mask/Enable register (06h) that allows the ALERT pin to be programmed to respond to a single user-defined event or to a conversion ready notification if desired. The Mask/Enable register allows the selection from one of the five available functions to monitor and set the conversion ready bit (CNVR, Mask/Enable register) to control the response of the ALERT pin. Based on the function being monitored, a value would then be entered into the Alert Limit register (07h) to set the corresponding threshold value that asserts the ALERT pin.

The ALERT pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt voltage overlimit (SOL)

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- Shunt voltage underlimit (SUL)
- Bus voltage overlimit (BOL)
- Bus voltage underlimit (BUL)
- Power overlimit (POL)

The ALERT pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable register exceeds the value programmed into the Alert Limit register. Only one of these alert functions can be enabled and monitored at a time. If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority and responds to the Alert Limit register value. For example, if the SOL and the SUL are both selected, the ALERT pin asserts when the Shunt Voltage Over Limit register exceeds the value in the Alert Limit register.

The conversion-ready state of the device can also be monitored at the ALERT pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. The conversion ready flag (CVRF) bit can be monitored at the ALERT pin along with one of the alert functions. If an alert function and the CNVR bit are both enabled for monitoring at the ALERT pin, then after the ALERT pin is asserted, the CVRF bit (D3) and the AFF bit (D4) in the Mask/Enable register must be read following the alert to determine the source of the alert. If the conversion ready feature is not desired, and the CNVR bit is not set, the ALERT pin only responds to an exceeded alert limit based on the alert function enabled.

If the alert function is not used, the ALERT pin can be left floating without impacting the operation of the device.

Refer to Figure 7-1 to see the relative timing of when the value in the Alert Limit register is compared to the corresponding converted value. For example, if the alert function that is enabled is Shunt Voltage Over Limit (SOL), following every shunt voltage conversion the value in the Alert Limit register is compared to the measured shunt voltage to determine if the measurements have exceeded the programmed limit. The AFF bit (D4, Mask/Enable register) asserts high any time the measured voltage exceeds the value programmed into the Alert Limit register. In addition to the AFF bit being asserted, the ALERT pin is asserted based on the Alert Polarity bit (APOL, D1, Mask/Enable register). If the Alert Latch is enabled, the AFF bit and ALERT pin remain asserted until either the Configuration register is written to or the Mask/Enable register is read.

The bus voltage alert functions (BOL and BUL, Mask/Enable register) compare the measured bus voltage to the Alert Limit register following every bus voltage conversion and assert the AFF bit and ALERT pin if the limit threshold is exceeded.

The power overlimit alert function (POL, Mask/Enable register) is also compared to the calculated power value following every bus voltage measurement conversion and asserts the AFF bit and ALERT pin if the limit threshold is exceeded.

The alert function compares the programmed alert limit value to the result of each corresponding conversion. Therefore, an alert can be issued during a conversion cycle where the averaged value of the signal does not exceed the alert limit. Triggering an alert based on this intermediate conversion allows for out-of-range events to be detected faster than the averaged output data registers are updated. This fast detection can be used to create alert limits for quickly changing conditions through the use of the alert function, as well as to create limits to longer-duration conditions through software monitoring of the averaged output values.

7.4 Device Functional Modes

7.4.1 Continuous Verses Triggered Operation

The INA234 has two operating modes, continuous and triggered, that determine how the ADC operates after these conversions. When the INA234 is in the normal operating mode (that is, the MODE bits of the Configuration register are set to '111'), it continuously converts a shunt voltage reading followed by a bus voltage reading.

In triggered mode, writing any of the triggered convert modes into the Configuration register (0h) (that is, the MODE bits of the Configuration register are set to 001) triggers a single-shot conversion. This action produces a single set of measurements. To trigger another single-shot conversion, the Configuration register must be written to again, even if the mode does not change.

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Although the INA234 can be read at any time, and the data from the last conversion remain available, the conversion ready flag bit (CVRF bit, Mask/Enable register) is provided to help coordinate single-shot or triggered conversions. The CVRF bit is set after all conversions, averaging, and multiplication operations are complete for a single cycle.

The CVRF bit clears under these conditions:

1. Writing to the Configuration register, except when configuring the MODE bits for power-down mode; or
2. Reading the Mask/Enable register.

7.4.2 Device Shutdown

In addition to the two operating modes (continuous and triggered), the INA234 also has a power-down mode that reduces the quiescent current and input bias current. The power-down mode reduces supply drain when the device is not being used. Full recovery from power-down mode requires 40 ms. The device remains in power-down mode until one of the active modes settings are written into the Configuration register.

7.4.3 Power-On Reset

Power-on reset (POR) is asserted when V_S drops below 0.95 V (typical) at which all of the registers are reset to their default values. The default power-up register values are shown in the reset column for each register description. Table 7-2 provides links to the register descriptions.

7.4.4 Averaging and Conversion Time Considerations

The INA234 has programmable conversion times for both the shunt voltage and bus voltage measurements. The conversion times for these measurements can be selected from as fast as 140 µs to as long as 8.244 ms. The conversion time settings, along with the programmable averaging mode, allow the INA234 to be configured to optimize the available timing requirements in a given application. For example, if a system requires that data be read every 5 ms, the INA234 can be configured with the conversion times set to 588 µs and the averaging mode set to 4. This configuration results in the data updating approximately every 4.7 ms. The INA234 can also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation allows for the time spent measuring the bus voltage to be reduced relative to the shunt voltage measurement. The shunt voltage conversion time can be set to 4.156 ms with the bus voltage conversion time set to 588 µs, and the averaging mode set to 1. This configuration also results in data updating approximately every 4.7 ms.

There are trade-offs associated with the conversion time settings and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the INA234 to reduce noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the INA234 to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an effect on the measurement accuracy. Figure 7-2 shows multiple conversion times to illustrate the effect of noise on the measurement. In order to achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages, based on the timing requirements of the system.

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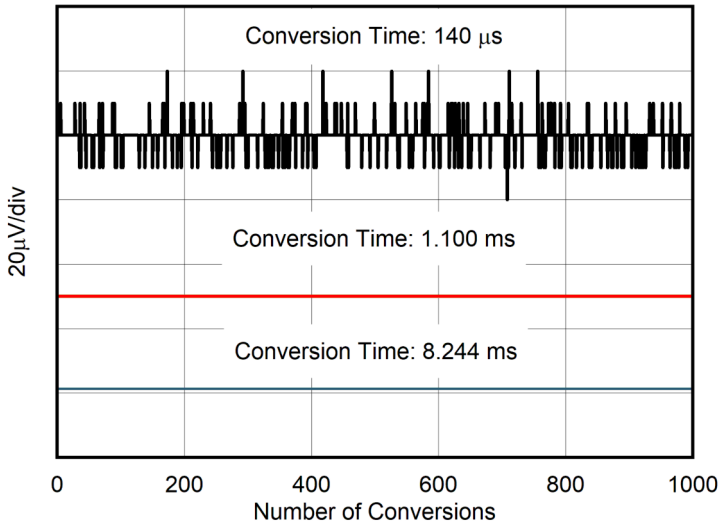


Figure 7-2. Noise vs. Conversion Time

7.5 Programming

7.5.1 I²C Serial Interface

The INA234 operates only as a target on both the SMBus and I²C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines. This noise introduction could occur from capacitive coupling signal edges between the two communication lines themselves or from other switching noise sources present in the system. Routing traces in parallel with ground in between layers on a printed-circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shielded communication lines reduce the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The INA234 supports the transmission protocol for fast mode up to 400 kHz and high-speed mode up to 2.94 MHz. All data bytes are transmitted most significant byte first and follow the SMBus 3.0 transfer protocol.

To communicate with the INA234, the controller must first address targets through a target address byte. The target address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device uses a single address pin, A0. Table 7-1 shows possible configurations for A0 and the corresponding address. The device samples the state of the A0 pin on every bus communication. The pin state for A0 must be established before any activity on the interface occurs. When connecting the SDA pin to A0 to set the device address, additional hold time of 100 ns is needed on the MSB of the I2C address to insure correct device addressing.

Table 7-1. Address Pins and Target Addresses

A0	Target Address
GND	1000000
VS	1000001
SDA	1000010
SCL	1000011

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7.5.2 Writing to and Reading Through the I²C Serial Interface

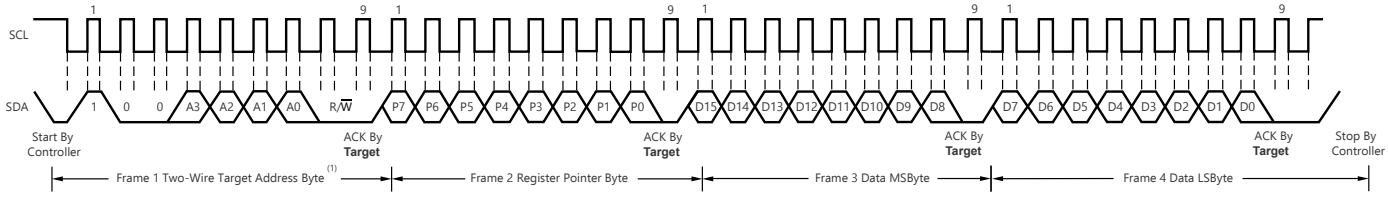
Accessing a specific register on the INA234 is accomplished by writing the appropriate value to the register pointer. Refer to *Register Maps* for a complete list of registers and corresponding addresses. The value for the register pointer (see Figure 7-5) is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address, with the R/$\overline{W}$ bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The controller may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a target address byte with the R/ $\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The controller then generates a start condition and sends the address byte for the target with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register pointer. This byte is followed by an *Acknowledge* from the controller; then the target transmits the least significant byte. The controller may or may not acknowledge receipt of the second data byte. The controller may terminate data transfer by generating a *Not-Acknowledge* after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

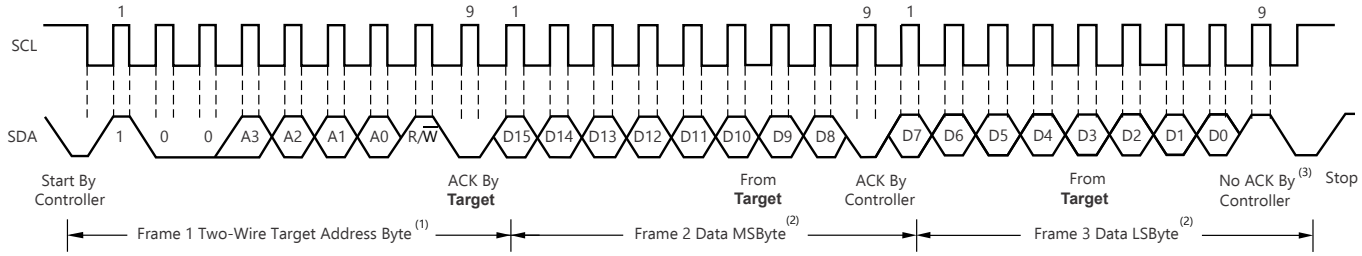
Figure 7-3 shows the write operation timing diagram. Figure 7-4 shows the read operation timing diagram. These diagrams are shown for reading/writing to 16 bit registers.

Register bytes are sent most-significant byte first, followed by the least significant byte.



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to Table 7-1.
B. The device does not support packet error checking (PEC) or perform clock stretching.

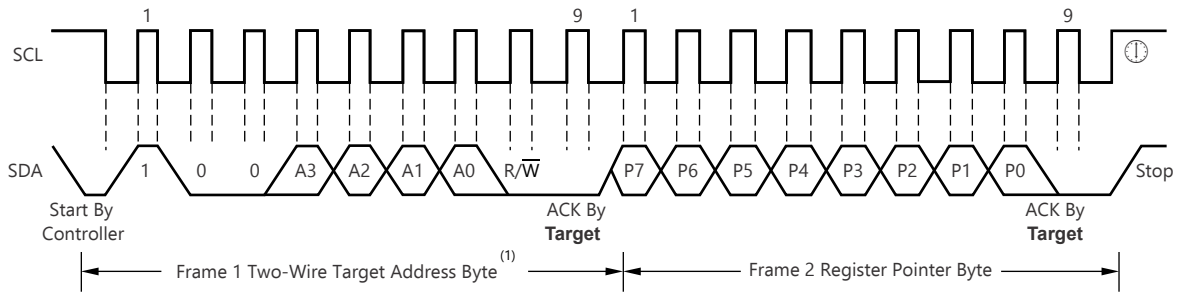
Figure 7-3. Timing Diagram for Write Word Format



A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to Table 7-1.
B. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 7-5.
C. ACK by the controller can also be sent.
D. The device does not support packet error checking (PEC) or perform clock stretching.

Figure 7-4. Timing Diagram for Read Word Format

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A. The value of the Target Address byte is determined by the setting of the A0 address pin. Refer to Table 7-1.

Figure 7-5. Typical Register Pointer Set

7.5.3 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The controller generates a start condition followed by a valid serial byte containing high-speed (HS) controller code *00001XXX*. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The device does not acknowledge the HS controller code, but does recognize it and switches its internal filters to support 2.94-MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.94 MHz are allowed. Instead of using a stop condition, use repeated start conditions to maintain the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

7.5.4 General Call Reset

A general call reset to multiple devices is implemented by addressing the general call address 0000 000, with the last R/$\overline{W}$ bit set to 0. This is then followed by the following data byte 0000 0110 (06h).

On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset. All INA234 devices on the bus will do a soft reset operation and return to the default power-up conditions

7.5.5 General Call Start Byte

A general call ADC conversion start command to multiple INA234 devices is implemented by addressing the general call address 0000 000, with the last R/$\overline{W}$ bit set to 1. No other data bytes are required. Be aware that other devices in the bus that use general call start commands on the bus will also trigger a start of conversion.

7.5.6 SMBus Alert Response

The INA234 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple targets. When an Alert occurs, the controller can broadcast the Alert Response target address (0001 100) with the Read/Write bit set high. Following this Alert Response, any target that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus.

The Alert Response can activate several different target devices simultaneously, similar to the I²C General Call. If more than one target attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until that device wins arbitration.

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7.6 Register Maps

7.6.1 Device Registers

Table 7-2 lists the INA234 registers. All register locations not listed in Table 7-2 should be considered as reserved locations and the register contents should not be modified.

Table 7-2. INA234 Registers

Address	Register Name	Register Size (bits)	Reset Value	Section
0h	Configuration Register	16	4127h	Go
1h	Shunt Voltage Register	16	0000h	Go
2h	Bus Voltage Register	16	0000h	Go
3h	Power Register	16	0000h	Go
4h	Current Register	16	0000h	Go
5h	Calibration Register	16	0000h	Go
6h	Mask/Enable Register	16	0000h	Go
7h	Alert Limit Register	16	0000h	Go
3Eh	Manufacturer ID Register	16	5449h	Go
3Fh	Device ID Register	16	A480h	Go

Complex bit access types are encoded to fit into small table cells. Table 7-3 shows the codes that are used for access types in this section.

Table 7-3. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

7.6.1.1 Configuration Register (Address = 0h) [reset = 4127h]

The configuration register is shown in Table 7-4.

Table 7-4. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0b	Set this bit to '1' to generate a system reset that is the same as power-on reset. Resets all registers to default values and then self-clears. **0b = Normal Operation** 1b = System Reset self clears registers to default values
14-13	Reserved	R	10b	Reserved value always returns 10b
12	ADCRANGE	R/W	0b	Enables the selection of the shunt full scale input across IN+ and IN–. **0b = ±81.92 mV** 1b = ±20.48 mV

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Table 7-4. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-9	AVG	R/W	000b	Sets the number of ADC conversion results to be averaged. The read-back registers are updated after averaging is completed. **000b = 1** 001b = 4 010b = 16 011b = 64 100b = 128 101b = 256 110b = 512 111b = 1024
8-6	VBUSCT	R/W	100b	Sets the conversion time of the VBUS measurement 000b = 140 µs 001b = 204 µs 010b = 332 µs 011b = 588 µs **100b = 1100 µs** 101b = 2116 µs 110b = 4156 µs 111b = 8244 µs
5-3	VSHCT	R/W	100b	Sets the conversion time of the SHUNT measurement 000b = 140 µs 001b = 204 µs 010b = 332 µs 011b = 588 µs **100b = 1100 µs** 101b = 2116 µs 110b = 4156 µs 111b = 8244 µs
2-0	MODE	R/W	111b	Operating mode, modes can be selected to operate the device either in Shutdown mode, continuous mode or triggered mode. The mode also allows user to select mux settings to set continuous or triggered mode on bus voltage, shunt voltage measurement. 000b = Shutdown 001b = Shunt Voltage triggered, single shot 010b = Bus Voltage triggered, single shot 011b = Shunt voltage and Bus voltage triggered, single shot 100b = Shutdown 101b = Continuous Shunt voltage 110b = Continuous Bus voltage **111b = Continuous Shunt and Bus voltage**

Return to the Summary Table.

7.6.1.2 Shunt Voltage Register (Address = 1h) [reset = 0000h]

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT} and is show in Table 7-5. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

Example: For a value of V_{SHUNT} = –80 mV:

1. Take the absolute value: 80 mV
2. Translate this number to a whole decimal number (80 mV ÷ 2.5 µV) = 32000
3. Convert this number to binary = 0111 1101 0000 0000
4. Complement the binary result = 1000 0010 1111 1111

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5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h

If averaging is enabled, this register displays the averaged value.

Table 7-5. Shunt Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	VSHUNT	R	000h	Differential voltage measured across the shunt output. Two's complement value.
3-0	Reserved	R	0h	Always returns 0. Remove these bits from the full result by doing a right arithmetic shift

Return to the Summary Table.

7.6.1.3 Bus Voltage Register (Address = 2h) [reset = 0000h]

The bus voltage register is shown in Table 7-6.

This register will only return positive values. If averaging is enabled, this register displays the averaged value.

Table 7-6. Bus Voltage Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0b	This bit returns Zero as common mode voltage is only positive
14-4	VBUS	R	000h	These bits readout the bus voltage of the system
3-0	Reserved	R	0h	Always returns 0. Remove these bits from the full result by doing a right arithmetic shift

Return to the Summary Table.

7.6.1.4 POWER Register (Address = 3h) [reset = 0000h]

The power register is shown in Table 7-7.

If averaging is enabled, this register displays the averaged value. The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register. This is an unsigned result.

Table 7-7. POWER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	POWER	R	0000h	This bit returns a calculated value of power in the system. This is an unsigned result.

Return to the Summary Table.

7.6.1.5 CURRENT Register (Address = 4h) [reset = 0000h]

CURRENT is shown in Table 7-8.

If averaging is enabled, this register displays the averaged value. The value of the Current Register is calculated by multiplying the decimal value in the Shunt Voltage Register with the decimal value of the Calibration Register.

Table 7-8. CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	CURRENT	R	000h	Calculated current output in Amperes. Two's complement value.
3-0	RESERVED	R	0h	Always returns 0. Remove these bits from the full result by doing a right arithmetic shift

Return to the Summary Table.

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7.6.1.6 Calibration Register (Address = 5h) [reset = 0000h]

The calibration register shown in Table 7-9 must be programmed to receive valid current and power results after initial power up or power cycle events.

This register provides the device with the value of the shunt resistor that was present to create the measured differential voltage. It also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB.

Table 7-9. Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	
14-0	SHUNT_CAL	R/W	0000h	Programmed value needed for doing the shunt voltage to current conversion.

Return to the Summary Table.

7.6.1.7 Mask/Enable Register (Address = 6h) [reset = 0000h]

The Mask/Enable Register is shown in Table 7-10.

Table 7-10. Mask/Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOL (Shunt Over-limit)	R/W	0b	Setting this bit high configures the ALERT pin to be asserted if the shunt voltage conversion result exceeds the value programmed in the LIMIT register
14	SUL (Shunt Under-limit)	R/W	0b	Setting this bit high configures the ALERT pin to be asserted if the shunt voltage conversion result is below the value programmed in the LIMIT register. Cannot be set if Shunt overlimit is set.
13	BOL (Bus Over-limit)	R/W	0b	Setting this bit high configures the ALERT pin to be asserted if the bus voltage conversion result exceeds the value programmed in the LIMIT register Cannot be set if Shunt overlimit or Shunt underlimit is set.
12	BUL (Bus Under-limit)	R/W	0b	Setting this bit high configures the ALERT pin to be asserted if the bus voltage conversion result is below the value programmed in the LIMIT register Cannot be set if Shunt over limit, Shunt under limit or Bus over limit is set.
11	POL (Power Over-limit)	R/W	0b	Setting this bit high configures the ALERT pin to be asserted if the power result exceeds the value programmed in the LIMIT register Cannot be set if Shunt over limit, Shunt under limit, Bus over limit or Bus under limit is set.
10	CNVR (Conversion Ready)	R/W	0b	Setting this bit high configures the ALERT pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion. **0b = Disable conversion ready flag on ALERT pin** 1b = Enables conversion ready flag on ALERT pin
9-6	Reserved	R	0000b	
5	MemError	R	0b	CRC or ECC error
4	AFF (Alert Function Flag)	R	0b	Alert Function Flag -While only one Alert Function can be monitored at the ALERT pin at a time, the Conversion Ready can also be enabled to assert the ALERT pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.

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Table 7-10. Mask/Enable Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CVRF (Conversion Ready Flag)	R	0b	Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Mask/Enable Register
2	OVF (Math Over-flow)	R	0b	This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid.
1	APOL (Alert Polarity)	R/W	0b	Alert Polarity bit sets the Alert pin polarity. **0b = Normal (Active-low open drain)** 1b= Inverted (active-high)
0	LEN (Alert Latch Enable)	R/W	0b	When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Alert Function Flag (AFF) bit resets to the idle states when the fault condition has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and AFF bit remains active following a fault until this register flag has been read. This bit must be set to use the I2C Alert Response function. **0b = Transparent** 1b = Latched Alert pin

Return to the Summary Table.

7.6.1.8 Alert Limit Register (Address = 7h) [reset = 0000h]

The alert limit register is shown in Table 7-11.

Table 7-11. Alert Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LIMIT	R/W	0000h	The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded. A two's complement value must be used for the Shunt Over Voltage limit. Limit values entered should match the format of the targeted register

Return to the Summary Table.

7.6.1.9 Manufacturer ID Register (Address = 3Eh) [reset = 5449h]

The manufacturer ID register is shown in Table 7-12.

Table 7-12. MANUFACTURE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANUFACTURE_ID	R	5449h	Reads back TI in ASCII

Return to the Summary Table.

7.6.1.10 Device ID Register (Address = 3Fh) [reset = A480h]

The Device ID register is shown in Table 7-13.

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Table 7-13. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	DIEID	R	A480h	Stores the device identification bits
3-0	Reserved	R	0h	Always read 0

Return to the Summary Table.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The INA234 is a current shunt monitor with an I^{2}C- and SMBus-compatible interface. The device monitors a shunt voltage drop to calculate the current and bus voltage at IN- pin to determine power. Programmable calibration value, conversion times, and averaging (combined with an internal multiplier) enable direct readouts of current in amperes and power in watts.

8.1.1 Device Measurement Range and Resolution

The INA234 device supports two input ranges for the shunt voltage measurement. The supported full scale differential input across the IN+ and IN– pins can be either ±81.92 mV or ±20.48 mV depending on the ADCRANGE bit in the Configuration Register (0h) register. The range for the bus voltage measurement at the IN- pin is from 0 V to 52.42 V, but is limited by process ratings to the max operating voltage.

Table 8-1 provides a description of full scale voltage on shunt and bus voltage measurements, along with their associated resolution.

Table 8-1. ADC Full Scale Values

PARAMETER	FULL SCALE VALUE	RESOLUTION
Shunt voltage	±81.92 mV (ADCRANGE = 0)	40 µV/LSB
	±20.48 mV (ADCRANGE = 1)	10 µV/LSB
Bus voltage	0 V to 52.4 V (Limit usable range to recommended operating voltage)	25.6 mV/LSB

The device shunt voltage and bus voltage measurements are read through the Shunt Voltage register (1h) and Bus Voltage register (2h), respectively. The digital output in shunt voltage and bus voltage registers is 16 bits with the last four bits reserved. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore the data value in shunt voltage register can be positive or negative. The bus voltage register data value is always positive. The output data can be directly converted into voltage by multiplying the digital value by its respective resolution size.

Furthermore, the device provides the flexibility to report calculated current in Amperes, power in Watts, as described in *Current and Power Calculations*.

8.1.2 Current and Power Calculations

For the INA234 to report current values in Amperes, a constant conversion value must be written in the calibration register that is dependent on the selected CURRENT_LSB and the shunt resistance used in the application. The value of the calibration register is calculated based on Equation 1. The term CURRENT_LSB is the chosen LSB step size for the CURRENT register where the current is stored. Equation 2 shows the minimum value of CURRENT_LSB is based on the maximum expected current, and it directly defines the maximum resolution of the CURRENT register. While the smallest CURRENT_LSB value yields highest resolution, it is common to select a higher round-number (no higher than 8x) value for the CURRENT_LSB in order to simplify the conversion of the CURRENT.

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The R_{SHUNT} term is the resistance value of the external shunt used to develop the differential voltage across the IN+ and IN– pins. Use Equation 1 for ADCRANGE = 0. For ADCRANGE = 1, the value of SHUNT_CAL must be divided by 4.

$$SHUNT_CAL = \frac{0.08192}{Current_LSB \times R_{SHUNT}} \quad (1)$$

where

- 0.08192 is an internal fixed value used to ensure scaling is maintained properly.
- CURRENT_LSB is a selected value for the current step size in amperes. Must be greater than or equal to CURRENT_LSB (minimum), but less than 8 x CURRENT_LSB(minimum) to reduce resolution loss.
- The value of SHUNT_CAL must be divided by 4 for ADCRANGE = 1.

$$CURRENT_LSB\ (minimum) = \frac{Maximum\ Expected\ Current}{2^{11}} \quad (2)$$

Note that the current is calculated following a shunt voltage measurement based on the value set in the SHUNT_CAL register. If the value loaded into the SHUNT_CAL register is zero, the current value reported through the CURRENT register is also zero.

After programming the SHUNT_CAL register with the calculated value, the measured current in Amperes can be read from the CURRENT register. Use Equation 3 to calculate the final value scaled by the CURRENT_LSB:

$$Current\ [A] = CURRENT_LSB \times CURRENT \quad (3)$$

where

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as a 16-bit value. Use Equation 4 to convert the power to Watts:

$$Power\ [W] = 32 \times CURRENT_LSB \times POWER \quad (4)$$

where

- POWER is the value read from the POWER register.
- CURRENT_LSB is selected value for the lsb size of the current calculation used in Equation 1.

Refer to *Detailed Design Procedure* for a design example using these equations.

8.1.3 ADC Output Data Rate and Noise Performance

The INA234 noise performance and effective resolution depend on the ADC conversion time. The device also supports digital averaging which can further help decrease digital noise. The flexibility of the device to select ADC conversion time and data averaging offers increased signal-to-noise ratio and achieves the highest dynamic range with lowest offset. The profile of the noise at lower signals levels is dominated by the system noise that is comprised mainly of 1/f noise or white noise. The effective resolution of the ADC can be increased by increasing the conversion time and increasing the number of averages.

Table 8-2 summarizes the output data rate conversion settings supported by the device. The fastest conversion setting is 140 µs. Typical noise-free resolution is represented as Effective Number of Bits (ENOB) based on device measured data. The ENOB is calculated based on noise peak-to-peak values, which assures that full noise distribution is taken into consideration.

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Table 8-2. INA234 Noise Performance

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±81.92-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±20.48-mV) (ADCRANGE = 1)
140	1	0.14	12.0	10.7
204	1	0.204	12.0	11.1
332	1	0.332	12.0	11.1
588	1	0.588	12.0	11.7
1100	1	1.1	12.0	12.0
2116	1	2.116	12.0	12.0
4156	1	4.156	12.0	12.0
8244	1	8.244	12.0	12.0
140	4	0.56	12.0	12.0
204	4	0.816	12.0	12.0
332	4	1.328	12.0	12.0
588	4	2.352	12.0	12.0
1100	4	4.4	12.0	12.0
2116	4	8.464	12.0	12.0
4156	4	16.624	12.0	12.0
8244	4	32.976	12.0	12.0
140	16	2.24	12.0	12.0
204	16	3.264	12.0	12.0
332	16	5.312	12.0	12.0
588	16	9.408	12.0	12.0
1100	16	17.6	12.0	12.0
2116	16	33.856	12.0	12.0
4156	16	66.496	12.0	12.0
8244	16	131.904	12.0	12.0
140	64	8.96	12.0	12.0
204	64	13.056	12.0	12.0
332	64	21.248	12.0	12.0
588	64	37.632	12.0	12.0
1100	64	70.4	12.0	12.0
2116	64	135.424	12.0	12.0
4156	64	265.984	12.0	12.0
8244	64	527.616	12.0	12.0
140	128	17.92	12.0	12.0
204	128	26.112	12.0	12.0
332	128	42.496	12.0	12.0
588	128	75.264	12.0	12.0
1100	128	140.8	12.0	12.0
2116	128	270.848	12.0	12.0
4156	128	531.968	12.0	12.0
8244	128	1055.232	12.0	12.0
140	256	35.84	12.0	12.0
204	256	52.224	12.0	12.0
332	256	84.992	12.0	12.0
588	256	150.528	12.0	12.0

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Table 8-2. INA234 Noise Performance (continued)

ADC CONVERSION TIME PERIOD [µs]	OUTPUT SAMPLE AVERAGING [SAMPLES]	OUTPUT SAMPLE PERIOD [ms]	NOISE-FREE ENOB (±81.92-mV) (ADCRANGE = 0)	NOISE-FREE ENOB (±20.48-mV) (ADCRANGE = 1)
1100	256	281.6	12.0	12.0
2116	256	541.696	12.0	12.0
4156	256	1063.936	12.0	12.0
8244	256	2110.464	12.0	12.0
140	512	71.68	12.0	12.0
204	512	104.448	12.0	12.0
332	512	169.984	12.0	12.0
588	512	301.056	12.0	12.0
1100	512	563.2	12.0	12.0
2116	512	1083.392	12.0	12.0
4156	512	2127.872	12.0	12.0
8244	512	4220.928	12.0	12.0
140	1024	143.36	12.0	12.0
204	1024	208.896	12.0	12.0
332	1024	339.968	12.0	12.0
588	1024	602.112	12.0	12.0
1100	1024	1126.4	12.0	12.0
2116	1024	2166.784	12.0	12.0
4156	1024	4255.744	12.0	12.0
8244	1024	8441.856	12.0	12.0

8.1.4 Filtering and Input Considerations

Measuring current is often noisy and such noise can be difficult to define. The INA234 offers several options for filtering by allowing the conversion times and number of averages to be selected independently in the Configuration register (0h). The conversion times can be set independently for the shunt voltage and bus voltage measurements to allow added flexibility when configuring the monitoring of the power-supply bus.

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500-kHz (±10% max) sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. These signals are at 1 MHz and higher and can be managed by incorporating filtering at the device input. The high frequency enables the use of low-value series resistors on the filter with negligible effects on measurement accuracy. In general, filtering the device input is only necessary if there are transients at exact harmonics of the 500 kHz (±10% max) sampling rate (greater than 1 MHz). Filter using the lowest possible series resistance (typically 100 Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1 µF and 1 µF. Figure 8-1 illustrates the device with a filter added at the input.

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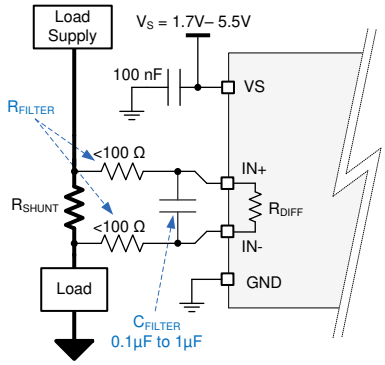


Figure 8-1. Input Filtering

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate 26 V across the inputs. A large differential scenario can be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors can support this voltage). Removing a short to ground can result in inductive kickbacks that can exceed the 26-V differential and 28-V common-mode rating of the device. Inductive kickback voltages are best controlled by Zener-type, transient-absorbing devices (commonly called *transzorbs*) combined with sufficient energy storage capacitance. The *Current Shunt Monitor with Transient Robustness Reference Design* describes a high-side, current-shunt monitor used to measure the voltage developed across a current-sensing resistor and how to better protect the current-sense device from transient overvoltage conditions.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition can result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, and the excessive dV/dt can activate the ESD protection in systems with large currents. Testing demonstrates that the addition of 10-Ω resistors in series with each input of the device sufficiently protects against dV/dt failures up to the 28-V rating of the device. Selecting these resistors in the range noted has minimal effect on accuracy.

8.2 Typical Application

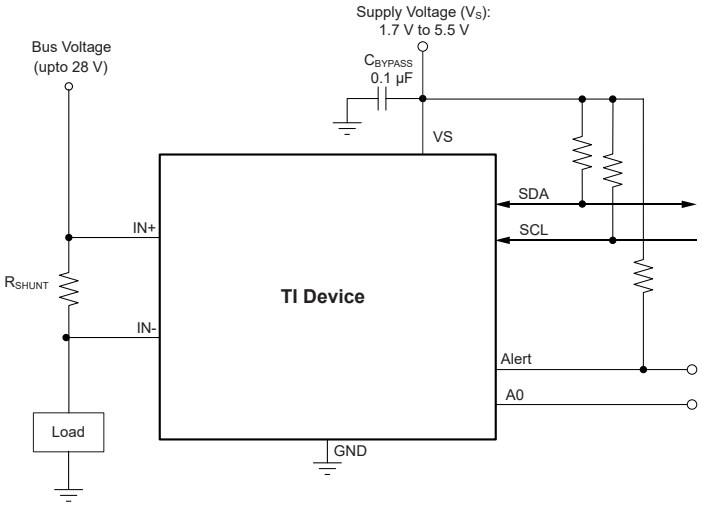


Figure 8-2. Typical High-Side Sensing Circuit Configuration, INA234

8.2.1 Design Requirements

The INA234 measures the voltage developed across a current-sensing resistor (R_{SHUNT}) when current passes through it. The device also measures the bus supply voltage and calculates power when calibrated. It also comes with alert capability, where the alert pin can be programmed to respond to a user-defined event or a conversion ready notification.

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Table 8-3 lists the design requirements for the circuit shown in Figure 8-2.

Table 8-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage (V_S)	3.3 V
Bus supply rail (V_{CM})	12 V
Average Current	6 A
Overcurrent fault threshold	9 A
Maximum current monitored (I_{MAX})	10 A
ADC Range Selection (V_{SENSE_MAX})	±81.92 mV

8.2.2 Application Curves

Figure 8-3 shows the ALERT pin response to a shunt overvoltage limit of 72 mV for a conversion time (t_{CT}) of 140 µs and averaging set to 1. Figure 8-4 shows the response for the same limit but with the conversion time increased to 1.1 ms. For the scope shots shown in these figures, persistence was enabled on the ALERT channel. Figure 8-3 and Figure 8-4 show how the ALERT response time can vary depending on when the fault condition occurs relative to the internal ADC clock of the INA234. For fault conditions that are just exceeding the limit threshold, the response time for the ALERT pin can vary from one to two conversion cycles. As mentioned previously, the variation is because of the timing on when the fault event occurs relative to the start time of the internal ADC conversion cycle. For fault events that greatly exceed the limit threshold, the alert can respond in less than one conversion cycle.

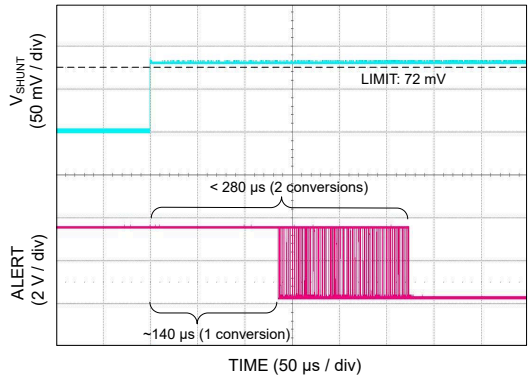


Figure 8-3. Alert Response (t_{CT} = 140 µs)

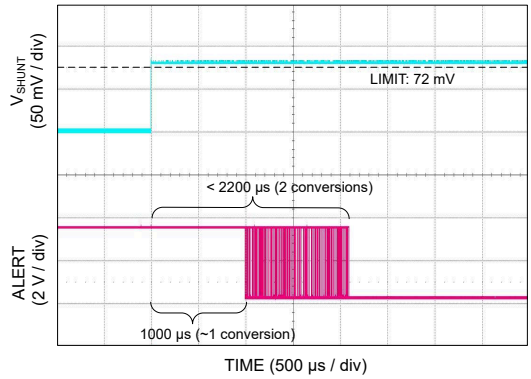


Figure 8-4. Alert Response (t_{CT} = 1.1 ms)

8.2.3 Detailed Design Procedure

This design example walks through the process of selecting the shunt resistor, programming the calibration register, setting the correct fault thresholds, and how to properly scale returned values from the device.

8.2.3.1 Select the Shunt Resistor

Using values from Table 8-3, the maximum value of the shunt resistor is calculated based on the value of the maximum current to be sensed (I_{MAX}) and the maximum allowable sense voltage (V_{SENSE_MAX}) for the chosen ADC range. When operating at the maximum current, the differential input voltage must not exceed the maximum full scale range of the device, V_{SENSE_MAX}. Using Equation 5 for the given design parameters, the maximum value for R_{SHUNT} is calculated to be 8.192 mΩ. The closest standard resistor value that is smaller than the maximum calculated value is 8.0 mΩ. Smaller resistors can be used to minimize power loss at the expense of reduced accuracy. The shunt resistor selected must have sufficient wattage to handle the power dissipation at maximum load at the desired operating temperature.

$$R_{SHUNT} < \frac{V_{SENSE_MAX}}{I_{MAX}} \quad (5)$$

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8.2.3.2 Configure the Device

The first step to program the INA234 is to properly set the device Configuration register (0h). On initial power up, the configuration register is set to the reset values (see Table 7-4). In the default power on state the device is set to measured on the ±81.92 mV range with the ADC continuously converting the shunt and bus (voltage at IN–) voltages. If the default power up conditions do not meet the design requirements, these registers will need to be set properly after each V_S power cycle event.

8.2.3.3 Program the Shunt Calibration Register

The shunt calibration register needs to be correctly programmed at each V_S power up in order for the device to properly report any result based on current. The first step is to calculate the minimum LSB value for the current by using Equation 2. Applying this equation with the maximum expected current of 10 A results in an minimum LSB size of 4.8828125 mA. The INA234 allows selection of the CURRENT_LSB to be up to 8 x larger than the minimum LSB size. For this example a value of 5 mA is used. Applying Equation 1 to the Current_LSB and selected value for the shunt resistor results in a shunt calibration register setting of 2048d (800h). Failure to set the value of the shunt calibration register will result in a zero value for any result based on current. Programming this register is not required for reading shunt voltage, bus voltage, or setting alert limits.

8.2.3.4 Set Desired Fault Thresholds

The INA234 has the ability to assert the Alert pin on several different fault conditions as described in *ALERT Pin*. The desired fault condition to assert the Alert pin needs to be selected by appropriately programming the Mask/Enable Register (6h). Fault thresholds are set by programming the desired trip threshold into the Alert Limit Register (7h).

For example, an over current fault condition would be selected by setting the SOL bit in the Mask/Enable Register to 1. The desired threshold for the over current condition would have to be programmed in the Alert Limit Register. In this example, the over current threshold is 9.0 A and the value of the current sense resistor is 8.0 mΩ, which give a shunt voltage limit of 72 mV. Once the shunt voltage limit is known, the value for the shunt over voltage limit register is calculated by dividing the shunt voltage limit by the shunt voltage LSB size.

For this case, the calculated value of the alert limit register is 72 mV / 40 µV = 1800d (708h). Since the bottom 4 bits of the shunt register are reserved the value programmed into the fault register must be left shifted by 4 or multiplied by 16. This results in a final alert limit register value of 28800 (7080h)

Values stored in the alert limit register are set to the default values after V_S power cycle events and need to be reprogrammed each time power is applied.

8.2.3.5 Calculate Returned Values

Table 8-4 below shows the register values assuming the design requirements shown in Table 8-3. User programmed values for the Configuration, Calibration, Mask/Enable and Alert limit registers are shown, as well as, the returned values for shunt voltage, current, bus voltage and power. Parametric values are calculated by multiplying the returned value by the LSB value.

Returned values for shunt voltage, current, and bus voltage need to be right shifted by 4, or divided by 16 to the correct 12-bit value before multiplying by the LSB value. The shifting is needed because the bottom 4 bits in the returned values are reserved and are always 0.

Table 8-4. Register Values

Register Name	Contents	Right Shifted 12 - bit Value	LSB Value	Calculated Value
Configuration (0h)	16679d (4127h)	—	—	—
Calibration (5h)	2048d (800h)	—	—	—
Mask/Enable (6h)	32768 (8000h)	—	—	—
Alert Limit (7h)	28800d (7080h)	1800d (708h)	40 µV/LSB	1800 × 40 µV = 0.072 V
Shunt Voltage (1h)	19200d (4B00h)	1200d (4B0h)	40 µV/LSB	1200 × 40 µV = 0.048 V
Bus Voltage (2h)	7500d (1D4Ch)	468d (1D4h)	25.6 mV/LSB	468 × 25.6 mV = 11.98 V
Current (4h)	19200d (4B00h)	1200d (4B0h)	5 mA/LSB	1200 × 5 mA = 6 A

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Table 8-4. Register Values (continued)

Register Name	Contents	Right Shifted 12 - bit Value	LSB Value	Calculated Value
Power (3h)	450d (1C2h)	—	Current LSB x 32 = 160 mW/LSB	450 × 160 mW = 72 W

Shunt Voltage and Current return values in two's complement format. In two's complement format a negative value in binary is represented by having a 1 in the most significant bit of the returned value. These values can be converted to decimal by first inverting all the bits and adding 1 to obtain the unsigned binary value. This value should then be converted to decimal with the negative sign applied.

9 Power Supply Recommendations

Figure 8-2 shows that the device input circuitry can accurately measure signals on common-mode voltages beyond the power-supply voltage, V_S. For example, the voltage applied to the vs. power supply pin can be 5 V, whereas the bus power-supply voltage being monitored (the common-mode voltage) can be as high as 28 V. The device can also withstand the full -0.3 V to 28 V range at the input pins, regardless of whether the device has power applied or not.

Place the required power-supply bypass capacitors as close as possible to the supply and ground pins of the device to ensure stability. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Connect the input pins (IN+ and IN–) to the sensing resistor using a Kelvin connection or a 4-wire connection. These connection techniques ensure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current-sensing resistor, any additional high-current carrying impedance causes significant measurement errors. Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

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10.2 Layout Example

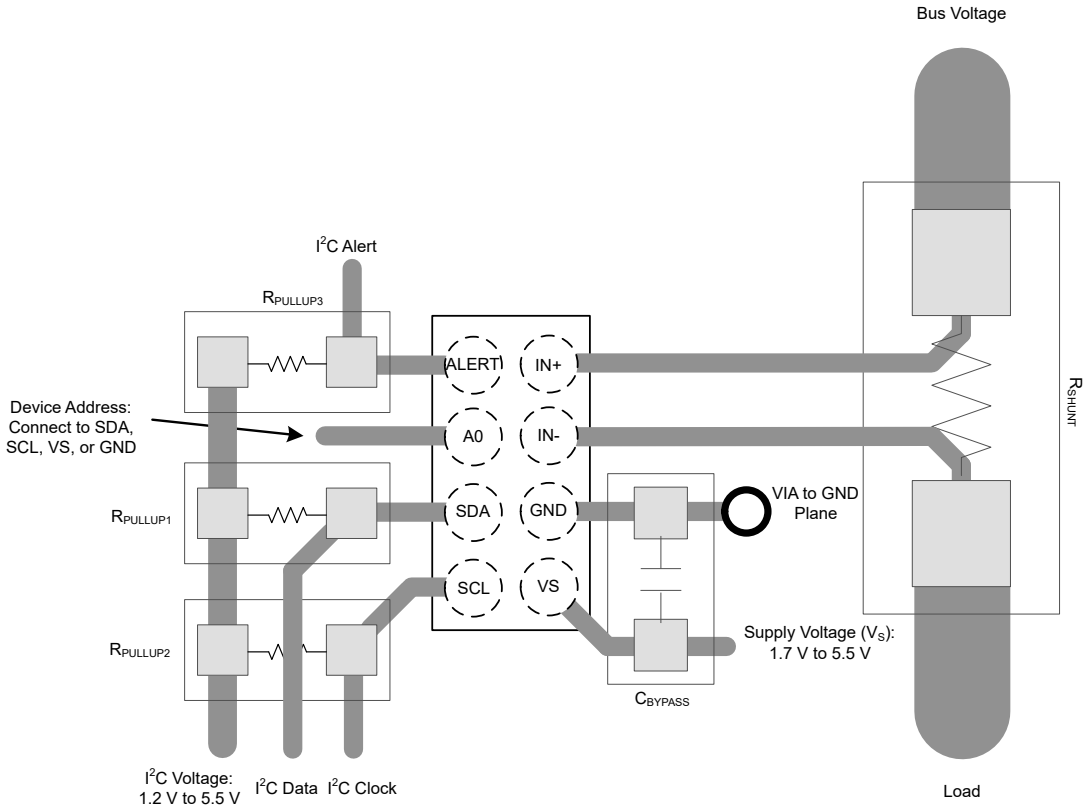


Figure 10-1. INA234 Layout Example (High Side)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support see the following:

INA234EVM and INA236EVM User's Guide (SBOU264)

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Current Shunt Monitor with Transient Robustness Reference Design* (TIDU473)
- Texas Instruments, *INA234EVM and INA236EVM User's Guide* (SBOU264)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA234AIYBJR	ACTIVE	DSBGA	YBJ	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1KX	Samples
PINA234AIYBJR	ACTIVE	DSBGA	YBJ	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

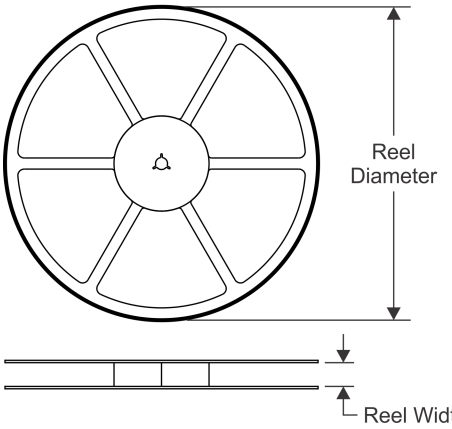
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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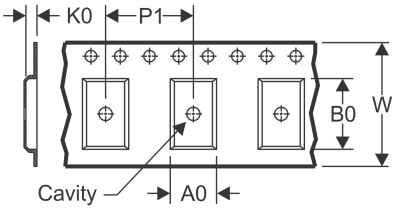
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

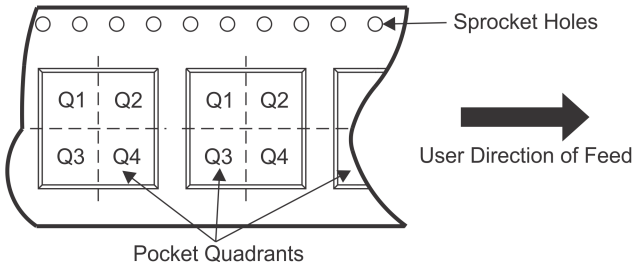


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

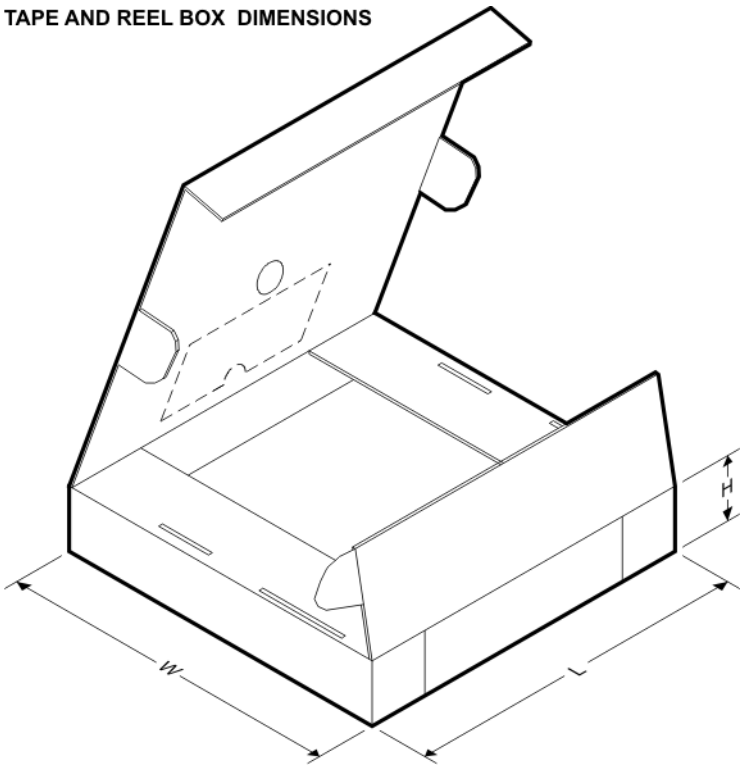
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA234AIYBJR	DSBGA	YBJ	8	3000	180.0	8.4	0.84	1.62	0.43	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

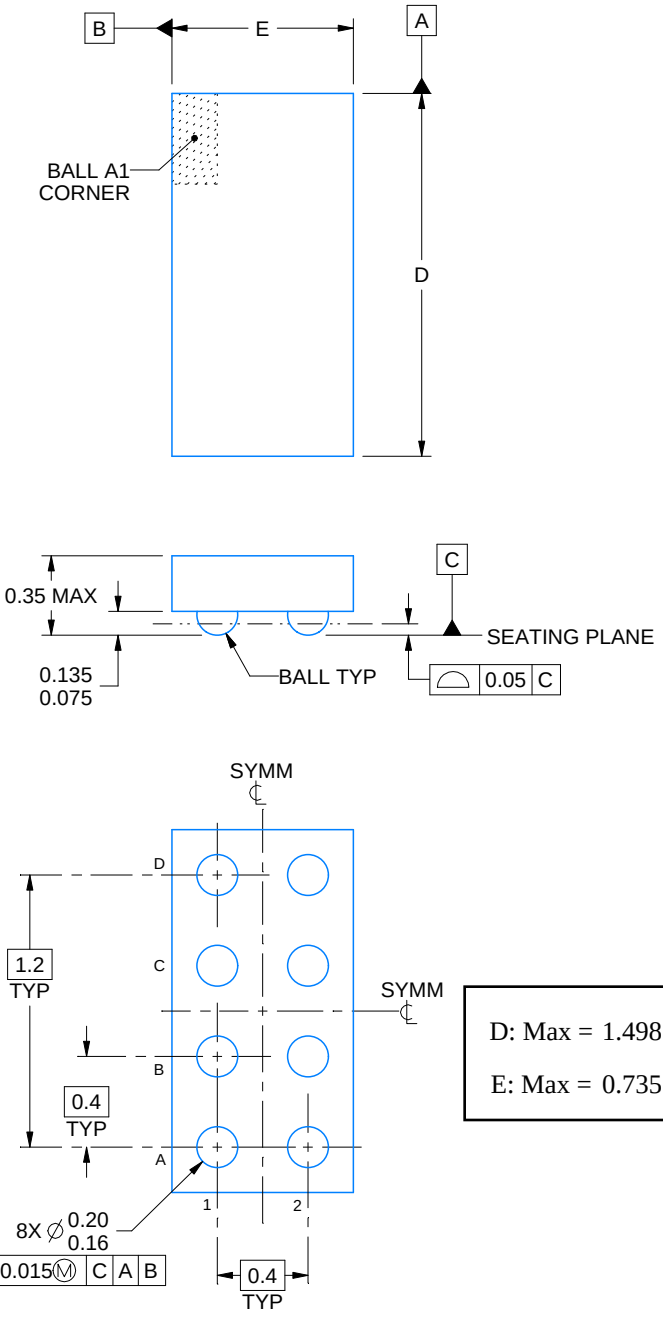
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA234AIYBJR	DSBGA	YBJ	8	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YBJ0008

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.498 mm, Min =1.438 mm

E: Max = 0.735 mm, Min =0.675 mm

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NOTES:

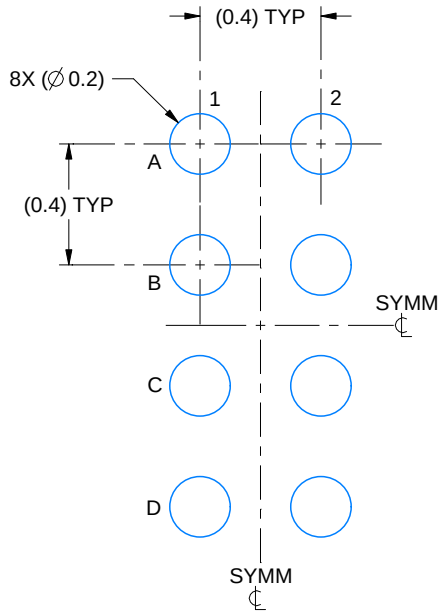
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

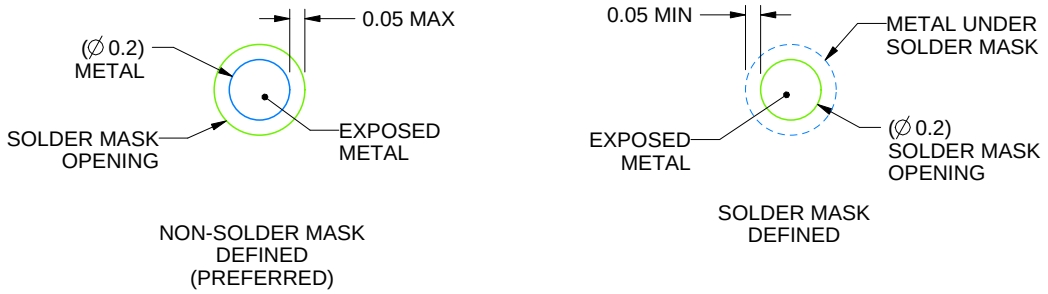
YBJ0008

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

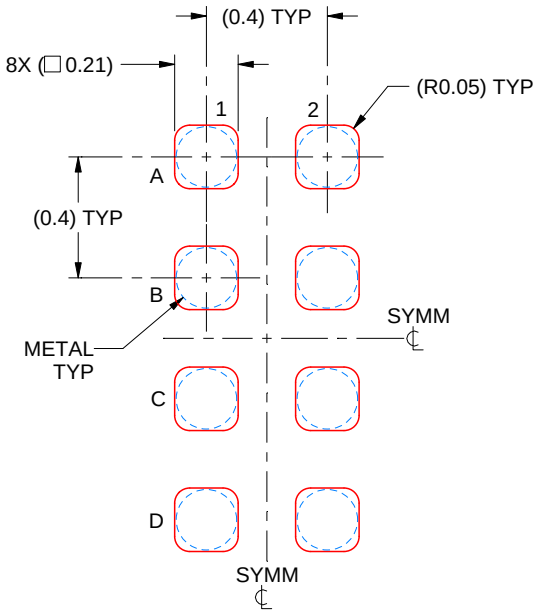
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBJ0008

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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