

74ABT125

Quad buffer; 3-state

Rev. 04 — 27 April 2010

Product data sheet

1. General description

The 74ABT125 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT125 device is a quad buffer that is ideal for driving bus lines. The device features four Output Enables ($\overline{1OE}$, $\overline{2OE}$, $\overline{3OE}$, $\overline{4OE}$), each controlling one of the 3-state outputs.

2. Features and benefits

- Quad bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: HIGH -32 mA ; LOW $+64\text{ mA}$
- Power-up 3-state
- Inputs are disabled during 3-state mode
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

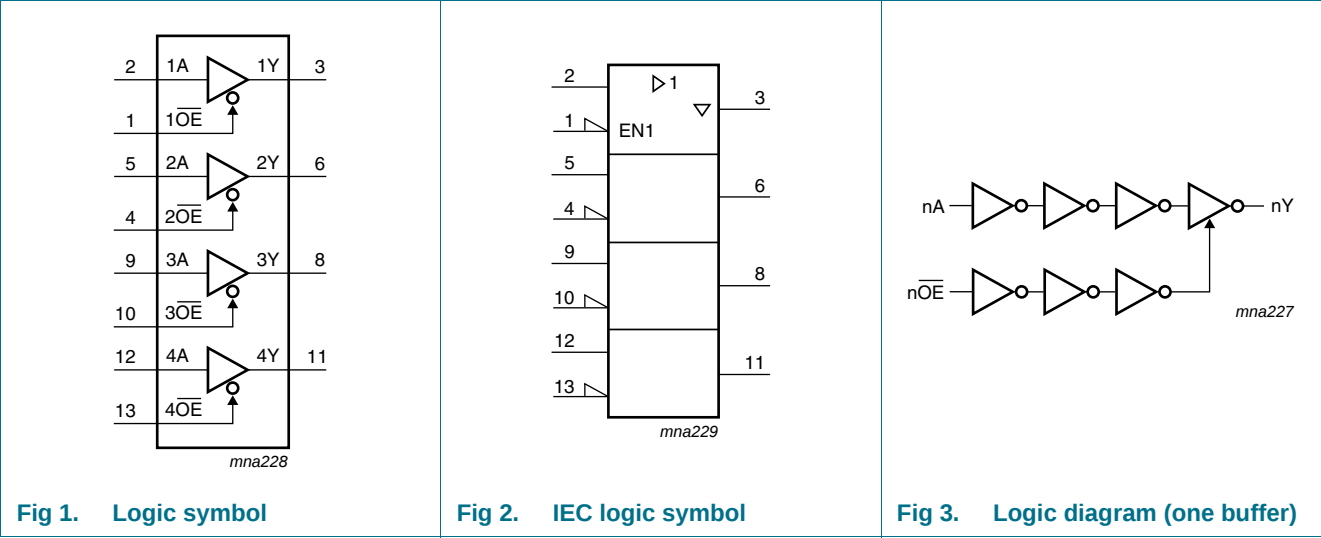
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT125N	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74ABT125D	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT125DB	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74ABT125PW	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ABT125BQ	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

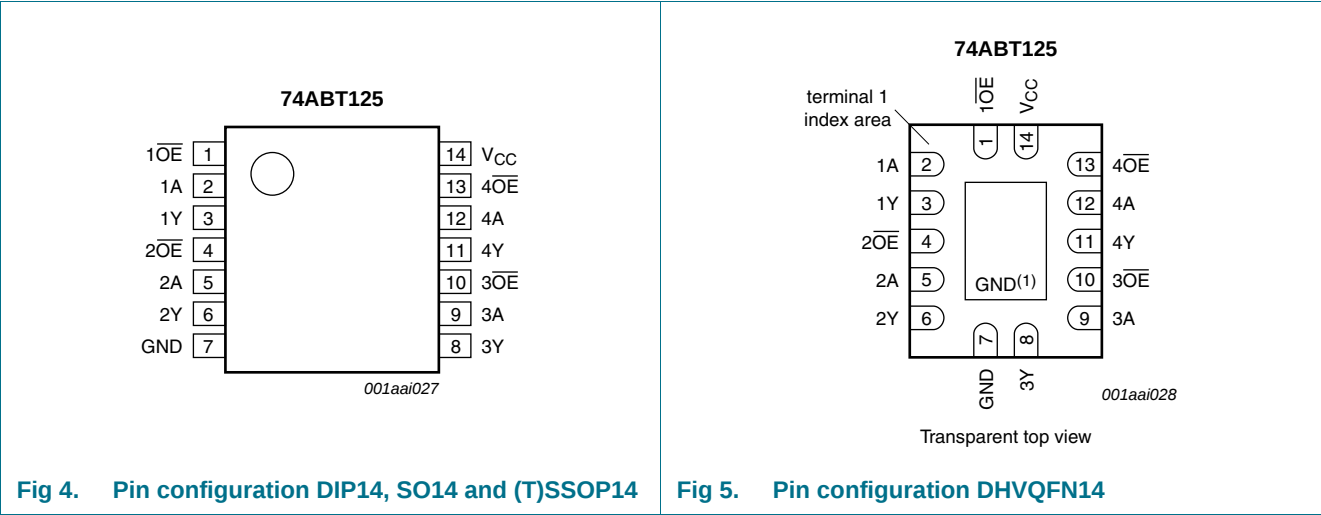


4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description		
Symbol	Pin	Description
$\overline{1OE}$ to $\overline{4OE}$	1, 4, 10, 13	output enable input (active LOW)
1A to 4A	2, 5, 9, 12	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection^[1]

Inputs		Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values^[1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-1.2	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	-0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
T _j	junction temperature		^[2] -	150	°C
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	^[3] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] SO14 packages: above 70 °C P_{tot} derate linearly with 8 mW/K
 SSOP14 and TSSOP20 packages: above 60 °C P_{tot} derate linearly with 5.5 mW/K
 DHVQFN14 packages: above 60 °C P_{tot} derate linearly with 4.5 mW/K

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		4.5	5.5	V
V _I	input voltage		0	V _{CC}	V
V _{IH}	HIGH-level input voltage		2.0	-	V
V _{IL}	LOW-level input voltage		-	0.8	V
I _{OH}	HIGH-level output current		-32	-	mA
I _{OL}	LOW-level output current		-	64	mA
Δt/ΔV	input transition rise and fall rate		-	10	ns/V
T _{amb}	ambient temperature	in free air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}$; $I_{IK} = -18\text{ mA}$	-	-0.9	-1.2	-	-1.2	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IL}$ or V_{IH}						
		$V_{CC} = 4.5\text{ V}$; $I_{OH} = -3\text{ mA}$	2.5	2.9	-	2.5	-	V
		$V_{CC} = 5.0\text{ V}$; $I_{OH} = -3\text{ mA}$	3.0	3.4	-	3.0	-	V
		$V_{CC} = 4.5\text{ V}$; $I_{OH} = -32\text{ mA}$	2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 4.5\text{ V}$; $I_{OL} = 64\text{ mA}$; $V_I = V_{IL}$ or V_{IH}	-	0.35	0.55	-	0.55	V
I_I	input leakage current	$V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or 5.5 V	-	± 0.01	± 1.0	-	± 1.0	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0.0\text{ V}$; V_I or $V_O \leq 4.5\text{ V}$	-	± 5.0	± 100	-	± 100	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.1\text{ V}$; $V_O = 0.5\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $\text{OE} = \text{don't care}$ [1]	-	± 5.0	± 50	-	± 50	μA
I_{OZ}	OFF-state output current	$V_{CC} = 5.5\text{ V}$; $V_I = V_{IL}$ or V_{IH}						
		$V_O = 2.7\text{ V}$	-	1.0	50	-	50	μA
		$V_O = 0.5\text{ V}$	-	-1.0	-50	-	-50	μA
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5\text{ V}$; $V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or V_{CC}	-	5.0	50	-	50	μA
I_O	output current	$V_{CC} = 5.5\text{ V}$; $V_O = 2.5\text{ V}$ [2]	-50	-100	-180	-50	-180	mA
I_{CC}	supply current	$V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or V_{CC}						
		outputs HIGH-state	-	65	250	-	250	μA
		outputs LOW-state	-	12	15	-	30	mA
		outputs disabled	-	65	250	-	50	μA
ΔI_{CC}	additional supply current	per control pin; $V_{CC} = 5.5\text{ V}$; one control input at 3.4 V, other inputs at V_{CC} or GND [3]						
		outputs enabled	-	0.5	1.5	-	1.5	mA
		outputs disabled	-	50	250	-	250	mA
		one enable input at 3.4 V and other inputs at V_{CC} or GND; outputs disabled	-	0.5	1.5	-	1.5	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	4	-	-	-	pF
C_O	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or V_{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$, a transition time of up to 100 μs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

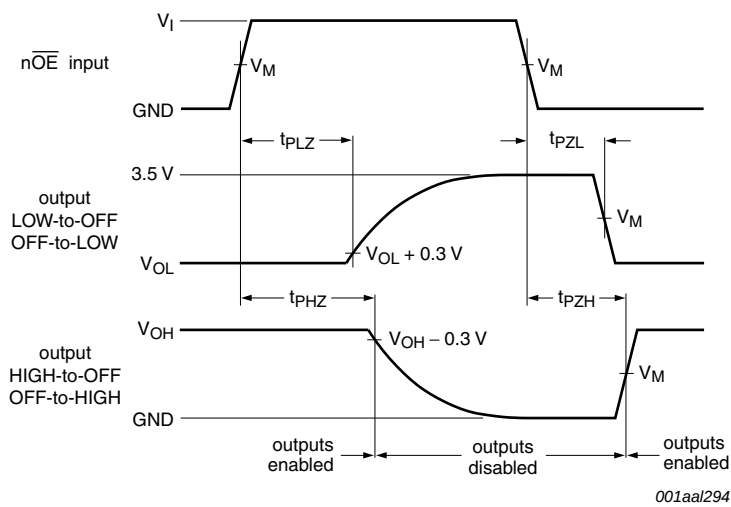
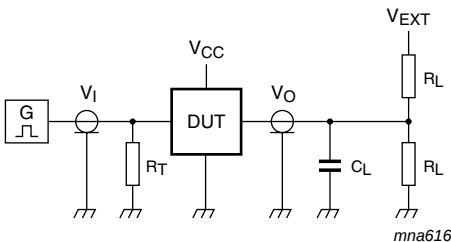
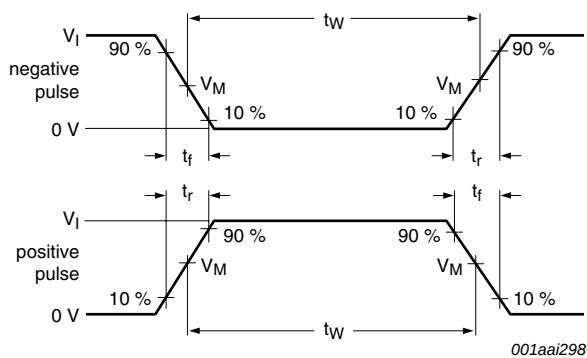


Fig 7. Enable and disable times



- a. Input pulse definition
- Test data is given in [Table 8](#).
- Test circuit definitions:
- R_L = Load resistance.
- C_L = Load capacitance including jig and probe capacitance.
- R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
- V_{EXT} = Test voltage for switching times.
- b. Test circuit

Fig 8. Load circuitry for switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_w	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

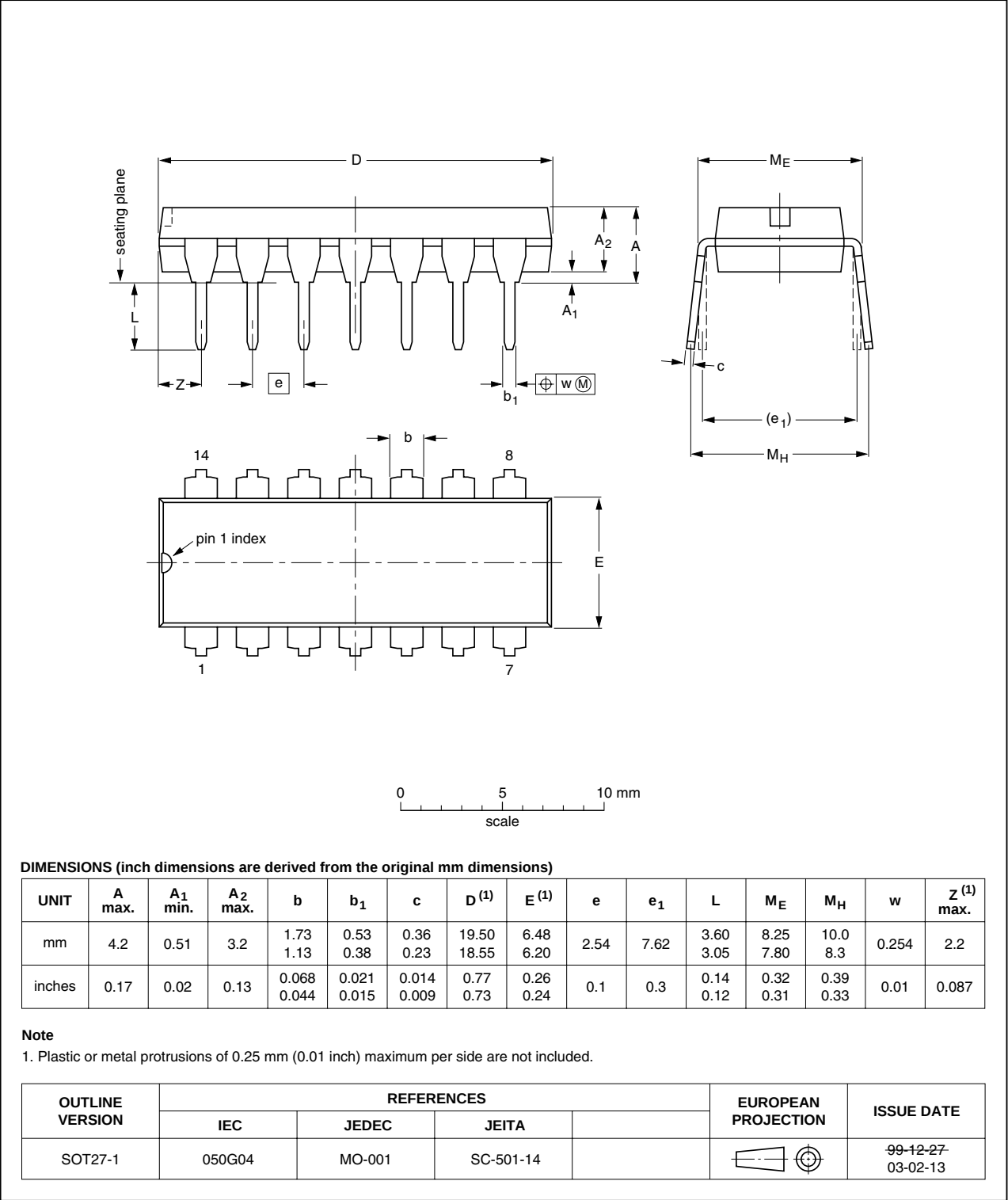


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm
SOT108-1

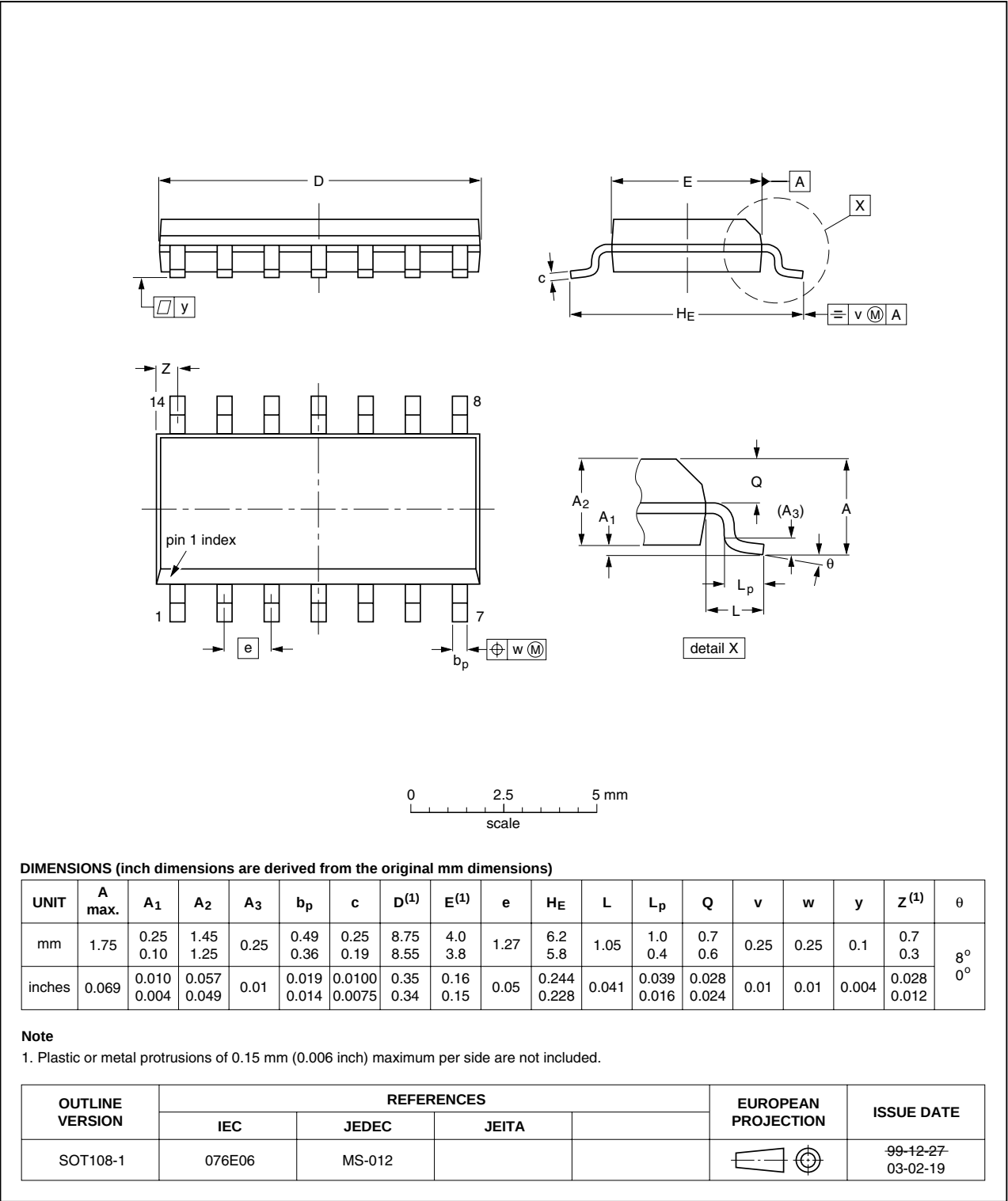


Fig 10. Package outline SOT108-1 (SO14)

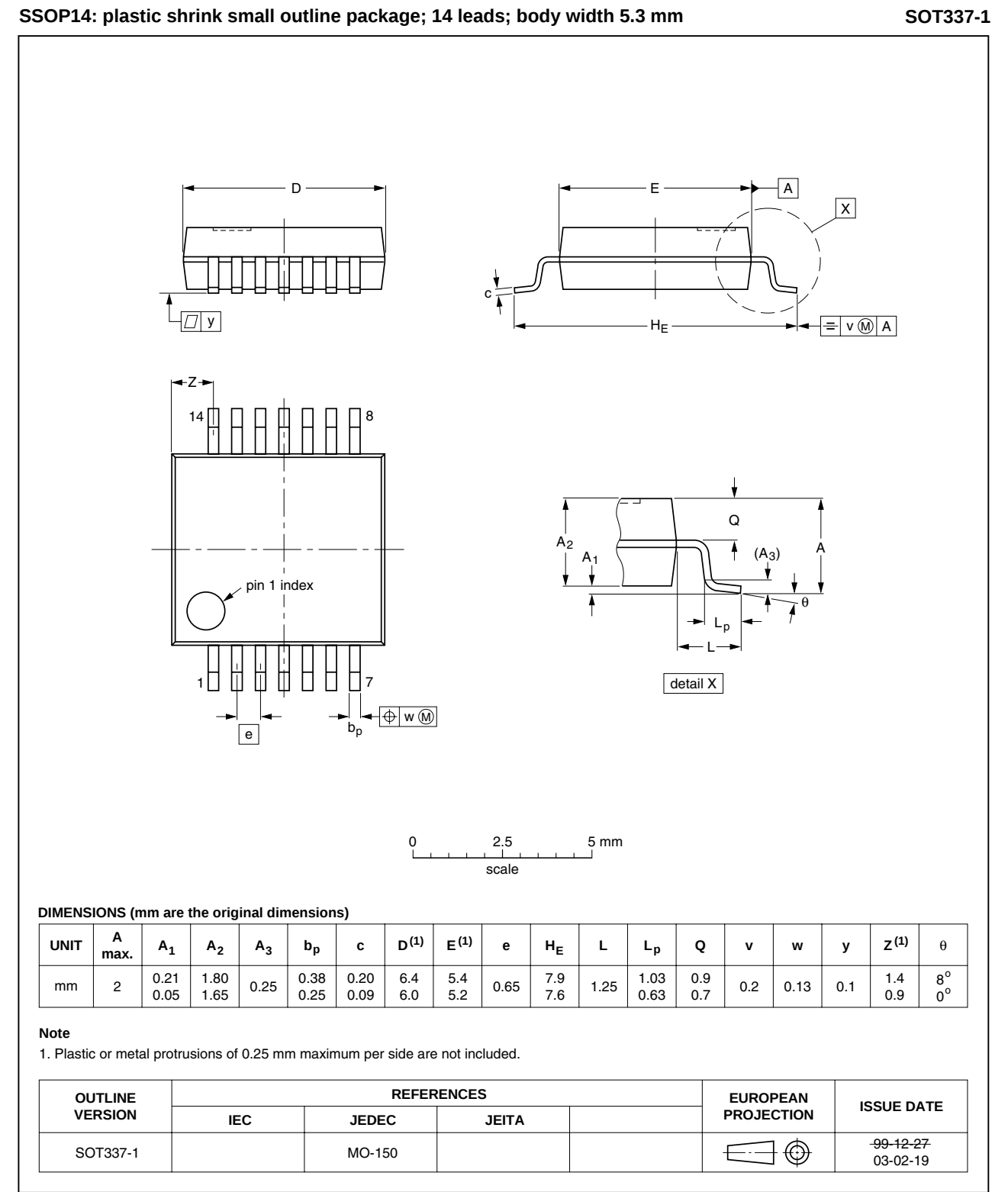


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

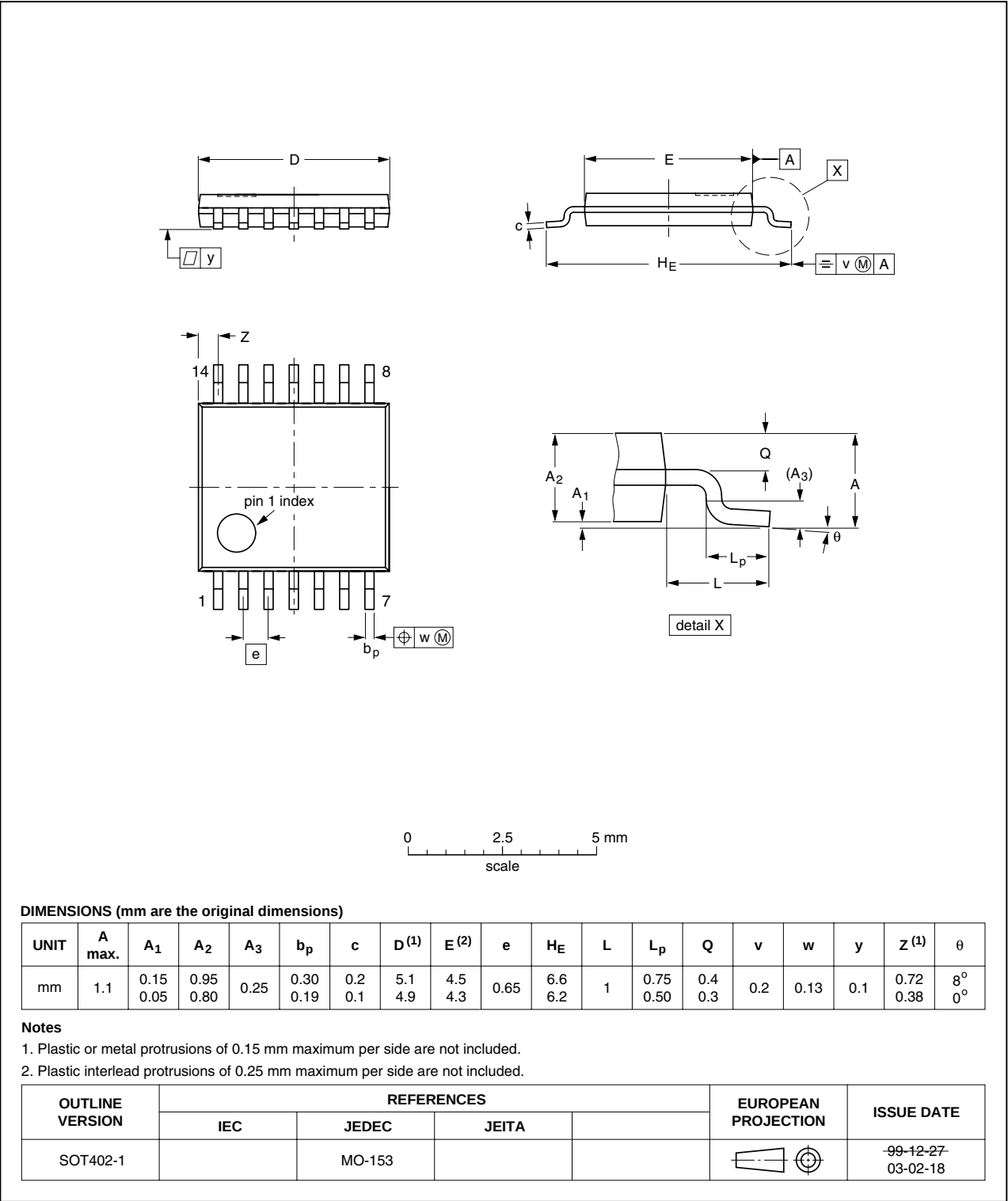


Fig 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

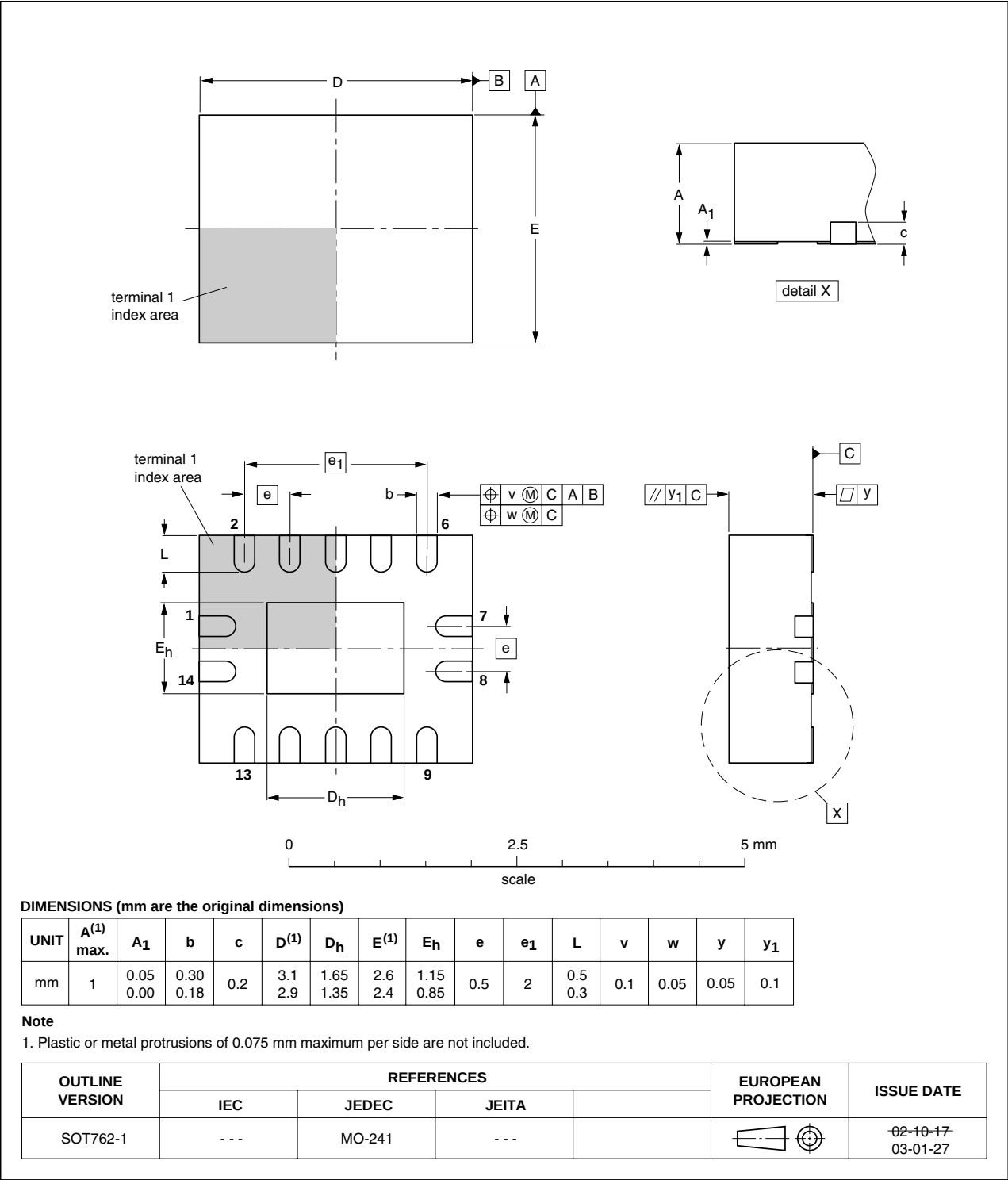


Fig 13. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BICMOS	BipolarCMOS
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT125_4	20100427	Product data sheet	-	74ABT125_3
Modifications:	• Table note 1 from Table 6 Transition time corrected.			
74ABT125_3	20080429	Product data sheet	-	74ABT125_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Pins renamed throughout the data sheet. • Package DHVQFN14 added to Section 3 “Ordering information” and Section 12 “Package outline”. • Figure 3 “Logic diagram (one buffer)” added to Section 4 “Functional diagram”. • Table 8 “Measurement points” and Table 9 “Test data” added. • Figure 8 “Test setup for switching times” updated. • Section 13 “Abbreviations” added.			
74ABT125_2	19980116	Product specification	-	74ABT125_1
74ABT125_1	19960305	-	-	-

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15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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