

Intel® 81341 and Intel® 81342 I/O Processors

Datasheet

Product Features

- Intel® 81341 I/O Processor contains one integrated Intel XScale® processor
- Intel® 81342 I/O Processor contains two integrated Intel XScale® processors
- Processor features
  - 800 MHz and 1.2 GHz
  - ARM* V5TE Compliant
  - Instruction/Data Cache: 32 KByte, 4-way Set Associative, NRU Replacement Algorithm, Lockable
  - Unified Level 2 Cache: 512 KByte Set Associative, NRU Replacement Algorithm
  - 128-Entry Branch Target Buffer
  - 8-Entry Write Buffer
  - 8-Entry Fill and Pend Buffer
- Internal Bus 400 MHz/128-bit
- Can support either PCI-X or PCI Express* as an endpoint
- Support for PCI Express* Lane Widths of x1, x2, x4, x8
- Multi-ported Memory Controller
  - Intel XScale® processor inputs and north internal bus, south internal bus and ADMA input ports
  - PC3200 and PC4300 Double Data Rate (DDR2 400, DDR2 533)
  - Up to 4 GB of 64-bit DDR2 400, DDR2 533
  - Optional Single-bit Error Correction, Multi-bit Detection ECC Support
  - Supports Registered and Unbuffered DDR2 Memory
  - 36-bit Addressable
  - 32-bit Memory Support
- Integrated SRAM Memory Controller (1 MB)
- Address Translation Unit
  - 2 KB or 4 KB Outbound Read Queue
  - 4 KB Outbound Write Queue
  - 4 KB Inbound Read and Write Queue
- Two Programmable 32-bit Timers and Watchdog Timer
- Sixteen General Purpose I/O Pins
- Three I^2C Bus Interface Units
- Two UART (16550) Units
  - 64 Byte Receive and Transmit FIFOs
  - 4 pin Master/Slave Capable
- Peripheral Bus Interface
  - 8-, 16-bit Data Bus with Two Chip Selects
  - 25 Demultiplexed Address Lines
- Interrupt Controller Unit
  - Four Priority Levels
  - Interrupt Pending Register
  - Vector Generation
  - 16 External Interrupt Pins with High Priority Interrupt (HPI#)
- 1357-ball, Flip Chip Ball Grid Array (FCBGA), 37.5 mm x 37.5 mm and 1.0 mm ball pitch
- Application DMA Controller
  - Three Independent Channels Connected to the MCU and the South Internal Bus
  - 4 KByte Data Transfer Queue
  - CRC 32C Calculation
  - Performs Optional XOR on Read Data

Order Number: 315039-003US
December 2007



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Revision History

Date	Revision	Description
December 2007	003	Revised for 4 GB memory support.
March 2007	002	Updated Legal page 2. Edited text in Section 2.1.2. Revise PCIXCAP description in Table 5. Updated Table 18 for Cgp, Cpcix, Cddr2 and Lpin values. Revised Table 17 for Tcase (Tc) maximum value to 100C. Revised Figure 27.
October 2006	001	Initial release



1.0 Introduction

1.1 About This Document

This document is a reference guide for the external architecture of the Intel® 81341 and 81342 I/O Processors (also known as the 81341 and 81342).

1.1.1 Terminology

To aid the discussion of the Intel® 81341 and 81342 I/O Processors architecture, the following terminology is used:

Downstream	At or toward a PCI bus with a higher number (after configuration)
Word	16 bits of data
Dword	32 bits of data
Qword	64 bits of data
Host processor	Processor located upstream from the Intel® 81341 and 81342 I/O Processors
Local processor	Intel XScale® processor within the Intel® 81341 and 81342 I/O Processors
Local bus	Intel® 81341 and 81342 I/O Processors internal bus
Local memory	Memory subsystem on the Intel XScale® processor, DDR2 SDRAM or Peripheral Bus Interface busses
Upstream	At or toward a PCI bus with a lower number (after configuration)

1.1.2 Other Relevant Documents

1. Intel XScale® *Microarchitecture Developer's Manual* (Order Number 273473)—Intel Corporation
2. *PCI Local Bus Specification*, Revision 2.3—PCI Special Interest Group
3. *PCI Hot-Plug Specification,* Revision 1.0—PCI Special Interest Group
4. *PCI Bus Power Management Interface Specification*, Revision 1.1—PCI Special Interest Group
5. *PCI Express Specification*, Revision 1.0a—PCI Special Interest Group



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2.0 Features

81341 and 81342 I/O Processors are a single- or dual-function PCI device that integrates one or two Intel XScale® processor(s) with intelligent peripherals including a PCI bus bridge. The 81341 and 81342 I/O Processors also support two internal busses: North XSI bus and South XSI bus. With the two internal busses, transactions can take place simultaneously on each bus. The north XSI bus provides one or two Intel XScale® processor(s) with low-latency access to either the DDR2 SDRAM Memory Controller or the on-chip SRAM Memory Controller. Peripherals that generate large burst transactions are located on the south XSI bus, thus allowing the two Intel XScale® processors exclusive access to the north XSI bus.

81341 and 81342 I/O Processors consolidate the following features into a single system:

- PCI–Local Memory Bus Address Translation Unit, function 0 programming interface
- Messaging Unit, function 0 programming interface
- Application Direct Memory Access (DMA) Controller (including offload for up to a 16-source XOR operation)
- Peripheral Bus Interface Unit
- Integrated DDR2 Memory Controller
- Integrated SRAM Memory Controller
- Two programmable timers per Intel XScale® processor
- Watchdog timer per Intel XScale® processor
- Three I^2C Bus Interface Units
- Two Serial Port Units
- Sixteen General-Purpose Input/Output (GPIO) ports
- Internal North Bus–South Bus Bridge

It is an integrated processor that addresses the needs of intelligent I/O storage applications and helps reduce intelligent I/O system costs.

2.1 Intel® 81341 and 81342 I/O Processors Features

Figure 1 shows the Intel® 81341 I/O Processor single-processor block diagram.

Figure 2 shows the Intel® 81342 I/O Processor two-processor block diagram.

Figure 1. Intel® 81341 I/O Processor Functional Block Diagram (Single processor)

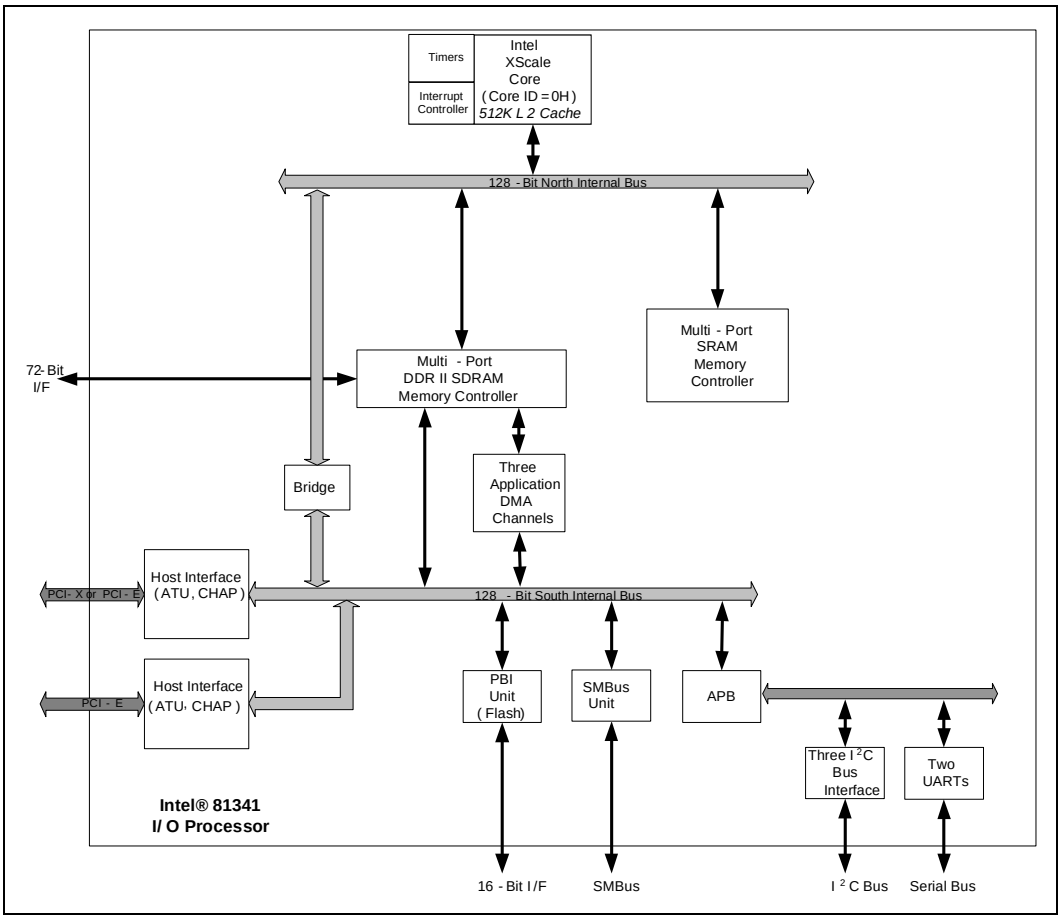
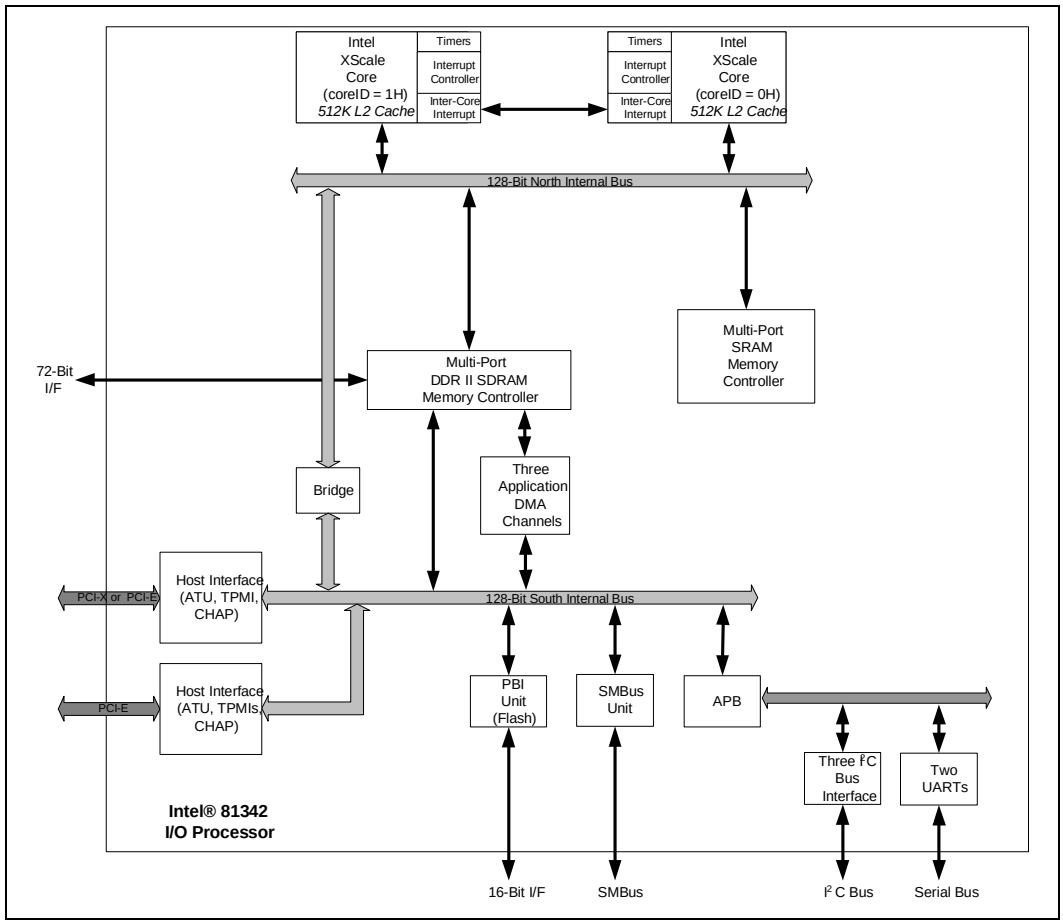


Figure 2. Intel® 81342 I/O Processor Functional Block Diagram (Two processor)



Note: The subsections that follow give a brief overview of each feature. Refer to the appropriate chapter in the *Intel® 81341 and 81342 I/O Processors Developer's Manual* for full technical descriptions.

2.1.1 Host Interface

81341 and 81342 I/O Processors can be set up as either a single or dual-function PCI device, providing PCI-X or PCI Express* interface or both PCI-X and PCI Express* interfaces. The PCI interface is selected as a reset option. Each function is independently controlled and provides the TPMI interface.

Intel® 81341 and 81342 I/O Processors are a single-function PCI device that provides either a PCI-X or PCI Express* host interface. The Address Translation Unit (ATU) and the Messaging Unit (MU) provide the programming interface between the host processor and the Intel® 81341 and 81342 I/O Processors. When PCI-X 1.0b is selected as the upstream (host) I/O interface, PCI Express* is available as a private (not visible to the host), downstream I/O interface. Likewise, when PCI Express* is selected as the upstream I/O interface, PCI-X 1.0b is available as a private, downstream I/O interface. The selection of the upstream I/O interface is a reset strap option.

2.1.2 Internal Busses

The 81341 and 81342 I/O Processors are built around two internal busses: north internal bus and south internal bus. The two busses use the same bus protocol. The north internal bus is 128 bits wide and operates at 400 MHz. The north bus connects the two Intel XScale® processors, which have direct access to the DDR2 SDRAM and SRAM. The north XSI bus is designed to provide the two Intel XScale® processors with low-latency access.

The south internal bus is 128 bits wide and operates at 400 MHz. The south XSI bus provides the data paths for burst transactions generated by the DMAs. The south XSI bus internal address and data busses are parity-protected on a byte-wise basis. Agents on the south XSI bus can generate and check address and data parity. The point-to-point interfaces between the agents and the DDR2 and SRAM Memory Controllers are also parity-protected on a byte-wise basis.

2.1.3 Application DMA Controllers

There are three Application DMA Controllers. The Application DMA Controller is dual-ported—with one of its ports connected to the south XSI bus and the other port to the DDR2 SDRAM Memory Controller. This Application DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and the DDR2 memory. The DMA controller also allows data transfer between DDR2 Memory. The DMA Controller supports chaining and unaligned data transfers. It is programmable through the Intel XScale® processor and the host processor.

In addition to simple data transfers, the ADMA performs XOR operations with up to 16 sources.

2.1.4 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to the 81341 and 81342 I/O Processors local memory. The ATU provides interface for the RAID Controller PCI function. The ATU supports transactions between PCI address space and the 81341 and 81342 I/O Processors address space. Address translation is controlled through programmable registers accessible from both the PCI interface and the Intel XScale® processor. Dual access to registers allows flexibility in mapping the two address spaces. The ATU also supports the following extended capability configuration headers:

1. Power Management header, as defined by *PCI Bus Power Management Interface Specification*, Revision 1.1.
2. Message Signaled Interrupt capability structure, as specified in *PCI Local Bus Specification*, Revision 2.3.
3. PCI-X Capabilities List Item, as specified in the *PCI-X Addendum to the Local Bus Specification,* Revision 1.0b.

2.1.5 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 81341 and 81342 I/O Processors. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues, and Index Registers. Each allows a host processor or external PCI device and the 81341 and 81342 I/O Processors to communicate through message passing and interrupt generation. The MU, in conjunction with the ATU, exists as the PCI interface for PCI function 0 when function 0 is set up as a RAID controller.



2.1.6 DDR2 Memory Controller

The DDR2 Memory Controller allows direct control of the 400/533 MHz DDR2 SDRAM memory subsystem. It features programmable chip selects and support for error-correction codes (ECC). The DDR2 Memory Controller is multi-ported with the following interfaces: south internal bus, ADMA controllers, north internal bus. The memory controller interface configuration support includes unbuffered DIMMs, registered DIMMs, and discrete DDR2 SDRAM devices.

2.1.7 SRAM Memory Controller

The SRAM Memory Controller allows direct control of a 1.0 MByte SRAM memory subsystem. It supports error correction codes (ECC). The SRAM is used to store firmware code, I/O exchange contexts and for general-purpose data storage.

2.1.8 Peripheral Bus Interface

The Peripheral Bus Interface Unit is a data communication path to the flash memory components or other peripherals of a 81341 and 81342 I/O Processors hardware system. The PBI includes support for either 8- or 16-bit devices. To perform these tasks at high bandwidth, the bus features a burst-transfer capability which allows successive 8/16-bit data transfers.

2.1.9 I^2C Bus Interface Units

There are three I^2C (Inter-Integrated Circuit) Bus Interface Units that allow the Intel XScale® processor to serve as a master and slave device residing on the I^2C bus. The I^2C0 allows the I/O processor to interface to a Storage Enclosure Processor (SEP). The bus allows the 81341 and 81342 I/O Processors to interface to other I^2C peripherals and microcontrollers for system management functions. For more information, refer to *I^2C Peripherals for Microcontrollers* (Philips Semiconductor)[1].

2.1.10 UART Units

The 81341 and 81342 I/O Processors includes two UART units. The UART units allow the two Intel XScale® processors to serve as a master and slave device residing on the UART bus. The UART units use a serial bus consisting of a two-pin interface. UART0 allows the 81341 and 81342 I/O Processors to interface to a console port for debugging. Also refer to the National Semiconductor* 16550 device specification[2].

2.1.11 Interrupt Controller Unit

Each Intel XScale® processor supports an Interrupt Controller Unit (ICU). The ICU aggregates interrupt sources both external and internal sources of the 81341 and 81342 I/O Processors to the Intel XScale® processor. The ICU supports high-performance interrupt processing with direct interrupt service routine vector generation on a per-source basis. Each source has programmability for masking, processor interrupt input, and priority.

2.1.12 XSI System Controller

Each XSI bus (north and south) employs an XSI system controller. The XSI system controller observes all the address or data bus requests from requestors and completors connected to the XSI bus. The XSI system controller handles XSI address

1. http://www.semiconductors.philips.com/buses/i2c/
2. http://www.national.com/pf/PC/PC16550D.html

bus arbitration, XSI data bus arbitration, framing Address bus cycles, and framing Data bus cycles. The XSI system controller provides the shared address and shared data paths from/to units.

2.1.13 Inter-Processor Communication

Each Intel XScale® processor can interrupt or issue a reset to the second Intel XScale® processor. Each processor can generate up to 32 interrupts to the second processor.

2.1.14 Timers

The 81341 and 81342 I/O Processors support two programmable 32-bit timers per processor. The 81341 and 81342 I/O Processors also support one watchdog timer per processor.

2.1.15 GPIO

The 81341 and 81342 I/O Processors includes sixteen General-Purpose I/O (GPIO) pins.



3.0 Package Information

3.1 Package Introduction

The Intel® 81341 and Intel® 81342 I/O Processors is offered in a 1357-ball FCBGA5 package.

3.2 Functional Signal Definitions

This section defines the pins and signals.

3.2.1 Signal Pin Descriptions

Table 1. Pin Description Nomenclature

Symbol	Description
I	Input pin only
O	Output pin only
I/O	Pin can be either an input or an output
OD	Open-drain pin
PWR	Power pin
GND	Ground pin
—	Pin must be connected as described
Sync (...)	Synchronous. Signal meets timings relative to a clock. • Sync (P): Synchronous to **P_CLKIN** • Sync (M): Synchronous to **M_CK[2:0]** / **M_CK#[2:0]** • Sync (T): Synchronous to **TCK**
Async	Asynchronous. Inputs can be asynchronous relative to all clocks. All asynchronous signals are level-sensitive.
R/W	Indicates read or write capability.
Rst (P)	The pin is reset with **WARM_RST#** or **P_RST#**.
Rst (M)	The pin is reset with **M_RST#**. **M_RST#** is asserted when the memory subsystem is reset.
Rst (PB)	The pin is reset with **PB_RSTOUT#**. **PB_RSTOUT#** is asserted when the Peripheral Bus Interface subsystem is reset.
Rst (T)	The pin is reset with **TRST#**.
ActLow	The pin is an active-low signal.
Diff	The pin is a differential signal pair. • "P" at the end of a differential pin name indicates "positive". • "N" at the end of a differential pin name indicates "negative".

Table 2. DDR2 SDRAM Signals (Sheet 1 of 2)

Name	Count	Type	Description
M_CK[2:0], M_CK#[2:0]	6	O Diff	Memory Clockout: is used to provide the three differential clock pairs to the unbuffered DIMM for the external SDRAM memory subsystem. Registered DIMMs use only the **M_CK[0]/M_CK#[0]** pair, which drives the input to the on-DIMM PLL.
M_RST#	1	O Async ActLow	Memory Reset: indicates that the memory subsystem has been reset. It is used to re-initialize registered DIMMs.
MA[14:0][a]	14	O Sync (M) Rst (M)	Memory Address Bus: carries the multiplexed row and column addresses to the SDRAM memory banks. Auto-precharge is not supported.
BA[2:0]	3	O Sync (M) Rst (M)	SDRAM Bank Address: controls which of the internal banks to read or write. **BA[1:0]** are used for 512 Mbit technology memory. **BA[2:0]** are used for 1 Gbit technology memory.
RAS#	1	O Sync (M) Rst (M) ActLow	SDRAM Row Address Strobe: indicates the presence of a valid row address on the Multiplexed Address Bus **MA[13:0]**.
CAS#	1	O Sync (M) Rst (M) ActLow	SDRAM Column Address Strobe: indicates the presence of a valid column address on the Multiplexed Address Bus **MA[13:0]**.
WE#	1	O Sync (M) Rst (M) ActLow	SDRAM Write Enable: indicates whether the current memory transaction is a read or write operation.
CS[1:0]#	2	O Sync (M) Rst (M) ActLow	SDRAM Chip Select: enables the SDRAM devices for a memory access. One for each physical bank.
CKE[1:0]	2	O Sync (M) Rst (M)	SDRAM Clock Enable enables: the clocks for the SDRAM memory. Deasserting places the SDRAM in self-refresh mode. One for each physical bank.
DQ[63:0]	64	I/O Sync (M) Rst (M)	SDRAM Data Bus: carries 64-bit data to and from memory. During the data cycle, read or write data is present on one or more contiguous bytes. During write operations, unused pins drive to determinate values.
CB[7:0]	8	I/O Sync (M) Rst (M)	SDRAM ECC Check Bits: carry the 8-bit ECC code to and from memory during data cycles.
DQS[8:0], DQS#[8:0]	18	I/O Sync (M) Rst (M) Diff	SDRAM Data Strobes: carry differential or single-ended strobe signals, output in write mode, and input in read mode for source synchronous data transfer.
DM[8:0]	9	O Sync (M) Rst (M)	SDRAM Data Mask: controls which bytes on the data bus are to be written. When **DM[8:0]** is asserted, the SDRAM devices do not accept valid data from the byte lanes.
M_VREF	1	I	SDRAM Voltage Reference: is used to supply the input switching reference voltage for the memory input signals.
ODT[1:0]	2	O Sync (M) Rst (M)	On-Die Termination: is used to turn on SDRAM on-die termination during writes.



Table 2. DDR2 SDRAM Signals (Sheet 2 of 2)

Name	Count	Type	Description
M_CAL[0]	1	O	Memory Calibration: Connected to an external calibration resistor. Memory output drivers reference the resistor to dynamically adjust drive strength to compensate for temperature and voltage variations. This pin connected through a 24.9 ohm 1% resistor to ground.
M_CAL[1]	1	O	Memory Calibration: Connected to an external calibration resistor. Memory output drivers reference the resistor to dynamically adjust ODT resistance to compensate for temperature and voltage variations. This pin connected through a 301 ohm 1% resistor to ground.
Total	135		

a. MA[14] was added for 4GB memory support. When 4GB memory is not used this pin is NC.

Table 3. Peripheral Bus Interface Signals

Name	Count	Type	Description
A[24:0]	25	O Rst (PB)	Peripheral Address Bus: carries the address bits for the current access. The PBI interface can address up to 32 MBytes.
D[15:0]	16	I/O Rst (PB)	Peripheral Data Bus: carries read or write data to and from memory. During write operations to 8-bit wide memory regions, the PBI drives unused bus pins to determinate values.
POE#	1	O Rst (PB) ActLow	Peripheral Output Enable: indicates whether bus access is write or read with respect to I/O processor and is valid during entire bus access. This pin can be used to control output enable on a peripheral device. 0 = Read 1 = Write
PWE#	1	O Rst (PB) ActLow	Peripheral Write Enable: indicates to the peripheral device whether or not to write data to the addressed space. This pin can be used to control the write enable on the peripheral device. 0 = Write 1 = Read
PCE[1:0]#	2	O Rst (PB) ActLow	Peripheral Chip Enable: Specifies which of the two memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. ***Note:*** These pins must be pulled up to V_{CC3P3} with external 8.2K ohm 5%, 1/16 W resistors for proper operation.
PB_RSTOUT#	1	O ActLow	Peripheral Bus Reset Out: can be used to reset the peripheral device. It has the same timing as the internal bus reset.
Total	46		



Table 4. Compact PCI Hot Swap Signals

Name	Count	Type	Description
HS_ENUM#	1	OD Rst (P) ActLow	Hot Swap Event: Conditionally asserted to notify system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing or quiesing a device driver.
HS_LSTAT	1	I Rst (P)	Hot Swap Latch Status: Input indicating state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. If Compact PCI Hot Swap not supported, tie this signal low.
HS_LED_OUT	1	O Rst (P)	Hot Swap LED Output: outputs a logic one to illuminate the Hot Swap blue LED.
HS_FREQ[1:0] / **CR_FREQ[1:0]**	2	I/O Rst (P)	Hot Swap Frequency: In Hot Swap mode, these pins are inputs, determining the bus frequency and mode during a PCI-X hot swap event. These are valid only when **PCIX_EP#** = 0 and **HS_SM#** = 0. 00 = 133 MHz PCI-X 01 = 100 MHz PCI-X 10 = 66 MHz PCI-X 11 = 33 or 66 MHz. PCI (frequency depends on **P_M66EN**) Central Resource Frequency: While in Central Resource mode, these pins are outputs, which control the external PCI-X clock generator. These are valid only when **PCIX_EP#** = 1. 00 = 133 MHz 01 = 100 MHz 10 = 66 MHz 11 = 33 MHz • These pins have internal pull-ups.
Total	5		

Table 5. PCI Bus Signals (Sheet 1 of 3)

Name	Count	Type	Description
P_AD[63:32]	32	I/O Sync (P) Rst (P)	PCI Address/Data: is the upper 32 bits of the PCI data bus driven during the data phase.
P_AD[31:0]	32	I/O Sync (P) Rst (P)	PCI Address/Data: is the multiplexed PCI address and lower 32 bits of the data bus.
P_CBE[7]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[6]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[5]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[4]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[3]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[2]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[1]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_CBE[0]#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables.
P_PAR64	1	I/O Sync (P) Rst (P)	PCI Bus Upper DWORD Parity is even parity across **P_AD[63:32]** and P_CBE_#[7:4].
P_REQ64#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Request 64-Bit Transfer indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of P_ACK64_#.
P_ACK64#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Acknowledge 64-Bit Transfer indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus.
P_PAR	1	I/O Sync (P) Rst (P)	PCI Bus Parity is even parity across **P_AD[31:0]** and P_CBE_#[3:0].
P_FRAME#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Cycle Frame is asserted to indicate the beginning and duration of an access.



Table 5. PCI Bus Signals (Sheet 2 of 3)

Name	Count	Type	Description
P_IRDY#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the address/data bus. During a read, it indicates that the processor is ready to accept the data.
P_TRDY#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Target Ready indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the address/data bus. During a write, it indicates that the target is ready to accept the data.
P_STOP#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Stop indicates a request to stop the current transaction on the PCI bus.
P_DEVSEL#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Device Select is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected.
P_SERR#	1	I/O OD Sync (P) Rst (P) ActLow	PCI Bus System Error is driven for address parity errors on the PCI bus.
P_RSTOUT#	1	O Async ActLow	PCI Reset Out is based on **P_RST#** and **WARM_RST#**. It brings PCI-specific registers, sequencers, and signals to a consistent state. When either **P_RST#** or **WARM_RST#** is asserted, it causes **P_RSTOUT#** to assert and: • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • Open-drain signals such as P_SERR_# are floated. **P_RSTOUT#** can be asynchronous to P_CLK when asserted or deasserted.
P_PERR#	1	I/O Sync (P) Rst (P) ActLow	PCI Bus Parity Error is asserted when a data parity error occurs during a PCI bus transaction.
P_M66EN	1	I	PCI Bus 66 MHz Enable indicates the speed of the PCI bus. When this signal is sampled high, the PCI bus speed is 66 MHz; when low, the bus speed is 33 MHz.
P_IDSEL	1	I Sync (P)	PCI Bus Initialization Device Select is used to select the Intel® 81341 and Intel® 81342 I/O Processors during a configuration read or write. ***Note:*** In central resource mode this pin must be pulled down to V_{SS} with an external 4.7K ohm 5%, 1/16 W resistor for proper operation.
P_GNT[0]# / P_REQ#	1	O Sync (P) ActLow	PCI Bus Grant: • Internal arbiter mode: This is one of four output grant signals from the internal arbiter. PCI Bus Request: • External arbiter mode: This is the output request signal for the ATU.
P_REQ[0]# / P_GNT#	1	I Sync (P) Rst (P) ActLow	PCI Bus Request: • Internal arbiter mode: This is one of four input request signals to the internal arbiter. PCI Bus Grant: • External arbiter mode: This is the input grant signal to the ATU.

Table 5. PCI Bus Signals (Sheet 3 of 3)

Name	Count	Type	Description
P_GNT[3:1]#	3	O Sync (P) ActLow	PCI Bus Grant: • External arbiter mode: Not used • Internal arbiter mode: These are three of four output grant signals from the internal arbiter.
P_REQ[3:1]#	3	I Sync (P) Rst (P) ActLow	PCI Bus Request: • External arbiter mode: Not used • Internal arbiter mode: These are three of four input request signals to the internal arbiter.
P_PCIXCAP	1	I	PCI-X Capability: Refer to the Intel® 81341 and Intel® 81342 I/O Processors *Specification Update* for more details.
P_BMI	1	O Sync (P) Rst (P)	PCI Bus Master Indicator indicates that the I/O processor is mastering a transaction on the PCI bus.
P_CAL[0]	1	O	PCI Calibration is connected to an external calibration resistor. The **V_{CCVIO}** PCI output drivers reference the resistor to dynamically adjust the drive strength to compensate for voltage and temperature variations. This pin is connected through a 22.1 ohm 1% resistor to ground.
P_CAL[1]	1	O	PCI Calibration is connected to an external calibration resistor. The PCI output drivers reference the resistor to dynamically adjust the ODT resistance to compensate for voltage and temperature variations. This pin is connected through a 121 ohm 1% resistor to ground.
P_CAL[2]	1	O	PCI Calibration is connected to an external calibration resistor. The **V_{CC3P3}** PCI output drivers reference the resistor to dynamically adjust the drive strength to compensate for voltage and temperature variations. This pin is connected through a 22.1 ohm 1% resistor to ground.
P_CLKIN	1	I	PCI Bus Input Clock provides the AC timing reference for all PCI transactions.
P_CLKOUT	1	O	PCI Bus Output Clock: When **REFCLKN**/**REFCLKP** are used, the I/O processor can generate the PCI output clocks. This pin is then connected to **P_CLKIN** and trace length matched to **P_CLKO[3:0]**.
P_CLKO[3:0]	4	O	PCI Bus Output Clocks: When **REFCLKN**/**REFCLKP** are used, the I/O processor can generate the PCI output clocks. These pins then provide the PCI clocks to devices on the PCI bus.
Total	105		



Table 6. PCI Express* Signals

Name	Count	Type	Description
REFCLKP, **REFCLKN**	2	I Diff	PCI Express* Clock is the 100 MHz differential input reference clock for the PCI Express* interface.
PETP[7:0], **PETN[7:0]**	16	O Diff	PCI Express* Transmit carries the differential output serial data and embedded clock for the PCI Express* interface.
PERP[7:0], **PERN[7:0]**	16	I Diff	PCI Express* Receive carries the differential input serial data and embedded clock for the PCI Express* interface.
PE_CALP, **PE_CALN**	2	I/O	PCI Express* Calibration pins are connected to an external calibration resistor. The PCI Express* output drivers can reference the resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations. A 1.4K ohm 1% resistor is connected between these two pins.
Total	36		

Table 7. Interrupt Signals

Name	Count	Type	Description
P_INT[D:A]# / XINT[3:0]# / GPIO[11:8]	4	OD I I/O Async Rst (P) ActLow	When **PCIX_EP#** = 0: • PCI Interrupt requests an interrupt from the central resource. The assertion and deassertion is asynchronous. A device asserts its **XINT[3:0]#** / **P_INT[D:A]#** line when requesting attention from its device driver. As soon as the **XINT[3:0]#** / **P_INT[D:A]#** signal is asserted, it remains asserted until the device driver clears the pending request. When **PCIX_EP#** = 1: • External Interrupt requests are used by external devices to request interrupt service. These pins are level-detect inputs and are internally synchronized. These pins go to the **XINT[3:0]#** inputs of the interrupt controller. The interrupt controller can steer the interrupt to either the FIQ or the IRQ internal interrupt input of the Intel XScale® processor. General Purpose I/O pins can be selected on a per-pin basis as general-purpose inputs or outputs. The default mode is a general-purpose input.
XINT[7:4]# / GPIO[15:12]	4	I I/O Async ActLow	External Interrupt Requests are used by external devices to request interrupt service. These pins are level-detect and are internally synchronized. These pins go to the **XINT[7:4]#** inputs of the interrupt controller. The interrupt controller can steer the interrupt to either the FIQ or the IRQ internal interrupt input of the Intel XScale® processor. General Purpose I/O pins can be selected on a per-pin basis as general-purpose inputs or outputs. The default mode is a general-purpose input.
GPIO[7:0] / XINT[15:8]# / PMONOUT	8	I/O I O Async Rst (P)	General Purpose I/O pins can be selected on a per-pin basis as general-purpose inputs or outputs. The default mode is a general-purpose input. External Interrupts are used by external devices to request interrupt service. These pins are level-detect and are internally synchronized. These pins go to the **XINT[15:8]#** inputs of the interrupt controller. These interrupts are dedicated to the Intel XScale® processor. To enable a given pin as an interrupt, it needs to be unmasked in the INTCTL[3:0] register. Performance Monitor Out: The PMON unit output indicator will generate a signal on the **GPIO[7]** pin when enabled in the PMONEN register. When enabled it will override the normal **GPIO[7]** function.
HPI#	1	I Async ActLow	High-Priority Interrupt causes a high-priority interrupt to the I/O processor. This pin is level-detect only and is internally synchronized.
NMI0#	1	I Async ActLow	Non-Maskable Interrupt causes a non-maskable data abort to the Intel XScale® processor 0 in the I/O processor. This pin is falling edge-detect only and is internally synchronized.
NMI1#	1	I Async ActLow	Non-Maskable Interrupt causes a non-maskable data abort to the Intel XScale® processor 1 in the I/O processor. This pin is falling edge-detect only and is internally synchronized. ***Note:*** This signal not applicable to the 81341 processor.
Total	19		



Table 8. I²C and SM Bus Signals

Name	Count	Type	Description
SCL0	1	I/O OD	I²C 0 Clock provides synchronous operation of the I²C bus.
SDA0	1	I/O OD	I²C 0 Data is used for data transfer and arbitration of the I²C bus.
SCL1	1	I/O OD	I²C 1 Clock provides synchronous operation of the I²C bus.
SDA1	1	I/O OD	I²C 1 Data is used for data transfer and arbitration of the I²C bus.
SCL2	1	I/O OD	I²C 2 Clock provides synchronous operation of the I²C bus.
SDA2	1	I/O OD	I²C 2 Data is used for data transfer and arbitration of the I²C bus.
SMBCLK	1	I/O OD	SM Bus Clock provides synchronous operation of the SM bus.
SMBDAT	1	I/O OD	SM Bus Data is used for data transfer and arbitration of the bus.
Total	8		

Note: Open drain outputs require an external pull-up resistor to pull up the signal to 3.3 V. The value of the pull-up resistor depends on the bus loading.

Table 9. UART Signals (Sheet 1 of 2)

Name	Count	Type	Description
U0_RXD	1	I Async	UART 0 Serial Input: Serial data input from device pin to the receive shift register.
U0_TXD	1	O Async	UART 0 Serial Output: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a reset operation.
U0_CTS#	1	I ActLow Async	UART 0 Clear to Send: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts CTS# high, the transmitting UART must stop transmission to prevent overflow of the receiving UART buffer. The CTS# signal is a modem-status input whose condition can be tested by the host processor or by the UART when in Autoflow Mode as described below: • Non-Autoflow Mode: When not in Autoflow Mode, bit[4] (CTS) of the Modem Status Register (MSR) indicates the state of CTS#. Bit[4] is the complement of the CTS# signal. Bit[0] (DCTS) of the Modem Status Register indicates whether the CTS# input has changed state since the previous reading of the Modem Status Register. CTS# has no effect on the transmitter. The user can program the UART to interrupt the processor when DCTS changes state. The programmer can then stall the outgoing data stream by starving the transmit FIFO or disabling the UART with the IER register. ***Note:*** When UART transmission is stalled by disabling the UART, the user does not receive an MSR interrupt when CTS# reasserts. This is because disabling the UART also disables interrupts. To work around this, the user can use Auto CTS in Autoflow Mode, or program the CTS# pin to interrupt. • Autoflow Mode: In Autoflow Mode, the UART transmit circuity checks the state of CTS# before transmitting each byte. When CTS# is high, no data is transmitted.
U0_RTS#	1	O ActLow Async	UART 0 Request to Send: This bit indicates to the remote device whether the UART is ready to receive data. When this bit is low, the UART is ready to receive data. A reset operation sets this signal to its inactive (high) state. LOOP Mode operation holds this signal in its inactive state. • Non-Autoflow Mode: The RTS# output signal can be asserted by setting bit[1] (RTS) of the Modem Control Register to 1. The RTS bit is the complement of the RTS# signal. • Autoflow Mode: RTS# is automatically asserted by the autoflow circuitry when the receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.
U1_RXD	1	I Async	UART 1 Serial Input: Serial data input from the device pin to the receive shift register.



Table 9. UART Signals (Sheet 2 of 2)

Name	Count	Type	Description
U1_TXD	1	O Async	UART 1 Serial Output: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a reset operation.
U1_CTS#	1	I ActLow Async	UART 1 Clear to Send: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts CTS# high, the transmitting UART must stop transmission to prevent overflow of the receiving UART buffer. The CTS# signal is a modem-status input whose condition can be tested by the host processor or by the UART when in Autoflow Mode as described below: • Non-Autoflow Mode: When not in Autoflow Mode, bit[4] (CTS) of the Modem Status Register (MSR) indicates the state of CTS#. Bit[4] is the complement of the CTS# signal. Bit[0] (DCTS) of the Modem Status Register indicates whether the CTS# input has changed state since the previous reading of the Modem Status Register. CTS# has no effect on the transmitter. The user can program the UART to interrupt the processor when DCTS changes state. The programmer can then stall the outgoing datastream by starving the transmit FIFO or disabling the UART with the IER register. ***Note:*** When UART transmission is stalled by disabling the UART, the user does not receive an MSR interrupt when CTS# reasserts. This is because disabling the UART also disables interrupts. To get around this, the user can use Auto CTS in Autoflow Mode, or program the CTS# pin to interrupt. • Autoflow Mode: In Autoflow Mode, the UART transmit circuitry checks the state of CTS# before transmitting each byte. When CTS# is high, no data is transmitted.
U1_RTS#	1	O ActLow Async	UART 1 Request to Send: This bit indicates to the remote device whether the UART is ready to receive data. When low, the UART is ready to receive data. A reset operation sets this signal to its inactive (high) state. LOOP Mode operation holds this signal in its inactive state. • Non-Autoflow Mode: The RTS# output signal can be asserted by setting bit[1] (RTS) of the Modem Control Register to 1. The RTS bit is the complement of the RTS# signal. • Autoflow Mode: RTS# is automatically asserted by the autoflow circuitry when the receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.
Total	8		

Table 10. Miscellaneous Signals

Name	Count	Type	Description
TCK	1	I	Test Clock provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the device on the rising clock edge, and data is clocked out on the falling clock edge.
TDI	1	I Sync (T)	Test Data Input is the JTAG serial input pin. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this pin is not being driven.
TDO	1	O Sync (T) Rst (T)	Test Data Output is the serial output pin for the JTAG feature. TDO is driven on the falling edge of **TCK** during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, **TDO** floats. The behavior of **TDO** is independent of other resets.
TRST#	1	I Async ActLow	Test Reset asynchronously resets the Test Access Port controller function of IEEE 1149 Boundary Scan Testing (JTAG). This pin has a weak internal pull-up. ***Note:*** This pin must be tied low when not used.
TMS	1	I Sync (T)	Test Mode Select is sampled on the rising edge of **TCK** to select the operation of the test logic for IEEE 1149 Boundary Scan testing. This pin has a weak internal pull-up.
NC	106	I/O	No Connect: Pins have no usable function and must not be connected to any signal, power, or ground.
P_RST#	1	I Async ActLow	Cold Reset is used to asynchronously reset the I/O processor when it is low. This signal must be asserted whenever the power supplies are outside of the specified ranges. • Registers are reset to default values. • Pins are driven to known states. • Sticky configuration bits are reset.
WARM_RST#	1	I Async ActLow	Warm Reset is the same as a cold reset, except sticky configuration bits are not reset. This pin should only be used when the sticky bit functionality is required. In this scenario, the WARM_RST# pin must be tied to the system reset PCI_RST# signal while the P_RST# pin can be tied to the system power good signal. If the sticky bit functionality is not required, the WARM_RST# pin should not be used and must be tied to Vcc. When the PCI Express interface is used as an endpoint, the PCI Express inband Hot Reset Mechanism can also be used to provide the sticky bit functionality. ***Note:*** Driving WARM_RST# using any other methods than suggested above may result in unpredictable behavior of the device.
THERMDA	1	I	Thermal Diode Anode is the anode of the thermal diode.
THERMDC	1	O	Thermal Diode Cathode is the cathode of the thermal diode.
PUR1	1	I	Pull-Up Required 1: This pin must be pulled up to $\mathbf{V_{CC3P3}}$ with an external 8.2K ohm 5%, 1/16 W resistor for proper operation.
Total	116		



Table 11. Power and Ground Signals

Name	Count	Type	Description
$V_{CC1P2PLLP}$	1	**PWR**	V_{CC} PLL PCI-X: Ball connected to a 1.2 V filtered board supply. Provides power to PLL that controls the PCI-X logic and interface.
$V_{CC1P2PLLD}$	1	**PWR**	V_{CC} PLL DDR: Ball connected to a 1.2 V filtered board supply. Provides power to the PLL that controls the DDR2 SDRAM interface and processor digital logic.
$V_{CC3P3PLLX}$	1	**PWR**	V_{CC} PLL X: Ball to be connected to a 3.3 V filtered board supply. This pin provides power to a voltage regulator, which supplies power to the PLL that controls the Intel XScale® processor and XSI processor logic.
VSSPLLP	1	**GND**	V_{SS} PLL PCI-X: Ball connected to capacitor of the **$V_{CC1P2PLLP}$** filter.
VSSPLLD	1	**GND**	V_{SS} PLL DDR2 SDRAM: Ball connected to capacitor of **$V_{CC1P2PLLD}$** filter.
VSSPLLX	1	**GND**	V_{SS} PLL X: Ball connected to capacitor of **$V_{CC3P3PLLX}$** filter.
V_{CC1P2}	204	**PWR**	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the processor logic.
$V_{CC1P2AE}$	8	**PWR**	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the PCI Express* analog logic.
V_{CC1P2E}	6	**PWR**	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the PCI Express* digital logic.
V_{CC1P2X}	119	**PWR**	1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the Intel XScale® processors.
V_{CCVIO}	21	**PWR**	VIO Power: Balls to be connected to a 3.3 V board power plane. These pins provide 3.3 V power to the PCI-X I/Os.
V_{CC1P8}	36	**PWR**	1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the DDR2 SDRAM interface I/Os.
V_{CC1P8E}	14	**PWR**	1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the PCI Express* interface I/Os.
V_{CC3P3}	42	**PWR**	3.3 V Power: Balls to be connected to a 3.3 V board power plane. These pins provide power to the PBI, miscellaneous pins, and PCI-X I/Os in Mode 1.
V_{SS}	403	**GND**	Ground: Balls to be connected to a board ground plane.
V_{SSE}	20	**GND**	PCI Express* Ground: Balls connected to a board ground plane.
Total	880		

Table 12. Reset Strap Signals (Sheet 1 of 3)

Name	Count	Type	Description
BOOT_WIDTH_8#	1	Reset Strap	PBI Boot Bus Width: Sets the default bus width for the PBI Memory Boot window. 0 = 8 bits wide 1 = 16 bits wide (default mode) ***Note:*** Muxed onto signal **A[0]**.
DF_SEL[2:0]	3	Reset Strap	Device Function Select: These straps select the number of storage ports assigned to each function within the Intel® 81341 and Intel® 81342 I/O Processors. ***Note:*** DF_SEL[2] muxed onto signal A[9] ***Note:*** DF_SEL[1] muxed onto signal A[8] ***Note:*** DF_SEL[0] muxed onto signal A[7] See the "Device Function Select" of the *Intel® 81341 and Intel® 81342 I/O Processors Developer's Manual* for additional details.
CFG_CYCLE_EN#	1	Reset Strap	Configuration Cycle Enable: Determines whether PCI interface retries configuration cycles until Host Lockout Bit is cleared in all enabled TPMI functions (TCFGR[5]). 0 = Configuration cycles enabled 1 = Configuration retry enabled (default mode) • PCI-X Interface: Configuration cycles are claimed and terminated with a retry status. • PCI Express* Interface: Configuration requests result in a completion TLP with Configuration Retry Status (CRS). ***Note:*** Muxed onto signal **A[1]**
HOLD_X0_IN_RST#	1	Reset Strap	Hold Intel XScale® Microprocessor 0 in Reset: Determines whether the Intel XScale® microprocessor number 0 is held in reset until the reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset 1 = Do not hold in reset (default mode) ***Note:*** Muxed onto signal **A[2]**
HOLD_X1_IN_RST#	1	Reset Strap	Hold Intel XScale® Microprocessor 1 in Reset: Determines whether the Intel XScale® microprocessor number 1 is held in reset until the reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset 1 = Do not hold in reset (default mode) ***Note:*** Muxed onto signal **A[3]** ***Note:*** This signal not applicable to the 81341 processor.
MEM_FREQ[1:0]	2	Reset Strap	Memory Frequency: Determines frequency at which DDR2 memory subsystem runs. 00 = Reserved 01 = Reserved 10 = 533 MHz 11 = 400 MHz (Default mode) ***Note:*** **MEM_FREQ[1]** muxed onto signal **A[5]** ***Note:*** **MEM_FREQ[0]** muxed onto signal **A[4]**
EXT_ARB#	1	Reset Strap	External Arbiter: Determines whether the PCI interface enables the integrated arbiter, or use an external arbiter. 0 = External arbiter 1 = Internal arbiter (default mode) ***Note:*** Muxed onto signal **A[6]**
INTERFACE_SEL_PCIX#	1	Reset Strap	0 = PCI-X is active 1 = PCI Express is active (default mode) When both interfaces are active, this strap selects the ATU that is function 0 in the internal address map. ***Note:*** Muxed onto signal **A[10]**
PCIX_EP#	1	Reset Strap	PCI-X End Point: Determines whether the PCI-X interface operates as an endpoint or a central resource. 0 = Endpoint 1 = Central resource (default mode) ***Note:*** Muxed onto signal **A[11]** ***Note:*** Setting both **PCIX_EP#** and PCIE_RC# to endpoint is unsupported.



Table 12. Reset Strap Signals (Sheet 2 of 3)

Name	Count	Type	Description
PCIE_RC#	1	Reset Strap	PCI-E Root Complex: Determines whether PCI Express* interface operates as an endpoint or a root complex. 0 = Root complex 1 = Endpoint (default mode) ***Note:*** Muxed onto signal **A[12]** Setting both **PCIX_EP#** and **PCIE_RC#** to endpoint is unsupported.
SMB_A5, **SMB_A3**, **SMB_A2**, **SMB_A1**	4	Reset Strap	SM Bus Address: Maps to address bit[5], bit[3], bit[2], and bit[1] where bits[7:0] represent address SMBus slave port responds to when access is attempted. 0 = Address bit is low 1 = Address bit is high (default mode) ***Note:*** **SMB_A5** muxed onto signal **A[16]** ***Note:*** **SMB_A3** muxed onto signal **A[15]** ***Note:*** **SMB_A2** muxed onto signal **A[14]** ***Note:*** **SMB_A1** muxed onto signal **A[13]**
PCIX_PULLUP#	1	Reset Strap	PCI-X Pull Up: Determines whether PCI interface has on-die pull-ups enabled. These may be used for the central resource bus keepers. 0 = Enable PCI pull-up resistors 1 = Disable PCI pull-up resistors (default mode) ***Note:*** Muxed onto signal **A[17]**
PCIX_32BIT#	1	Reset Strap	32-Bit PCI-X Bus: Indicates width of the PCI-X bus to PCI-X Status Register. Enables pull-ups for upper half of bus when in 32-bit mode. 0 = 32-bit wide PCI-X bus 1 = 64-bit wide PCI-X bus (default mode) ***Note:*** Muxed onto signal **A[18]**
PCIXM1_100#	1	Reset Strap	PCI-X Mode 1 100 MHz Enable: In Central Resource Mode, this bit limits PCI-X bus to 100 MHz while in mode 1: 0 = Limit PCI-X mode 1 to 100 MHz 1 = 133 MHz enabled (default mode) ***Note:*** Muxed onto signal **A[19]**
HS_SM#	1	Reset Strap	Hot Swap Startup Mode: In End Point Mode, this bit determines whether Hot Swap mode is enabled. 0 = Hot Swap Mode enabled 1 = Hot Swap Mode disabled (default mode) ***Note:*** Muxed onto signal **A[21]**
FW_TIMER_OFF#	1	Reset Strap	Firmware Timer Off: Disables 400 mS firmware timer for development and debug. When enabled, timer automatically clears Configuration Cycle Retry (CCR) bit in PCSR after 400 mS regardless of processor state. When disabled, CCR bit functions as normal based on state of CFG_CYCLE_EN# pin at rising edge of P_RST#. 0 = Firmware timer disabled 1 = Firmware timer enabled (default mode) ***Note:*** Muxed onto signal **A[22]**
CONTROLLER_ONLY#	1	Reset Strap	Controller-Only Enable: 0 = Controller only, RAID disabled 1 = RAID enabled (default mode) ***Note:*** Muxed onto signal **A[23]**
LK_DN_RST_BYPASS#	1	Reset Strap	Link Down Reset Bypass: Disables the full chip reset that would normally be caused by a Link Down or hot reset. 0 = Do not reset on Link Down 1 = Reset on Link Down (default mode) ***Note:*** Muxed onto signal **A[24]**

Table 12. Reset Strap Signals (Sheet 3 of 3)

Name	Count	Type	Description
CLK_SRC_PCIE#	1	Reset Strap	Clock Source PCI-E: Selects PCI Express* Refclk pair as the input clock to the PLLs that control most internal logic. 0 = Source clock is **REFCLKP**/**REFCLKN** 1 = Source clock is **P_CLKIN** (default mode) ***Note:*** When **P_CLKO[3:0]** are used this pin must be pulled low. ***Note:*** Muxed onto signal **PWE#**
Total	25		

Reset strap signals are latched on the rising edge of **P_RST#**. All reset strap signals are internally pulled to logic 1 by default. An external 4.7K ohm 5%, 1/16 W pull-down resistor is required to force a logic 0 on these pins.



Table 13. Functional Pin Mode Behavior (Sheet 1 of 4)

Pin	Boundary Scan High Z	Reset (End Point)	Reset (Central Resource)	Normal	32-Bit SDRAM	PCIX_32BIT#	PCIX_PULLUP#	When only PCI-X Interface Active	When only PCI Express* Interface Active
M_CK[2:0], M_CK#[2:0]	Z	VO	VO	VO	–	–	–	–	–
M_RST#	Z	0*	0*	VO	–	–	–	–	–
MA[14:0][a]	Z	VO	VO	VO	–	–	–	–	–
BA[2:0]	Z	VO	VO	VO	–	–	–	–	–
RAS#	Z	VO	VO	VO	–	–	–	–	–
CAS#	Z	VO	VO	VO	–	–	–	–	–
WE#	Z	VO	VO	VO	–	–	–	–	–
CS[1:0]#	Z	VO	VO	VO	–	–	–	–	–
CKE[1:0]	Z	0*	0*	VO	–	–	–	–	–
DQ[63:32]	Z	Z*	Z*	VB	Z	–	–	–	–
DQ[31:0]	Z	Z*	Z*	VB	–	–	–	–	–
CB[7:0]	Z	Z*	Z*	VB	–	–	–	–	–
DQS[8], DQS#[8]	Z	Z*	Z*	VB	–	–	–	–	–
DQS[7:4], DQS#[7:4]	Z	Z*	Z*	VB	Z	–	–	–	–
DQS[3:0], DQS#[3:0]	Z	Z*	Z*	VB	–	–	–	–	–
DM[8]	Z	VO*	VO*	VO	–	–	–	–	–
DM[7:4]	Z	VO*	VO*	VO	–	–	–	–	–
DM[3:0]	Z	VO*	VO*	VO	–	–	–	–	–
M_VREF	–	AI	AI	AI	–	–	–	–	–
ODT[1:0]	Z	0*	0*	VO	–	–	–	–	–
M_CAL[1:0]	Z	Z*	Z*	AO	–	–	–	–	–
A[24:0]	Z	H	H	VO	–	–	–	–	–
D[15:0]	Z	H	H	VB	–	–	–	–	–
POE#	Z	H	H	VO	–	–	–	–	–
PWE#	Z	H	H	VO	–	–	–	–	–
PB_RSTOUT#	Z	0	0	VO	–	–	–	–	–
PCE[1:0]#	Z	H	H	VO	–	–	–	–	–
HS_ENUM#	Z	Z	Z	VO	–	–	–	–	–
HS_LSTAT	–	VI	VI	VI	–	–	–	–	–
HS_LED_OUT	Z	1	1	VO	–	–	–	–	–
HS_FREQ[1:0] / CR_FREQ[1:0]	Z	H	H	H	–	–	–	–	–

Notes:

1 = driven to V_{CC}
0 = driven to V_{SS}
X = driven to unknown state
ID = The input is disabled.
H = pulled up to V_{CC}
PD = pull-up disabled
L = pulled down to V_{SS}
ODT = On Die Termination
GND = Tie to Ground.

EA = External Arbiter mode
IA = Internal Arbiter mode
Z = output, pull-up/down disabled
VB = acts like a Valid Bidirectional pin
VO = a Valid Output level is driven.
VI = need to drive a Valid Input level.
AO = Analog Output level
AI = Analog Input level
* = after power fail sequence completes
"-" = unaffected by this mode

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.

Table 13. Functional Pin Mode Behavior (Sheet 2 of 4)

Pin	Boundary Scan High Z	Reset (End Point)	Reset (Central Resource)	Normal	32-Bit SDRAM	PCIX_32BIT#	PCIX_PULLUP#	When only PCI-X Interface Active	When only PCI Express* Interface Active
P_AD[63:32]	Z	Z	Z	VB	–	H	H	–	H
P_AD[31:0]	Z	Z	0	VB	–	–	–	–	H
P_CBE[7:4]#	Z	Z	Z	VB	–	H	H	–	H
P_CBE[3:0]#	Z	Z	0	VB	–	–	–	–	H
P_PAR64	Z	Z	Z	VB	–	H	H	–	H
P_REQ64#	Z	VI	0	VB	–	–	H	–	H
P_ACK64#	Z	Z	Z	VB	–	–	H	–	H
P_PAR	Z	Z	0	VB	–	–	–	–	H
P_FRAME#	Z	VI	VO	VB	–	–	H	–	H
P_IRDY#	Z	VI	VO	VB	–	–	H	–	H
P_TRDY#	Z	VI	VO	VB	–	–	H	–	H
P_STOP#	Z	VI	VO	VB	–	–	H	–	H
P_DEVSEL#	Z	VI	VO	VB	–	–	H	–	H
P_SERR#	Z	Z	Z	VB	–	–	H	–	H
P_RSTOUT#	Z	0	0	VO	–	–	–	–	VO
P_PERR#	Z	VI	VO	VB	–	–	H	–	H
P_M66EN	–	VI	VI	VI	–	–	–	–	H
P_IDSEL	–	VI	VI	VI	–	–	–	–	H
P_GNT[0]# / P_REQ#	Z	$Z_{(EA)}$ $H_{(IA)}$	$Z_{(EA)}$ $H_{(IA)}$	VO	–	–	–	–	H
P_REQ[0]# / P_GNT#	–	$VI_{(EA)}$ $H_{(IA)}$	$VI_{(EA)}$ $H_{(IA)}$	$VI_{(EA)}$ $H_{(IA)}$	–	–	–	–	H
P_GNT[3:1]#	Z	H	H	VO	–	–	–	–	H
P_REQ[3:1]#	–	H	H	H	–	–	–	–	H
P_CLKIN	–	VI	VI	VI	–	–	–	–	GND
P_CLKOUT	Z	Z	VO	VO	–	–	–	–	Z
P_CLKO[3:0]	Z	Z	VO	VO	–	–	–	–	Z
P_PCIXCAP	–	AI	AI	AI	–	–	–	–	GND
P_BMI	Z	VO	VO	VO	–	–	–	–	VO
P_CAL[2:0]	Z	AO	AO	AO	–	–	–	–	VO
REFCLKP, REFCLKN	–	VI	VI	VI	–	–	–	GND/ VI	–
PETP[7:0], PETN[7:0]	–	Z	Z	VO	–	–	–	Z	–

Notes:

1 = driven to V_{CC}
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ID = The input is disabled.
H = pulled up to V_{CC}
PD = pull-up disabled
L = pulled down to V_{SS}
ODT = On Die Termination
GND = Tie to Ground.

EA = External Arbiter mode
IA = Internal Arbiter mode

Z = output, pull-up/down disabled
VB = acts like a Valid Bidirectional pin
VO = a Valid Output level is driven.
VI = need to drive a Valid Input level.
AO = Analog Output level
AI = Analog Input level
* = after power fail sequence completes
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Table 13. Functional Pin Mode Behavior (Sheet 3 of 4)

Pin	Boundary Scan High Z	Reset (End Point)	Reset (Central Resource)	Normal	32-Bit SDRAM	PCIX_32BIT#	PCIX_PULLUP#	When only PCI-X Interface Active	When only PCI Express* Interface Active
PERP[7:0], PERN[7:0]	–	ID	ID	VI	–	–	–	Z	–
PE_CALP	–	AO	AO	AO	–	–	–	Z	–
PE_CALN	–	AO	AO	AO	–	–	–	Z	–
P_INT[D:A]# / XINT[3:0]#	Z	Z/VI	Z/VI	VB	–	–	H	–	–
XINT[7:4]#	–	VI	VI	VI	–	–	–	–	–
GPIO[7:0] / XINT[15:8]# / PMONOUT	Z	VI	VI	VB	–	–	–	–	–
HPI#	–	VI	VI	VI	–	–	–	–	–
NMI0#	–	VI	VI	VI	–	–	–	–	–
NMI1#	–	VI	VI	VI	–	–	–	–	–
SCL0	Z	Z	Z	VB	–	–	–	–	–
SDA0	Z	Z	Z	VB	–	–	–	–	–
SCL1	Z	Z	Z	VB	–	–	–	–	–
SDA1	Z	Z	Z	VB	–	–	–	–	–
SCL2	Z	Z	Z	VB	–	–	–	–	–
SDA2	Z	Z	Z	VB	–	–	–	–	–
SMBCLK	Z	Z	Z	VB	–	–	–	–	–
SMBDAT	Z	Z	Z	VB	–	–	–	–	–
U0_RXD	–	VI	VI	VI	–	–	–	–	–
U0_TXD	Z	1	1	VO	–	–	–	–	–
U0_CTS#	–	VI	VI	VI	–	–	–	–	–
U0_RTS#	Z	1	1	VO	–	–	–	–	–
U1_RXD	–	VI	VI	VI	–	–	–	–	–
U1_TXD	Z	1	1	VO	–	–	–	–	–
U1_CTS#	–	VI	VI	VI	–	–	–	–	–
U1_RTS#	Z	1	1	VO	–	–	–	–	–
TCK	–	VI	VI	VI	–	–	–	–	–
TDI	–	H	H	H	–	–	–	–	–

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Table 13. Functional Pin Mode Behavior (Sheet 4 of 4)

Pin	Boundary Scan High Z	Reset (End Point)	Reset (Central Resource)	Normal	32-Bit SDRAM	PCIX_32BIT#	PCIX_PULLUP#	When only PCI-X Interface Active	When only PCI Express* Interface Active
TDO	–	Z	Z	VO	–	–	–	–	–
TRST#	–	H	H	H	–	–	–	–	–
TMS	–	H	H	H	–	–	–	–	–
P_RST#	–	VI	VI	VI	–	–	–	–	–
WARM_RST#	–	VI	VI	VI	–	–	–	–	–
NC	-/Z	Z/H	Z/H	Z/H	–	–	–	–	–
THERMDA	–	AI	AI	AI	–	–	–	–	–
THERMDC	–	AO	AO	AO	–	–	–	–	–

Notes:

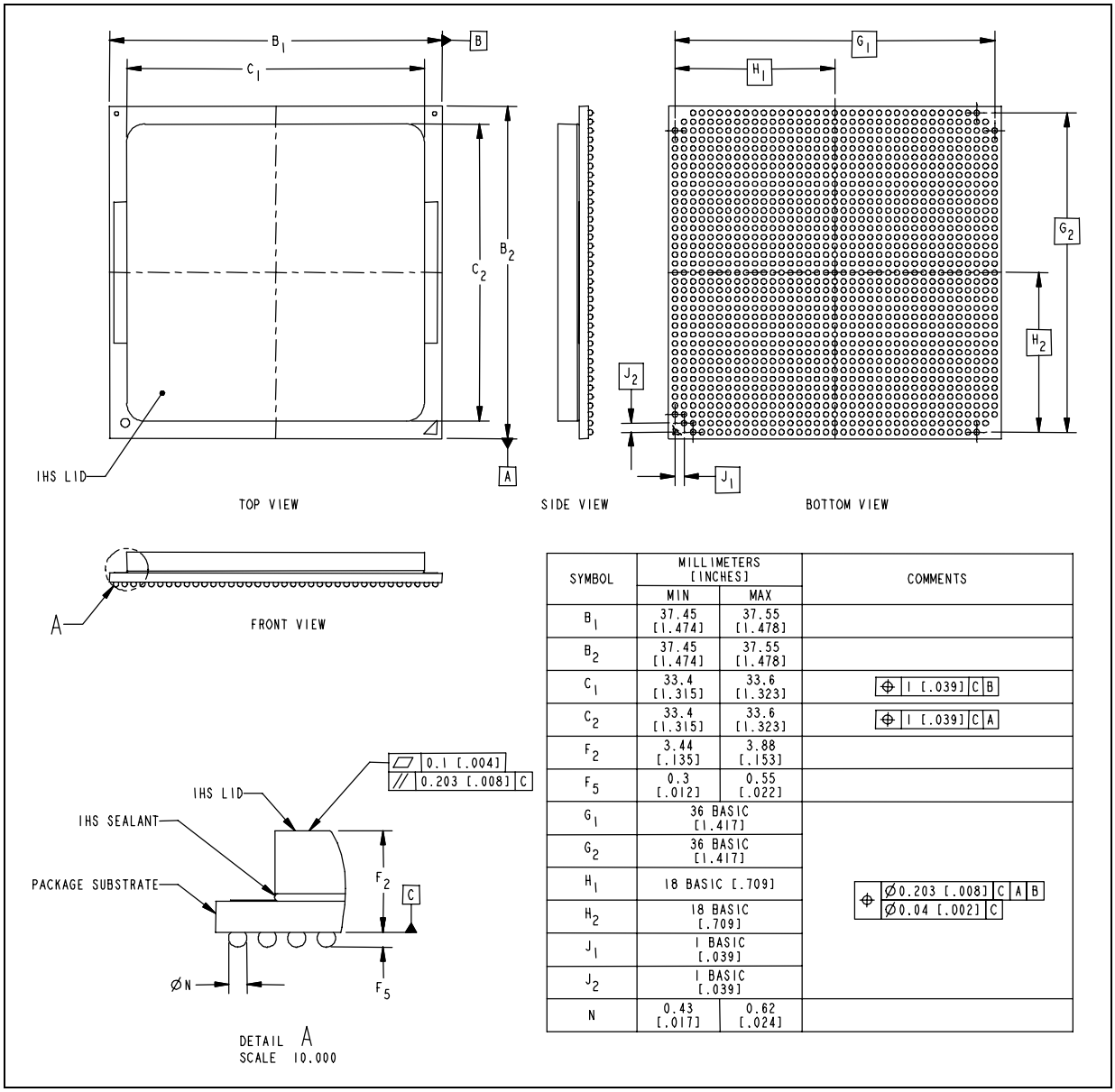
1 = driven to V_{CC}
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X = driven to unknown state
ID = The input is disabled.
H = pulled up to V_{CC}
PD = pull-up disabled
L = pulled down to V_{SS}
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Figure 3. 1357-Lead FCBGA Package (Top and Bottom Views)



SYMBOL	MILLIMETERS [INCHES]		COMMENTS
	MIN	MAX	
B_1	37.45 [1.474]	37.55 [1.478]	
B_2	37.45 [1.474]	37.55 [1.478]	
C_1	33.4 [1.315]	33.6 [1.323]	⌖ | 1 [.039] | C | B
C_2	33.4 [1.315]	33.6 [1.323]	⌖ | 1 [.039] | C | A
F_2	3.44 [.135]	3.88 [.153]	
F_5	0.3 [.012]	0.55 [.022]	
G_1	36 BASIC [1.417]		
G_2	36 BASIC [1.417]		
H_1	18 BASIC [.709]		⌖ | Ø0.203 [.008] | C | A | B Ø0.04 [.002] | C
H_2	18 BASIC [.709]		
J_1	1 BASIC [.039]		
J_2	1 BASIC [.039]		
N	0.43 [.017]	0.62 [.024]	





The following figures show the Intel® 81341 and 81342 I/O processors ballout diagrams:

- Figure 4, "Intel® 81341 and 81342 I/O processors Ballout— Package Top (Left Side)" on page 40
- Figure 5, "Intel® 81341 and 81342 I/O processors Ballout— Package Top (Right Side)" on page 41
- Figure 6, "Intel® 81341 and 81342 I/O processors Ballout — Package Bottom (Left Side)" on page 42
- Figure 7, "Intel® 81341 and 81342 I/O processors Ballout — Package Bottom (Right Side)" on page 43

The following tables show the Intel® 81341 and 81342 I/O processors ball and signal listings:

- Table 14, "Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings" on page 44
- Table 15, "Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings" on page 55

Figure 4. Intel® 81341 and 81342 I/O processors Ballout— Package Top (Left Side)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
37			vss	dq[63]	dqs[7]	dqs#[7]	dq[57]	dq[56]	dq[60]	dq[43]	dq[47]	dqs[5]	dqs#[5]	dq[41]	dq[40]	dq[44]	cb[2]	cb[6]	dqs#[8]
36		vss	dq[59]	dq[58]	dq[62]	vss	dm[7]	dq[61]	vss	vss	dq[42]	dq[46]	vss	dm[5]	dq[45]	vss	cb[3]	cb[7]	dqs[8]
35	vss	nc	dq[51]	dq[50]	dqs[6]	dqs#[6]	dm[6]	dq[53]	dq[52]	dq[35]	dq[34]	dqs[4]	dqs#[4]	dm[4]	dq[37]	dq[36]	m_ck#[2]	vss	dm[8]
34	nc	nc	vss	dq[55]	dq[54]	vss	dq[49]	dq[48]	vss	vss	dq[39]	dq[38]	vss	dq[33]	dq[32]	vss	m_ck[2]	m_ck#[0]	m_ck[0]
33	nc	nc	ma[14][a]	nc	vss	odt[1]	cs#[1]	ma[13]	odt[0]	cas#	we#	vss	cs#[0]	ras#	ba[0]	ma[10]	ba[1]	ma[0]	vss
32	nc	nc	nc	nc	nc	vcc3p3	vcc3p3	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8
31	nc	nc	nc	nc	nc	nc	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
30	nc	vss	nc	vss	nc	nc	vcc3p3	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
29	nc	nc	nc	nc	nc	nc	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vsspllx	thermda	nc
28	nc	nc	nc	nc	nc	nc	vcc3p3	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	thermdc	vcc1p2x
27	nc	vss	nc	vss	nc	nc	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
26	nc	nc	nc	nc	nc	nc	vcc3p3	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
25	nc	nc	nc	nc	nc	nc	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
24	vss	vss	vss	vss	vcc1p2	vcc1p2	vcc1p2	vss	vcc1p2	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
23	nc	nc	nc	nc	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
22	nc	nc	nc	nc	vcc1p2	vcc1p2	vcc1p2	vss	vcc1p2	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
21	vss	vss	vss	vss	nc	nc	nc	vss	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
20	nc	nc	nc	nc	nc	nc	nc	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
19	nc	nc	nc	nc	vcc1p8	vcc1p8	vcc1p8	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
18	vss	vss	vss	vss	vcc1p8	vcc1p8	vcc1p8	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
17	nc	nc	nc	nc	vcc1p2	vss	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
16	nc	nc	nc	nc	nc	nc	nc	vss	vss	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
15	vss	vss	vss	vss	nc	nc	nc	vss	vcc1p2	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
14	nc	nc	nc	nc	vss	vcc1p2	vss	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
13	nc	nc	nc	nc	vcc1p2	vss	vcc1p2	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
12	vss	vss	vss	vss	vss	vcc1p2	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
11	gpio[1]	gpio[3]	gpio[7]	gpio[5]	gpio[6]	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vsspllp	vcc1p2pllp	vss	vcc1p2	vss	vcc1p2	vss
10	gpio[0]	vss	gpio[2]	vss	gpio[4]	vcc3p3	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
9	xint#[1]	xint#[3]	xint#[5]	xint#[4]	xint#[7]	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
8	xint#[2]	xint#[0]	xint#[6]	nmi0#	hs_led_out	vcc3p3	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
7	hs_enum#	vss	hpi#	vss	nmi1.#	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
6	u0_rts#	u0_rxd	hs_lstat	hs_freq[1]	hs_freq[0]	vcc3p3	vcc3p3	vccvio	vcc3p3	vcc3p3	vccvio	vccvio	vcc3p3	vccvio	vcc3p3	vcc3p3	vccvio	vcc3p3	vcc3p3
5	u0_cts#	u0_txd	u1_rxd	nc	vcc3p3	p_cal[0]	p_gnt#[3]	vccvio	p_gnt#[0]	p_ad[31]	vccvio	p_ad[26]	p_idsel	vccvio	p_ad[16]	p_trdy#	vccvio	p_ad[13]	p_ad[9]
4	u1_cts#	u1_txd	u1_rts#	vss	warm_rst#	p_bmi	vss	p_req#[3]	p_gnt#[1]	vss	p_ad[30]	p_ad[24]	vss	p_ad[20]	p_frame#	vss	p_par	p_ad[11]	vss
3	vss	p_clko[3]	p_clko[2]	p_cal[2]	nc	p_cal[1]	p_req#[2]	p_gnt#[2]	nc	p_ad[27]	p_ad[28]	p_ad[23]	p_ad[22]	p_ad[18]	p_devsel#	p_stop#	p_ad[15]	p_ad[12]	p_cbe#[0]
2		vss	p_clko[0]	p_clkout	vss	p_rst#	vss	nc	nc	vss	p_ad[25]	p_ad[21]	vss	p_cbe#[2]	p_pcixcap	vss	p_cbe#[1]	p_ad[10]	vss
1			vss	p_clkin	p_clko[1]	p_rstout#	nc	p_req#[1]	p_req#[0]	p_ad[29]	p_cbe#[3]	p_ad[19]	p_ad[17]	p_irdy#	p_perr#	p_ser#	p_ad[14]	p_m66en	vss
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

a. MA[14] only needed for 4GB memory support, otherwise this pin is NC.

Figure 5. Intel® 81341 and 81342 I/O processors Ballout— Package Top (Right Side)

Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	
cb[1]	cb[0]	dq[27]	dq[31]	dqs[3]	dqs# [3]	dq[25]	dq[24]	dq[28]	dq[11]	dq[15]	dqs[1]	dqs# [1]	dq[9]	dm[1]	vss			37
cb[5]	cb[4]	vss	dq[26]	dq[30]	vss	dm[3]	dq[29]	vss	vss	dq[10]	dq[14]	vss	dq[8]	dq[13]	dq[12]	vss		36
vss	m_ck [1]	dq[19]	dq[18]	dqs[2]	dqs# [2]	dm[2]	dq[21]	dq[20]	dq[3]	dq[2]	dqs[0]	dqs# [0]	dm[0]	dq[5]	dq[4]	m_cal [0]	vss	35
ma[2]	m_ck# [1]	vss	dq[23]	dq[22]	vss	dq[17]	dq[16]	vss	vss	dq[7]	dq[6]	vss	dq[1]	dq[0]	vss	m_cal [1]	vss	34
ma[1]	ma[3]	ma[4]	ma[6]	vss	ma[5]	ma[8]	ma[7]	ma[9]	ma[11]	ma[12]	vss	ba[2]	cke[0]	cke[1]	m_rst#	m_vref	vss	33
vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	vcc1 p8	32
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc3 p3	vcc3 p3	vss	tck	vss	trst#	31
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc3 p3	vcc3 p3	vcc3 p3	tdo	tms	tdi	30
vcc3 p3pllx	vss	vcc1 p2x	vsspll d	vcc1 p2plld	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc3 p3	scl1	sda2	sda1	scl0	smb clk	29
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc3 p3	scl2	vss	sda0	vss	smb dat	28
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	vcc1 p2x	27
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc1 p8e	vcc1 p8e	vcc1 p8e	vcc1 p8e	vcc1 p8e	vcc1 p8e	26
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p8e	vcc1 p8e	vsse	vsse	vsse	vsse	25
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vcc1 p2ae	vcc1 p8e	petn [7]	petp [7]	pem [7]	perp [7]	24
vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p8e	petn [6]	petp [6]	pem [6]	perp [6]	23
vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2x	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2ae	vcc1 p8e	vsse	vsse	vsse	vsse	22
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p8e	petn [5]	petp [5]	pem [5]	perp [5]	21
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	refclkp	nc	nc	pe_ calp	petn [4]	petp [4]	pem [4]	perp [4]	20
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	refclkn	nc	nc	pe_ caln	vsse	vsse	vsse	vsse	19
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2ae	vcc1 p8e	petn [3]	petp [3]	pem [3]	perp [3]	18
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p8e	petn [2]	petp [2]	pem [2]	perp [2]	17
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2ae	vcc1 p2e	vsse	vsse	vsse	vsse	16
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2ae	vcc1 p2e	petn [1]	petp [1]	pem [1]	perp [1]	15
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2e	vcc1 p2e	petn [0]	petp [0]	pem [0]	perp [0]	14
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2e	vcc1 p2e	vsse	vsse	vsse	vsse	13
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	vcc1 p2	12
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc3 p3	pce# [1]	a[21]	a[19]	a[18]	a[22]	11
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc3 p3	a[20]	vss	pce# [0]	vss	a[13]	10
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc3 p3	nc	a[9]	a[12]	a[8]	a[14]	9
vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vcc3 p3	PUR1	a[10]	pb_ rstout#	a[1]	a[6]	8
vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc1 p2	vss	vcc3 p3	a[11]	vss	a[15]	vss	a[2]	7
vccvio	vccvio	vcc3 p3	vccvio	vccvio	vcc3 p3	vccvio	vccvio	vcc3 p3	vccvio	vccvio	vcc3 p3	vcc3 p3	d[15]	a[16]	a[17]	a[3]	a[7]	6
p_ad [4]	vccvio	p_ cbe# [7]	p_ par64	vccvio	p_ad [56]	p_ad [52]	vccvio	p_ad [44]	p_ad [40]	vccvio	p_ad [32]	d[10]	vcc3 p3	d[9]	d[4]	a[4]	a[5]	5
p_ad [6]	p_ad [0]	vss	p_ cbe# [5]	p_ad [60]	vss	p_ad [54]	p_ad [48]	vss	p_ad [42]	p_ad [36]	vss	poe#	d[2]	vss	d[3]	d[8]	d[1]	4
p_ad [5]	p_ad [2]	p_ req64#	p_ad [63]	p_ad [62]	p_ad [58]	p_ad [51]	p_ad [50]	p_ad [46]	p_ad [39]	p_ad [38]	p_ad [34]	pwe#	d[12]	d[11]	a[23]	d[0]	vss	3
p_ad [7]	p_ad [1]	vss	p_ cbe# [4]	p_ad [59]	vss	p_ad [53]	p_ad [47]	vss	p_ad [41]	p_ad [35]	vss	d[14]	d[6]	d[5]	a[0]	vss		2
p_ad [8]	p_ad [3]	p_ ack64#	p_ cbe# [6]	p_ad [61]	p_ad [57]	p_ad [55]	p_ad [49]	p_ad [45]	p_ad [43]	p_ad [37]	p_ad [33]	a[24]	d[7]	d[13]	vss			1
Y	AA	AB	AC	AD	AE	AF	AG	AH	AJ	AK	AL	AM	AN	AP	AR	AT	AU	

Figure 6. Intel® 81341 and 81342 I/O processors Ballout — Package Bottom (Left Side)

	AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W
37			vss	dm[1]	dq[9]	dqs#[1]	dqs[1]	dq[15]	dq[11]	dq[28]	dq[24]	dq[25]	dqs#[3]	dqs[3]	dq[31]	dq[27]	cb[0]	cb[1]	dqs#[8]
36		vss	dq[12]	dq[13]	dq[8]	vss	dq[14]	dq[10]	vss	vss	dq[29]	dm[3]	vss	dq[30]	dq[26]	vss	cb[4]	cb[5]	dqs[8]
35	vss	m_cal[0]	dq[4]	dq[5]	dm[0]	dqs#[0]	dqs[0]	dq[2]	dq[3]	dq[20]	dq[21]	dm[2]	dqs#[2]	dqs[2]	dq[18]	dq[19]	m_ck[1]	vss	dm[8]
34	vss	m_cal[1]	vss	dq[0]	dq[1]	vss	dq[6]	dq[7]	vss	vss	dq[16]	dq[17]	vss	dq[22]	dq[23]	vss	m_ck#[1]	ma[2]	m_ck[0]
33	vss	m_vref	m_rst#	cke[1]	cke[0]	ba[2]	vss	ma[12]	ma[11]	ma[9]	ma[7]	ma[8]	ma[5]	vss	ma[6]	ma[4]	ma[3]	ma[1]	vss
32	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8
31	trst#	vss	tck	vss	vcc3p3	vcc3p3	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
30	tdi	tms	tdo	vcc3p3	vcc3p3	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
29	smbclk	scl0	sda1	sda2	scl1	vcc3p3	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2plld	vssplld	vcc1p2x	vss	vcc3p3pllx	nc
28	smbdat	vss	sda0	vss	scl2	vcc3p3	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
27	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
26	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p8e	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
25	vsse	vsse	vsse	vsse	vcc1p8e	vcc1p8e	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
24	perp[7]	pern[7]	petp[7]	petn[7]	vcc1p8e	vcc1p2ae	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
23	perp[6]	pern[6]	petp[6]	petn[6]	vcc1p8e	vcc1p2ae	vss	vcc1p2	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss
22	vsse	vsse	vsse	vsse	vcc1p8e	vcc1p2ae	vcc1p2	vss	vcc1p2	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x
21	perp[5]	pern[5]	petp[5]	petn[5]	vcc1p8e	vcc1p2ae	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
20	perp[4]	pern[4]	petp[4]	petn[4]	pe_calp	nc	nc	refclkp	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
19	vsse	vsse	vsse	vsse	pe_caln	nc	nc	refclkn	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
18	perp[3]	pern[3]	petp[3]	petn[3]	vcc1p8e	vcc1p2ae	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
17	perp[2]	pern[2]	petp[2]	petn[2]	vcc1p8e	vcc1p2ae	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
16	vsse	vsse	vsse	vsse	vcc1p2e	vcc1p2ae	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
15	perp[1]	pern[1]	petp[1]	petn[1]	vcc1p2e	vcc1p2ae	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
14	perp[0]	pern[0]	petp[0]	petn[0]	vcc1p2e	vcc1p2e	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
13	vsse	vsse	vsse	vsse	vcc1p2e	vcc1p2e	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
12	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
11	a[22]	a[18]	a[19]	a[21]	pce#[1]	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
10	a[13]	vss	pce#[0]	vss	a[20]	vcc3p3	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
9	a[14]	a[8]	a[12]	a[9]	nc	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
8	a[6]	a[1]	pb_rstout#	a[10]	PUR1	vcc3p3	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2
7	a[2]	vss	a[15]	vss	a[11]	vcc3p3	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss
6	a[7]	a[3]	a[17]	a[16]	d[15]	vcc3p3	vcc3p3	vccvio	vccvio	vcc3p3	vccvio	vccvio	vcc3p3	vccvio	vccvio	vcc3p3	vccvio	vccvio	vcc3p3
5	a[5]	a[4]	d[4]	d[9]	vcc3p3	d[10]	p_ad[32]	vccvio	p_ad[40]	p_ad[44]	vccvio	p_ad[52]	p_ad[56]	vccvio	p_par64	p_cbe#[7]	vccvio	p_ad[4]	p_ad[9]
4	d[1]	d[8]	d[3]	vss	d[2]	poe#	vss	p_ad[36]	p_ad[42]	vss	p_ad[48]	p_ad[54]	vss	p_ad[60]	p_cbe#[5]	vss	p_ad[0]	p_ad[6]	vss
3	vss	d[0]	a[23]	d[11]	d[12]	pwe#	p_ad[34]	p_ad[38]	p_ad[39]	p_ad[46]	p_ad[50]	p_ad[51]	p_ad[58]	p_ad[62]	p_ad[63]	p_req64#	p_ad[2]	p_ad[5]	p_cbe#[0]
2		vss	a[0]	d[5]	d[6]	d[14]	vss	p_ad[35]	p_ad[41]	vss	p_ad[47]	p_ad[53]	vss	p_ad[59]	p_cbe#[4]	vss	p_ad[1]	p_ad[7]	vss
1			vss	d[13]	d[7]	a[24]	p_ad[33]	p_ad[37]	p_ad[43]	p_ad[45]	p_ad[49]	p_ad[55]	p_ad[57]	p_ad[61]	p_cbe#[6]	p_ack64#	p_ad[3]	p_ad[8]	vss
	AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W

Figure 7. Intel® 81341 and 81342 I/O processors Ballout — Package Bottom (Right Side)

V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
cb[6]	cb[2]	dq[44]	dq[40]	dq[41]	dqs#[5]	dqs[5]	dq[47]	dq[43]	dq[60]	dq[56]	dq[57]	dqs#[7]	dqs[7]	dq[63]	vss			37
cb[7]	cb[3]	vss	dq[45]	dm[5]	vss	dq[46]	dq[42]	vss	vss	dq[61]	dm[7]	vss	dq[62]	dq[58]	dq[59]	vss		36
vss	m_ck#[2]	dq[36]	dq[37]	dm[4]	dqs#[4]	dqs[4]	dq[34]	dq[35]	dq[52]	dq[53]	dm[6]	dqs#[6]	dqs[6]	dq[50]	dq[51]	nc	vss	35
m_ck#[0]	m_ck[2]	vss	dq[32]	dq[33]	vss	dq[38]	dq[39]	vss	vss	dq[48]	dq[49]	vss	dq[54]	dq[55]	vss	nc	nc	34
ma[0]	ba[1]	ma[10]	ba[0]	ras#	cs#[0]	vss	we#	cas#	odt[0]	ma[13]	cs#[1]	odt[1]	vss	nc	ma[14][a]	nc	nc	33
vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc1p8	vcc3p3	vcc3p3	nc	nc	nc	nc	nc	32
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	nc	nc	nc	nc	nc	nc	31
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc3p3	nc	nc	vss	nc	vss	nc	30
thermda	vsspllx	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	nc	nc	nc	nc	nc	nc	29
thermdc	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc3p3	nc	nc	nc	nc	nc	nc	28
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	nc	nc	vss	nc	vss	nc	27
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc3p3	nc	nc	nc	nc	nc	nc	26
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vcc3p3	nc	nc	nc	nc	nc	nc	25
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2	vss	vcc1p2	vcc1p2	vcc1p2	vss	vss	vss	vss	24
vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2	vcc1p2	vcc1p2	vcc1p2	nc	nc	nc	nc	23
vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2x	vss	vcc1p2	vss	vcc1p2	vcc1p2	vcc1p2	nc	nc	nc	nc	22
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vss	nc	nc	nc	vss	vss	vss	vss	21
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	nc	nc	nc	nc	nc	nc	nc	20
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc1p8	vcc1p8	vcc1p8	nc	nc	nc	nc	19
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p8	vcc1p8	vcc1p8	vss	vss	vss	vss	18
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vss	vcc1p2	nc	nc	nc	nc	17
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vss	vss	nc	nc	nc	nc	nc	nc	nc	16
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc1p2	vss	nc	nc	nc	vss	vss	vss	vss	15
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vss	vcc1p2	vss	nc	nc	nc	nc	14
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc1p2	vss	vcc1p2	nc	nc	nc	nc	13
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc1p2	vss	vss	vss	vss	vss	12
vcc1p2	vss	vcc1p2	vss	vcc1p2pllp	vsspllp	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc3p3	gpio[6]	gpio[5]	gpio[7]	gpio[3]	gpio[1]	11
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc3p3	gpio[4]	vss	gpio[2]	vss	gpio[0]	10
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc3p3	xint#[7]	xint#[4]	xint#[5]	xint#[3]	xint#[1]	9
vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vcc3p3	hs_led_out	nmi0#	xint#[6]	xint#[0]	xint#[2]	8
vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc1p2	vss	vcc3p3	nmi1#	vss	hp#	vss	hs_enum#	7
vcc3p3	vccvio	vcc3p3	vcc3p3	vccvio	vcc3p3	vccvio	vccvio	vcc3p3	vcc3p3	vccvio	vcc3p3	vcc3p3	hs_freq[0]	hs_freq[1]	hs_lstat	u0_rxd	u0_rts#	6
p_ad[13]	vccvio	p_trdy#	p_ad[16]	vccvio	p_idsel	p_ad[26]	vccvio	p_ad[31]	p_gnt#[0]	vccvio	p_gnt#[3]	p_cal[0]	vcc3p3	nc	u1_rxd	u0_txd	u0_cts#	5
p_ad[11]	p_par	vss	p_frame#	p_ad[20]	vss	p_ad[24]	p_ad[30]	vss	p_gnt#[1]	p_req#[3]	vss	p_bmi	warm_rst#	vss	u1_rts#	u1_txd	u1_cts#	4
p_ad[12]	p_ad[15]	p_stop#	p_devsel#	p_ad[18]	p_ad[22]	p_ad[23]	p_ad[28]	p_ad[27]	nc	p_gnt#[2]	p_req#[2]	p_cal[1]	nc	p_cal[2]	p_clko[2]	p_clko[3]	vss	3
p_ad[10]	p_cbe#[1]	vss	p_pcixcap	p_cbe#[2]	vss	p_ad[21]	p_ad[25]	vss	nc	nc	vss	p_rst#	vss	p_clkout	p_clko[0]	vss		2
p_m66en	p_ad[14]	p_serr#	p_perr#	p_irdy#	p_ad[17]	p_ad[19]	p_cbe#[3]	p_ad[29]	p_req#[0]	p_req#[1]	nc	p_rstout#	p_clko[1]	p_clkin	vss			1
V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

a. MA[14] only needed for 4GB memory support, otherwise this pin is NC.

Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 1 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
A1	–	B7	vss	C13	nc
A2	–	B8	xint#[0]	C14	nc
A3	vss	B9	xint#[3]	C15	vss
A4	u1_cts#	B10	vss	C16	nc
A5	u0_cts#	B11	gpio[3]	C17	nc
A6	u0_rts#	B12	vss	C18	vss
A7	hs_enum#	B13	nc	C19	nc
A8	xint#[2]	B14	nc	C20	nc
A9	xint#[1]	B15	vss	C21	vss
A10	gpio[0]	B16	nc	C22	nc
A11	gpio[1]	B17	nc	C23	nc
A12	vss	B18	vss	C24	vss
A13	nc	B19	nc	C25	nc
A14	nc	B20	nc	C26	nc
A15	vss	B21	vss	C27	nc
A16	nc	B22	nc	C28	nc
A17	nc	B23	nc	C29	nc
A18	vss	B24	vss	C30	nc
A19	nc	B25	nc	C31	nc
A20	nc	B26	nc	C32	nc
A21	vss	B27	vss	C33	ma[14][a]
A22	nc	B28	nc	C34	vss
A23	nc	B29	nc	C35	dq[51]
A24	vss	B30	vss	C36	dq[59]
A25	nc	B31	nc	C37	vss
A26	nc	B32	nc	D1	p_clkin
A27	nc	B33	nc	D2	p_clkout
A28	nc	B34	nc	D3	p_cal[2]
A29	nc	B35	nc	D4	vss
A30	nc	B36	vss	D5	nc
A31	nc	B37	–	D6	hs_freq[1]
A32	nc	C1	vss	D7	vss
A33	nc	C2	p_clko[0]	D8	nmi0#
A34	nc	C3	p_clko[2]	D9	xint#[4]
A35	vss	C4	u1_rts#	D10	vss
A36	–	C5	u1_rxd	D11	gpio[5]
A37	–	C6	hs_lstat	D12	vss
B1	–	C7	hpi#	D13	nc
B2	vss	C8	xint#[6]	D14	nc
B3	p_clko[3]	C9	xint#[5]	D15	vss
B4	u1_txd	C10	gpio[2]	D16	nc
B5	u0_txd	C11	gpio[7]	D17	nc
B6	u0_rxd	C12	vss	D18	vss



Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 2 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
D19	nc	E25	nc	F31	nc
D20	nc	E26	nc	F32	vcc3p3
D21	vss	E27	nc	F33	odt[1]
D22	nc	E28	nc	F34	vss
D23	nc	E29	nc	F35	dqs#[6]
D24	vss	E30	nc	F36	vss
D25	nc	E31	nc	F37	dqs#[7]
D26	nc	E32	nc	G1	nc
D27	vss	E33	vss	G2	vss
D28	nc	E34	dq[54]	G3	p_req#[2]
D29	nc	E35	dqs[6]	G4	vss
D30	vss	E36	dq[62]	G5	p_gnt#[3]
D31	nc	E37	dqs[7]	G6	vcc3p3
D32	nc	F1	p_rstout#	G7	vss
D33	nc	F2	p_rst#	G8	vcc1p2
D34	dq[55]	F3	p_cal[1]	G9	vss
D35	dq[50]	F4	p_bmi	G10	vcc1p2
D36	dq[58]	F5	p_cal[0]	G11	vss
D37	dq[63]	F6	vcc3p3	G12	vcc1p2
E1	p_clko[1]	F7	vcc3p3	G13	vcc1p2
E2	vss	F8	vcc3p3	G14	vss
E3	nc	F9	vcc3p3	G15	nc
E4	warm_rst#	F10	vcc3p3	G16	nc
E5	vcc3p3	F11	vcc3p3	G17	vss
E6	hs_freq[0]	F12	vcc1p2	G18	vcc1p8
E7	nmi1#	F13	vss	G19	vcc1p8
E8	hs_led_out	F14	vcc1p2	G20	nc
E9	xint#[7]	F15	nc	G21	nc
E10	gpio[4]	F16	nc	G22	vcc1p2
E11	gpio[6]	F17	vss	G23	vcc1p2
E12	vss	F18	vcc1p8	G24	vcc1p2
E13	vcc1p2	F19	vcc1p8	G25	vcc3p3
E14	vss	F20	nc	G26	vcc3p3
E15	nc	F21	nc	G27	vcc3p3
E16	nc	F22	vcc1p2	G28	vcc3p3
E17	vcc1p2	F23	vcc1p2	G29	vcc3p3
E18	vcc1p8	F24	vcc1p2	G30	vcc3p3
E19	vcc1p8	F25	nc	G31	vcc3p3
E20	nc	F26	nc	G32	vcc3p3
E21	nc	F27	nc	G33	cs#[1]
E22	vcc1p2	F28	nc	G34	dq[49]
E23	vcc1p2	F29	nc	G35	dm[6]
E24	vcc1p2	F30	nc	G36	dm[7]

Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 3 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
G37	dq[57]	J6	vcc3p3	K12	vss
H1	p_req#[1]	J7	vss	K13	vcc1p2
H2	nc	J8	vcc1p2	K14	vss
H3	p_gnt#[2]	J9	vss	K15	vcc1p2
H4	p_req#[3]	J10	vcc1p2	K16	vss
H5	vccvio	J11	vss	K17	vcc1p2
H6	vccvio	J12	vcc1p2	K18	vss
H7	vcc1p2	J13	vss	K19	vcc1p2
H8	vss	J14	vcc1p2	K20	vss
H9	vcc1p2	J15	vcc1p2	K21	vcc1p2
H10	vss	J16	vss	K22	vss
H11	vcc1p2	J17	vss	K23	vcc1p2x
H12	vss	J18	vcc1p2	K24	vss
H13	vcc1p2	J19	vss	K25	vcc1p2x
H14	vss	J20	vcc1p2	K26	vss
H15	vss	J21	vss	K27	vcc1p2x
H16	vss	J22	vcc1p2	K28	vss
H17	vcc1p2	J23	vss	K29	vcc1p2x
H18	vss	J24	vcc1p2	K30	vss
H19	vcc1p2	J25	vss	K31	vcc1p2x
H20	vss	J26	vcc1p2x	K32	vcc1p8
H21	vss	J27	vss	K33	cas#
H22	vss	J28	vcc1p2x	K34	vss
H23	vcc1p2	J29	vss	K35	dq[35]
H24	vss	J30	vcc1p2x	K36	vss
H25	vcc1p2x	J31	vss	K37	dq[43]
H26	vss	J32	vcc1p8	L1	p_cbe#[3]
H27	vcc1p2x	J33	odt[0]	L2	p_ad[25]
H28	vss	J34	vss	L3	p_ad[28]
H29	vcc1p2x	J35	dq[52]	L4	p_ad[30]
H30	vss	J36	vss	L5	vccvio
H31	vcc1p2x	J37	dq[60]	L6	vccvio
H32	vcc1p8	K1	p_ad[29]	L7	vss
H33	ma[13]	K2	vss	L8	vcc1p2
H34	dq[48]	K3	p_ad[27]	L9	vss
H35	dq[53]	K4	vss	L10	vcc1p2
H36	dq[61]	K5	p_ad[31]	L11	vss
H37	dq[56]	K6	vcc3p3	L12	vcc1p2
J1	p_req#[0]	K7	vcc1p2	L13	vss
J2	nc	K8	vss	L14	vcc1p2
J3	nc	K9	vcc1p2	L15	vss
J4	p_gnt#[1]	K10	vss	L16	vcc1p2
J5	p_gnt#[0]	K11	vcc1p2	L17	vss



Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 4 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
L18	vcc1p2	M24	vss	N30	vcc1p2x
L19	vss	M25	vcc1p2x	N31	vss
L20	vcc1p2	M26	vss	N32	vcc1p8
L21	vss	M27	vcc1p2x	N33	cs#[0]
L22	vcc1p2x	M28	vss	N34	vss
L23	vss	M29	vcc1p2x	N35	dqs#[4]
L24	vcc1p2x	M30	vss	N36	vss
L25	vss	M31	vcc1p2x	N37	dqs#[5]
L26	vcc1p2x	M32	vcc1p8	P1	p_irdy#
L27	vss	M33	vss	P2	p_cbe#[2]
L28	vcc1p2x	M34	dq[38]	P3	p_ad[18]
L29	vss	M35	dqs[4]	P4	p_ad[20]
L30	vcc1p2x	M36	dq[46]	P5	vccvio
L31	vss	M37	dqs[5]	P6	vccvio
L32	vcc1p8	N1	p_ad[17]	P7	vcc1p2
L33	we#	N2	vss	P8	vss
L34	dq[39]	N3	p_ad[22]	P9	vcc1p2
L35	dq[34]	N4	vss	P10	vss
L36	dq[42]	N5	p_idsel	P11	vcc1p2pllp
L37	dq[47]	N6	vcc3p3	P12	vss
M1	p_ad[19]	N7	vss	P13	vcc1p2
M2	p_ad[21]	N8	vcc1p2	P14	vss
M3	p_ad[23]	N9	vss	P15	vcc1p2
M4	p_ad[24]	N10	vcc1p2	P16	vss
M5	p_ad[26]	N11	vsspllp	P17	vcc1p2
M6	vccvio	N12	vcc1p2	P18	vss
M7	vcc1p2	N13	vss	P19	vcc1p2
M8	vss	N14	vcc1p2	P20	vss
M9	vcc1p2	N15	vss	P21	vcc1p2
M10	vss	N16	vcc1p2	P22	vss
M11	vcc1p2	N17	vss	P23	vcc1p2x
M12	vss	N18	vcc1p2	P24	vss
M13	vcc1p2	N19	vss	P25	vcc1p2x
M14	vss	N20	vcc1p2	P26	vss
M15	vcc1p2	N21	vss	P27	vcc1p2x
M16	vss	N22	vcc1p2x	P28	vss
M17	vcc1p2	N23	vss	P29	vcc1p2x
M18	vss	N24	vcc1p2x	P30	vss
M19	vcc1p2	N25	vss	P31	vcc1p2x
M20	vss	N26	vcc1p2x	P32	vcc1p8
M21	vcc1p2	N27	vss	P33	ras#
M22	vss	N28	vcc1p2x	P34	dq[33]
M23	vcc1p2x	N29	vss	P35	dm[4]

Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 5 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
P36	dm[5]	T5	p_trdy#	U11	vss
P37	dq[41]	T6	vcc3p3	U12	vcc1p2
R1	p_perr#	T7	vcc1p2	U13	vss
R2	p_pcixcap	T8	vss	U14	vcc1p2
R3	p_devsel#	T9	vcc1p2	U15	vss
R4	p_frame#	T10	vss	U16	vcc1p2
R5	p_ad[16]	T11	vcc1p2	U17	vss
R6	vcc3p3	T12	vss	U18	vcc1p2
R7	vss	T13	vcc1p2	U19	vss
R8	vcc1p2	T14	vss	U20	vcc1p2
R9	vss	T15	vcc1p2	U21	vss
R10	vcc1p2	T16	vss	U22	vcc1p2x
R11	vss	T17	vcc1p2	U23	vss
R12	vcc1p2	T18	vss	U24	vcc1p2x
R13	vss	T19	vcc1p2	U25	vss
R14	vcc1p2	T20	vss	U26	vcc1p2x
R15	vss	T21	vcc1p2	U27	vss
R16	vcc1p2	T22	vss	U28	vcc1p2x
R17	vss	T23	vcc1p2x	U29	vsspllx
R18	vcc1p2	T24	vss	U30	vcc1p2x
R19	vss	T25	vcc1p2x	U31	vss
R20	vcc1p2	T26	vss	U32	vcc1p8
R21	vss	T27	vcc1p2x	U33	ba[1]
R22	vcc1p2x	T28	vss	U34	m_ck[2]
R23	vss	T29	vcc1p2x	U35	m_ck#[2]
R24	vcc1p2x	T30	vss	U36	cb[3]
R25	vss	T31	vcc1p2x	U37	cb[2]
R26	vcc1p2x	T32	vcc1p8	V1	p_m66en
R27	vss	T33	ma[10]	V2	p_ad[10]
R28	vcc1p2x	T34	vss	V3	p_ad[12]
R29	vss	T35	dq[36]	V4	p_ad[11]
R30	vcc1p2x	T36	vss	V5	p_ad[13]
R31	vss	T37	dq[44]	V6	vcc3p3
R32	vcc1p8	U1	p_ad[14]	V7	vcc1p2
R33	ba[0]	U2	p_cbe#[1]	V8	vss
R34	dq[32]	U3	p_ad[15]	V9	vcc1p2
R35	dq[37]	U4	p_par	V10	vss
R36	dq[45]	U5	vccvio	V11	vcc1p2
R37	dq[40]	U6	vccvio	V12	vss
T1	p_serr#	U7	vss	V13	vcc1p2
T2	vss	U8	vcc1p2	V14	vss
T3	p_stop#	U9	vss	V15	vcc1p2
T4	vss	U10	vcc1p2	V16	vss



Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 6 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
V17	vcc1p2	W23	vss	Y29	vcc3p3pllx
V18	vss	W24	vcc1p2x	Y30	vss
V19	vcc1p2	W25	vss	Y31	vcc1p2x
V20	vss	W26	vcc1p2x	Y32	vcc1p8
V21	vcc1p2	W27	vss	Y33	ma[1]
V22	vss	W28	vcc1p2x	Y34	ma[2]
V23	vcc1p2x	W29	nc	Y35	vss
V24	vss	W30	vcc1p2x	Y36	cb[5]
V25	vcc1p2x	W31	vss	Y37	cb[1]
V26	vss	W32	vcc1p8	AA1	p_ad[3]
V27	vcc1p2x	W33	vss	AA2	p_ad[1]
V28	thermdc	W34	m_ck[0]	AA3	p_ad[2]
V29	thermda	W35	dm[8]	AA4	p_ad[0]
V30	vss	W36	dqs[8]	AA5	vccvio
V31	vcc1p2x	W37	dqs#[8]	AA6	vccvio
V32	vcc1p8	Y1	p_ad[8]	AA7	vss
V33	ma[0]	Y2	p_ad[7]	AA8	vcc1p2
V34	m_ck#[0]	Y3	p_ad[5]	AA9	vss
V35	vss	Y4	p_ad[6]	AA10	vcc1p2
V36	cb[7]	Y5	p_ad[4]	AA11	vss
V37	cb[6]	Y6	vccvio	AA12	vcc1p2
W1	vss	Y7	vcc1p2	AA13	vss
W2	vss	Y8	vss	AA14	vcc1p2
W3	p_cbe#[0]	Y9	vcc1p2	AA15	vss
W4	vss	Y10	vss	AA16	vcc1p2
W5	p_ad[9]	Y11	vcc1p2	AA17	vss
W6	vcc3p3	Y12	vss	AA18	vcc1p2
W7	vss	Y13	vcc1p2	AA19	vss
W8	vcc1p2	Y14	vss	AA20	vcc1p2
W9	vss	Y15	vcc1p2	AA21	vss
W10	vcc1p2	Y16	vss	AA22	vcc1p2x
W11	vss	Y17	vcc1p2	AA23	vss
W12	vcc1p2	Y18	vss	AA24	vcc1p2x
W13	vss	Y19	vcc1p2	AA25	vss
W14	vcc1p2	Y20	vss	AA26	vcc1p2x
W15	vss	Y21	vcc1p2	AA27	vss
W16	vcc1p2	Y22	vss	AA28	vcc1p2x
W17	vss	Y23	vcc1p2x	AA29	vss
W18	vcc1p2	Y24	vss	AA30	vcc1p2x
W19	vss	Y25	vcc1p2x	AA31	vss
W20	vcc1p2	Y26	vss	AA32	vcc1p8
W21	vss	Y27	vcc1p2x	AA33	ma[3]
W22	vcc1p2x	Y28	vss	AA34	m_ck#[1]

Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 7 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AA35	m_ck[1]	AC4	p_cbe#[5]	AD10	vss
AA36	cb[4]	AC5	p_par64	AD11	vcc1p2
AA37	cb[0]	AC6	vccvio	AD12	vss
AB1	p_ack64#	AC7	vss	AD13	vcc1p2
AB2	vss	AC8	vcc1p2	AD14	vss
AB3	p_req64#	AC9	vss	AD15	vcc1p2
AB4	vss	AC10	vcc1p2	AD16	vss
AB5	p_cbe#[7]	AC11	vss	AD17	vcc1p2
AB6	vcc3p3	AC12	vcc1p2	AD18	vss
AB7	vcc1p2	AC13	vss	AD19	vcc1p2
AB8	vss	AC14	vcc1p2	AD20	vss
AB9	vcc1p2	AC15	vss	AD21	vcc1p2
AB10	vss	AC16	vcc1p2	AD22	vss
AB11	vcc1p2	AC17	vss	AD23	vcc1p2x
AB12	vss	AC18	vcc1p2	AD24	vss
AB13	vcc1p2	AC19	vss	AD25	vcc1p2x
AB14	vss	AC20	vcc1p2	AD26	vss
AB15	vcc1p2	AC21	vss	AD27	vcc1p2x
AB16	vss	AC22	vcc1p2x	AD28	vss
AB17	vcc1p2	AC23	vss	AD29	vcc1p2plld
AB18	vss	AC24	vcc1p2x	AD30	vss
AB19	vcc1p2	AC25	vss	AD31	vcc1p2x
AB20	vss	AC26	vcc1p2x	AD32	vcc1p8
AB21	vcc1p2	AC27	vss	AD33	vss
AB22	vss	AC28	vcc1p2x	AD34	dq[22]
AB23	vcc1p2x	AC29	vssplld	AD35	dqs[2]
AB24	vss	AC30	vcc1p2x	AD36	dq[30]
AB25	vcc1p2x	AC31	vss	AD37	dqs[3]
AB26	vss	AC32	vcc1p8	AE1	p_ad[57]
AB27	vcc1p2x	AC33	ma[6]	AE2	vss
AB28	vss	AC34	dq[23]	AE3	p_ad[58]
AB29	vcc1p2x	AC35	dq[18]	AE4	vss
AB30	vss	AC36	dq[26]	AE5	p_ad[56]
AB31	vcc1p2x	AC37	dq[31]	AE6	vcc3p3
AB32	vcc1p8	AD1	p_ad[61]	AE7	vss
AB33	ma[4]	AD2	p_ad[59]	AE8	vcc1p2
AB34	vss	AD3	p_ad[62]	AE9	vss
AB35	dq[19]	AD4	p_ad[60]	AE10	vcc1p2
AB36	vss	AD5	vccvio	AE11	vss
AB37	dq[27]	AD6	vccvio	AE12	vcc1p2
AC1	p_cbe#[6]	AD7	vcc1p2	AE13	vss
AC2	p_cbe#[4]	AD8	vss	AE14	vcc1p2
AC3	p_ad[63]	AD9	vcc1p2	AE15	vss



Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 8 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AE16	vcc1p2	AF22	vss	AG28	vcc1p2x
AE17	vss	AF23	vcc1p2x	AG29	vss
AE18	vcc1p2	AF24	vss	AG30	vcc1p2x
AE19	vss	AF25	vcc1p2x	AG31	vss
AE20	vcc1p2	AF26	vss	AG32	vcc1p8
AE21	vss	AF27	vcc1p2x	AG33	ma[7]
AE22	vcc1p2x	AF28	vss	AG34	dq[16]
AE23	vss	AF29	vcc1p2x	AG35	dq[21]
AE24	vcc1p2x	AF30	vss	AG36	dq[29]
AE25	vss	AF31	vcc1p2x	AG37	dq[24]
AE26	vcc1p2x	AF32	vcc1p8	AH1	p_ad[45]
AE27	vss	AF33	ma[8]	AH2	vss
AE28	vcc1p2x	AF34	dq[17]	AH3	p_ad[46]
AE29	vss	AF35	dm[2]	AH4	vss
AE30	vcc1p2x	AF36	dm[3]	AH5	p_ad[44]
AE31	vss	AF37	dq[25]	AH6	vcc3p3
AE32	vcc1p8	AG1	p_ad[49]	AH7	vcc1p2
AE33	ma[5]	AG2	p_ad[47]	AH8	vss
AE34	vss	AG3	p_ad[50]	AH9	vcc1p2
AE35	dqs#[2]	AG4	p_ad[48]	AH10	vss
AE36	vss	AG5	vccvio	AH11	vcc1p2
AE37	dqs#[3]	AG6	vccvio	AH12	vss
AF1	p_ad[55]	AG7	vss	AH13	vcc1p2
AF2	p_ad[53]	AG8	vcc1p2	AH14	vss
AF3	p_ad[51]	AG9	vss	AH15	vcc1p2
AF4	p_ad[54]	AG10	vcc1p2	AH16	vss
AF5	p_ad[52]	AG11	vss	AH17	vcc1p2
AF6	vccvio	AG12	vcc1p2	AH18	vss
AF7	vcc1p2	AG13	vss	AH19	vcc1p2
AF8	vss	AG14	vcc1p2	AH20	vss
AF9	vcc1p2	AG15	vss	AH21	vcc1p2
AF10	vss	AG16	vcc1p2	AH22	vss
AF11	vcc1p2	AG17	vss	AH23	vcc1p2x
AF12	vss	AG18	vcc1p2	AH24	vss
AF13	vcc1p2	AG19	vss	AH25	vcc1p2x
AF14	vss	AG20	vcc1p2	AH26	vss
AF15	vcc1p2	AG21	vss	AH27	vcc1p2x
AF16	vss	AG22	vcc1p2x	AH28	vss
AF17	vcc1p2	AG23	vss	AH29	vcc1p2x
AF18	vss	AG24	vcc1p2x	AH30	vss
AF19	vcc1p2	AG25	vss	AH31	vcc1p2x
AF20	vss	AG26	vcc1p2x	AH32	vcc1p8
AF21	vcc1p2	AG27	vss	AH33	ma[9]

Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 9 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AH34	vss	AK3	p_ad[38]	AL9	vss
AH35	dq[20]	AK4	p_ad[36]	AL10	vcc1p2
AH36	vss	AK5	vccvio	AL11	vss
AH37	dq[28]	AK6	vccvio	AL12	vcc1p2
AJ1	p_ad[43]	AK7	vcc1p2	AL13	vss
AJ2	p_ad[41]	AK8	vss	AL14	vcc1p2
AJ3	p_ad[39]	AK9	vcc1p2	AL15	vss
AJ4	p_ad[42]	AK10	vss	AL16	vcc1p2
AJ5	p_ad[40]	AK11	vcc1p2	AL17	vss
AJ6	vccvio	AK12	vss	AL18	vcc1p2
AJ7	vss	AK13	vcc1p2	AL19	nc
AJ8	vcc1p2	AK14	vss	AL20	nc
AJ9	vss	AK15	vcc1p2	AL21	vss
AJ10	vcc1p2	AK16	vss	AL22	vcc1p2
AJ11	vss	AK17	vcc1p2	AL23	vss
AJ12	vcc1p2	AK18	vss	AL24	vcc1p2x
AJ13	vss	AK19	refclkn	AL25	vss
AJ14	vcc1p2	AK20	refclkp	AL26	vcc1p2x
AJ15	vss	AK21	vcc1p2	AL27	vcc1p2x
AJ16	vcc1p2	AK22	vss	AL28	vcc1p2x
AJ17	vss	AK23	vcc1p2	AL29	vss
AJ18	vcc1p2	AK24	vss	AL30	vcc1p2x
AJ19	vss	AK25	vcc1p2x	AL31	vss
AJ20	vcc1p2	AK26	vss	AL32	vcc1p8
AJ21	vss	AK27	vcc1p2x	AL33	vss
AJ22	vcc1p2	AK28	vss	AL34	dq[6]
AJ23	vss	AK29	vcc1p2x	AL35	dqs[0]
AJ24	vcc1p2x	AK30	vss	AL36	dq[14]
AJ25	vss	AK31	vcc1p2x	AL37	dqs[1]
AJ26	vcc1p2x	AK32	vcc1p8	AM1	a[24]
AJ27	vcc1p2x	AK33	ma[12]	AM2	d[14]
AJ28	vcc1p2x	AK34	dq[7]	AM3	pwe#
AJ29	vss	AK35	dq[2]	AM4	poe#
AJ30	vcc1p2x	AK36	dq[10]	AM5	d[10]
AJ31	vss	AK37	dq[15]	AM6	vcc3p3
AJ32	vcc1p8	AL1	p_ad[33]	AM7	vcc3p3
AJ33	ma[11]	AL2	vss	AM8	vcc3p3
AJ34	vss	AL3	p_ad[34]	AM9	vcc3p3
AJ35	dq[3]	AL4	vss	AM10	vcc3p3
AJ36	vss	AL5	p_ad[32]	AM11	vcc3p3
AJ37	dq[11]	AL6	vcc3p3	AM12	vcc1p2
AK1	p_ad[37]	AL7	vss	AM13	vcc1p2e
AK2	p_ad[35]	AL8	vcc1p2	AM14	vcc1p2e



Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 10 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AM15	vcc1p2ae	AN21	vcc1p8e	AP27	vcc1p2x
AM16	vcc1p2ae	AN22	vcc1p8e	AP28	vss
AM17	vcc1p2ae	AN23	vcc1p8e	AP29	sda2
AM18	vcc1p2ae	AN24	vcc1p8e	AP30	vcc3p3
AM19	nc	AN25	vcc1p8e	AP31	vss
AM20	nc	AN26	vcc1p8e	AP32	vcc1p8
AM21	vcc1p2ae	AN27	vcc1p2x	AP33	cke[1]
AM22	vcc1p2ae	AN28	scl2	AP34	dq[0]
AM23	vcc1p2ae	AN29	scl1	AP35	dq[5]
AM24	vcc1p2ae	AN30	vcc3p3	AP36	dq[13]
AM25	vcc1p8e	AN31	vcc3p3	AP37	dm[1]
AM26	vcc1p8e	AN32	vcc1p8	AR1	vss
AM27	vcc1p2x	AN33	cke[0]	AR2	a[0]
AM28	vcc3p3	AN34	dq[1]	AR3	a[23]
AM29	vcc3p3	AN35	dm[0]	AR4	d[3]
AM30	vcc3p3	AN36	dq[8]	AR5	d[4]
AM31	vcc3p3	AN37	dq[9]	AR6	a[17]
AM32	vcc1p8	AP1	d[13]	AR7	a[15]
AM33	ba[2]	AP2	d[5]	AR8	pb_rstout#
AM34	vss	AP3	d[11]	AR9	a[12]
AM35	dqs#[0]	AP4	vss	AR10	pce#[0]
AM36	vss	AP5	d[9]	AR11	a[19]
AM37	dqs#[1]	AP6	a[16]	AR12	vcc1p2
AN1	d[7]	AP7	vss	AR13	vsse
AN2	d[6]	AP8	a[10]	AR14	petp[0]
AN3	d[12]	AP9	a[9]	AR15	petp[1]
AN4	d[2]	AP10	vss	AR16	vsse
AN5	vcc3p3	AP11	a[21]	AR17	petp[2]
AN6	d[15]	AP12	vcc1p2	AR18	petp[3]
AN7	a[11]	AP13	vsse	AR19	vsse
AN8	PUR1	AP14	petn[0]	AR20	petp[4]
AN9	nc	AP15	petn[1]	AR21	petp[5]
AN10	a[20]	AP16	vsse	AR22	vsse
AN11	pce#[1]	AP17	petn[2]	AR23	petp[6]
AN12	vcc1p2	AP18	petn[3]	AR24	petp[7]
AN13	vcc1p2e	AP19	vsse	AR25	vsse
AN14	vcc1p2e	AP20	petn[4]	AR26	vcc1p8e
AN15	vcc1p2e	AP21	petn[5]	AR27	vcc1p2x
AN16	vcc1p2e	AP22	vsse	AR28	sda0
AN17	vcc1p8e	AP23	petn[6]	AR29	sda1
AN18	vcc1p8e	AP24	petn[7]	AR30	tdo
AN19	pe_caln	AP25	vsse	AR31	tck
AN20	pe_calp	AP26	vcc1p8e	AR32	vcc1p8

Table 14. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Ball Listings (Sheet 11 of 11)

Ball	Signal	Ball	Signal	Ball	Signal
AR33	m_rst#	AT23	pern[6]	AU13	vsse
AR34	vss	AT24	pern[7]	AU14	perp[0]
AR35	dq[4]	AT25	vsse	AU15	perp[1]
AR36	dq[12]	AT26	vcc1p8e	AU16	vsse
AR37	vss	AT27	vcc1p2x	AU17	perp[2]
AT1	–	AT28	vss	AU18	perp[3]
AT2	vss	AT29	scl0	AU19	vsse
AT3	d[0]	AT30	tms	AU20	perp[4]
AT4	d[8]	AT31	vss	AU21	perp[5]
AT5	a[4]	AT32	vcc1p8	AU22	vsse
AT6	a[3]	AT33	m_vref	AU23	perp[6]
AT7	vss	AT34	m_cal[1]	AU24	perp[7]
AT8	a[1]	AT35	m_cal[0]	AU25	vsse
AT9	a[8]	AT36	vss	AU26	vcc1p8e
AT10	vss	AT37	–	AU27	vcc1p2x
AT11	a[18]	AU1	–	AU28	smbdat
AT12	vcc1p2	AU2	–	AU29	smbclk
AT13	vsse	AU3	vss	AU30	tdi
AT14	pern[0]	AU4	d[1]	AU31	trst#
AT15	pern[1]	AU5	a[5]	AU32	vcc1p8
AT16	vsse	AU6	a[7]	AU33	vss
AT17	pern[2]	AU7	a[2]	AU34	vss
AT18	pern[3]	AU8	a[6]	AU35	vss
AT19	vsse	AU9	a[14]	AU36	–
AT20	pern[4]	AU10	a[13]	AU37	–
AT21	pern[5]	AU11	a[22]		
AT22	vsse	AU12	vcc1p2		

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin can be a NC.



Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 1 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
–	A1	cb[2]	U37	dq[8]	AN36
–	A2	cb[3]	U36	dq[9]	AN37
–	A36	cb[4]	AA36	dq[10]	AK36
–	A37	cb[5]	Y36	dq[11]	AJ37
–	B1	cb[6]	V37	dq[12]	AR36
–	B37	cb[7]	V36	dq[13]	AP36
–	AT1	cke[0]	AN33	dq[14]	AL36
–	AT37	cke[1]	AP33	dq[15]	AK37
–	AU1	cs#[0]	N33	dq[16]	AG34
–	AU2	cs#[1]	G33	dq[17]	AF34
–	AU36	d[0]	AT3	dq[18]	AC35
–	AU37	d[1]	AU4	dq[19]	AB35
a[0]	AR2	d[2]	AN4	dq[20]	AH35
a[1]	AT8	d[3]	AR4	dq[21]	AG35
a[2]	AU7	d[4]	AR5	dq[22]	AD34
a[3]	AT6	d[5]	AP2	dq[23]	AC34
a[4]	AT5	d[6]	AN2	dq[24]	AG37
a[5]	AU5	d[7]	AN1	dq[25]	AF37
a[6]	AU8	d[8]	AT4	dq[26]	AC36
a[7]	AU6	d[9]	AP5	dq[27]	AB37
a[8]	AT9	d[10]	AM5	dq[28]	AH37
a[9]	AP9	d[11]	AP3	dq[29]	AG36
a[10]	AP8	d[12]	AN3	dq[30]	AD36
a[11]	AN7	d[13]	AP1	dq[31]	AC37
a[12]	AR9	d[14]	AM2	dq[32]	R34
a[13]	AU10	d[15]	AN6	dq[33]	P34
a[14]	AU9	dm[0]	AN35	dq[34]	L35
a[15]	AR7	dm[1]	AP37	dq[35]	K35
a[16]	AP6	dm[2]	AF35	dq[36]	T35
a[17]	AR6	dm[3]	AF36	dq[37]	R35
a[18]	AT11	dm[4]	P35	dq[38]	M34
a[19]	AR11	dm[5]	P36	dq[39]	L34
a[20]	AN10	dm[6]	G35	dq[40]	R37
a[21]	AP11	dm[7]	G36	dq[41]	P37
a[22]	AU11	dm[8]	W35	dq[42]	L36
a[23]	AR3	dq[0]	AP34	dq[43]	K37
a[24]	AM1	dq[1]	AN34	dq[44]	T37
ba[0]	R33	dq[2]	AK35	dq[45]	R36
ba[1]	U33	dq[3]	AJ35	dq[46]	M36
ba[2]	AM33	dq[4]	AR35	dq[47]	L37
cas#	K33	dq[5]	AP35	dq[48]	H34
cb[0]	AA37	dq[6]	AL34	dq[49]	G34
cb[1]	Y37	dq[7]	AK34	dq[50]	D35

Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 2 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
dq[51]	C35	hs_led_out	E8	nc	A34
dq[52]	J35	hs_lstat	C6	nc	B13
dq[53]	H35	m_cal[0]	AT35	nc	B14
dq[54]	E34	m_cal[1]	AT34	nc	B16
dq[55]	D34	m_ck#[0]	V34	nc	B17
dq[56]	H37	m_ck#[1]	AA34	nc	B19
dq[57]	G37	m_ck#[2]	U35	nc	B20
dq[58]	D36	m_ck[0]	W34	nc	B22
dq[59]	C36	m_ck[1]	AA35	nc	B23
dq[60]	J37	m_ck[2]	U34	nc	B25
dq[61]	H36	m_rst#	AR33	nc	B26
dq[62]	E36	m_vref	AT33	nc	B28
dq[63]	D37	ma[0]	V33	nc	B29
dqs#[0]	AM35	ma[1]	Y33	nc	B31
dqs#[1]	AM37	ma[2]	Y34	nc	B32
dqs#[2]	AE35	ma[3]	AA33	nc	B33
dqs#[3]	AE37	ma[4]	AB33	nc	B34
dqs#[4]	N35	ma[5]	AE33	nc	B35
dqs#[5]	N37	ma[6]	AC33	nc	C13
dqs#[6]	F35	ma[7]	AG33	nc	C14
dqs#[7]	F37	ma[8]	AF33	nc	C16
dqs#[8]	W37	ma[9]	AH33	nc	C17
dqs[0]	AL35	ma[10]	T33	nc	C19
dqs[1]	AL37	ma[11]	AJ33	nc	C20
dqs[2]	AD35	ma[12]	AK33	nc	C22
dqs[3]	AD37	ma[13]	H33	nc	C23
dqs[4]	M35	nc	A13	nc	C25
dqs[5]	M37	nc	A14	nc	C26
dqs[6]	E35	nc	A16	nc	C27
dqs[7]	E37	nc	A17	nc	C28
dqs[8]	W36	nc	A19	nc	C29
gpio[0]	A10	nc	A20	nc	C30
gpio[1]	A11	nc	A22	nc	C31
gpio[2]	C10	nc	A23	nc	C32
gpio[3]	B11	nc	A25	ma[14][a]	C33
gpio[4]	E10	nc	A26	nc	D5
gpio[5]	D11	nc	A27	nc	D13
gpio[6]	E11	nc	A28	nc	D14
gpio[7]	C11	nc	A29	nc	D16
hpi#	C7	nc	A30	nc	D17
hs_enum#	A7	nc	A31	nc	D19
hs_freq[0]	E6	nc	A32	nc	D20
hs_freq[1]	D6	nc	A33	nc	D22



Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 3 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
nc	D23	nc	AM19	p_ad[35]	AK2
nc	D25	nc	AM20	p_ad[36]	AK4
nc	D26	nc	AN9	p_ad[37]	AK1
nc	D28	nmi0#	D8	p_ad[38]	AK3
nc	D29	nmi1#	E7	p_ad[39]	AJ3
nc	D31	odt[0]	J33	p_ad[40]	AJ5
nc	D32	odt[1]	F33	p_ad[41]	AJ2
nc	D33	p_ack64#	AB1	p_ad[42]	AJ4
nc	E3	p_ad[0]	AA4	p_ad[43]	AJ1
nc	E15	p_ad[1]	AA2	p_ad[44]	AH5
nc	E16	p_ad[2]	AA3	p_ad[45]	AH1
nc	E20	p_ad[3]	AA1	p_ad[46]	AH3
nc	E21	p_ad[4]	Y5	p_ad[47]	AG2
nc	E25	p_ad[5]	Y3	p_ad[48]	AG4
nc	E26	p_ad[6]	Y4	p_ad[49]	AG1
nc	E27	p_ad[7]	Y2	p_ad[50]	AG3
nc	E28	p_ad[8]	Y1	p_ad[51]	AF3
nc	E29	p_ad[9]	W5	p_ad[52]	AF5
nc	E30	p_ad[10]	V2	p_ad[53]	AF2
nc	E31	p_ad[11]	V4	p_ad[54]	AF4
nc	E32	p_ad[12]	V3	p_ad[55]	AF1
nc	F15	p_ad[13]	V5	p_ad[56]	AE5
nc	F16	p_ad[14]	U1	p_ad[57]	AE1
nc	F20	p_ad[15]	U3	p_ad[58]	AE3
nc	F21	p_ad[16]	R5	p_ad[59]	AD2
nc	F25	p_ad[17]	N1	p_ad[60]	AD4
nc	F26	p_ad[18]	P3	p_ad[61]	AD1
nc	F27	p_ad[19]	M1	p_ad[62]	AD3
nc	F28	p_ad[20]	P4	p_ad[63]	AC3
nc	F29	p_ad[21]	M2	p_bmi	F4
nc	F30	p_ad[22]	N3	p_cal[0]	F5
nc	F31	p_ad[23]	M3	p_cal[1]	F3
nc	G1	p_ad[24]	M4	p_cal[2]	D3
nc	G15	p_ad[25]	L2	p_cbe#[0]	W3
nc	G16	p_ad[26]	M5	p_cbe#[1]	U2
nc	G20	p_ad[27]	K3	p_cbe#[2]	P2
nc	G21	p_ad[28]	L3	p_cbe#[3]	L1
nc	H2	p_ad[29]	K1	p_cbe#[4]	AC2
nc	J2	p_ad[30]	L4	p_cbe#[5]	AC4
nc	J3	p_ad[31]	K5	p_cbe#[6]	AC1
nc	W29	p_ad[32]	AL5	p_cbe#[7]	AB5
nc	AL19	p_ad[33]	AL1	p_clkin	D1
nc	AL20	p_ad[34]	AL3	p_clko[0]	C2

Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 4 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
p_clko[1]	E1	perp[3]	AU18	u0_rxd	B6
p_clko[2]	C3	perp[4]	AU20	u0_txd	B5
p_clko[3]	B3	perp[5]	AU21	u1_cts#	A4
p_clkout	D2	perp[6]	AU23	u1_rts#	C4
p_devsel#	R3	perp[7]	AU24	u1_rxd	C5
p_frame#	R4	petn[0]	AP14	u1_txd	B4
p_gnt#[0]	J5	petn[1]	AP15	vcc1p2	E13
p_gnt#[1]	J4	petn[2]	AP17	vcc1p2	E17
p_gnt#[2]	H3	petn[3]	AP18	vcc1p2	E22
p_gnt#[3]	G5	petn[4]	AP20	vcc1p2	E23
p_idsel	N5	petn[5]	AP21	vcc1p2	E24
p_irdy#	P1	petn[6]	AP23	vcc1p2	F12
p_m66en	V1	petn[7]	AP24	vcc1p2	F14
p_par	U4	petp[0]	AR14	vcc1p2	F22
p_par64	AC5	petp[1]	AR15	vcc1p2	F23
p_pcixcap	R2	petp[2]	AR17	vcc1p2	F24
p_perr#	R1	petp[3]	AR18	vcc1p2	G8
p_req#[0]	J1	petp[4]	AR20	vcc1p2	G10
p_req#[1]	H1	petp[5]	AR21	vcc1p2	G12
p_req#[2]	G3	petp[6]	AR23	vcc1p2	G13
p_req#[3]	H4	petp[7]	AR24	vcc1p2	G22
p_req64#	AB3	poe#	AM4	vcc1p2	G23
p_rst#	F2	pwe#	AM3	vcc1p2	G24
p_rstout#	F1	ras#	P33	vcc1p2	H7
p_serr#	T1	refclkn	AK19	vcc1p2	H9
p_stop#	T3	refclkp	AK20	vcc1p2	H11
p_trdy#	T5	scl0	AT29	vcc1p2	H13
pb_rstout#	AR8	scl1	AN29	vcc1p2	H17
pce#[0]	AR10	scl2	AN28	vcc1p2	H19
pce#[1]	AN11	sda0	AR28	vcc1p2	H23
pe_caln	AN19	sda1	AR29	vcc1p2	J8
pe_calp	AN20	sda2	AP29	vcc1p2	J10
pern[0]	AT14	smbclk	AU29	vcc1p2	J12
pern[1]	AT15	smbdat	AU28	vcc1p2	J14
pern[2]	AT17	tck	AR31	vcc1p2	J15
pern[3]	AT18	tdi	AU30	vcc1p2	J18
pern[4]	AT20	tdo	AR30	vcc1p2	J20
pern[5]	AT21	thermda	V29	vcc1p2	J22
pern[6]	AT23	thermdc	V28	vcc1p2	J24
pern[7]	AT24	tms	AT30	vcc1p2	K7
perp[0]	AU14	trst#	AU31	vcc1p2	K9
perp[1]	AU15	u0_cts#	A5	vcc1p2	K11
perp[2]	AU17	u0_rts#	A6	vcc1p2	K13



Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 5 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc1p2	K15	vcc1p2	T13	vcc1p2	AB9
vcc1p2	K17	vcc1p2	T15	vcc1p2	AB11
vcc1p2	K19	vcc1p2	T17	vcc1p2	AB13
vcc1p2	K21	vcc1p2	T19	vcc1p2	AB15
vcc1p2	L8	vcc1p2	T21	vcc1p2	AB17
vcc1p2	L10	vcc1p2	U8	vcc1p2	AB19
vcc1p2	L12	vcc1p2	U10	vcc1p2	AB21
vcc1p2	L14	vcc1p2	U12	vcc1p2	AC8
vcc1p2	L16	vcc1p2	U14	vcc1p2	AC10
vcc1p2	L18	vcc1p2	U16	vcc1p2	AC12
vcc1p2	L20	vcc1p2	U18	vcc1p2	AC14
vcc1p2	M7	vcc1p2	U20	vcc1p2	AC16
vcc1p2	M9	vcc1p2	V7	vcc1p2	AC18
vcc1p2	M11	vcc1p2	V9	vcc1p2	AC20
vcc1p2	M13	vcc1p2	V11	vcc1p2	AD7
vcc1p2	M15	vcc1p2	V13	vcc1p2	AD9
vcc1p2	M17	vcc1p2	V15	vcc1p2	AD11
vcc1p2	M19	vcc1p2	V17	vcc1p2	AD13
vcc1p2	M21	vcc1p2	V19	vcc1p2	AD15
vcc1p2	N8	vcc1p2	V21	vcc1p2	AD17
vcc1p2	N10	vcc1p2	W8	vcc1p2	AD19
vcc1p2	N12	vcc1p2	W10	vcc1p2	AD21
vcc1p2	N14	vcc1p2	W12	vcc1p2	AE8
vcc1p2	N16	vcc1p2	W14	vcc1p2	AE10
vcc1p2	N18	vcc1p2	W16	vcc1p2	AE12
vcc1p2	N20	vcc1p2	W18	vcc1p2	AE14
vcc1p2	P7	vcc1p2	W20	vcc1p2	AE16
vcc1p2	P9	vcc1p2	Y7	vcc1p2	AE18
vcc1p2	P13	vcc1p2	Y9	vcc1p2	AE20
vcc1p2	P15	vcc1p2	Y11	vcc1p2	AF7
vcc1p2	P17	vcc1p2	Y13	vcc1p2	AF9
vcc1p2	P19	vcc1p2	Y15	vcc1p2	AF11
vcc1p2	P21	vcc1p2	Y17	vcc1p2	AF13
vcc1p2	R8	vcc1p2	Y19	vcc1p2	AF15
vcc1p2	R10	vcc1p2	Y21	vcc1p2	AF17
vcc1p2	R12	vcc1p2	AA8	vcc1p2	AF19
vcc1p2	R14	vcc1p2	AA10	vcc1p2	AF21
vcc1p2	R16	vcc1p2	AA12	vcc1p2	AG8
vcc1p2	R18	vcc1p2	AA14	vcc1p2	AG10
vcc1p2	R20	vcc1p2	AA16	vcc1p2	AG12
vcc1p2	T7	vcc1p2	AA18	vcc1p2	AG14
vcc1p2	T9	vcc1p2	AA20	vcc1p2	AG16
vcc1p2	T11	vcc1p2	AB7	vcc1p2	AG18

Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 6 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc1p2	AG20	vcc1p2ae	AM22	vcc1p2x	R22
vcc1p2	AH7	vcc1p2ae	AM23	vcc1p2x	R24
vcc1p2	AH9	vcc1p2ae	AM24	vcc1p2x	R26
vcc1p2	AH11	vcc1p2e	AM13	vcc1p2x	R28
vcc1p2	AH13	vcc1p2e	AM14	vcc1p2x	R30
vcc1p2	AH15	vcc1p2e	AN13	vcc1p2x	T23
vcc1p2	AH17	vcc1p2e	AN14	vcc1p2x	T25
vcc1p2	AH19	vcc1p2e	AN15	vcc1p2x	T27
vcc1p2	AH21	vcc1p2e	AN16	vcc1p2x	T29
vcc1p2	AJ8	vcc1p2plld	AD29	vcc1p2x	T31
vcc1p2	AJ10	vcc1p2pllp	P11	vcc1p2x	U22
vcc1p2	AJ12	vcc1p2x	H25	vcc1p2x	U24
vcc1p2	AJ14	vcc1p2x	H27	vcc1p2x	U26
vcc1p2	AJ16	vcc1p2x	H29	vcc1p2x	U28
vcc1p2	AJ18	vcc1p2x	H31	vcc1p2x	U30
vcc1p2	AJ20	vcc1p2x	J26	vcc1p2x	V23
vcc1p2	AJ22	vcc1p2x	J28	vcc1p2x	V25
vcc1p2	AK7	vcc1p2x	J30	vcc1p2x	V27
vcc1p2	AK9	vcc1p2x	K23	vcc1p2x	V31
vcc1p2	AK11	vcc1p2x	K25	vcc1p2x	W22
vcc1p2	AK13	vcc1p2x	K27	vcc1p2x	W24
vcc1p2	AK15	vcc1p2x	K29	vcc1p2x	W26
vcc1p2	AK17	vcc1p2x	K31	vcc1p2x	W28
vcc1p2	AK21	vcc1p2x	L22	vcc1p2x	W30
vcc1p2	AK23	vcc1p2x	L24	vcc1p2x	Y23
vcc1p2	AL8	vcc1p2x	L26	vcc1p2x	Y25
vcc1p2	AL10	vcc1p2x	L28	vcc1p2x	Y27
vcc1p2	AL12	vcc1p2x	L30	vcc1p2x	Y31
vcc1p2	AL14	vcc1p2x	M23	vcc1p2x	AA22
vcc1p2	AL16	vcc1p2x	M25	vcc1p2x	AA24
vcc1p2	AL18	vcc1p2x	M27	vcc1p2x	AA26
vcc1p2	AL22	vcc1p2x	M29	vcc1p2x	AA28
vcc1p2	AM12	vcc1p2x	M31	vcc1p2x	AA30
vcc1p2	AN12	vcc1p2x	N22	vcc1p2x	AB23
vcc1p2	AP12	vcc1p2x	N24	vcc1p2x	AB25
vcc1p2	AR12	vcc1p2x	N26	vcc1p2x	AB27
vcc1p2	AT12	vcc1p2x	N28	vcc1p2x	AB29
vcc1p2	AU12	vcc1p2x	N30	vcc1p2x	AB31
vcc1p2ae	AM15	vcc1p2x	P23	vcc1p2x	AC22
vcc1p2ae	AM16	vcc1p2x	P25	vcc1p2x	AC24
vcc1p2ae	AM17	vcc1p2x	P27	vcc1p2x	AC26
vcc1p2ae	AM18	vcc1p2x	P29	vcc1p2x	AC28
vcc1p2ae	AM21	vcc1p2x	P31	vcc1p2x	AC30



Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 7 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc1p2x	AD23	vcc1p2x	AU27	vcc1p8e	AN23
vcc1p2x	AD25	vcc1p8	E18	vcc1p8e	AN24
vcc1p2x	AD27	vcc1p8	E19	vcc1p8e	AN25
vcc1p2x	AD31	vcc1p8	F18	vcc1p8e	AN26
vcc1p2x	AE22	vcc1p8	F19	vcc1p8e	AP26
vcc1p2x	AE24	vcc1p8	G18	vcc1p8e	AR26
vcc1p2x	AE26	vcc1p8	G19	vcc1p8e	AT26
vcc1p2x	AE28	vcc1p8	H32	vcc1p8e	AU26
vcc1p2x	AE30	vcc1p8	J32	vcc3p3	E5
vcc1p2x	AF23	vcc1p8	K32	vcc3p3	F6
vcc1p2x	AF25	vcc1p8	L32	vcc3p3	F7
vcc1p2x	AF27	vcc1p8	M32	vcc3p3	F8
vcc1p2x	AF29	vcc1p8	N32	vcc3p3	F9
vcc1p2x	AF31	vcc1p8	P32	vcc3p3	F10
vcc1p2x	AG22	vcc1p8	R32	vcc3p3	F11
vcc1p2x	AG24	vcc1p8	T32	vcc3p3	F32
vcc1p2x	AG26	vcc1p8	U32	vcc3p3	G6
vcc1p2x	AG28	vcc1p8	V32	vcc3p3	G25
vcc1p2x	AG30	vcc1p8	W32	vcc3p3	G26
vcc1p2x	AH23	vcc1p8	Y32	vcc3p3	G27
vcc1p2x	AH25	vcc1p8	AA32	vcc3p3	G28
vcc1p2x	AH27	vcc1p8	AB32	vcc3p3	G29
vcc1p2x	AH29	vcc1p8	AC32	vcc3p3	G30
vcc1p2x	AH31	vcc1p8	AD32	vcc3p3	G31
vcc1p2x	AJ24	vcc1p8	AE32	vcc3p3	G32
vcc1p2x	AJ26	vcc1p8	AF32	vcc3p3	J6
vcc1p2x	AJ27	vcc1p8	AG32	vcc3p3	K6
vcc1p2x	AJ28	vcc1p8	AH32	vcc3p3	N6
vcc1p2x	AJ30	vcc1p8	AJ32	vcc3p3	R6
vcc1p2x	AK25	vcc1p8	AK32	vcc3p3	T6
vcc1p2x	AK27	vcc1p8	AL32	vcc3p3	V6
vcc1p2x	AK29	vcc1p8	AM32	vcc3p3	W6
vcc1p2x	AK31	vcc1p8	AN32	vcc3p3	AB6
vcc1p2x	AL24	vcc1p8	AP32	vcc3p3	AE6
vcc1p2x	AL26	vcc1p8	AR32	vcc3p3	AH6
vcc1p2x	AL27	vcc1p8	AT32	vcc3p3	AL6
vcc1p2x	AL28	vcc1p8	AU32	vcc3p3	AM6
vcc1p2x	AL30	vcc1p8e	AM25	vcc3p3	AM7
vcc1p2x	AM27	vcc1p8e	AM26	vcc3p3	AM8
vcc1p2x	AN27	vcc1p8e	AN17	vcc3p3	AM9
vcc1p2x	AP27	vcc1p8e	AN18	vcc3p3	AM10
vcc1p2x	AR27	vcc1p8e	AN21	vcc3p3	AM11
vcc1p2x	AT27	vcc1p8e	AN22	vcc3p3	AM28

Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 8 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vcc3p3	AM29	vss	B21	vss	H16
vcc3p3	AM30	vss	B24	vss	H18
vcc3p3	AM31	vss	B27	vss	H20
vcc3p3	AN5	vss	B30	vss	H21
PUR1	AN8	vss	B36	vss	H22
vcc3p3	AN30	vss	C1	vss	H24
vcc3p3	AN31	vss	C12	vss	H26
vcc3p3	AP30	vss	C15	vss	H28
vcc3p3pllx	Y29	vss	C18	vss	H30
vccvio	H5	vss	C21	vss	J7
vccvio	H6	vss	C24	vss	J9
vccvio	L5	vss	C34	vss	J11
vccvio	L6	vss	C37	vss	J13
vccvio	M6	vss	D4	vss	J16
vccvio	P5	vss	D7	vss	J17
vccvio	P6	vss	D10	vss	J19
vccvio	U5	vss	D12	vss	J21
vccvio	U6	vss	D15	vss	J23
vccvio	Y6	vss	D18	vss	J25
vccvio	AA5	vss	D21	vss	J27
vccvio	AA6	vss	D24	vss	J29
vccvio	AC6	vss	D27	vss	J31
vccvio	AD5	vss	D30	vss	J34
vccvio	AD6	vss	E2	vss	J36
vccvio	AF6	vss	E12	vss	K2
vccvio	AG5	vss	E14	vss	K4
vccvio	AG6	vss	E33	vss	K8
vccvio	AJ6	vss	F13	vss	K10
vccvio	AK5	vss	F17	vss	K12
vccvio	AK6	vss	F34	vss	K14
vss	A3	vss	F36	vss	K16
vss	A12	vss	G2	vss	K18
vss	A15	vss	G4	vss	K20
vss	A18	vss	G7	vss	K22
vss	A21	vss	G9	vss	K24
vss	A24	vss	G11	vss	K26
vss	A35	vss	G14	vss	K28
vss	B2	vss	G17	vss	K30
vss	B7	vss	H8	vss	K34
vss	B10	vss	H10	vss	K36
vss	B12	vss	H12	vss	L7
vss	B15	vss	H14	vss	L9
vss	B18	vss	H15	vss	L11



Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 9 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vss	L13	vss	P16	vss	U19
vss	L15	vss	P18	vss	U21
vss	L17	vss	P20	vss	U23
vss	L19	vss	P22	vss	U25
vss	L21	vss	P24	vss	U27
vss	L23	vss	P26	vss	U31
vss	L25	vss	P28	vss	V8
vss	L27	vss	P30	vss	V10
vss	L29	vss	R7	vss	V12
vss	L31	vss	R9	vss	V14
vss	M8	vss	R11	vss	V16
vss	M10	vss	R13	vss	V18
vss	M12	vss	R15	vss	V20
vss	M14	vss	R17	vss	V22
vss	M16	vss	R19	vss	V24
vss	M18	vss	R21	vss	V26
vss	M20	vss	R23	vss	V30
vss	M22	vss	R25	vss	V35
vss	M24	vss	R27	vss	W1
vss	M26	vss	R29	vss	W2
vss	M28	vss	R31	vss	W4
vss	M30	vss	T2	vss	W7
vss	M33	vss	T4	vss	W9
vss	N2	vss	T8	vss	W11
vss	N4	vss	T10	vss	W13
vss	N7	vss	T12	vss	W15
vss	N9	vss	T14	vss	W17
vss	N13	vss	T16	vss	W19
vss	N15	vss	T18	vss	W21
vss	N17	vss	T20	vss	W23
vss	N19	vss	T22	vss	W25
vss	N21	vss	T24	vss	W27
vss	N23	vss	T26	vss	W31
vss	N25	vss	T28	vss	W33
vss	N27	vss	T30	vss	Y8
vss	N29	vss	T34	vss	Y10
vss	N31	vss	T36	vss	Y12
vss	N34	vss	U7	vss	Y14
vss	N36	vss	U9	vss	Y16
vss	P8	vss	U11	vss	Y18
vss	P10	vss	U13	vss	Y20
vss	P12	vss	U15	vss	Y22
vss	P14	vss	U17	vss	Y24

Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 10 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vss	Y26	vss	AC27	vss	AF30
vss	Y28	vss	AC31	vss	AG7
vss	Y30	vss	AD8	vss	AG9
vss	Y35	vss	AD10	vss	AG11
vss	AA7	vss	AD12	vss	AG13
vss	AA9	vss	AD14	vss	AG15
vss	AA11	vss	AD16	vss	AG17
vss	AA13	vss	AD18	vss	AG19
vss	AA15	vss	AD20	vss	AG21
vss	AA17	vss	AD22	vss	AG23
vss	AA19	vss	AD24	vss	AG25
vss	AA21	vss	AD26	vss	AG27
vss	AA23	vss	AD28	vss	AG29
vss	AA25	vss	AD30	vss	AG31
vss	AA27	vss	AD33	vss	AH2
vss	AA29	vss	AE2	vss	AH4
vss	AA31	vss	AE4	vss	AH8
vss	AB2	vss	AE7	vss	AH10
vss	AB4	vss	AE9	vss	AH12
vss	AB8	vss	AE11	vss	AH14
vss	AB10	vss	AE13	vss	AH16
vss	AB12	vss	AE15	vss	AH18
vss	AB14	vss	AE17	vss	AH20
vss	AB16	vss	AE19	vss	AH22
vss	AB18	vss	AE21	vss	AH24
vss	AB20	vss	AE23	vss	AH26
vss	AB22	vss	AE25	vss	AH28
vss	AB24	vss	AE27	vss	AH30
vss	AB26	vss	AE29	vss	AH34
vss	AB28	vss	AE31	vss	AH36
vss	AB30	vss	AE34	vss	AJ7
vss	AB34	vss	AE36	vss	AJ9
vss	AB36	vss	AF8	vss	AJ11
vss	AC7	vss	AF10	vss	AJ13
vss	AC9	vss	AF12	vss	AJ15
vss	AC11	vss	AF14	vss	AJ17
vss	AC13	vss	AF16	vss	AJ19
vss	AC15	vss	AF18	vss	AJ21
vss	AC17	vss	AF20	vss	AJ23
vss	AC19	vss	AF22	vss	AJ25
vss	AC21	vss	AF24	vss	AJ29
vss	AC23	vss	AF26	vss	AJ31
vss	AC25	vss	AF28	vss	AJ34



Table 15. Intel® 81341 and 81342 I/O processors 1357-Lead Package—Alphabetical Signal Listings (Sheet 11 of 11)

Signal	Ball	Signal	Ball	Signal	Ball
vss	AJ36	vss	AM36	vsse	AR22
vss	AK8	vss	AP4	vsse	AR25
vss	AK10	vss	AP7	vsse	AT13
vss	AK12	vss	AP10	vsse	AT16
vss	AK14	vss	AP28	vsse	AT19
vss	AK16	vss	AP31	vsse	AT22
vss	AK18	vss	AR1	vsse	AT25
vss	AK22	vss	AR34	vsse	AU13
vss	AK24	vss	AR37	vsse	AU16
vss	AK26	vss	AT2	vsse	AU19
vss	AK28	vss	AT7	vsse	AU22
vss	AK30	vss	AT10	vsse	AU25
vss	AL2	vss	AT28	vssplld	AC29
vss	AL4	vss	AT31	vsspllp	N11
vss	AL7	vss	AT36	vsspllx	U29
vss	AL9	vss	AU3	warm_rst#	E4
vss	AL11	vss	AU33	we#	L33
vss	AL13	vss	AU34	xint#[0]	B8
vss	AL15	vss	AU35	xint#[1]	A9
vss	AL17	vsse	AP13	xint#[2]	A8
vss	AL21	vsse	AP16	xint#[3]	B9
vss	AL23	vsse	AP19	xint#[4]	D9
vss	AL25	vsse	AP22	xint#[5]	C9
vss	AL29	vsse	AP25	xint#[6]	C8
vss	AL31	vsse	AR13	xint#[7]	E9
vss	AL33	vsse	AR16		
vss	AM34	vsse	AR19		

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin can be a NC.

4.0 Electrical Specifications

Table 16. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage temperature	–10° C to +45° C
Supply voltage V_{CC3P3} wrt. V_{SS}	–0.5 V to +4.1 V
Supply voltage V_{CC1P8E} wrt. V_{SSE}	–0.5 V to +2.5 V
Supply voltage V_{CC1P8} wrt. V_{SS}	–0.5 V to +2.5 V
Supply voltage V_{CCVIO} wrt. V_{SS}	–0.5 V to +4.1 V
Supply voltage V_{CC1P2X} wrt. V_{SS}	–0.5 V to +1.8 V
Supply voltage V_{CC1P2} wrt. V_{SS}	–0.5 V to +1.8 V
Supply voltage $V_{CC1P2AE}$ wrt. V_{SSE}	–0.5 V to +1.8 V
Supply voltage V_{CC1P2E} wrt. V_{SSE}	–0.5 V to +1.8 V
Voltage on any ball wrt. V_{SS}	–0.5 V to V_{CCP} +0.5 V

†**WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Notice: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.



Table 17. Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{CC3P3}	3.3 V supply voltage for PCI-X category 2 signals and general purpose I/Os	3.0	3.6	V	
V_{CC1P8E}	1.8 V supply voltage for PCI Express* interface	1.71	1.89	V	
V_{CC1P8}	1.8 V supply voltage for DDR2 SDRAM memory interface I/Os	1.71	1.89	V	
V_{CCVIO}	3.3 V supply voltage for PCI-X category 1 signals	3.0	3.6	V	
V_{CC1P2X}	1.2 V supply voltage for Intel XScale® processors	1.164	1.236	V	
V_{CC1P2}	1.2 V supply voltage for most digital logic	1.164	1.236	V	
V_{CC1P2E}	1.2 V supply voltage for PCI Express* interface digital logic	1.164	1.236	V	
$V_{CC1P2AE}$	1.2 V supply voltage for PCI Express* interface analog logic	1.164	1.236	V	
$V_{CC1P2PLLP}$	1.2 V supply voltage for PCI-X PLL	1.164	1.236	V	
$V_{CC1P2PLLD}$	1.2 V supply voltage for DDR2 SDRAM PLL processor logic PLL.	1.164	1.236	V	
$V_{CC3P3PLLX}$	3.3 V supply voltage for processor logic PLL	3.0	3.6	V	
M_VREF	Memory I/O reference voltage	$0.49V_{CC1P8}$	$0.51V_{CC1P8}$	V	
T_C	Case temperature under bias	0	100	°C	

4.1 V_{CCPLL} Pin Requirements

To reduce clock jitter, the $V_{CC1P2PLLD}$, $V_{CC1P2PLLP}$, and $V_{CC3P3PLLX}$ balls for the phase-lock loop (PLL) circuits are isolated on the package. The low-pass filters, as shown in the following figures, reduce noise-induced clock jitter and its effects on timing relationships in system design.

This paragraph pertains to the $V_{CC1P2PLLD}$, $V_{CC1P2PLLP}$, $V_{CC3P3PLLX}$ filters. The filter components must be able to handle a DC current of 30 mA. Use a shielded type inductor to minimize magnetic pickup. The total series resistance from the board VCC plane (before the filter) to the VCCPLL ball must be less than 1.5 ohm (including component and trace resistance). The total series resistance from the board VCC plane (before the filter) to the top plate of the capacitor must be greater than 0.35 ohm (including component and trace resistance). The nodes connecting VCCPLL and VSSPLL to the capacitor must be as short as possible (less than 0.1 W). VCCPLL and VSSPLL must be routed close to each other to minimize loop area. The VSSPLL balls must be connected to the filter only and not to any other ground, as shown in Figure 8 and Figure 9. The inductor and capacitor must be placed close to each other. Any discrete resistor must be placed between the VCC board plane and the inductor. If the trace and component resistance is high enough, a discrete resistor might not be required.

The bypass capacitor must be placed as close to the supply pins as possible. The series impedances to both the supply pin and the PCB analog ground plane must be an order of magnitude lower than the ESR and ESL specified for the capacitor.

Figure 8. $V_{CC3P3PLLX}$ Low-Pass Filter

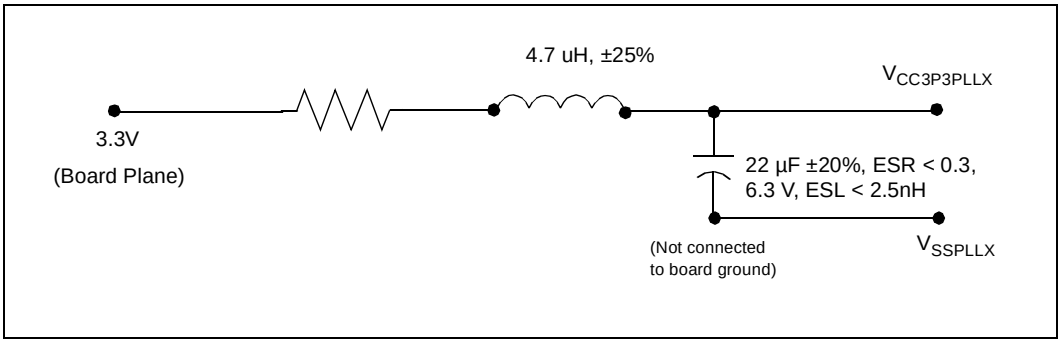
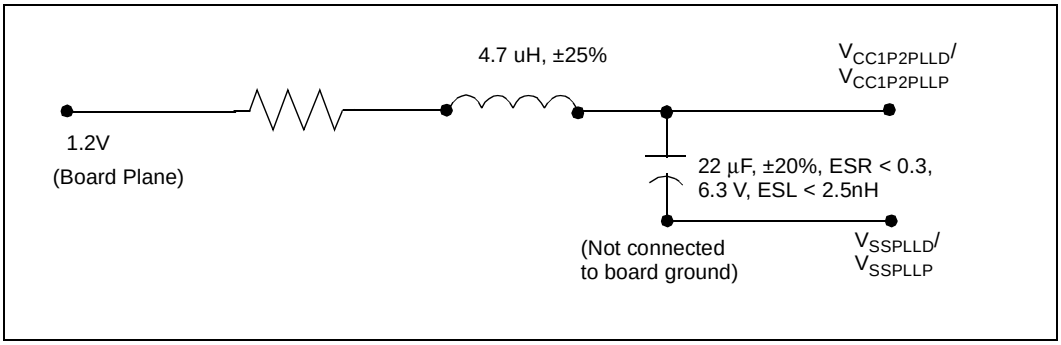


Figure 9. $V_{CC1P2PLLD}$, $V_{CC1P2PLLP}$ Low-Pass Filter



4.2 Targeted DC Specifications

Table 18. DC Characteristics

Symbol	Parameter	Minimum	Maximum	Units	Notes
V_{IL1}	Input Low Voltage (General Purpose).	-0.3	$0.3V_{CC3P3}$	V	2
V_{IH1}	Input High Voltage (General Purpose).	2.0	V_{CC3P3} + 0.3	V	2
V_{IL2}	Input Low Voltage (PCI).	-0.5	$0.3V_{CC3P3}$	V	
V_{IL3}	Input Low Voltage (PCI-X).	-0.5	$0.35V_{CC3P3}$	V	
V_{IH3}	Input High Voltage (PCI-X/PCI).	$0.5V_{CC3P3}$	V_{CC3P3} + 0.5	V	
V_{IL4}	Input Low Voltage (DDR2 SDRAM).	-0.3	**M_VREF** - 0.125	V	
V_{IH4}	Input High Voltage (DDR2 SDRAM).	**M_VREF** + 0.125	V_{CC1P8} + 0.3	V	
V_{OL1}	Output Low Voltage (General Purpose).	–	0.4	V	I_{OL} = 10 mA 2
V_{OH1}	Output High Voltage (General Purpose).	2.6	–	V	I_{OH} = -10 mA 2
V_{OL2}	Output Low Voltage (PCI-X).	–	$0.1V_{CC3P3}$	V	I_{OL} = 1.50 mA
V_{OH2}	Output High Voltage (PCI-X).	$0.9V_{CC3P3}$	–	V	I_{OH} = -0.50 mA
V_{OL3}	Output Low Voltage (DDR2 SDRAM driver set to 21Ω).		0.28	V	I_{OL} = 11 mA
V_{OH3}	Output High Voltage (DDR2 SDRAM driver set to 21Ω).	1.42		V	I_{OH} = -11 mA
V_{OL4}	Output Low Voltage (DDR2 SDRAM driver set to 50Ω).		0.28	V	I_{OL} = 5 mA
V_{OH4}	Output High Voltage (DDR2 SDRAM driver set to 50Ω).	1.42		V	I_{OH} = -5 mA
I_{LI1}	Input Leakage Current for General Purpose pins when internal pull up resistors are not enabled.		±5	µA	$0 \le V_{IN} \le V_{CC3P3}$ 3
I_{LI2}	Input Leakage Current for PCI-X pins when internal pull up resistors are not enabled.		±10	µA	$0 \le V_{IN} \le V_{CC3P3}$ (Cat. 2) $0 \le V_{IN} \le V_{CCVIO}$ (Cat. 1) 3
I_{LI3}	Input Leakage Current for DDR2 pins when internal pull up resistors are not enabled.		±2	µA	$0 \le V_{IN} \le V_{CC1P8}$ 3
R_{GP}	Internal pull up resistor value for General Purpose pins.	28.5	38.7	KΩ	1
R_{PCIX}	Internal pull up resistor value for PCI-X pins.	5.9	8.1	KΩ	1
C_{GP}	General Purpose pin Capacitance.	1	4.5	pF	1
C_{PCIX}	PCI-X pin Capacitance.	1	4.5	pF	1
C_{DDR2}	DDR2 pin Capacitance.	1	4.5	pF	1
L_{PIN}	Ball Inductance.	1	12	nH	1

Notes:
1. Not tested, guaranteed by design.
2. General Purpose signals include all signals that are not part of the DDR2, PCI-X and PCI-Express interfaces and analog pins.
3. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

Table 19. I_{CC} Characteristics

Symbol	Parameter	Typ	Max	Units	Notes
Icc12 Active Two Cores (81342) (Power Supply)	Power Supply Current: • PCI Express A&D • Intel XScale® michroarchitectures - 800MHz - 1200MHz		 6.93 7.69	A	1, 2, 4
Icc12 Active Single Core (81341) (Power Supply)	Power Supply Current: • PCI Express A&D • Intel XScale® michroarchitectures - 800MHz - 1200MHz		 6.53 7.28	A	1, 2, 4
Icc18 Active (Power Supply)	Power Supply Current: • PCI Express I/Os • DDR-II (533)		1.52	A	1, 2, 4
Icc33 Active (Power Supply)	Power Supply Current: • PCI, PBI, GPIO • PCI-X I/Os		0.69	A	1, 2
Icc12 Active Two Cores (81342) (Thermal)	Thermal Current: • PCI Express A&D • Intel XScale® michroarchitecture: 800MHz 1200MHz	 4.82 6.00		A	1, 3, 4
Icc12 Active Single Core (81341) (Thermal)	Thermal Current: • PCI Express A&D • Intel XScale® michroarchitecture: 800MHz 1200MHz	 4.48 5.62		A	1, 3, 4
Icc18 Active (Thermal)	Thermal Current: • PCI Express I/Os • DDR-II (533)	1.31		A	1, 3, 4
Icc33 Active (Thermal)	Thermal Current:: • PCI, PBI, GPIO • PCI-X I/Os	0.58		A	1, 3

Notes:

1. Measured with the device operating and outputs loaded to the test condition in Figure 17, "AC Test Load for all Signals Except PCI, PCI-Express and DDR2" on page 85.
2. Icc Active (Power Supply) value is provided for selecting the system power supply. This is based on the worst case data patterns and skew material at the following worst case voltages: Vcc33 = 3.63 V, Vcc18 = 1.89 V, Vcc12 = 1.24 V and ambient temperature = 55°C.
3. Icc Active (Thermal) value is provided for selecting the system thermal design power (TDP). This is based on the following typical voltages: Vcc33 = 3.3 V, Vcc18 = 1.8 V, Vcc12 = 1.2 V and ambient temperature = 55°C.
4. The Customer Reference Boards use a 1.2 V switching regulator for all the 1.2 V supplies (Vcc1p2, Vcc1p2x, Vcc1p2e, Vcc1p2ae) and a 1.8 V switching regulator for all 1.8 V supplies: (Vcc1p8, Vcc1p8e).



4.3 Targeted AC Specifications

4.3.1 Clock Signal Timings

Table 20. PCI Clock Timings

Symbol	Parameter	PCI-X 133		PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max		
T_{C1}	PCI Clock Cycle Time Jitter Class 1	7.5	11	10	15	15	22	15	25	30	50	ns	1
T_{C2}	PCI Clock Cycle Time Jitter Class 2	7.375	11	9.875	15	14.8	22	14.8	25	29.7	50		1
T_{CH1}	PCI clock High Time	2.5		3		5.5		5.5		10		ns	
T_{CL1}	PCI clock Low Time	2.5		3		5.5		5.5		10		ns	
	PCI clock Period Jitter	125	-125	125	-125	200	-200	200	-200	300	-300	ps	3
T_{SR1}	PCI clock Slew Rate	1.5	4	1.5	4	1.5	4	1.5	4	1	4	V/ns	2
PCI Spread Spectrum Requirements													
f_{mod}	PCI clock modulation frequency	30	33	30	33	30	33	30	33			KHz	
f_{spread}	PCI clock frequency spread	-1	0	-1	0	-1	0	-1	0			%	
PCI Output Clocks													
	PCI output clock skew		250		350		350		350		350	ps	
	PCI output clock period jitter	100	-100	150	-150	150	-150	150	-150	150	-150	ps	4, 5

Notes:
1. The clock frequency may not change beyond the spread-spectrum limits except while **P_RST#** or **WARM_RST#** is asserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
3. Period jitter is the deviation between any single period of the clock and the average period of the clock.
4. If a jitter class 2 input clock is used, output clocks can not support jitter class 1.
5. The deviation between any single period of the clock and the average period of the clock.

Table 21. PCI Express* Clock Timings

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
TF2	PCI Express* Clock Frequency		100		MHz	4
TC2	PCI Express* Clock Cycle Time	9.872			ns	
DF0	Frequency Variation	-300		300	ppm	
TCCJ	Cycle to Cycle Jitter			125	ps	
TPPJ	Peak to Peak Jitter (5–50 MHz)			50	ps	
Dc	Clock Duty Cycle	45		55	%	
Trise	REFCLK Rise Time	175		350	ps	1, 2, 7
Tfall	REFCLK Fall Time	175		350	ps	1, 2, 7
Tvrise	REFCLK Rise Time Variation			125	ps	
Tvfall	REFCLK Fall Time Variation			125	ps	
	Rise-Fall Matching			20	%	
Vca	Absolute Cross Point	0.25		0.55	V	1, 3, 8, 14
Vcr	Relative Cross Point	Calc		Calc		5, 13
Tvc	Total Variation of Vc over all edges			0.14	V	14
	Rising Edge Ringback	0.56			V	Absolute Min.
	Falling Edge Ringback			0.25	V	Absolute Max.
Vhi	High Level Voltage	0.66	0.71	0.85	V	8, 9
Vli	Low Level Voltage	-0.15	0	0.15	V	8, 10
Vrb	Ringback Voltage			0.10	V	8
Vovs	Maximum Overshoot			Vhi+0.3	V	8, 11
Vuds	Minimum Undershoot			-0.30	V	8, 12

Notes:

1. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK equals the falling edge of REFCLK#.
2. Measured from V_{OL} = 0.175 V to V_{OH} = 0.525 V. Valid only for rising REFCLK and falling REFCLK#. Signal must be monotonic through the V_{OL} to V_{OH} region for T_{RISE} and T_{FALL}.
3. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
4. The average period over any 1 µs period of time must be greater than the minimum specified period.
5. V_{CROSS}(rel) Min and Max are derived using the following:
   V_{CROSS}(rel) Min = 0.5 (V_{havg} - 0.710) + 0.250
   V_{CROSS}(rel) Max = 0.5 (V_{havg} - 0.710) + 0.550
6. (see for further clarification).
7. Measurement taken from single-ended waveform.
8. Measurement taken from differential waveform.
9. V_{HIGH} is defined as the statistical average High value as obtained by using the Oscilloscope V_{HIGH} Math function.
10. V_{LOW} is defined as the statistical average Low value as obtained by using the Oscilloscope V_{LOW} Math function.
11. Overshoot is defined as the absolute value of the maximum voltage.
12. Undershoot is defined as the absolute value of the minimum voltage.
13. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
14. ΔV_{CROSS} is defined as the total variation of all crossing voltages of Rising REFCLK and Falling REFCLK#. This is the maximum allowed variance in V_{CROSS} for any particular system.
15. Refer to Section 4.3.2.1 in the *PCI Express Base Specification* for information regarding PPM considerations.



Table 22. DDR2 Output Clock Timings

Symbol	Parameter	DDR2-400		DDR2-533		Units	Notes
		Min.	Max	Min.	Max		
T_{C2}	DDR2 SDRAM clock Cycle Time Average	5.00		3.75		ns	
T_{CH2}	DDR2 SDRAM clock High Time	2.25		1.69		ns	
T_{CL2}	DDR2 SDRAM clock LowTime	2.25		1.69		ns	
T_{CS2}	DDR2 SDRAM clock Period Jitter	100	-100	100	-100	ps	
T_{skew2}	DDR2 SDRAM clock skew for any differential clock pair to any other clock pair		250		250	ps	
T_{skew3}	DDR2 SDRAM clock skew for any clock pair to any system memory strobe		250		250	ps	

4.3.2 DDR2 SDRAM Interface Signal Timings

Table 23. DDR2 SDRAM Signal Timings

Symbol	Parameter	Min.	Max	Units	Notes
Tvb1	DQ, CB and DM write output valid time before DQS	0.530		ns	1, 3
Tva1	DQ, CB and DM write output valid time after DQS	0.530		ns	1, 3
Tvb2	DQS write output valid time before M_CK (DQS early)		0.200	ns	1, 3
Tva2	DQS write output valid time after M_CK (DQS late)		0.530	ns	1, 3
Tvb3	MA, BA, **RAS#**, **CAS#**, **WE#** write output valid before M_CK rising edge.	4.900		ns	1, 3
Tva3	MA, BA, **RAS#**, **CAS#**, **WE#** write output valid after M_CK rising edge.	1.530		ns	1, 3
Tvb4	CS#, CKE, ODT write output valid before M_CK rising edge. Unbuffered mode	2.090		ns	1, 3
Tva4	CS#, CKE, ODT write output valid after M_CK rising edge. Unbuffered mode	0.590		ns	1, 3
Tvb5	CS#, CKE, ODT write output valid before M_CK rising edge. Registered mode	1.150		ns	1, 3
Tva5	CS#, CKE, ODT write output valid after M_CK rising edge. Registered mode	1.530		ns	1, 3
Tis6	DQ, CB read input setup time before DQS rising or falling edges.	-0.670		ns	2
Tih6	DQ, CB read input hold time after DQS rising or falling edges.	1.250		ns	2
Tov7	**M_CK[2:0]** output valid from **P_CLKIN** or REFCLK	0.460	1.930	ns	

Notes:
1. See Figure 14, "DDR2 SDRAM Write Timings" on page 84.
2. See Figure 15, "DQS Falling Edge Output Access Time to/from M_CK Rising Edge" on page 84. Timings valid when the DQS delay is programmed for the default 90 degree phase shift.
3. See Figure 18, "AC Test Load for DDR2 SDRAM Signals" on page 85.



4.3.3 Peripheral Bus Interface Signal Timings

Table 24. Peripheral Bus Interface Signal Timings

Symbol	Parameter	Min.	Nom.	Max.	Units
A2D	Address to Data wait-states	4	-	20	clks
D2D	Data to Data wait-states	4	-	20	clks
REC	Recovery wait-states	1	-	20	clks
N	Number of Data phases	1	-	4	phases
Tasc	Address setup to CE#	25	30	-	ns
Taso	Address setup to OE#	10	15	-	ns
Tasw	Address setup to WE#	25	30	-	ns
Tah	Address hold from CE#,OE#	Nom - 5	REC × 15	-	ns
Tahw	Address hold from WE#	Nom - 5	(REC+1) × 15	-	ns
Twce	CE# pulse width	Nom - 5	(A2D + 2 + ((N - 1)(D2D + 2))) × 15	-	ns
Twoe	OE# pulse width	Nom - 5	(A2D + 3 + ((N - 1)(D2D + 2))) × 15	-	ns
Twwe	WE# pulse width	Nom - 5	(A2D + 1) × 15	-	ns
Tdsw	Write Data setup to WE#	Nom - 5	(A2D + 1) × 15	-	ns
Tdhw	Write Data hold from WE#	10	15	20	ns
Tad1	1st Read Data access time from Address	-	(A2D + 4) × 15	Nom - 11	ns
TadN	Nth Read Data access time from Address	-	(D2D + 2) × 15	Nom - 11	ns
Tcd	Read Data access time from CE#	-	(A2D + 2) × 15	Nom - 11	ns
Toe	Read Data access time from OE#	0	(A2D + 3) × 15	Nom - 11	ns
Tdh	Read Data hold time from Address, CE#, OE#	0	(REC + 2) × 15	Nom - 5	ns

Notes:
1. See Figure 25, "PBI Output Timings" on page 88 and Figure 26, "PBI External Device Timings (Flash)" on page 89.

4.3.4 I²C/SMBus Interface Signal Timings

Table 25. I²C/SMBus Signal Timings

Symbol	Parameter	Std. Mode		Fast Mode		Units	Notes
		Min.	Max	Min.	Max		
FSCL	**SCL** Clock Frequency	0	100	0	400	KHz	
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7		1.3		µs	(1)
T_{HDSTA}	Hold Time (repeated) START Condition	4		0.6		µs	(1,3)
T_{LOW}	**SCL** Clock Low Time	4.7		1.3		µs	(1,2)
THIGH	**SCL** Clock High Time	4		0.6		µs	(1,2)
TSUSTA	Setup Time for a Repeated START Condition	4.7		0.6		µs	(1)
THDDAT	Data Hold Time	0	3.45	0	0.9	µs	(1)
TSUDAT	Data Setup Time	250		100		ns	(1)
T_{SR}	**SCL** and **SDA** Rise Time		1000	$20 + 0.1C_b$	300	ns	(1,4)
T_{SF}	**SCL** and **SDA** Fall Time		300	$20 + 0.1C_b$	300	ns	(1,4)
T_{SUSTO}	Setup Time for STOP Condition	4		0.6		µs	(1)

Notes:
1. See Figure 13, "I2C Interface Signal Timings" on page 83.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.
5. Std Mode I²C signal timings apply for SMBus timing.



4.3.5 PCI Bus Interface Signal Timings

Table 26. PCI Signal Timings

Symbol	Parameter			PCI-X 133 PCI-X 100		PCI-X 66		PCI 66		PCI 33		Units	Notes
				Min.	Max	Min.	Max	Min.	Max	Min.	Max		
T_{OV1}	Clock to Output Valid Delay			0.7	3.7	0.7	3.7	1	6	2	11	ns	1, 3
T_{OF}	Clock to Output Float Delay				7		7		14		28	ns	1, 4
T_{IS1}	Input Setup to clock			1.2		1.7		3		7		ns	2
T_{IH1}	Input Hold time from clock			0.5		0.5		0		0		ns	2
T_{RST}	Reset Active Time			1		1		1		1		ms	
T_{RF}	Reset Active to output float delay				40		40		40		40	ns	
T_{IS3}	REQ64# to Reset setup time			10		10		10		10		clocks	
T_{IH2}	Reset to REQ64# hold time			0	50	0	50	0	50	0	50	ns	
T_{IS4}	PCI-X initialization pattern to Reset setup time			10		10						clocks	
T_{IH3}	Reset to PCI-X initialization pattern hold time			0	50	0	50					ns	

Notes:
1. See the timing measurement conditions in; Figure 11, "Output Timing Measurement Waveforms" on page 82.
2. See the timing measurement conditions in: Figure 12, "Input Timing Measurement Waveforms" on page 83.
3. See Figure 19, "PCI/PCI-X TOV(max) Rising Edge AC Test Load" on page 86,Figure 20, "PCI/PCI-X TOV(max) Falling Edge AC Test Load" on page 86, Figure 21, "PCI/PCI-X TOV(min) AC Test Load" on page 86.
4. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4.3.6 PCI Express* Differential Transmitter (Tx) Output Specifications

Table 27. PCI Express* Rx Input Specifications

Symbol	Parameter	Min.	Nom	Max	Units	Notes
$V_{DIFFp-p}$	Differential input voltage	0.175		1.200	V	1
J_{TOTAL}	Total output jitter			0.65	UI	2
V_{CM-AC}	AC common mode			100	mV	3
T_{Reye}	Receiver eye opening	0.35			UI	4
$RL\text{-}Diff_{RX}$	Differential return loss	12			dB	5
$RL\text{-}CM_{TX}$	Common mode return loss	6			dB	5
$Z_{RX-OUT-DC}$	DC differential output impedance	90	100	110	Ohm	6
$Z_{RX-Match-DC}$	D+/D- impedance matching	-5		+5	%	7
$V_{RX-SQUELCH}$	Squelch detect threshold	75		175	mV	8
Cin_{RX}	AC coupled	75			nf	9
$L_{SKEW-RX}$	Lane to lane skew at Rx			20	UI	10

Notes:

1. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 \times V_{RMAx}$. Measured at the package pins of the receiver. See Figure 12.
2. Max Jitter tolerated by Rx. This is the nominal value tolerated at the package pin of the receiver device. A receiver must therefore tolerate any additional jitter generated by the package to the die.
3. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
4. See Figure 24, "Receiver Eye Opening (Differential)" on page 87.
5. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode (i.e. as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω. Applicable during active (L0) and Align states only.
6. DC Differential Mode Impedance 100 Ω ±10% tolerance.
7. DC impedance matching between two lanes of a port.
8. Peak-to-Peak value. Measured at the pin of the receiver. Differential signal below this level will indicate a squelch condition.
9. All receivers shall be AC coupled to the media.
10. Lane skew at the Receiver that must be tolerated.



Table 28. PCI Express* Tx Output Specifications

Symbol	Parameter	Min.	Nom	Max	Units	Notes
UI	Unit Interval		400		ps	1
$V_{DIFFp-p}$	Differential output voltage	0.800		1.200	V	2
T_{rise}, T_{fall}	Driver Rise/Fall Time	0.2		0.4	UI	3
$V_{TX-CM-AC}$	AC Common Mode			20	mV	4
$V_{TX-CM-DC\ delta}$	Common Mode Active to Sleep mode delta	-50		+50	mV	
$RL\text{-}Diff_{TX}$	Differential Return Loss	15			dB	5
$RL\text{-}CM_{TX}$	Common Mode Return Loss	6			dB	5
$Z_{TX-OUT-DC}$	DC Differential Output Impedance	90	100	110	Ω	6
$Z_{TX-Match-DC}$	D+/D- impedance matching	-5		+5	%	7
$L_{SKEW-TX}$	Lane to Lane Skew at Tx			500	ps	8
J_{TOTAL}	Total Output Jitter.			0.35	UI	9
T_{Deye}	Minimum Transmitter eye opening.	0.65			UI	10
$I_{TX-SHORT}$	Short circuit Current	-100		100	mA	11
$V_{TX-IDLE}$	Sleep mode Voltage Output	0	0	20	mV	12

Notes:

1. ±300 ppm. UI does not account for SSC dictated variations. No test load is necessarily associated with this value. This UI spec is a "before transmission" specification and represents the nominal time of each bit transmission or width.
2. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 \times V_{DMAx}$. Specified at the package pins into a 100 Ω test load as shown in Figure 22, "Transmitter Test Load (100 W diff Load)" on page 86. Max level set by maximum single ended voltage after a reflection from an open. This value is for the first bit after a transition on the data lines. Subsequent bits of the same polarity shall have an amplitude of 6 dB (±0.5 db) less as measured differentially peak to peak than the specified value.
3. 20–80% at transmitter. Slower rise/fall times are better.
4. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
5. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode (i.e. as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω. Applicable during active (L0) and Align states only.
6. DC Differential Mode Impedance 100 Ω ±10% tolerance. All devices shall employ on-chip adaptive impedance matching circuits to ensure the best possible termination/Zout for its Transmitters (as well as receivers).
7. DC impedance matching between two lanes of a port.
8. Between any two lanes within a single transmitter.
9. Clock source PPM mismatch is in addition to this value. Measured over 250 UI.
10. See Figure 23, "Transmitter Eye Diagram" on page 87.
11. Between any voltage from max supply to gnd with power on or off.
12. Squelch condition. Both signals brought to $V_{CM-DC-|VD+ - VD-|}$

4.3.7 PCI Express* Differential Receiver (Rx) Input Specifications

Table 29. PCI Express* Rx Input Specifications

Symbol	Parameter	Min.	Nom	Max	Units	Notes
$V_{DIFFp-p}$	Differential input voltage	0.175		1.200	V	1
J_{TOTAL}	Total Output Jitter.			0.65	UI	2
V_{CM-AC}	AC Common Mode			100	mV	3
T_{Reye}	Receiver eye opening.	0.35			UI	4
RL-$Diff_{RX}$	Differential Return Loss	15			dB	5
RL-CM_{TX}	Common Mode Return Loss	6			dB	5
$Z_{RX-OUT-DC}$	DC Differential Output Impedance	90	100	110	Ω	6
$Z_{RX-Match-DC}$	D+/D- impedance matching	0-5		+5	%	7
$V_{RX-SQUELCH}$	Squelch detect threshold	75		175	mV	8
Cin_{RX}	AC coupled	400			pf	9
$L_{SKEW-RX}$	Lane to Lane Skew at Rx			20	UI	10

Notes:

1. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 * V_{RMAx}$. Measured at the package pins of the receiver. See Figure 12.
2. Max Jitter tolerated by Rx. This is the nominal value tolerated at the package pin of the receiver device. A receiver must therefore tolerate any additional jitter generated by the package to the die.
3. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
4. See Figure 24, "Receiver Eye Opening (Differential)" on page 87.
5. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode (i.e. as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω. Applicable during active (L0) and Align states only.
6. DC Differential Mode Impedance 100 Ω ±10% tolerance.
7. DC impedance matching between two lanes of a port.
8. Peak to Peak value. Measured at the pin of the receiver. Differential signal below this level will indicate a squelch condition.
9. All receivers shall be AC coupled to the media.
10. Lane skew at the Receiver that must be tolerated.



4.3.8 Boundary Scan Test Signal Timings

Table 30. Boundary Scan Test Signal Timings

Symbol	Parameter	Min.	Max	Units	Notes
T_{JTF}	**TCK** Frequency	0	66	MHz	
T_{JTCH}	**TCK** High Time	7.0		ns	Measured at 1.5 V (1)
TJTCL	**TCK** Low Time	7.0		ns	Measured at 1.5 V (1)
T_{JTCR}	**TCK** Rise Time		5	ns	0.8 V to 2.0 V (1)
T_{JTCF}	**TCK** Fall Time		5	ns	2.0 V to 0.8 V (1)
T_{JTIS1}	Input Setup to **TCK**—**TDI**, **TMS**	3.0		ns	(3)
T_{JTIH1}	Input Hold from **TCK**—**TDI**, **TMS**	2.0		ns	(3)
T_{JTOV1}	**TDO** Output Valid Delay	4.25	13.25	ns	Relative to falling edge of **TCK** (2)
T_{OF1}	**TDO** Float Delay	4.25	13.25	ns	Relative to falling edge of **TCK** (4)

Notes:
1. Not tested.
2. See Figure 11, "Output Timing Measurement Waveforms" on page 82.
3. See Figure 12, "Input Timing Measurement Waveforms" on page 83.
4. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 11, "Output Timing Measurement Waveforms" on page 82.

4.4 AC Timing Waveforms

Figure 10. Clock Timing Measurement Waveforms

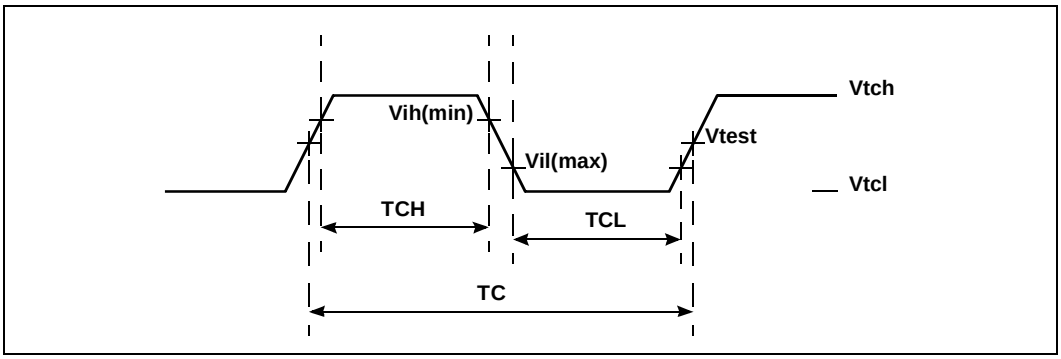


Figure 11. Output Timing Measurement Waveforms

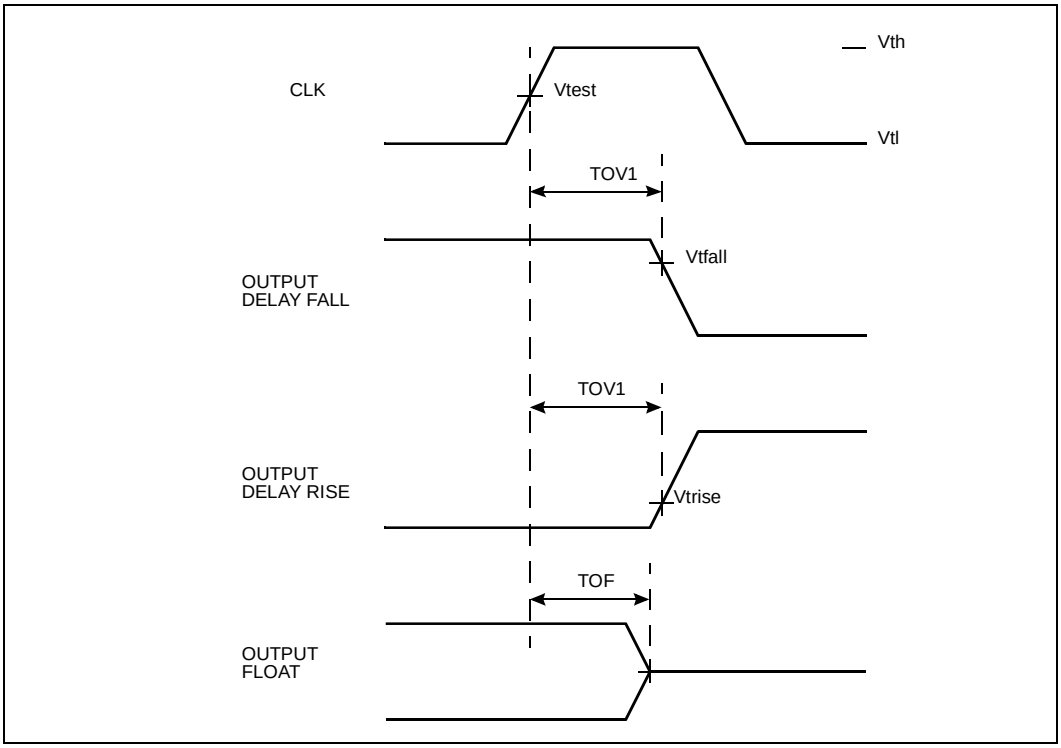


Figure 12. Input Timing Measurement Waveforms

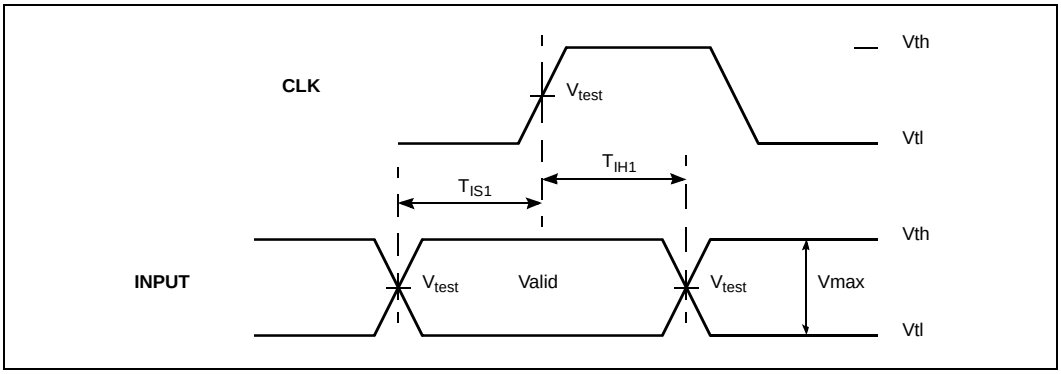


Figure 13. I²C Interface Signal Timings

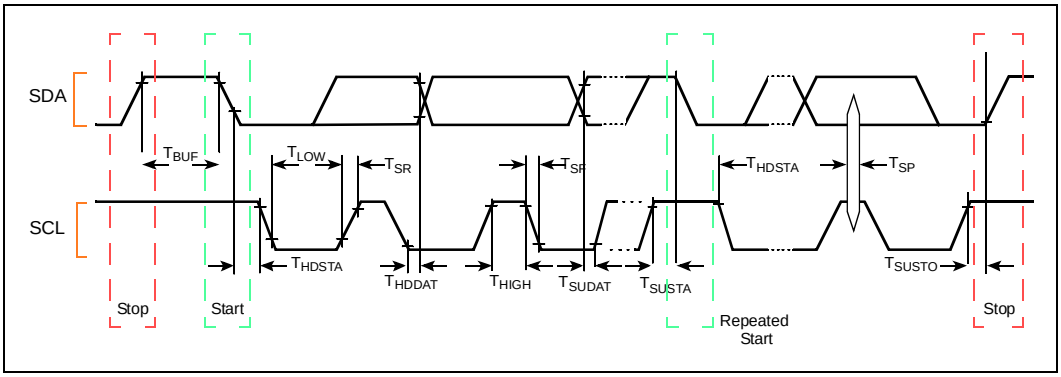


Figure 14. DDR2 SDRAM Write Timings

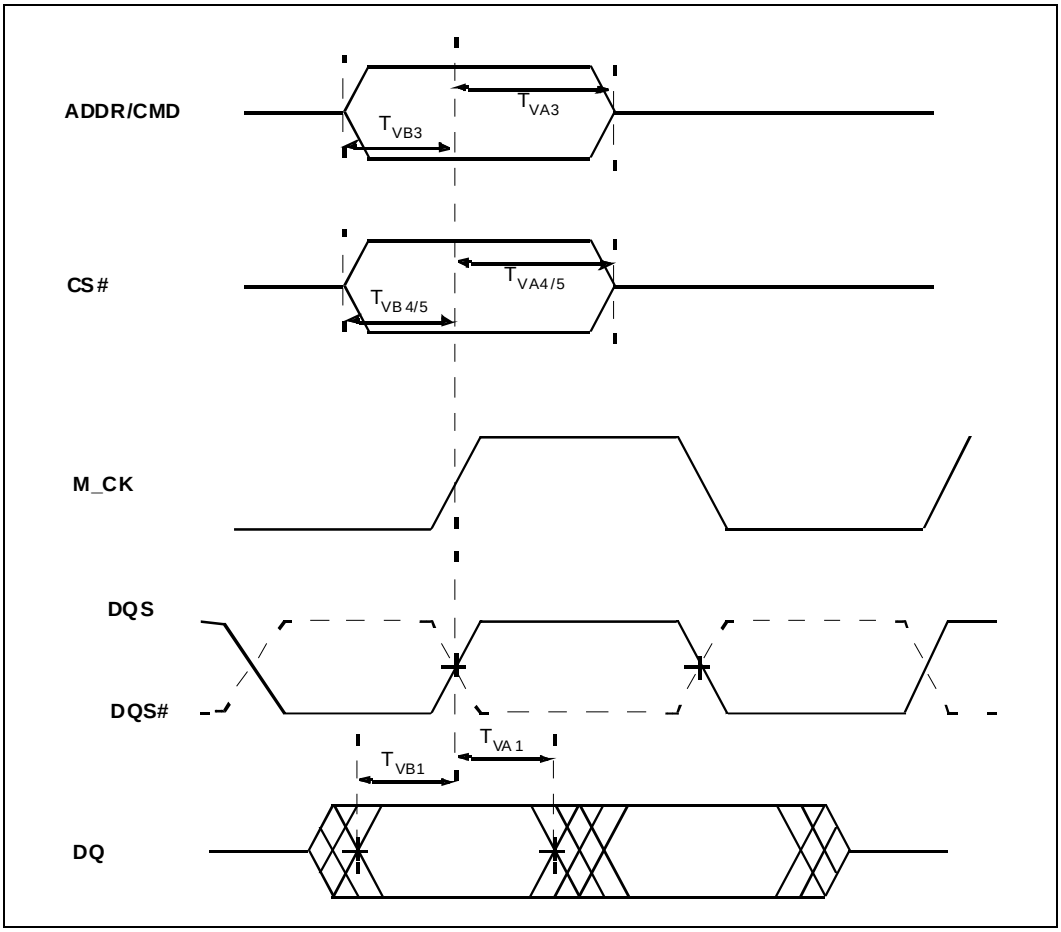


Figure 15. DQS Falling Edge Output Access Time to/from M_CK Rising Edge

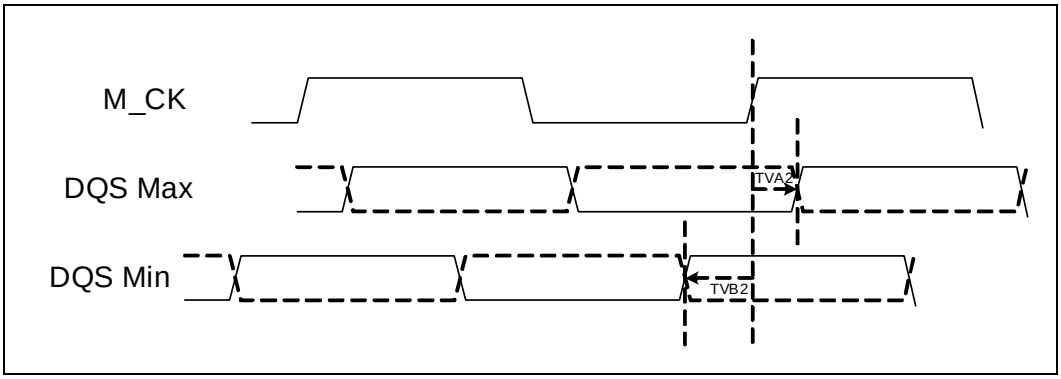


Figure 16. DDR2 SDRAM Read Timings

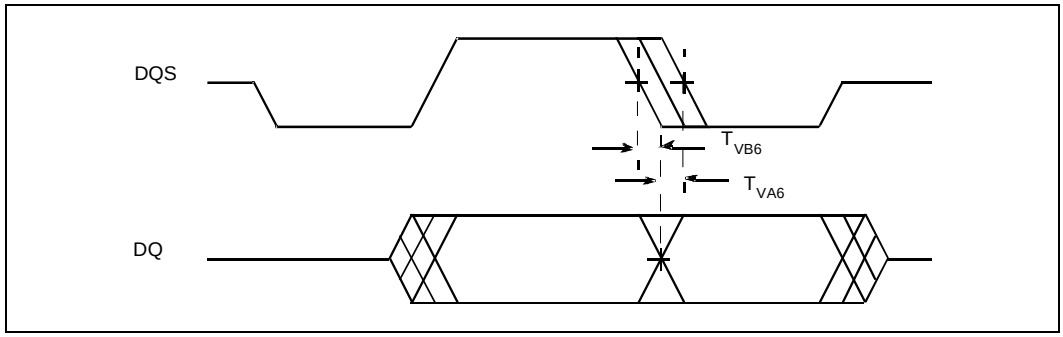


Table 31. AC Measurement Conditions

Symbol		PCI-X	PCI	DDR2	PBI	Units	Notes
Vth		$0.6V_{CC3P3}$	$0.6V_{CC3P3}$	M_VREF+0.250	2.0	V	
V_{tl}		$0.25V_{CC3P3}$	$0.2V_{CC3P3}$	M_VREF-0.250	0.8	V	
V_{test}		$0.4V_{CC3P3}$	$0.4V_{CC3P3}$	$0.5V_{CC1P8}$	1.5	V	
V_{trise}		$0.285V_{CC3P3}$	$0.285V_{CC3P3}$	$0.5V_{CC1P8}$	1.5	V	
V_{tfall}		$0.615V_{CC3P3}$	$0.615V_{CC3P3}$	$0.5V_{CC1P8}$	1.5	V	
V_{max}		$0.35V_{CC3P3}$	$0.4V_{CC3P3}$	1.0	1.2	V	
Slew Rate		1.5	1.5	1.0	1.0	V/nS	1

Notes:
1. Input signal slew rate is measured between V_{il} and V_{ih}

Figure 17. AC Test Load for all Signals Except PCI, PCI-Express and DDR2

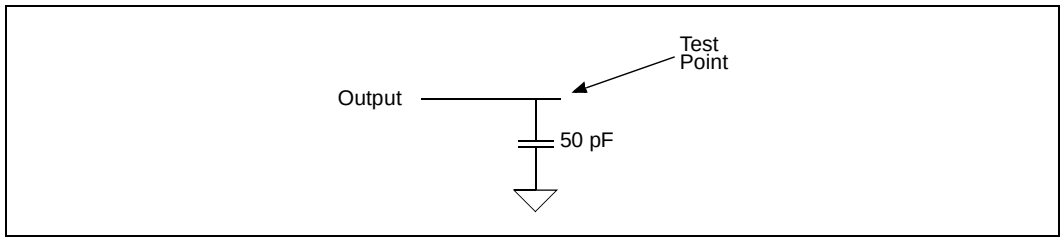


Figure 18. AC Test Load for DDR2 SDRAM Signals

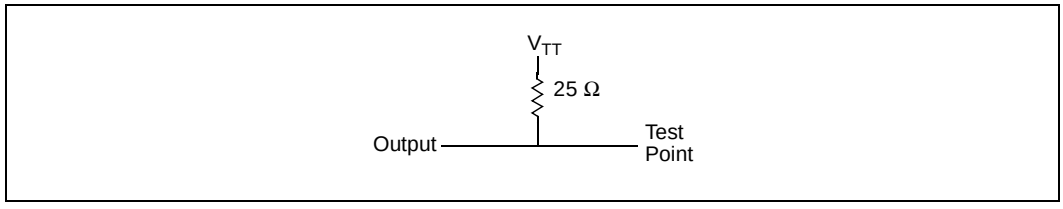


Figure 19. PCI/PCI-X $T_{OV(max)}$ Rising Edge AC Test Load

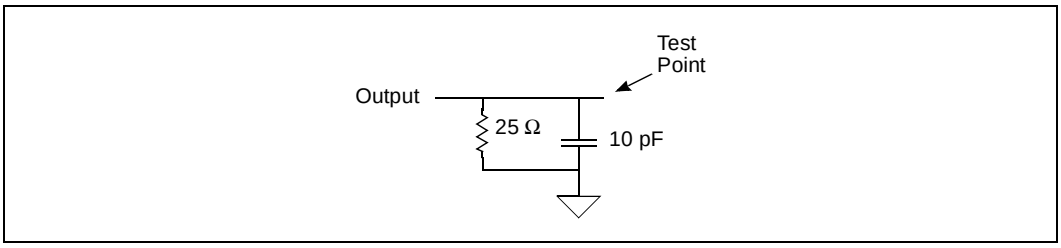


Figure 20. PCI/PCI-X $T_{OV(max)}$ Falling Edge AC Test Load

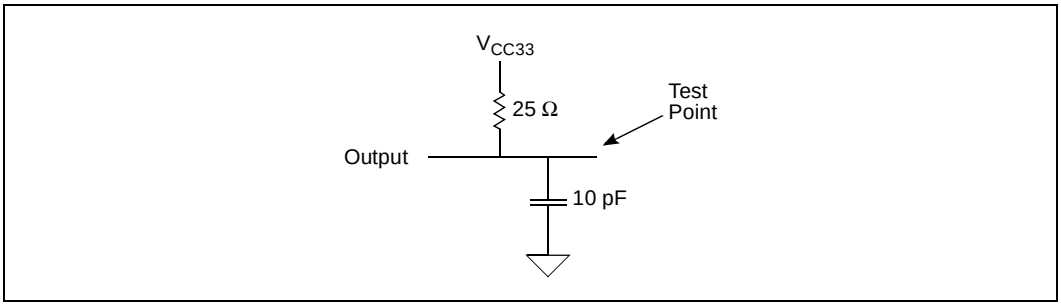


Figure 21. PCI/PCI-X $T_{OV(min)}$ AC Test Load

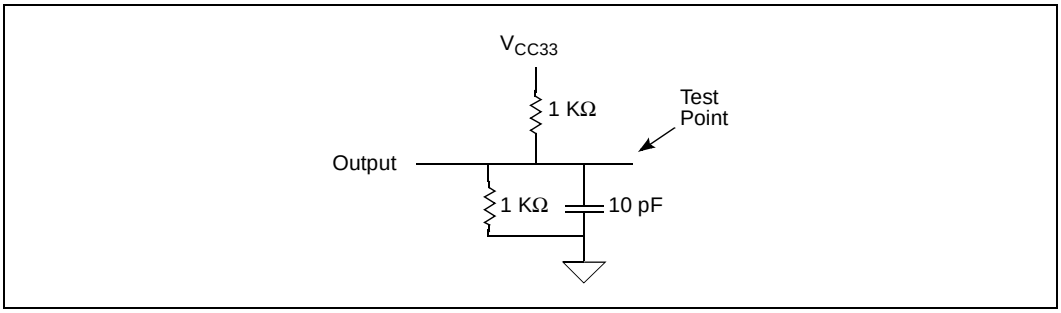


Figure 22. Transmitter Test Load (100 Ω diff Load)

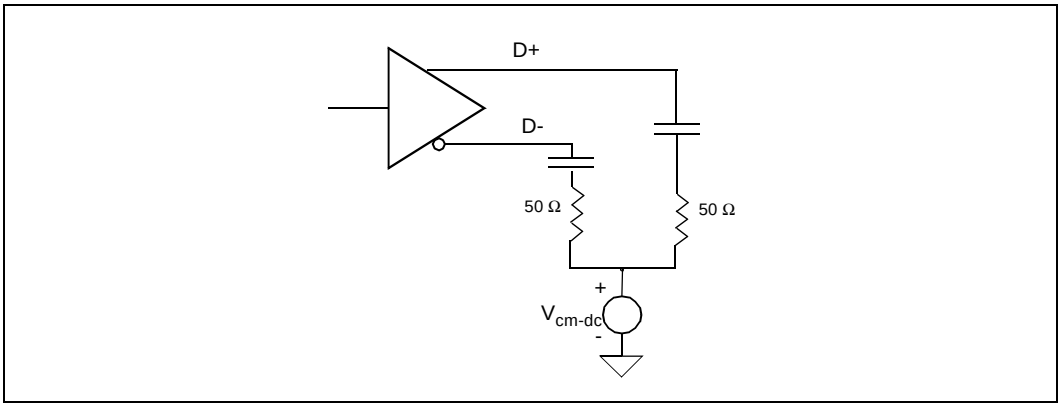


Figure 23. Transmitter Eye Diagram

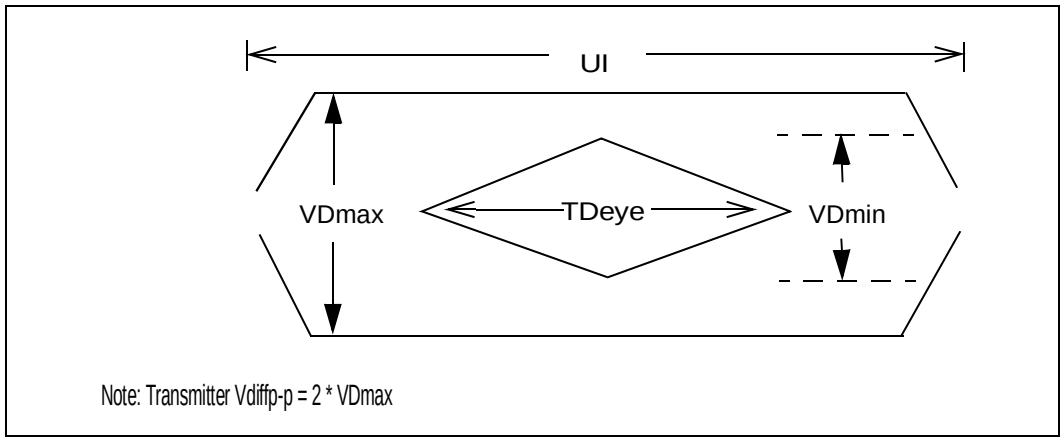


Figure 24. Receiver Eye Opening (Differential)

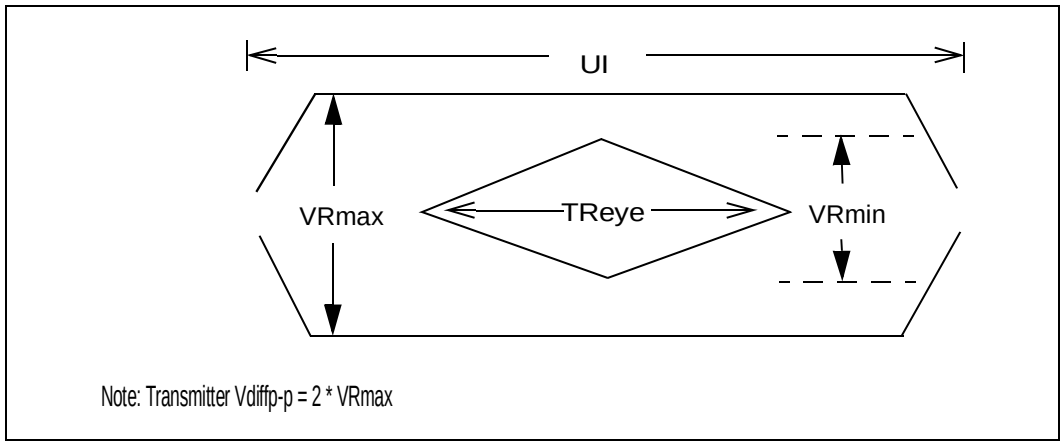
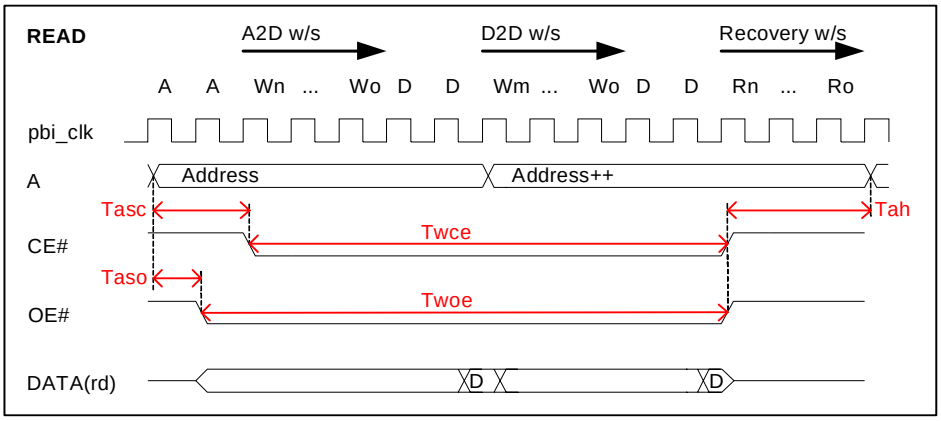
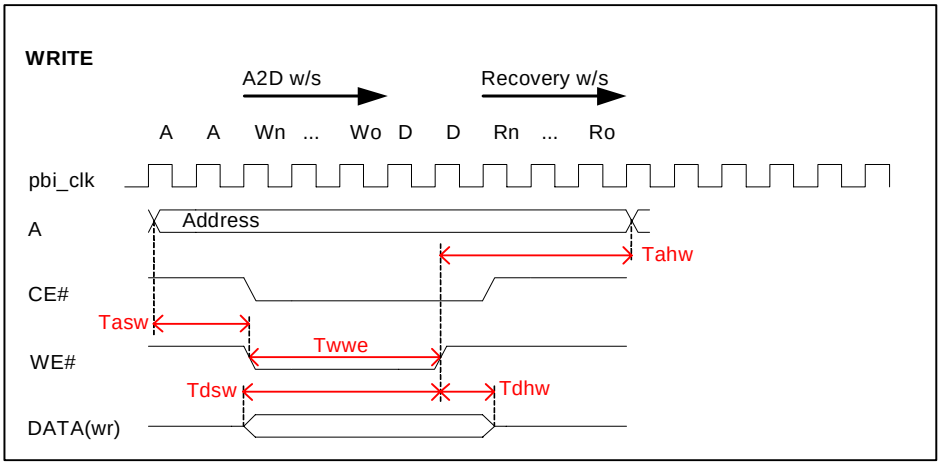


Figure 25. PBI Output Timings

PBI Output Timings - READ

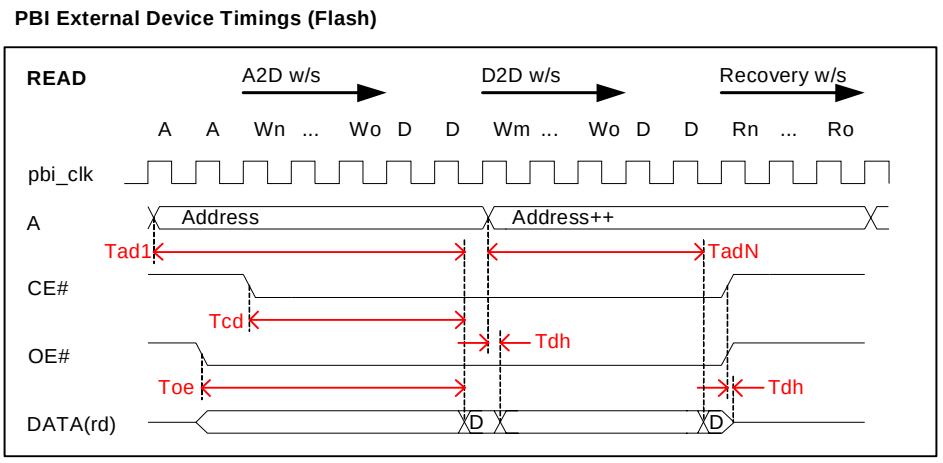


PBI Output Timings - WRITE



Notes:
(1) pbi_clk is provided as a virtual clock and is not available as an external signal.
(2) Timings are based on 66 MHz PBI_CLK.

Figure 26. PBI External Device Timings (Flash)



Notes:
(1) pbi_clk is provided as a virtual clock and is not available as an external signal.
(2) Timings are based on 66 MHz PBI_CLK.

Figure 27. Intel® 81341 and 81342 I/O Processors 1.2V/1.8V Power Sequencing System Requirements

- Signal/Ball names concerned: vcc1p8s, vcc1p2as and vcc1p2ds
- 1.8V supply should never exceed the 1.2V supply (analog or digital) when vcc1p2 < nominal
- The 3.3V supplies and VccVio supplies don't have any sequencing requirements.

