1.8V to 3.3V LVCMOS High Performance Clock Buffer Family

5PB11xx

DATASHEET

Description

The 5PB11xx is a high-performance LVCMOS Clock Buffer Family. It has best-in-class additive phase jitter of 50fsec RMS.

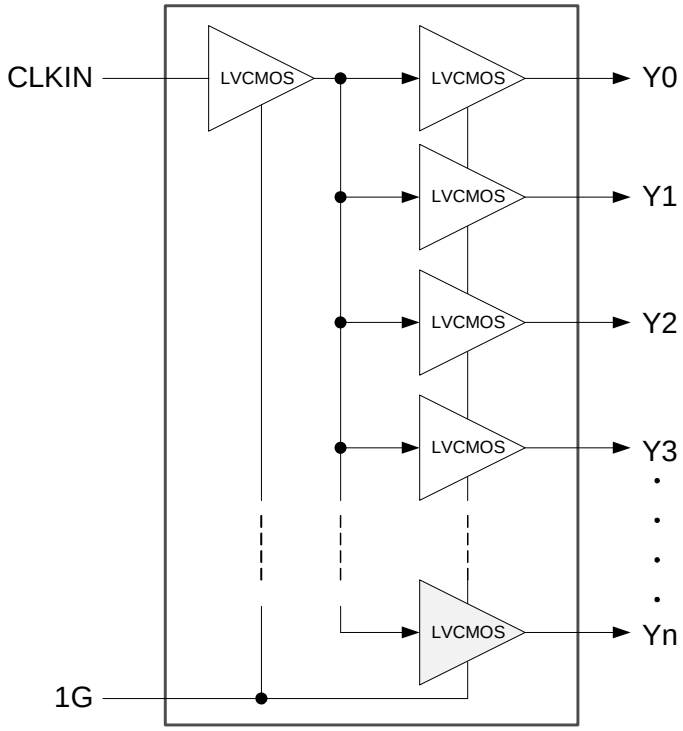
There are five different fan-out variations, 1:2 to 1:10, available.

The IDT5PB11xx also supports a synchronous glitch-free Output Enable function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It comes in various packages and can operate from a 1.8V to 3.3V supply.

Features

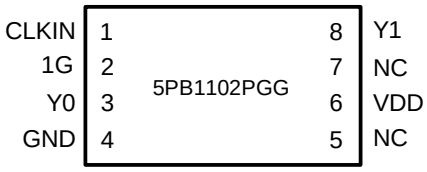
- High performance 1:2, 1:4, 1:6, 1:8, 1:10 LVCMOS clock buffer
- Very low pin-to-pin skew < 50ps
- Very low additive jitter < 50fs
- Supply voltage: 1.8V to 3.3V
- f_{MAX} = 200MHz
- Integrated serial termination for 50Ω channel
- Packaged in 8-, 14-, 16-, 20-pin TSSOP and as small as 2 × 2 mm DFN and QFN packages
- Industrial (-40°C to +85°C) and extended (-40°C to +105°C) temperature ranges

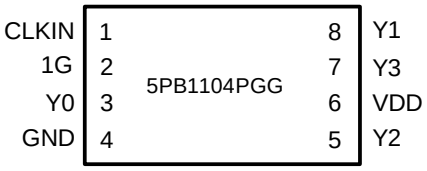
Block Diagram

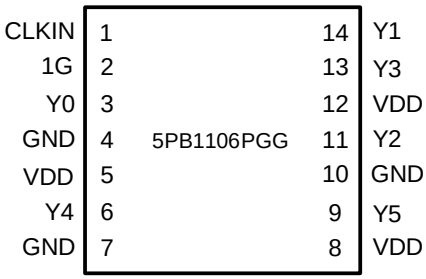


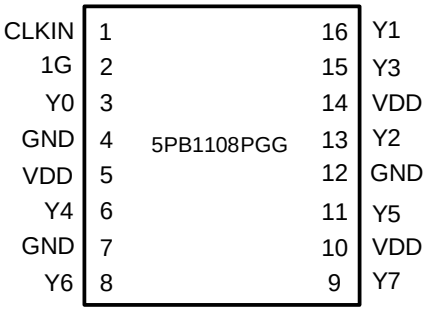
 ©2017 Integrated Device Technology, Inc.

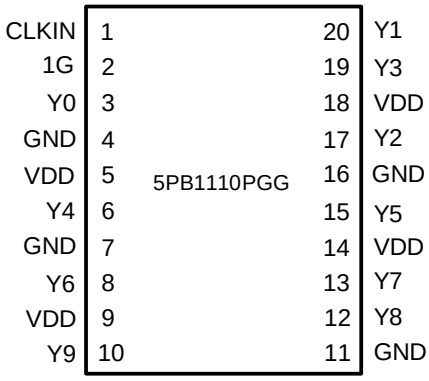
Pin Assignments for TSSOP Packages







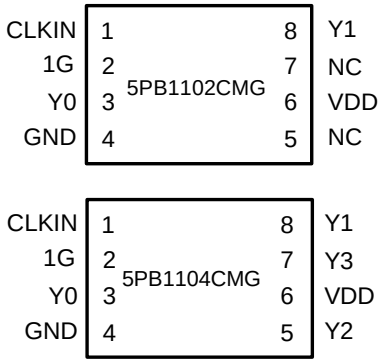


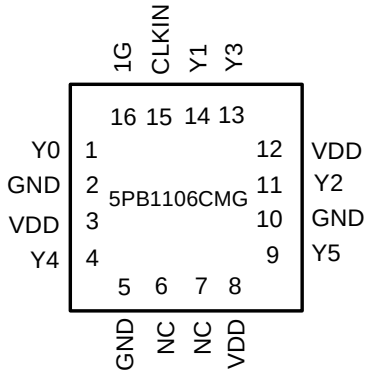


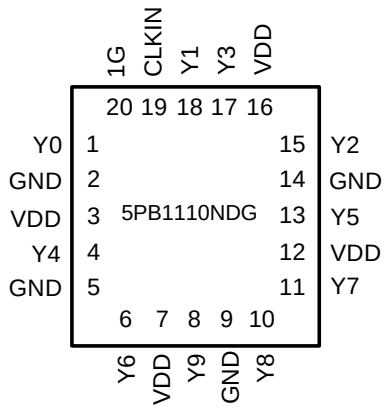
Pin Descriptions for TSSOP Packages

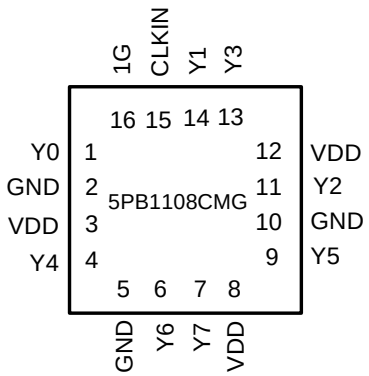
Device Number	LVCMOS Clock Input	Clock Output Enable	LVCMOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, . . . Y9	V_{DD}	GND
5PB1102PGG	1	2	3, 8	6	4
5PB1104PGG	1	2	3, 8, 5, 7	6	4
5PB1106PGG	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
5PB1108PGG	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12
5PB1110PGG	1	2	3, 20, 17, 19, 6, 15, 8, 13, 12, 10	5, 9, 14, 18	4, 7, 11, 16

Pin Assignments for DFN/QFN Packages









Pin Descriptions for DFN/QFN Packages

Device Number	LVCMOS Clock Input	Clock Output Enable	LVCMOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, . . . Y9	V_{DD}	GND
5PB1102CMG	1	2	3, 8	6	4
5PB1104CMG	1	2	3, 5, 7, 8	6	4
5PB1106CMG	15	16	1, 4, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1108CMG	15	16	1, 4, 6, 7, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1110NDG	19	20	1, 4, 6, 8, 10, 11, 13, 15, 17, 18	3, 7, 12, 16	2, 5, 9, 14

Output Logic Table

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

After at least three cycles of input clock toggling. Output Enable function is asynchronous to eliminate any intermediate incorrect output clock cycles during transition which may cause frequency peaking to the downstream device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5PB11xx. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Output Enable and All Outputs	-0.4 V to VDD+0.5 V
CLKIN	-0.4 V to 3.465V
Ambient Operating Temperature (industrial)	-40 to +85°C
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (industrial)	-40		+85	°C
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, CLKIN	V_{IH}	Note 1	0.7 x VDD		VDD	V
Input Low Voltage, CLKIN	V_{IL}	Note 1			0.3 x VDD	V
Input High Voltage, 1G	V_{IH}		1.6		VDD	V
Input Low Voltage, 1G	V_{IL}				0.6	V
Output High Voltage	V_{OH}	I_{OH} = -5mA	1.4			V
Output Low Voltage	V_{OL}	I_{OL} = 5mA			0.4	V
Nominal Output Impedance	Z_O			50		Ω
Input Capacitance	C_{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		8		mA
5PB1104		100MHz, No load, 25°C		12		
5PB1106		100MHz, No load, 25°C		16		
5PB1108		100MHz, No load, 25°C		21		
5PB1110		100MHz, No load, 25°C		25		

Notes: 1. Nominal switching threshold is VDD/2

VDD = 2.5V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, CLKIN	V_{IH}	Note 1	0.7 x VDD		VDD	V
Input Low Voltage, CLKIN	V_{IL}	Note 1			0.3 x VDD	V
Input High Voltage, 1G	V_{IH}		1.8		VDD	V
Input Low Voltage, 1G	V_{IL}				0.7	V
Output High Voltage	V_{OH}	I_{OH} = -8mA	1.9			V
Output Low Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
Nominal Output Impedance	Z_O			50		Ω
Input Capacitance	C_{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		10		mA
5PB1104		100MHz, No load, 25°C		15		
5PB1106		100MHz, No load, 25°C		22		
5PB1108		100MHz, No load, 25°C		28		
5PB1110		100MHz, No load, 25°C		33		

VDD = 3.3V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, CLKIN	V_{IH}	Note 1	0.7 x VDD		VDD	V
Input Low Voltage, CLKIN	V_{IL}	Note 1			0.3 x VDD	V
Input High Voltage, 1G	V_{IH}		2		VDD	V
Input Low Voltage, 1G	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12mA			0.7	V
Nominal Output Impedance	Z_O			50		Ω
Input Capacitance	C_{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		12		mA
5PB1104		100MHz, No load, 25°C		20		
5PB1106		100MHz, No load, 25°C		25		
5PB1108		100MHz, No load, 25°C		35		
5PB1110		100MHz, No load, 25°C		40		

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time (2pF load)	t_{OR}	0.36V to 1.44V, C_L = 2 pF		0.5	0.75	ns
Output Fall Time (2pF load)	t_{OF}	1.44V to 0.36V, C_L = 2 pF		0.5	0.75	ns
Output Rise Time (5pF load)	t_{OR}	0.36V to 1.44V, C_L = 5 pF		0.8	1.0	ns
Output Fall Time (5pF load)	t_{OF}	1.44V to 0.36V, C_L = 5 pF		0.8	1.0	ns
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		Note 1	1.5	1.9	2.5	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1106)		Rising edges at VDD/2, Note 2		35	58	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t_{EN}	$C_L \leq$ 5pF			3	cycles
Output Disable Time	t_{DIS}	$C_L \leq$ 5pF			3	cycles

VDD = 2.5V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time (2pF load)	t_{OR}	0.5V to 2.0V, C_L = 2 pF		0.4	0.7	ns
Output Fall Time (2pF load)	t_{OF}	2.0V to 0.5V, C_L = 2 pF		0.4	0.7	ns
Output Rise Time (5pF load)	t_{OR}	0.5V to 2.0V, C_L = 5 pF		0.75	1.0	ns
Output Fall Time (5pF load)	t_{OF}	2.0V to 0.5V, C_L = 5 pF		0.75	1.0	ns
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay (5PB1102/04)		Note 1	1.9	2.4	2.9	ns
Propagation Delay (5PB1106/08)			2.0	2.4	3.3	ns
Propagation Delay (5PB1110)			2.0	2.4	3.0	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1106)		Rising edges at VDD/2, Note 2		35	58	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t_{EN}	$C_L \leq$ 5pF			3	cycles
Output Disable Time	t_{DIS}	$C_L \leq$ 5pF			3	cycles

VDD = 3.3V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time (2pF load)	t_{OR}	0.66V to 2.64V, C_L = 2pF		0.45	0.6	ns
Output Fall Time (2pF load)	t_{OF}	2.64V to 0.66V, C_L = 2pF		0.45	0.6	ns
Output Rise Time (5pF load)	t_{OR}	0.66V to 2.64V, C_L = 5pF		0.7	1.0	ns
Output Fall Time (5pF load)	t_{OF}	2.64V to 0.66V, C_L = 5pF		0.7	1.0	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay (5PB1102/04)		Note 1	1.7	2	2.4	ns
Propagation Delay (5PB1106/08)			1.7	2	2.7	ns
Propagation Delay (5PB1110)			1.7	2	2.5	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1106)		Rising edges at VDD/2, Note 2		35	58	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t_{EN}	$C_L \leq 5pF$			3	cycles
Output Disable Time	t_{DIS}	$C_L \leq 5pF$			3	cycles

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Phase Noise Plots

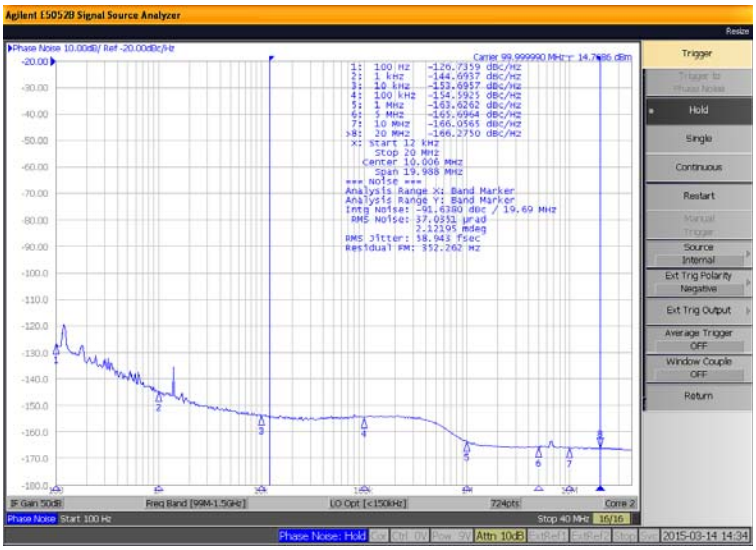


Figure 1. 5PB11xx Reference Phase Noise 58.9fs (12kHz to 20MHz)

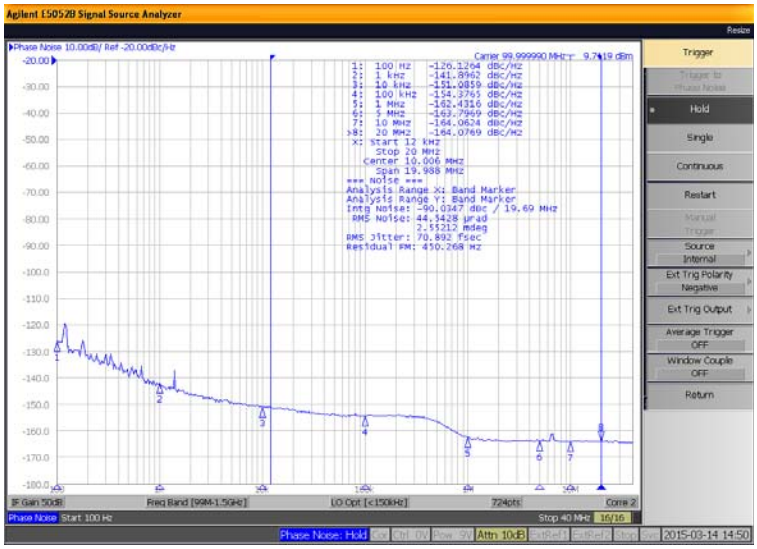
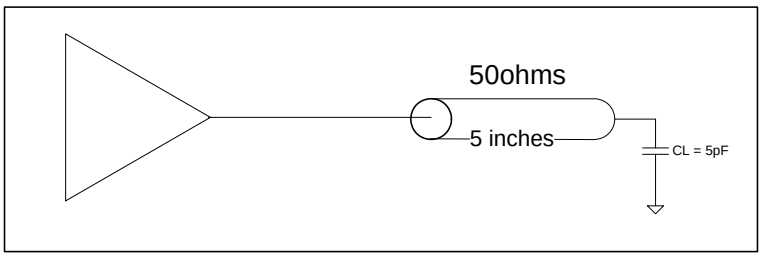


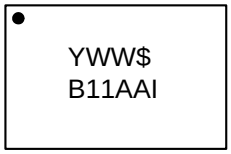
Figure 2. 5PB11xx Output Phase Noise 70.9fs (12kHz to 20MHz)

The phase noise plots above show the low additive jitter of the 5PB11xx high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5PB11xx has about 70.9fs of RMS phase jitter. This results in a low additive phase jitter of only 39fs.

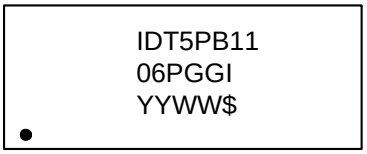
Test Load and Circuit



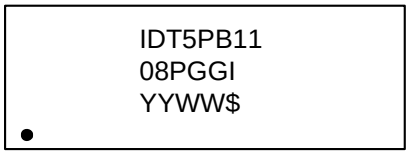
Marking Diagrams (industrial temperature range)



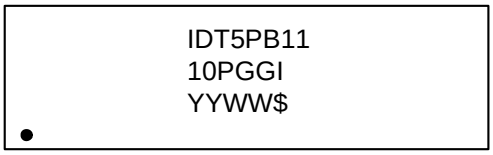
8-pin TSSOP



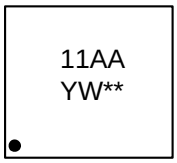
14-pin TSSOP



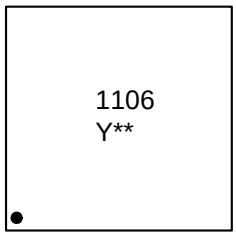
16-pin TSSOP



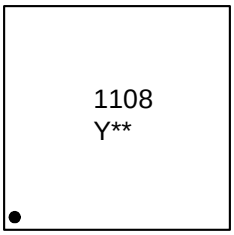
20-pin TSSOP



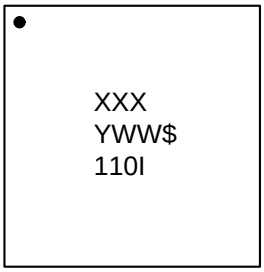
8-pin DFN



16-pin QFN



16-pin QFN

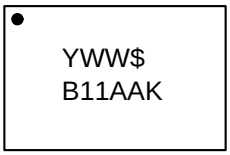


20-pin QFN

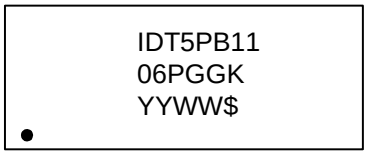
Notes:

1. “AA” denotes the last two digits of the part number for 8-pin TSSOP and DFN (e.g. 02, 04).
2. “**” is the lot sequence.
3. “XXX” denotes the last three characters of the Asm lot (20-pin QFN only).
4. “YYWW”, “YWW”, “YW”, or “Y” is the last digit(s) of the year and week that the part was assembled.
5. “$” denotes the mark code.
6. “G” after the two-letter package code denotes RoHS compliant package.
7. “I” denotes industrial temperature range device.
8. Bottom marking: LOT and COO (TSSOP only).

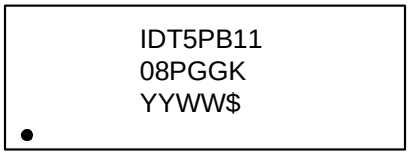
Marking Diagrams (extended temperature range)



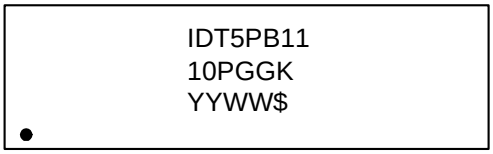
8-pin TSSOP



14-pin TSSOP



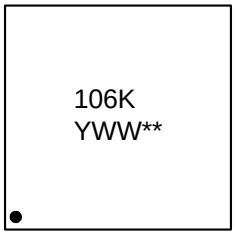
16-pin TSSOP



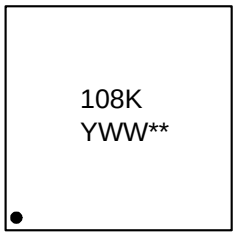
20-pin TSSOP



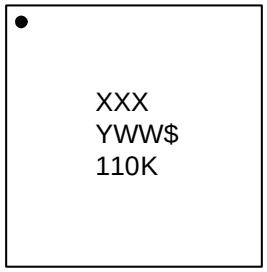
8-pin DFN



16-pin QFN



16-pin QFN



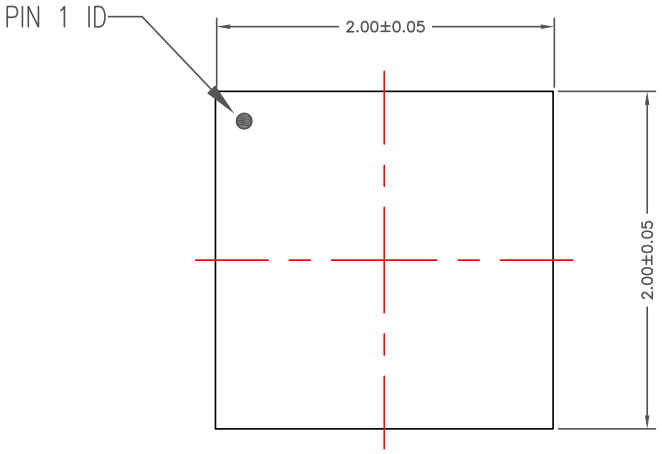
20-pin QFN

Notes:

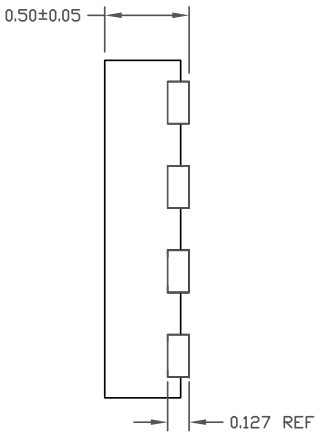
1. “AA” denotes the last two digits of the part number for 8-pin TSSOP and DFN (e.g. 02, 04).
2. “**” is the lot sequence.
3. “XXX” denotes the last three characters of the Asm lot (20-pin QFN only).
4. “YYWW”, “YWW”, “YW”, or “Y” is the last digit(s) of the year and week that the part was assembled.
5. “$” denotes the mark code.
6. “G” after the two-letter package code denotes RoHS compliant package.
7. “K” denotes extended temperature range device.
8. Bottom marking: LOT and COO (TSSOP only).

Package Outline and Dimensions (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)

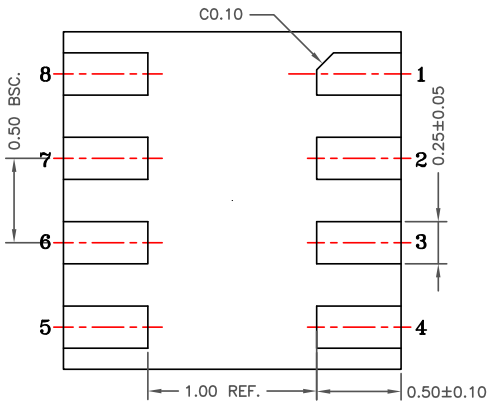
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/18/14	J.HUA



TOP VIEW



SIDE VIEW



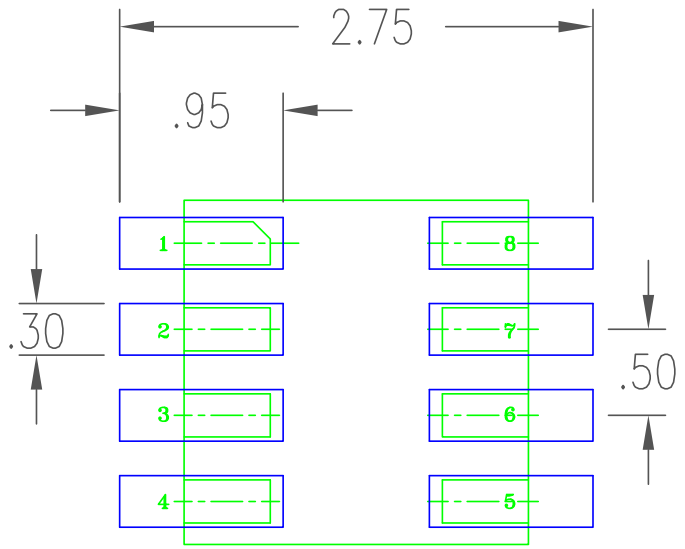
BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT. www.IDT.com	6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284–8200 FAX: (408) 492–8674
APPROVALS	DATE	TITLE	CMG8 PACKAGE OUTLINE 2.0 X 2.0 mm BODY 0.5mm PITCH VFQFN
DRAWN PAC	09/10/14		
CHECKED J. Hua	09/10/14		
		SIZE C	DRAWING No. PSC–4490 REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/18/14	J.HUA



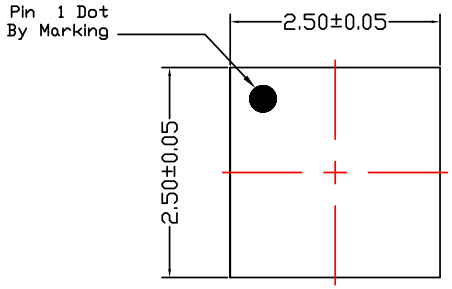
RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

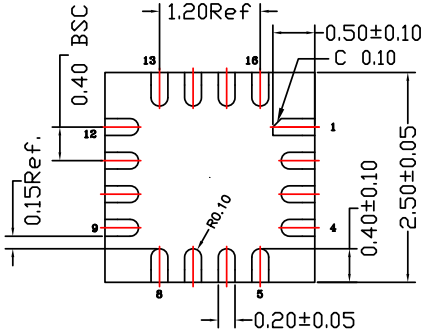
TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT. www.IDT.com	6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	CMG8 PACKAGE OUTLINE 2.0 X 2.0 mm BODY 0.5 mm PITCH VFQFN
DRAWN RAC	09/10/14		
CHECKED			
		SIZE C	DRAWING No. PSC-4490 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Package Outline and Dimensions (16-pin VFQFN, 2.5mm x 2.5mm Body, 0.4mm pitch)

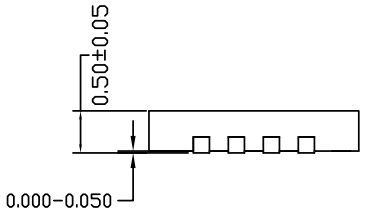
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/03/14	JH
01	ADD PIN1 CHAMFER	12/11/14	JH



TOP VIEW



BOTTOM VIEW



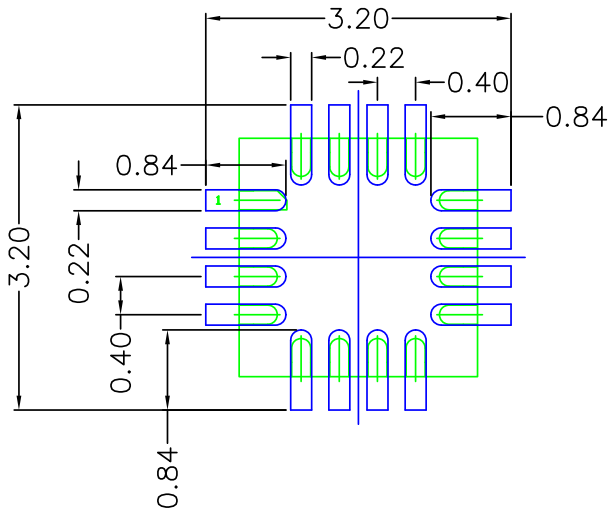
SIDE VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX± ANGULAR ±1°	IDT™ www.IDT.com 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS / DATE DRAWN 04/03/14 CHECKED	TITLE CMG 16 PACKAGE OUTLINE 2.5 x 2.5 mm BODY 0.40 mm PITCH VFQFN
	SIZE C · DRAWING No. PSC-4478 · REV 01
	DO NOT SCALE DRAWING · SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/03/14	JH
01	ADD PIN1 CHAMFER	12/11/14	JH



RECOMMENDED LAND PATTERN DIMENSION

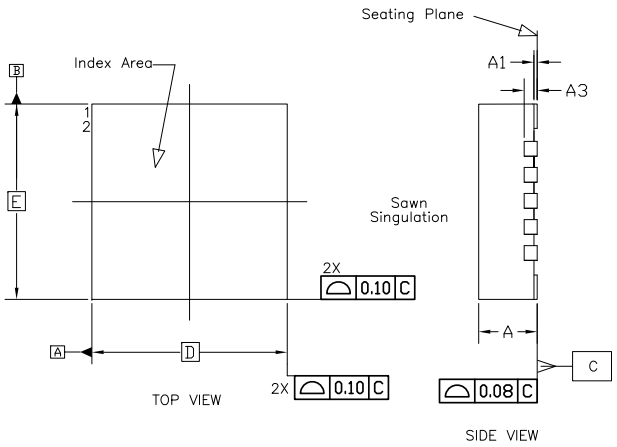
NOTES:

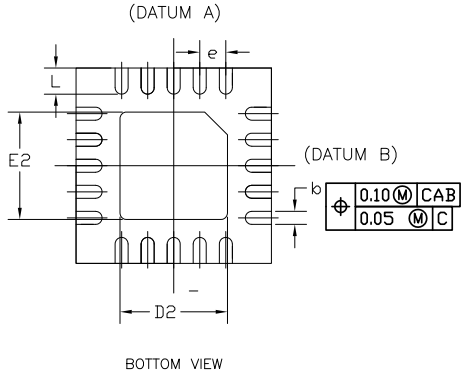
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX± ANGULAR ±1°		IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE	CMG 16 PACKAGE OUTLINE 2.5 x 2.5 mm BODY 0.40 mm PITCH VFQFN
DRAWN	04/03/14		
CHECKED			
		SIZE: C	DRAWING No.: PSC-4478 — REV: 01
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Package Outline and Dimensions (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	3/30/16	JH





DIMENSION			
Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 Ref	
b	0.17	0.20	0.25
e		0.40 BASIC	
N		20	
ND		5	
NE		5	
D		3.00 BASIC	
E		3.00 BASIC	
D2	1.55	1.65	1.75
E2	1.55	1.65	1.75
L	0.30	0.40	0.50

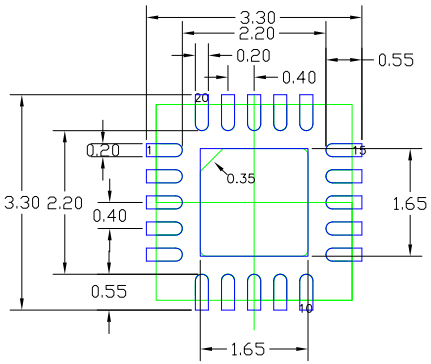
NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.

TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX± ANGULAR ±1°		IDT® www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE	ND/NDG 20 PACKAGE OUTLINE 3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ 0.40 PITCH QFN
DRAWN RAC	3/30/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4179-02 REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 2

Package Outline and Dimensions, cont. (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	3/30/16	JH



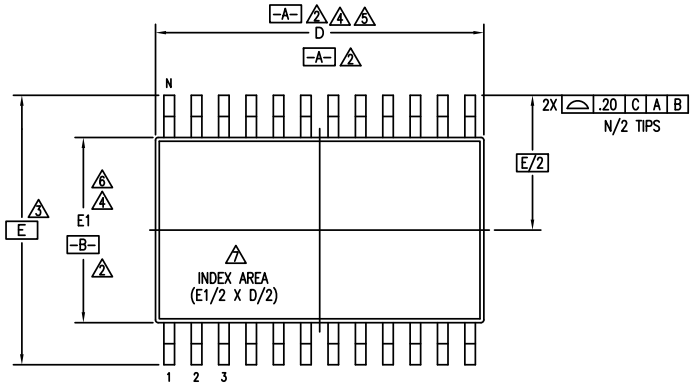
RECOMMENDED LAND PATTERN DIMENSION

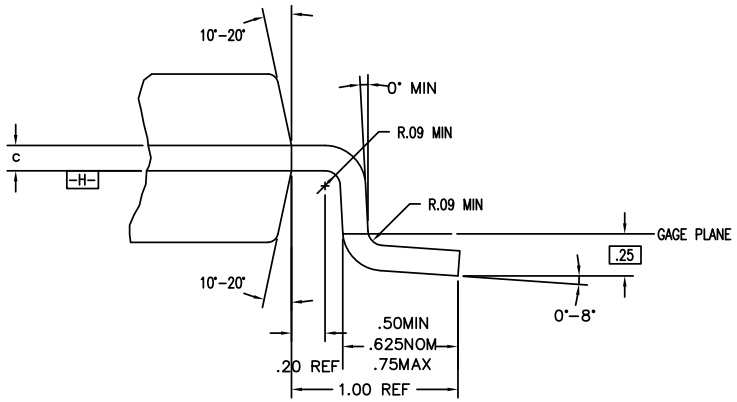
NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± ±1° XX± XXX±		IDT® www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE ND/NDG 20 PACKAGE OUTLINE 3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ 0.40 PITCH QFN	
DRAWN RAC	3/30/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4179-02 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

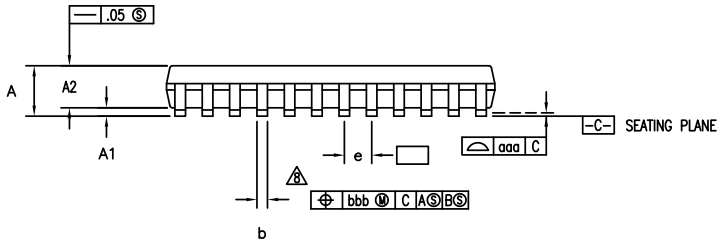
Package Outline and Dimensions (8-, 14-, 16-, 20-pin TSSOP)

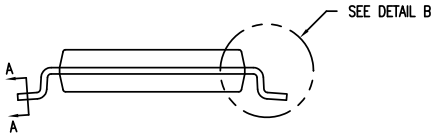
DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
08/25/98	02	ADD 14 & 16 LD	T. VU
07/10/99	03	ADD 8 LD	T. VU
5/23/01	04	ADDED TOPMARK TO TITLE	
10/14/04	05	ADD "GREEN" PGG NOMENCLATURE	TU VU
3/8/13	06	ADDED PACKAGE CODE	RAC
9/3/14	07	ADD TOLERANCE FOR A, A1, E AND b	CK LEE
3/10/17	08	ADD OPTION T1	R.TANH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

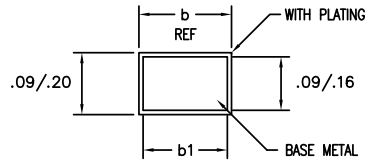




DETAIL B







SECTION A-A

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

IDT™ www.IDT.com

2975 Stender Way
Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE PG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE	DRAWING No.	REV
C	PSC-4056	08

DO NOT SCALE DRAWING | SHEET 1 OF 3

Package Outline and Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)

DATE CREATED	REVISIONS REV	DESCRIPTION	AUTHOR
08/25/98	02	ADD 14 & 16 LD	T. VU
07/10/99	03	ADD 8 LD	T. VU
5/23/01	04	ADDED TOPMARK TO TITLE	
10/14/04	05	ADD "GREEN" PGG NOMENCLATURE	TU VU
3/8/13	06	ADDED PACKAGE CODE	RAC
9/3/14	07	ADD TOLERANCE FOR A, A1, E AND b	CK LEE
3/10/17	08	ADD OPTION T1	R.TANH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

	PG/PGG8				PG/PGG14				PG/PGG16				PG/PGG20				PG/PGG24				PG/PGG28			
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB-1			NOTE	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20		.85	1.10	1.20	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05	
D	2.90	3.00	3.10	4,5	4.90	5.00	5.10	4,5	4.90	5.00	5.10	4,5	6.40	6.50	6.60	4,5	7.70	7.80	7.90	4,5	9.60	9.70	9.80	4,5
E	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3	6.20	6.40	6.60	3
E1	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6
e	.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC			
b	.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30		.19	.25	.30	
b1	.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25	
aaa	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
bbb	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
N	8				14				16				20				24				28			

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–153, VARIATION AA, AB–1, AB, AC, AD & AE

	OPTION T1 PGG14T1 JEDEC VARIATION AB-1			
SYMBOL	MIN	NOM	MAX	NOTE
A	.90	1.10	1.20	
A1	.05	.10	.15	
A2	.80	1.00	1.05	
D	4.90	5.00	5.10	4,5
E	6.20	6.40	6.60	3
E1	4.30	4.40	4.50	4,6
e	.65 BSC			
b	.19	.25	.30	
b1	.19	.22	.25	
c	.09	–	.20	
aaa	–	–	.10	
bbb	–	–	.10	
N	14			

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

IDT™ www.IDT.com
2975 Stender Way
Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH

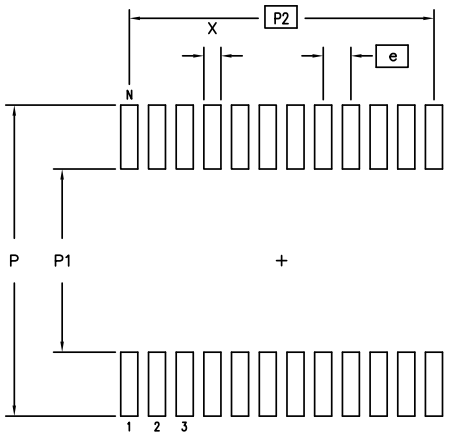
SIZE	DRAWING No.	REV
C	PSC–4056	08

DO NOT SCALE DRAWING | SHEET 2 OF 3

Package Outline and Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)

DATE CREATED	REVISIONS		
	REV	DESCRIPTION	AUTHOR
08/25/98	02	ADD 14 & 16 LD	T. VU
07/10/99	03	ADD 8 LD	T. VU
5/23/01	04	ADDED TOPMARK TO TITLE	
10/14/04	05	ADD "GREEN" PGG NOMENCLATURE	TU VU
3/8/13	06	ADDED PACKAGE CODE	RAC
9/3/14	07	ADD TOLERANCE FOR A, A1, E AND b	CK LEE
3/10/17	08	ADD OPTION T1	R.TANH
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40
P2	1.95 BSC		3.90 BSC		4.55 BSC		5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	8		14		16		20		24		28	

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

IDT™
www.IDT.com
2975 Stender Way
Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE PG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE	DRAWING No.	REV
C	PSC-4056	08

DO NOT SCALE DRAWING | SHEET 3 OF 3

Ordering Information (industrial temperature range)

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5PB1102PGGI	see page 8	Tubes	8-pin TSSOP	-40 to +85 °C
5PB1102PGGI8		Tape and Reel	8-pin TSSOP	-40 to +85 °C
5PB1104PGGI		Tubes	8-pin TSSOP	-40 to +85 °C
5PB1104PGGI8		Tape and Reel	8-pin TSSOP	-40 to +85 °C
5PB1106PGGI		Tubes	14-pin TSSOP	-40 to +85 °C
5PB1106PGGI8		Tape and Reel	14-pin TSSOP	-40 to +85 °C
5PB1108PGGI		Tubes	16-pin TSSOP	-40 to +85 °C
5PB1108PGGI8		Tape and Reel	16-pin TSSOP	-40 to +85 °C
5PB1110PGGI		Tubes	20-pin TSSOP	-40 to +85 °C
5PB1110PGGI8		Tape and Reel	20-pin TSSOP	-40 to +85 °C
5PB1102CMGI		Cut Tape	8-pin DFN	-40 to +85 °C
5PB1102CMGI8		Tape and Reel	8-pin DFN	-40 to +85 °C
5PB1104CMGI		Cut Tape	8-pin DFN	-40 to +85 °C
5PB1104CMGI8		Tape and Reel	8-pin DFN	-40 to +85 °C
5PB1104CMGI/W		Tape and Reel	8-pin DFN	-40 to +85 °C
5PB1106CMGI		Cut Tape	16-pin QFN	-40 to +85 °C
5PB1106CMGI8		Tape and Reel	16-pin QFN	-40 to +85 °C
5PB1108CMGI		Cut Tape	16-pin QFN	-40 to +85 °C
5PB1108CMGI8		Tape and Reel	16-pin QFN	-40 to +85 °C
5PB1110NDGI		Tubes	20-pin QFN	-40 to +85 °C
5PB1110NDGI8		Tape and Reel	20-pin QFN	-40 to +85 °C

Ordering Information (extended temperature range)

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5PB1102PGGK	see page 9	Tubes	8-pin TSSOP	-40 to +105 °C
5PB1102PGGK8		Tape and Reel	8-pin TSSOP	-40 to +105 °C
5PB1104PGGK		Tubes	8-pin TSSOP	-40 to +105 °C
5PB1104PGGK8		Tape and Reel	8-pin TSSOP	-40 to +105 °C
5PB1106PGGK		Tubes	14-pin TSSOP	-40 to +105 °C
5PB1106PGGK8		Tape and Reel	14-pin TSSOP	-40 to +105 °C
5PB1108PGGK		Tubes	16-pin TSSOP	-40 to +105 °C
5PB1108PGGK8		Tape and Reel	16-pin TSSOP	-40 to +105 °C
5PB1110PGGK		Tubes	20-pin TSSOP	-40 to +105 °C
5PB1110PGGK8		Tape and Reel	20-pin TSSOP	-40 to +105 °C
5PB1102CMGK		Cut Tape	8-pin DFN	-40 to +105 °C
5PB1102CMGK8		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1104CMGK		Cut Tape	8-pin DFN	-40 to +105 °C
5PB1104CMGK8		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1104CMGK/W		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1106CMGK		Cut Tape	16-pin QFN	-40 to +105 °C
5PB1106CMGK8		Tape and Reel	16-pin QFN	-40 to +105 °C
5PB1108CMGK		Cut Tape	16-pin QFN	-40 to +105 °C
5PB1108CMGK8		Tape and Reel	16-pin QFN	-40 to +105 °C
5PB1110NDGK		Tubes	20-pin QFN	-40 to +105 °C
5PB1110NDGK8		Tape and Reel	20-pin QFN	-40 to +105 °C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	03/20/15	B. Chandhoke	Initial release.
B	05/19/15	B. Chandhoke	1. Expanded Output Enable function text in General Description, and within the note under “Output Logic Table”. 2. Updated all “Buffer Additive Phase Jitter, RMS” conditions from 125MHz to 156.25MHz.
C	06/09/15	B. Chandhoke	1. Corrected typos in part numbers in DC Electrical Tables. 2. Updated existing Output Rise/Fall Time specs for 5pF load. 3. Added additional Output Rise/Fall specs for 2pF load.
D	06/15/15	B. Chandhoke	Fixed typos in Output Rise/Fall Time 5pF specs for CL conditions; should be 5pF; not 2pF.
E	06/22/15	B. Chandhoke	Changed 3.3V Operating Voltage spec from 3.15V min to 3.135V min; 3.45V max to 3.465V max.
F	08/24/15	B. Chandhoke	1. Added 5PB1104CMGI**W** orderable part. 2. Updated Abs Max Ratings table for “Output Enable and All outputs” and “CLKIN”; changed -0.5 V to -0.4 and added -0.4 to... respectively.
G	05/13/16	H.G.	Replace NDG20 package outline drawing with latest version.
H	12/15/16	J. Chen	Updated marking diagrams for all TSSOP devices.
J	02/10/17	Y.G.	Change Propagation Delay maximum spec in 1.8V AC electrical characterization table from 2.2 to 2.5ns.
K	03/28/17	Y.G.	1. Updated Propagation Delay specifications for 5PB1106/08/10; 2.5V and 3.3V. 2. Updated output-output skew maximum specifications for 5PB1106; 1.8V, 2.5V, 3.3V. 3. Updated legal disclaimer. 4. Updated package outline drawings.

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