SIO1007

LPC Super I/O LPC IrDA Hot Docking Chip with UART

Product Features

- 3.3 Volt Operation (5V tolerant)
- Programmable Wakeup Event Interface (IO_PME# Pin)
- SMI Support (IO_SMI# Pin)
- GPIOs (16)
- Programmable internal pull-up resistors
- Two IRQ Input Pins
- XNOR Chain
- PC99a and ACPI 1.0 Compliant
- 64-Pin STQFP RoHS Compliant Package
- Intelligent Auto Power Management
- One Full Function Serial Port
  - High Speed 16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- Infrared Communications Controller
  - Three IR Ports
  - Multi-Protocol Serial Communications Controllers
  - Two IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - One Consumer IR Port with support for NEC PPM and RC5 with PME Wake-up Option
  - Multiple Base I/O Address options, 15 IRQ Options and 3 DMA Options
- LPC Bus Host Interface
  - Supports LPC Bus frequencies of 19.2MHz to 33MHz
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PCI nCLKRUN Support
  - Power Management Event (IO_PME#) Interface Pin
- LPC PortSwitch Interface
  - Secondary Switchable LPC Interface (3.3V only)
  - Trusted cycles blocked
  - Buffered 14 MHz output
  - Switched PCI Clock output

Description

The Microchip SIO1007 is a 3.3V PC 99 and ACPI 1.0 compliant Super I/O Controller. The SIO1007 implements the LPC interface with the LPC PortSwitch Interface. The LPC PortSwitch Interface is a hot-switchable external Docking LPC interface with trusted cycle block. The SIO1007 also features a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI nCLKRUN support, relocatable configuration ports and three DMA channel options. The part also includes 16 GPIO pins.

The SIO1007 incorporates one 8-pin 16C550A compatible UART. In addition, the SIO1007 provides a second UART to support a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats, as well as Consumer IR. There is a second IR port, which supports NEC PPM and RC5, as well as Consumer IR protocols.

The SIO1007 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. The SIO1007 also features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the UARTs.

The SIO1007 supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows ‘9x, 2K, ME, XP and PC99. The I/O Address, DMA Channel and Hardware IRQ of each device in the SIO1007 may be reprogrammed through the internal configuration registers. There are 192 I/O address location options, a Serialized IRQ interface, and three DMA channels.

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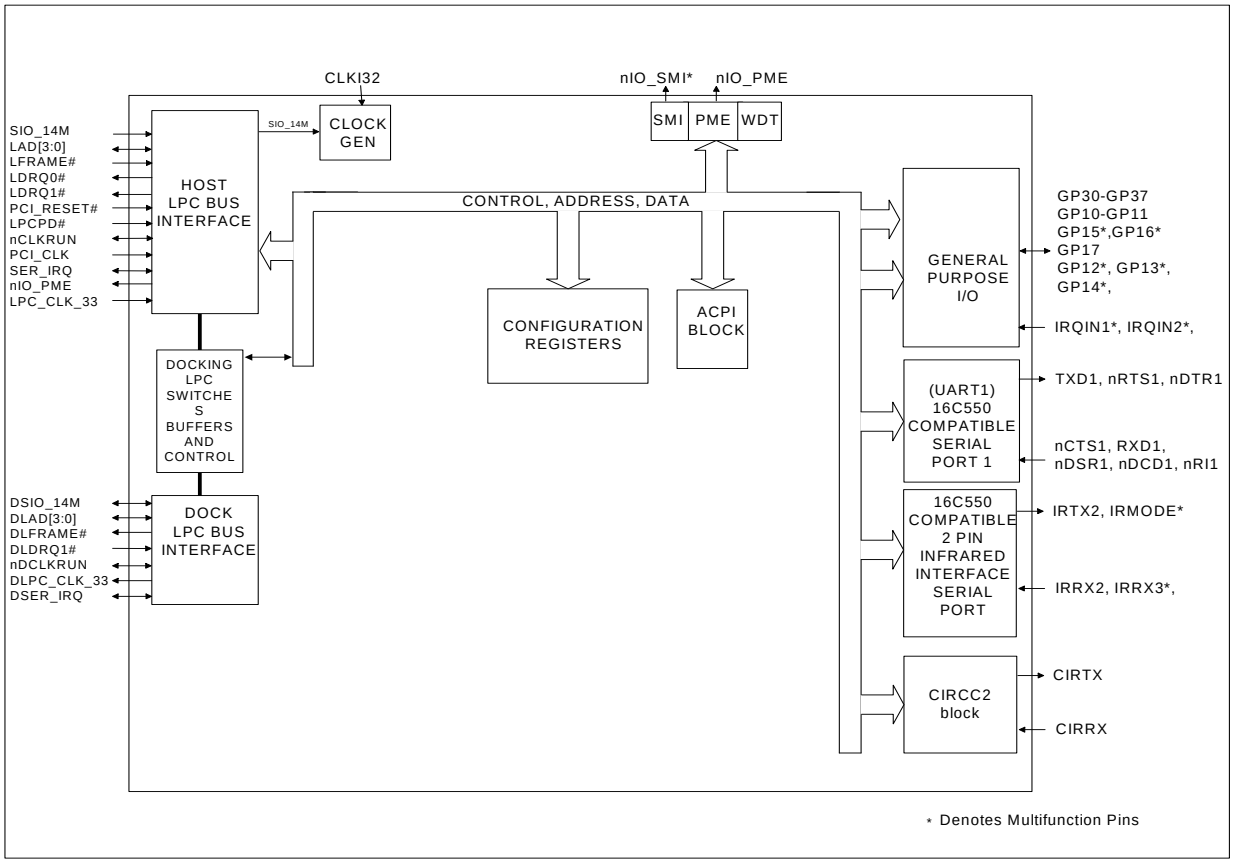
Table of Contents

1.0 Block Diagram 4
2.0 Pin Layout 5
3.0 Pin Configuration 6
4.0 Signal Description 7
5.0 Power Functionality 12
6.0 Super I/O Registers 14
7.0 LPC Interface 15
8.0 LPC PortSwitch 18
9.0 Serial Port (UART) 21
10.0 Infrared Interface 34
11.0 Power Management 40
12.0 Serial IRQ 41
13.0 PCI CLKRUN Support 45
14.0 General Purpose I/O 47
15.0 System Management Interrupt (SMI) 51
16.0 PME Support 52
17.0 Runtime Registers 53
18.0 Configuration 57
19.0 Operational Description 87
20.0 Timing Diagrams 90
21.0 XNOR-Chain Test Mode 100
22.0 Package Outline 103
Appendix A: Data Sheet Revision History 104
The Microchip Web Site 105
Customer Change Notification Service 105
Customer Support 105
Product Identification System 106

1.0 BLOCK DIAGRAM

FIGURE 1-1: SIO1007 Block Diagram

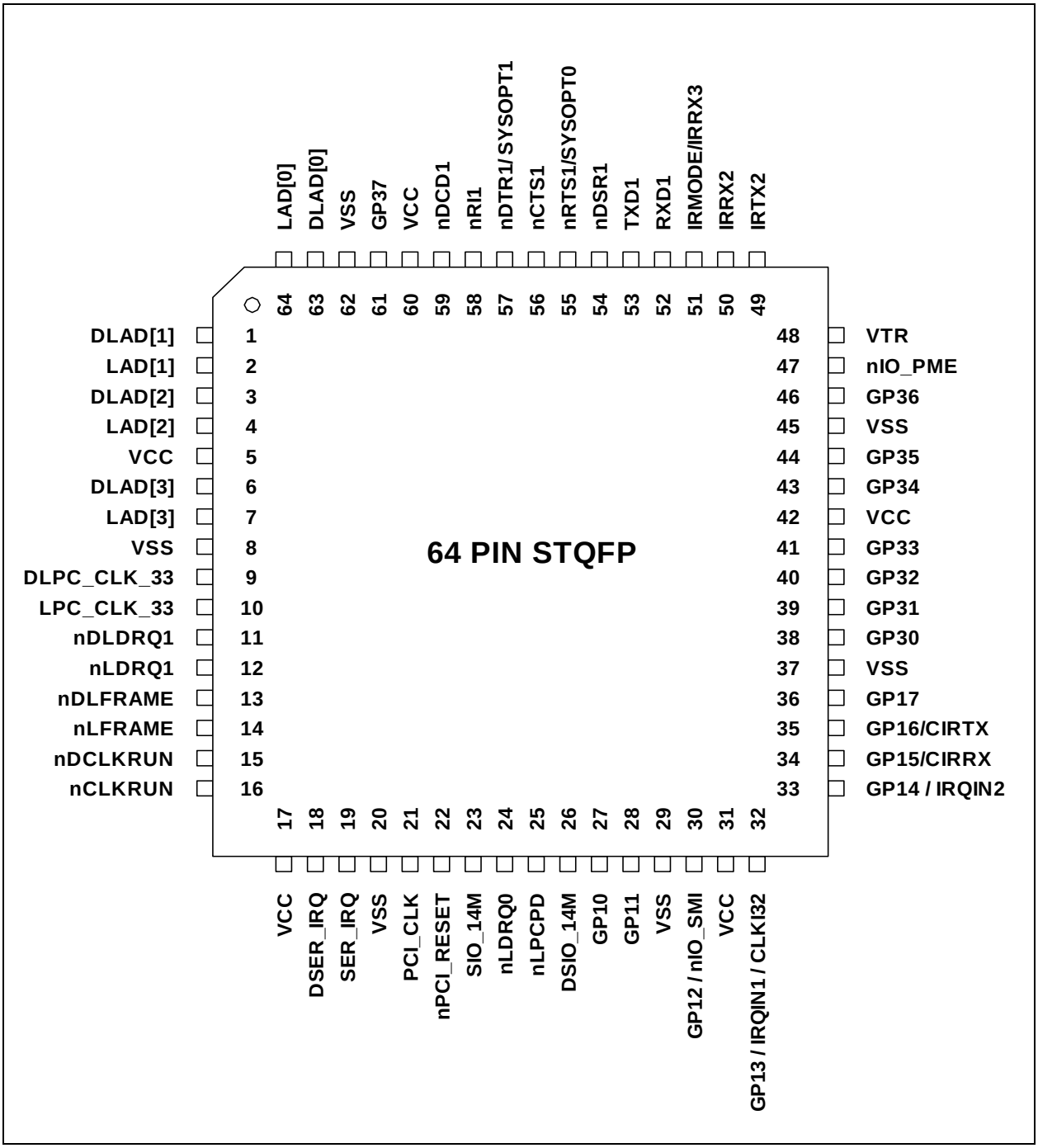


1.1 Reference Documents

- CIRCC 2.X Block Product Architecture Specification Revision 0.7, dated August 26, 2004
- IRCC 2.X Block Data Sheet/Product Architecture Specification (Contact Microchip, unpublished)

2.0 PIN LAYOUT

FIGURE 2-1: SIO1007 64 PIN STQFP



3.0 PIN CONFIGURATION

TABLE 3-1: PIN CONFIGURATION

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	DLAD[1]	17	VCC	33	GP14 / IRQIN2	49	IRTX2
2	LAD[1]	18	DSER_IRQ	34	GP15/CIRRX	50	IRRX2
3	DLAD[2]	19	SER_IRQ	35	GP16/CIRTX	51	IRMODE/IRRX3
4	LAD[2]	20	VSS	36	GP17	52	RXD1
5	VCC	21	PCI_CLK	37	VSS	53	TXD1
6	DLAD[3]	22	nPCI_RESET	38	GP30	54	nDSR1
7	LAD[3]	23	SIO_14M	39	GP31	55	nRTS1/SYSOPT0
8	VSS	24	nLDRQ0	40	GP32	56	nCTS1
9	DLPC_CLK_33	25	nLPCPD	41	GP33	57	nDTR1/ SYSOPT1
10	LPC_CLK_33	26	DSIO_14M	42	VCC	58	nRI1
11	nDLDRQ1	27	GP10	43	GP34	59	nDCD1
12	nLDRQ1	28	GP11	44	GP35	60	VCC
13	nDLFRAME	29	VSS	45	VSS	61	GP37
14	nLFRAME	30	GP12 / nIO_SMI	46	GP36	62	VSS
15	nDCLKRUN	31	VCC	47	nIO_PME	63	DLAD[0]
16	nCLKRUN	32	GP13 /IRQIN1 / CLKI32	48	VTR	64	LAD[0]

4.0 SIGNAL DESCRIPTION

4.1 Pin Functions

TABLE 4-1: PIN FUNCTIONS

STQFP Pin #	Name	Description	Buffer Name	Input Buffer Power Well	Output Buffer Power Well	Notes
POWER AND GROUND PINS (18)						
5, 17, 31, 42, 60	VCC	+3.3 Volt Supply Voltage				
48	VTR	+3.3 Volt Standby Supply Voltage				
23	VBAT	Battery Voltage				
8, 20, 29, 37, 45, 62	VSS	Ground				
CLOCK (1)						
23	SIO_14M	14.318MHz Clock Input	I	VCC	N/A	
PROCESSOR/HOST LPC INTERFACE (11)						
19	SER_IRQ	Serial IRQ pin used with the PCI_CLK pin to transfer interrupts from this device to the host.	PCI_IO	VCC	VCC	4-3
7,4,2, 64	LAD[3:0]	Active high LPC I/O used for multiplexed command, address and data bus.	PCI_IO	VCC	VCC	4-3
14	nLFRAME	Active low input indicates start of new cycle and termination of broken cycle.	PCI_I	VCC	N/A	4-3
24	nLDRQ0	Active low output used for encoded DMA/Bus Master request for the LPC interface.	PCI_O	VCC	VCC	4-3
12	nLDRQ1	Active low signal between this device and the LPC Host used for encoded DMA/Bus Master request for docking LPC Super I/O to the LPC Host.	PCI_O	VCC	VCC	4-3
22	nPCI_RESET	Active low input used as LPC Interface Reset.	PCI_I	VCC	N/A	
25	nLPCPD	Active low input Power Down signal indicates that this device should prepare for power to be shut-off on the LPC interface.	PCI_I	VCC	N/A	4-1 4-3
21	PCI_CLK	PCI clock input.	PCI_ICLK	VCC	N/A	
10	LPC_CLK_33	PCI clock input from clock source dedicated to docking interface.		VCC	VCC	4-3
16	nCLKRUN	This signal is used to indicate the PCI clock status and to request that a stopped clock be started.	PCI_OD	VCC	VCC	4-3
DOCK INTERFACE(11)						
18	DSER_IRQ	Serial IRQ pin between this device and the Docking LPC SIO used with the DLPC_CLK_33 pin to transfer interrupts between this device and the LPC Host.		VCC	VCC	4-3

TABLE 4-1: PIN FUNCTIONS (CONTINUED)

STQFP Pin #	Name	Description	Buffer Name	Input Buffer Power Well	Output Buffer Power Well	Notes
6,3,1, 63	DLAD[3:0]	Active high LPC signals used for multiplexed command, address and data bus between this device and the Docking LPC SIO.		VCC	VCC	4-3
13	nDLFRAME	Active low signal indicates start of new cycle and termination of broken cycle to the Docking LPC SIO.		VCC	VCC	4-3
11	nDLDRQ1	Active low signal between this device and the LPC Host used for encoded DMA/Bus Master request for docking LPC Super I/O to the LPC Host.		VCC	VCC	4-3
9	DLPC_CLK_33	Dedicated PCI clock switch output between this device and the Docking LPC SIO.			VCC	4-3
15	nDCLKRUN	This signal between this device and the Docking LPC SIO is used to indicate the PCI clock status and to request that a stopped clock be started.		VCC	VCC	4-3
26	DSIO_14M	Buffered 14 Mhz clock output between this device and the Docking LPC SIO.	O24		VCC	
SERIAL PORT INTERFACE (8)						
59	nDCD1	Active low Data Carrier Detect inputs for the serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of nDCD signal by reading bit 7 of Modem Status Register (MSR). A nDCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDCD changes state. **Note:** Bit 7 of MSR is the complement of nDCD.	I	VCC	N/A	
54	nDSR1	Active low Data Set Ready inputs for the serial port. Handshake signal, which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of nDSR signal by reading bit 5 of Modem Status Register (MSR). A nDSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDSR changes state. **Note:** Bit 5 of MSR is the complement of nDSR.	I	VCC	N/A	
52	RXD1	Receiver serial data input for port 1.	IS	VCC	N/A	

TABLE 4-1: PIN FUNCTIONS (CONTINUED)

STQFP Pin #	Name	Description	Buffer Name	Input Buffer Power Well	Output Buffer Power Well	Notes
55	nRTS1 (SYSOPT0)	Active low Request to Send outputs for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). nRTS is forced inactive during loop mode operation. At the deasserting edge of PCIRST#, the nRTS pin is latched to determine the configuration base address: 0 = Index Base I/O Address bits A[7:0]= 2E Hex; 1 = Index Base I/O Address bits A[7:0]==4E Hex.	O8	N/A	VCC	4-2
53	TXD1	Transmit serial data output for port 1.	O12	N/A	VCC	
56	nCTS1	Active low Clear to Send inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of nCTS signal by reading bit 4 of Modem Status Register (MSR). A nCTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when nCTS changes state. The nCTS signal has no effect on the transmitter. **Note:** Bit 4 of MSR is the complement of nCTS.	I	VCC	N/A	
57	nDTR1 (SYSOPT1)	Active low Data Terminal Ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the nDTR signal to inactive mode (high). nDTR is forced inactive during loop mode operation. At the deasertting edge of PCIRST#, the nDTR1 pin is latched to determine the configuration base address: 0 = Index Base I/O Address bits A[15:8]=00 Hex; 1 = Index Base I/O Address bits A[15:8]= 16 Hex.	OP14	N/A	VCC	4-2

TABLE 4-1: PIN FUNCTIONS (CONTINUED)

STQFP Pin #	Name	Description	Buffer Name	Input Buffer Power Well	Output Buffer Power Well	Notes
58	nRI1	Active low Ring Indicator inputs for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of nRI signal by reading bit 6 of Modem Status Register (MSR). A nRI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nRI changes state. **Note:** Bit 6 of MSR is the complement of nRI.	I	VTR	N/A	
INFRARED INTERFACE (3)						
50	IRRX2	IR Receive	IS	VTR		
49	IRTX2	IR Transmit	O12		VCC	
51	IRMODE/ IRRX3	IR mode.IR Receive 3.	O6/ IS	VTR	VTR	
MISCELLANEOUS (34)						
34	GP15 /CIRRX	Dedicated General Purpose Input/Output. Consumer IR Receiver	IS/O8/OD8/ IS	VTR	VCC	4-4
35	GP16 /CIRTX	Dedicated General Purpose Input/Output. Consumer IR Transmitter	IO12/OD12/ O12	VTR	VCC	4-4 4-5
27,28,34,35,36,38,39,49,41,43,44,46,61	GP10,GP11 GP15-GP17 GP30-GP37	Dedicated General Purpose Input/Output.	IO8/OD8	VTR	VCC	4-4
30	GP12/ nIO_SMI	General Purpose Input/Output. Active low System Management Interrupt Output.	I(I/O12/OD12) /(O12/OD12	VTR,	VCC	4-4
32	GP13/ IRQIN1/ CLKI32	General Purpose Input/Output. External Interrupt Input. Steerable onto one of the 15 Serial IRQs. 32kHz suspend clock input.	(IS/O8/OD8)/ IS IS	VTR	VCC	4-4
33	GP14/ IRQIN2	General Purpose Input/Output. External Interrupt Input. Steerable onto one of the 15 Serial IRQs.	(I/O8/OD8)/ I	VTR, VCC	VCC	4-4
47	nIO_PME	This active low Power Management Event signal allows this device to request wakeup.	(O12/OD12)		VTR	

Note: The “n” as the first letter of a signal name or the “#” as the suffix of a signal name indicates an “Active Low” signal.

Note 4-1 The LPCPD# pin may be tied high. The LPC interface will function properly if the PCI_RESET# signal follows the protocol defined for the LRESET# signal in the "Low Pin Count Interface Specification".

Note 4-2 The nRTS1/SYSOPT0 and the nDTS1/SYSOPT1 pins require external pullup/pull-down resistors to set the default base I/O address for configuration to 0x002E, 0x004E, 0x162E, or 0x164E.

Note 4-3 The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are not 5V tolerant and do not have ChiProtect.

Note 4-4 These pins have an internal 45uA pull-up that is only active when the programmed via the GPIO Pull-up Registers (CR37-CR38). The default state for the pin is for the pull-up to be enabled.

Note 4-5 IIf CIRTX signal function is used and interfaced to a transceiver requiring duty cycle protection, an external 5KOhm pulldown resistor should be used. In addition the an internal 45µA pullup resistor on the CIRTX pin should be disabled by clearing the the GP16 bit in CR38 on page 82.

4.2 Buffer Type Description

Note: The buffer type values are specified at VCC=3.3V.

TABLE 4-2: BUFFER TYPES

Buffer Type	Description
I	Input, TTL Compatible.
IS	Input with Schmitt Trigger.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
IS/O8	Input with Schmitt Trigger/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
OP14	Output, 14mA sink, 14mA source.
O24	Output, 24mA sink, 12mA source.
PCI_IO	Input/Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 4-6)
PCI_O	Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 4-6)
PCI_I	Input. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 4-6)
PCI_ICLK	Clock Input. These pins must meet the PCI 3.3V AC and DC Characteristics and timing. (Note 4-7)

Note 4-6 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2.

Note 4-7 See the “PCI Local Bus Specification,” Revision 2.1, Section 4.2.2 and 4.2.3.

5.0 POWER FUNCTIONALITY

The SIO1007 has two power planes: VCC and VTR. The SIO1007 is a 3.3 Volt part. Both the VCC and VTR supply are 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values subsection.

5.1 3.3 Volt Operation / 5 Volt Tolerance

The SIO1007 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant and ChiProtect.

A 5V tolerant pin input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

ChiProtect pins can be connected to a powered up external input or output device when the SIO1007 is unpowered. For example, this includes an external device outputting a high to an unpowered pin if the voltage does not exceed the Maximum Ratings, Positive Voltage on any pin, with respect to Ground parameter (+5.5V).

See Table 4-1 and the associated Note 4-4 to identify the non-5V tolerant pins.

5.2 VTR Support

The SIO1007 requires a trickle supply (V_{TR}) to provide sleep current for the programmable wake-up events in the PME interface when V_{CC} is removed. If the SIO1007 is not intended to provide wake-up capabilities on standby current, V_{TR} can be connected to V_{CC}. The V_{TR} pin generates a V_{TR} Power-on-Reset signal to initialize these components.

Note:	If V_{TR} is to be used for programmable wake-up events when V_{CC} is removed, V_{TR} must be at its full minimum potential at least 10 µs before V_{CC} begins a power-on cycle. When V_{TR} and V_{CC} are fully powered, the potential difference between the two supplies must not exceed 500mV.

5.3 Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as V_{CC} cycles on and off. When the internal PWRGOOD signal is “1” (active), $V_{CC} > 2.3V$ (nominal), and the SIO1007 host interface is active. When the internal PWRGOOD signal is “0” (inactive), $V_{CC} \leq 2.3V$ (nominal), and the SIO1007 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The SIO1007 device pins IO_PME#, nRI1, IRRX2, IRTX2, IRMODE/IRRX3 and all GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided V_{TR} is powered. See Trickle Power Functionality section.

5.4 Trickle Power Functionality

When the SIO1007 is running under VTR only, the PME wakeup events are active and (if enabled) able to assert the IO_PME# pin active low. The following lists the wakeup events:

- UART 1 Ring Indicator
- IR Receive (IRRX2)
- CIRCC2 block

Note:	The GP13/IRQIN1/CLKI32 pin must be connected to a 32kHz suspend clock source (i.e., available under VTR and the CLKI32 alternate function programmed on the GP13/IRQIN1/CLKI32 pin) for the NEC PPM and RC5 wake events to be operational.

- GPIOs for wakeup. See below.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means they will, at a minimum, source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup inputs are GP10-GP17, GP20-GP24, GP30-GP37. These GPIOs function as follows:

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are for PME wakeup as a GPIO function (or alternate function).

See the table in the GPIO section for more information.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- Runtime register block (includes all PME, SMI, GP data registers)
- Pins for PME Wakeup:

  GPIOs (GP10-GP17, GP30-GP37)

  IO_PME#

  nRI1, IRRX2

5.5 Maximum Current Values

See the Operational Description section for the maximum current values.

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The pin that is powered by VTR (as output) is IO_PME#. This pin, if configured as a push-pull output, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V).

5.6 Power Management Events (PME/SCI)

The SIO1007 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal. See the PME Support section.

6.0 SUPER I/O REGISTERS

The address map, shown below in Table 6-1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the following blocks can be moved via the configuration registers: Serial Port Com 1, Serial Port Com 2, Synchronous Communications Engine (SCE), CIRCC2, Runtime Registers, Configuration, LPC Docking. Some addresses are used to access more than one register.

6.1 Host Processor Interface (LPC)

The host processor communicates with the SIO1007 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 6-1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide. Section 18.5, "Logical Device Base I/O Address and Range," on page 85 for base address, activation and power control for each logical device.

TABLE 6-1: SUPER I/O BLOCK ADDRESSES

Address	Block Name	Notes
Base+(0-7)	Serial Port Com 1	
ACE:Base1+(0-7) SCE:Base2+(0-7)	Serial Port Com 2 SCE	IR Support FIR and CIR
Base+(0-7)	CIRCC2	Consumer IR Support NEC PPM and RC5
Base + (0-F)	Runtime Registers	
Base + (0-1)	Configuration	
Base + 0	LPC Docking	

Note 1: Refer to the configuration register descriptions for setting the base address.

2: Serial Port COM 2 block provides IR Support (FIR and CIR) but does not have standard 8 pin UART interface.

3: The Runtime Register Block includes all PME, SMI, and GP data registers.

7.0 LPC INTERFACE

The following sub-sections specify the implementation of the LPC bus.

7.1 LPC Interface Signal Definition

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

Signal Name	Type	Description
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset.
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.
IO_PME#	OD	Power Mgt Event signal. Allows the SIO1007 to request wakeup.
LPCPD#	Input	Powerdown Signal. Indicates that the SIO1007 should prepare for power to be shut on the LPC interface.
SER_IRQ	I/O	Serial IRQ.
PCI_CLK	Input	PCI Clock.
CLKRUN#	I/OD	Clock Run. Allows the SIO1007 to request the stopped PCI_CLK be started.

LPC Cycles

The following cycle types are supported by the LPC protocol.

Cycle Type	Transfer Size
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 Byte
DMA Read	1 Byte

The SIO1007 ignores cycles that it does not support.

Field Definitions

The data transfers are based on specific fields that are used in various combinations, depending on the cycle type. These fields are driven onto the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the SIO1007. See the *Low Pin Count (LPC) Interface Specification* Revision 1.0 from Intel, Section 4.2 for definition of these fields.

LFRAME# Usage

LFRAME# is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the SIO1007 to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the SIO1007 monitors the bus to determine whether the cycle is intended for it. The use of LFRAME# allows the SIO1007 to enter a lower power state internally. There is no need for the SIO1007 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the SIO1007 samples LFRAME# active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The LFRAME# signal functions as described in the Low Pin Count (LPC) Interface Specification Revision 1.0.

I/O Read and Write Cycles

The SIO1007 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the SIO1007. DMA write cycles involve the transfer of data from the SIO1007 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the SIO1007 are 1 byte.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

DMA Protocol

DMA on the LPC bus is handled through the use of the LDRQ# lines from the SIO1007 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Specification Revision 1.0.

7.1.1 POWER MANAGEMENT

CLOCKRUN Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.1.

LPCPD Protocol

The SIO1007 will function properly if the nLPCPD signal goes active and then inactive again without nPCI_RESET becoming active. This is a requirement for notebook power management functions.

Although the LPC Bus spec 1.0 section 8.2 states, "After LPCPD# goes back inactive, the LPC I/F will always be reset using LRST#", this statement does not apply for mobile systems. LRST# (PCI_RESET#) will not occur if the LPC Bus power was not removed. For example, when exiting a "light" sleep state (ACPI S1, APM POS), LRST# (PCI_RESET#) will not occur. When exiting a "deeper" sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRST# (PCI_RESET#) will occur.

The LPCPD# pin is implemented as a “local” powergood for the LPC bus in the SIO1007. It is not used as a global powergood for the chip. It is used to reset the LPC block and hold it in reset.

An internal powergood is implemented in SIO1007 to minimize power dissipation in the entire chip.

Prior to going to a low-power state, the system will assert the LPCPD# signal. It will go active at least 30 microseconds prior to the LCLK# (PCI_CLK) signal stopping low and power being shut to the other LPC I/F signals.

Upon recognizing LPCPD# active, the SIO1007 will drive the LDRQ# signal low or tri-state, and do so until LPCPD# goes back inactive.

Upon recognizing LPCPD# inactive, the SIO1007 will drive its LDRQ# signal high.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.2.

SYNC Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2.1.8 for a table of valid SYNC values.

Typical Usage

The SYNC pattern is used to add wait states. For read cycles, the SIO1007 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the SIO1007 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The SIO1007 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.

The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The SIO1007 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the SIO1007 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The SIO1007 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

SYNC Patterns and Maximum Number of SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The SIO1007 has protection mechanisms to complete the cycle.

SYNC Error Indication

The SIO1007 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the SIO1007, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the SIO1007. If the host was writing data to the SIO1007, the data had already been transferred.

In the case of multiple byte cycles, such as DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

I/O and DMA START Fields

I/O and DMA cycles use a START field of 0000.

Reset Policy

The following rules govern the reset policy:

1. When PCI_RESET# goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
2. When PCI_RESET# goes active (low):
   a) the host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
   b) the SIO1007 ignores LFRAME#, tristate the LAD[3:0] pins and drive the LDRQ# signal inactive (high).

7.1.2 LPC TRANSFERS

Wait State Requirements

I/O Transfers

The SIO1007 inserts three wait states for an I/O read and two wait states for an I/O write cycle. A SYNC of 0110 is used for all I/O transfers. The exception to this is for transfers where IOCHRDY would be deasserted in an ISA transfer (i.e., IrCC transfers) in which case the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

DMA Transfers

The SIO1007 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

See the example timing for the LPC cycles in the Timing Diagrams section.

8.0 LPC PORTSWITCH

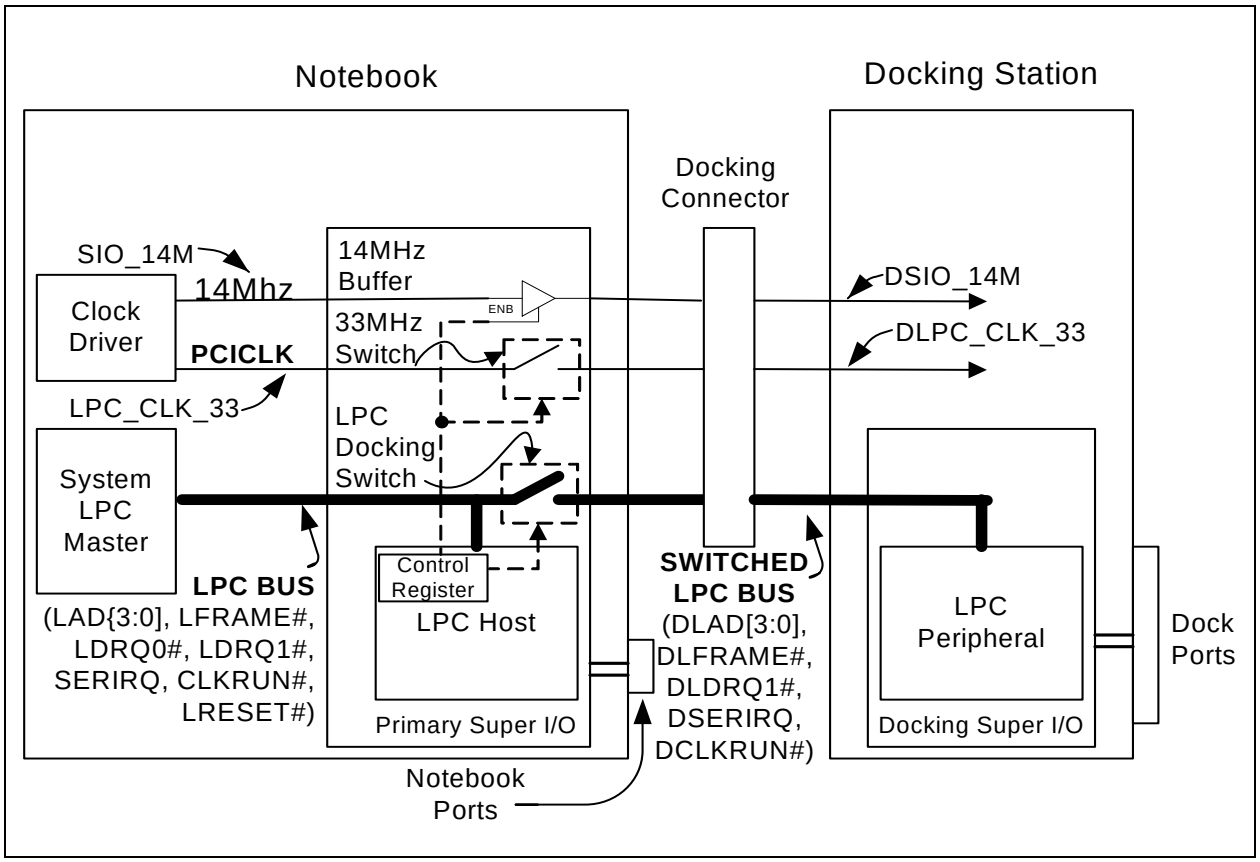
The SIO1007 Portswitch Interface provides a hot-switchable Docking LPC interface available to an external Super I/O device contained within a docking station. The Docking LPC bus signals, when enabled, will be routed through low impedance (≈10Ω), bi-directional switches contained in the SIO1007. The SIO1007 controls the enabling of the LPC docking interface. When the SIO1007 LPC Docking interface is enabled, the SIO1007 autonomously blocks all trusted LPC cycles while forwarding all standard LPC cycles to the LPC Docking interface.

A switchable PCICLK is available to be supplied to an external devices contained within a docking station. The SIO1007 Docking PCICLK output is a low skewed switched version of the input. which, when enabled, is routed through low impedance (≈10Ω), bi-directional switch contained in the SIO1007. The SIO1007 controls the enabling of the Docking PCICLK output.

A switchable 14.318MHz clock is available to external devices contained within a docking station. The SIO1007 Docking 14.318MHz clock output is a buffered version of the input. The SIO1007 controls the enabling of the Docking 14MHz clock output.

See Figure 8-1.for an illustration of a System level docking solution using the LPC PortSwitch Interface.

FIGURE 8-1: DOCKING SOLUTION USING THE LPC PORTSWTICH™ INTERFACE



8.1 LPC PortSwitch Interface

The signals to be switched in the LPC PortSwitch interface are shown in Table 8-1. All signals except SIO_14M and DSIO_14M are 3.3V only. SIO_14M and DSIO_14M are 5 Volt tolerant.

TABLE 8-1: LPC DOCKING INTERFACE

Host Side Interface	Dock Side Interface	Switch Control Bit
LAD[3:0]	DLAD[3:0]	DLPC_SWITCH
LFRAME#	DLFRAME#	DLPC_SWITCH
LDRQ1#	DLDRQ1#	DLPC_SWITCH
NCLKRUN	NDCLKRUN	DLPC_SWITCH
SER_IRQ	SER_IRQ	DLPC_SWITCH
LPC_CLK_33	DLPC_CLK_33	DCLK_33
SIO_14M	DSIO_14M	DCLK_14

APPLICATION NOTE: The system design must include weak pullup resistors in the docking station (~100KOhm) on the DLAD[3:0] and DLFRAME# signals to maintain an inactive docking LPC interface.

8.2 PortSwitch Docking Controls

The SIO1007 provides three programmable bits which independently control the switching of the 14.318MHz clock and the dedicated docking PCICLK and the remainder of the LPC interface. The switching is provided in the Docking LPC Switch Register described in Section 8.3.1.

8.3 Registers

8.3.1 LOGICAL DEVICE FOR LPC DOCKING.

The LPC Docking Base Address Registers (CR3B and CR3C) are used to select the base address of LPC Docking runtime register space. Valid addresses for LPC Docking runtime register space can be set to locations on single-byte boundaries from 100H - FFFH. To disable LPC Docking runtime register decoding, set the Docking Activate Register (CR3A)-bit 3 to ‘0’. When writing the LPC Docking Base Address registers (CR3B and CR3A) the set LPC Docking Activate Register (CR3A) -bit 3 must be set to ‘0’.

For detailed description of the LPC Docking Activate Register (CR3A) and the LPC Docking Base Address Registers (CR3B and CR3C.) See Section 18.0 for details description of Configuration Registers.

8.3.2 DOCKING LPC SWITCH REGISTER

The Docking LPC Switch Register controls the connection and disconnection of the Docking LPC Interface.

TABLE 8-2: DOCKING LPC SWITCH REGISTER

Address	DLPC Runtime Registers Base Address + 0
Power	VCC
DEFAULT	00h

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R	R	R	R	R	R	R	R/W
BIT Name	RESERVED					DCLK_14	DCLK_33	DLPCSWITCH

DLPC_SWITCH – D0

When DLPC SWITCH is asserted ‘1’, the bi-directional Docking LPC switches will be switched on and the DLPC pin connections will be connected to the LPC bus. When DLPC SWITCH is deasserted ‘0’, the DLPC pin connections will be disconnected from the LPC bus.

DCLK_33– D1

When DCLK_33 bit is asserted ‘1’, the bi-directional switch for the dedicated docking PCICLK will be switched on and the DLPC_CLK_33 pin will be connected to the LPC_CLK_33 pin. When DCLK_33 bit is deasserted ‘0’, the DLPC_-CLK_33 pin will be disconnected from the LPC_CLK_33 pin and the DLPC_CLK_33 pin will be an open circuit.

Note:	The PCICLK signals are not bi-directional however, the switch only provides a low series impedance (≈10Ω).

DCLK_14– D2

When DCLK_14 bit is asserted ‘1’, the buffer is enabled and the DSIO_14M pin will provide a buffered version DSIO_14M pin. When DCLK_14 bit is deasserted ‘0’, the DSIO_14M pin will be tri-stated.

9.0 SERIAL PORT (UART)

The SIO1007 incorporates one 8-pin 16C550A compatible UART. In addition, the SIO1007 provides an second UART supporting a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats (used by Sharp and other PDAs), as well as Consumer IR. See Section 10.0, for description of Infrared Interface.

The SIO1007 incorporates two full function UARTs. They are compatible with the 16450, the 16450 ACE registers and the 16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA 1.2 (4Mbps), HP-SIR, ASK-IR and Consumer IR infrared modes of operation.

9.1 Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The SIO1007 contains two serial ports, each of which contain a register set as described below.

TABLE 9-1: ADDRESSING THE SERIAL PORT

DLAB (Note 9-1)	A2	A1	A0	Register Name
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

Note 9-1 DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

9.1.1 RECEIVE BUFFER REGISTER (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

9.1.2 TRANSMIT BUFFER REGISTER (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

9.1.3 INTERRUPT ENABLE REGISTER (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SIO1007. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2

This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic "0".

9.1.4 FIFO CONTROL REGISTER (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level.

Note:	DMA is not supported. The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16). See the Configuration section for description on these registers.

Bit 0

Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. DMA modes are not supported in this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

9.1.5 INTERRUPT IDENTIFICATION REGISTER (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic "0".

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

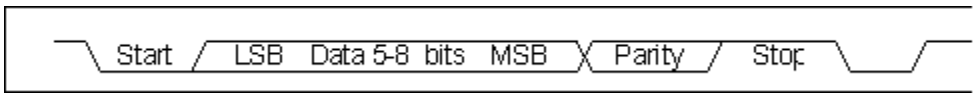
TABLE 9-2: INTERRUPT CONTROL TABLE

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

9.1.6 LINE CONTROL REGISTER (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE

FIGURE 9-1: SERIAL DATA



This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

Bit 2	Word Length	Number of Stop Bits
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3

Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4

Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5

Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6

Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7

Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

9.1.7 MODEM CONTROL REGISTER (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8-bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. he receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7

These bits are permanently set to logic zero.

9.1.8 LINE STATUS REGISTER (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note:	Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode, this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

Bit 7

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

9.1.9 MODEM STATUS REGISTER (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0

Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1

Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3

Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note:	Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4

This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5

This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6

This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7

This bit is the complement of the Data Carrier

Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

9.1.10 SCRATCHPAD REGISTER (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8-bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

9.2 Programmable Baud Rate Generator (AND Divisor Latches DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded, the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 9-3 shows the baud rates possible.

9.3 Effect of The Reset on Register File

The Reset Function Table (Table 9-4) details the effect of the Reset input on each of the registers of the Serial Port.

9.4 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

a) The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
b) The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
c) The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
d) The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

a) A FIFO timeout interrupt occurs if all the following conditions exist:

   At least one character is in the FIFO.

   The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).

   The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

   This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12-bit character.
b) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
c) When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
d) When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

a) The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

b) The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

9.5 FIFO Polled Mode Operation

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.

Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.

Bit 5 indicates when the XMIT FIFO is empty.

Bit 6 indicates that both the XMIT FIFO and shift register are empty.

Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

TABLE 9-3: BAUD RATES

Desired Baud Rate	Divisor Used to Generate 16X Clock	Percent Error Difference Between Desired and Actual (Note 9-2)	High Speed Bit (Note 9-3)
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note 9-2 The percentage error for all baud rates, except where indicated otherwise, is 0.2%.

Note 9-3 The High Speed bit is located in the Device Configuration Space.

TABLE 9-4: RESET FUNCTION TABLE

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

TABLE 9-5: REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL

Regiser Address (Note 9-4)	Register Name	Reg. Symbol	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 9-5)	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Modem Status Interrupt (EMSI)	0	0	0	0
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit	Interrupt ID Bit	Interrupt ID Bit (Note 9-9)	0	0	FIFOs Enabled (Note 9-9)	FIFOs Enabled (Note 9-9)
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 9-11)	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select (Note 9-11)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)	OUT1 (Note 9-7)	OUT2 (Note 9-7)	Loop	0	0	0
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 9-6)	Error in RCVR FIFO (Note 9-9)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)	Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
ADDR = 7	Scratch Register (Note 9-8)	SCR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

UART Register Summary Notes:

Note 9-4 DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 9-5 Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 9-6 When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Note 9-7 This bit no longer has a pin associated with it.

Note 9-8 When operating in the XT mode, this register is not available.

Note 9-9 These bits are always zero in the non-FIFO mode.

Note 9-10 Writing a one to this bit has no effect. DMA modes are not supported in this chip.

Note 9-11 The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16).

9.6 Notes on Serial Port Operation

9.6.1 FIFO MODE OPERATION

GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

9.6.2 TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO, the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

9.7 Logical Device IRQ and DMA Operation

Any time the IRQ or DMA channel for a UART logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel is disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (active bit or address not valid).

The Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupts disabled.

Disabling DMA Enable bit, disables DMA for UART2. Refer to the IrCC specification.

9.8 Output Pin States

The TXD1, nRTS1 & nDTR1 pin states change prior to intialization depending on VCC POR, and the state of the UART1 Power bit (bit[3] in CR02 on page 61).

TABLE 9-6: OUTPUT PIN STATES

Power CR02 Bit[3]	VCC POR	State of TXD1, nRTS1 & nDTR1 Pins
0 Default	Active edge	Tristate
0	After POR	Tristate
1		HIGH

10.0 INFRARED INTERFACE

The SIO1007 contains two infrared (IR) blocks: IRCC2.0 and CIRCC2. The IRCC2.0 block is an IrDA v1.2 compliant port and the CIRCC2.0 block is a dedicated Consumer IR port.

The SIO1007 IRCC2.0 block provides a two-way wireless communications port using infrared as the transmission medium. The IRCC2.0 block provides the following protocols: IrDA v1.2 (SIR/FIR), ASKIR, and Consumer IR. For detailed description of the IRCC2.0 block see IRCC 2.X Block Data Sheet (Contact Microchip, unpublished) The IRCC2.0 block implemented in the SIO1007 has a Chip ID value of 0xF2 in SCE Register, Block 3, Address 2 and contains a GP Counter, Dual IR support and a 128 byte FIFO.

The SIO1007 CIRCC2.0 block provides a wireless communications port for receiving and transmitting CIR protocols. In particular, it has special logic to recognize and decode NEC PPM and RC5 protocols. When the 8051 and the host are both in a sleep state, the CIR block can be configured to generate a wake event when it detects a command via one of these protocols. For detailed description of the CIRCC2.0 block see CIRCC 2.X Block Specification Revision 0.7, dated August 26, 2004.

10.1 CIR and FIR Overview

10.1.1 IRDA SIR/FIR AND ASKIR

IrDA SIR (v1.0) specifies asynchronous serial communication at baud rates up to 115.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by the absence of an infrared pulse during the bit time. Please refer to Section 20.0, "Timing Diagrams" for the parameters of these pulses and the IrDA waveforms.

IrDA FIR (v1.2) includes IrDA v1.0 SIR and additionally specifies synchronous serial communications at data rates up to 4Mbps.

Data is transferred LSB first in packets that can be up to 2048 bits in length. IrDA v1.2 includes 576Mbps and 1.152Mbps data rates using an encoding scheme that is similar to SIR. The 4Mbps data rate uses a pulse position modulation (PPM) technique.

The ASKIR infrared allows asynchronous serial communication at baud rates up to 19.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a 500KHz carrier waveform for the duration of the serial bit time. A one is signaled by the absence of carrier during the bit time. Refer to Section 20.0, "Timing Diagrams" for the parameters of the ASKIR waveforms.

10.1.2 CONSUMER IR

The SIO1007 Consumer IR interface is a general-purpose Amplitude Shift Keyed encoder/decoder with programmable carrier and bit-cell rates that can emulate many popular TV Remote encoding formats; including, 38KHz PPM, NEC PPM and RC5. The carrier frequency is programmable from 1.6MHz to 6.25KHz. The bit-cell rate range is 100KHz to 390Hz.

10.2 IRCC2.0 Infrared Interface

The IrDA v1.0 (SIR) and ASKIR formats are driven by the ACE registers found in UART2. The UART2 registers are described in "Serial Port (UART)" section. The base address for UART2 is programmed in CR25, the UART2 Base Address Register (see CR25 on page 74).

The IrDA V1.2 (FIR) and Consumer IR formats are driven by the SCE registers. Descriptions of these registers can be found in the Infrared Communications Controller Specification. The Base Address for the SCE registers is programmed in CR2B, the SCE Base Address Register (see CR2B on page 76, CR1E on page 71). The base address may be programmed when the SCE (FIR) logical device activate bit in CR3A-bit0 is cleared to 0 and no address decoding takes place for the SCE (FIR) logical device.

10.2.1 IRCC2.0 HARDWARE INTERFACE

The IRCC2.0 IR hardware interface is shown in FIGURE 10-1: on page 36. This interface supports two types of external FIR transceiver modules. One uses a mode pin (IR Mode) to program the data rate, while the other has a second Rx data pin (IRRX3). These functions are selected through CR29 as shown in Table 10-1.

TABLE 10-1: FIR TRANSCEIVER MODULE-TYPE SELECT

HP Mode (Note 10-1)	Function
0	IR Mode
1	IRRX3

Note 10-1 HPMODE is CR29, BIT 4 (see CR29 on page 75). Refer to Figure 10-1, "Infrared Interface Block Diagram" for HPMODE implementation.

The FAST bit is used to select between the SIR mode and FIR mode receiver, regardless of the transceiver type. If FAST = 1, the FIR mode receiver is selected; if FAST = 0, the SIR mode receiver is selected (Table 10-2).

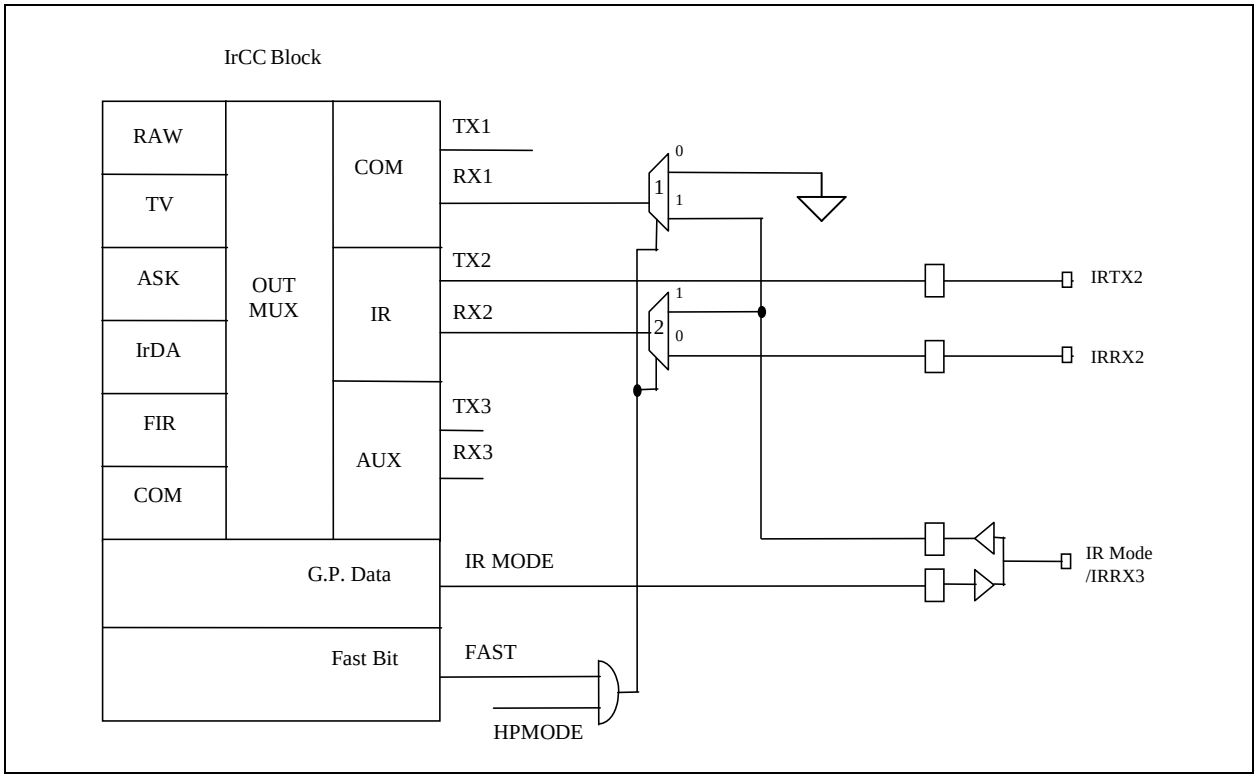
TABLE 10-2: IR RX DATA PIN SELECTION

Control Signals		Inputs	
FAST	**HPMODE**	**RX1**	**RX2**
0	X	RX1=RXD2	RX2=IRRX2
X	0	RX1=RXD2	RX2=IRRX2
1	1	RX1=IR Mode/IRRX3	RX2=IR Mode/IRRX3

10.2.2 IR HALF DUPLEX TURNAROUND DELAY TIME

If the Half Duplex option is chosen there is an IR Half Duplex Time-out that constrains IRCC direction mode changes. This time-out starts as each bit is transferred and prevents direction mode changes until the time-out expires. The timer is restarted whenever new data arrives in the current direction mode. For example, if data is loaded into the transmit buffer while a character is being received, the transmission will not start until the last bit has been received and the time-out expires. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The Half Duplex Time-out is programmable from 0 to 25.5ms in 100 s increments (see CR2D on page 77).

FIGURE 10-1: INFRARED INTERFACE BLOCK DIAGRAM



10.2.3 IRCC2.0 IRTX TRANSMIT PINS

The IRTX2 pin defaults to output, low on VCC POR and PCI Reset. This pin is not powered by VTR. This pin functions as described below.

Following a VCC POR, the IRTX2 pins will be output and low. They will remain low until one of the following conditions are met.

IRTX2 Pin (CR0A on page 63 bits [7:6]=01):

- This pin will remain low following a VCC POR until serial port 2 is enabled by setting the UART2 power down bit (CR02, bit 7), at which time the pin will reflect the state of the IR transmit output of the IRCC block (if IR is enabled through the IR Option Register for Serial Port 2).

The IRTX2 pin will be driven low whenever serial port 2 is disabled (UART2 power down bit is cleared).

Note that bits[7,6] of CR0A can be used to override this functionality of driving the IRTX2 pin low when UART2 is powered down. If these bit are set to '11', then the IRTX2 pin is high-z.

10.2.4 GENERATING IRCC2.0 INTERRUPT EVENTS

The IRCC2.0 block generates one type of interrupt event: a runtime event.

The runtime event (if enabled) may be reported as an SMI event or a Serial IRQ event.

The description of the “INT” that is used to generate a runtime event from the SCE block. The interrupt status and enable bits in the IRCC2,0 block are defined in the IRCC 2.X Block Data Sheet (Contact Microchip, unpublished). If a runtime event occurs bit[1] of the SMI_STS2 register at offset 09h of the Runtime register block will be set. If bit[1] of the SMI_EN2 register is one and if SMI’s are enabled on the IO_SMI# pin an SMI event will be generated.

This runtime event can also be routed to the Serial IRQs. To enable Serial IRQs for the IRCC2.0 runtime events, software must select an IRQ channel in the UART Interrupt Selection register. See CR28 on page 74.

APPLICATION NOTE: To generate a Serial IRQ for the IRCC2.0 block, the ACE block must be located in a valid Base I/O range and the OUT2 bit in the MCR register must be set to 1.

10.3 IRDA PME Wakeup

The IR Receive activity can wake up the system from a sleep state using the SIO1007 nIO_PME output. The IRRX2 pin wake event is falling edge detected.

APPLICATION NOTE: Very narrow pulses, which are rejected by the IRCC block, can generate wakeup events.

10.4 CIRCC2 Infrared Interface

The following section describes the features that are unique to the CIRCC2 block in the SIO1007. For more information, consult the CIRCC 2.X Block Specification Revision 0.7, dated August 26, 2004.

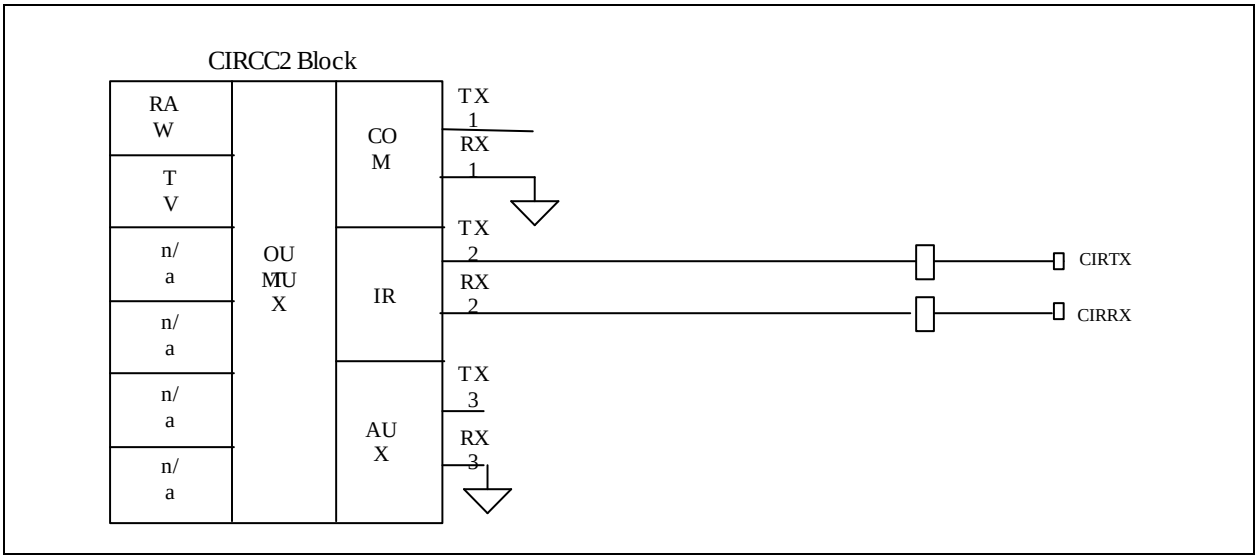
10.4.1 CIRCC2 PIN INTERFACE

The CIRRX and CIRTX signals that are multiplexed on the GP15 and GP16 pins respectively are used to interface to the CIRCC2 block.

APPLICATION NOTE: If CIRTX signal function is used and interfaced to a transceiver requiring duty cycle protection, an external 5KOhm pulldown resistor should be used. In addition the an internal 45µA pullup resistor on the CIRTX pin should be disabled by clearing the the GP16 bit in CR38 on page 82.

The CIRCC2 block has three ports that can be used to bring out the IR signals to three different pairs of pins. In the SIO1007 implementation, only one of these ports is utilized (See Figure 10-2). This port is selected by the CIRCC2 Output Mux bits, which may be programmed in the CR0A Configuration Register (see Section 18.4.11, "CR0A," on page 63) or in the SCE Configuration Register B, which is located in the CIRCC2 Runtime Registers. The SCE Configuration Register B is located in Register Block One of the CIRCC2 Runtime Registers, which is defined in the CIRCC 2.X Block Specification Revision 0.7, dated August 26, 2004.

FIGURE 10-2: CIRCC2 INFRARED INTERFACE BLOCK DIAGRAM



10.4.2 CIRCC2 OPERATIONAL POWER STATES

The CIRCC2 block is powered by VTR. This block is fully operational under VCC and supports NEC PPM and RC5 wake events under VTR only (VCC=0V).

When VCC is on, the CIRCC2 clock source is derived from the 14.318MHz clock input. When VCC is off, the CIRCC2 clock source may be derived from the internal PLL to provide clock support for the CIR wake features. The CIR wake features are only operational if the CLOCKI32 pin is connected to a 32kHz suspend clock, the alternate function on the GP13/IRQIN1/CLKI32 pin is configured for CLOCKI32, and the CLOCKI32 PLL is powered.

The CLOCKI32 signal is the alternate function on the GP13/IRQIN1/CLKI32 pin. The functions for this pin are selected by the CR34 on page 80.

The CLOCKI32 PLL is enabled when VCC transitions to the OFF state if the PLL is Powered. The PLL defaults to the off state to conserve power. To enable the PLL to operate when the device is in a sleep state (VTR Only) the CIRCC2 PLL can be enabled via the CIRCC2 PLL Power bit located in bit[5] of CR02. See CR02 on page 61.

10.4.3 CONFIGURING THE CIRCC2 BLOCK

The CIRCC2 block defaults to the powered down state. To enable the CIRCC2 block to be operational the CIRCC2 logical Device Base address must initialized via CR1F and CR20, the activate bit in CR3A-bit2 set to one and the CIRCC2 Power Down bit in CR02 must be set to one.

The configuration and control registers for the CIRCC2 block are located in the SCE registers defined in the Consumer Infrared Communications Controller 2 (CIRCC2) specification. Some of these registers are shadowed in the SIO1007 Configuration Registers. The following table summarizes all the registers that are shadowed in the configuration register space for the CIRCC2 block. The table lists the Configuration register location, the corresponding SCE register location, the read/write ability in both locations and the POR conditions for each corresponding location.

TABLE 10-3: SUMMARY OF POR AND READ/WRITE CONDITIONS FOR CIRCC2 SHADOWED REGISTERS/BITS

CR#	Configuration Register/Bits	SCE/ACE Registers/Bits	Read/Write		POR Condition for Specific Bits	
			CR	SCE	CR	SCE
CR0A	ECP FIFO Threshold/IR MUX • Bits[5:4] CIRCC2 Output Mux	SCE: Register Block 1, Address 1, • Bits[D7:D6] Output Mux for CIRCC2 Block	R/W	R/W	VTR Only	VTR Only
CR0B	CIRCC2 Mode Register • Bits[5:0]	SCE: Register Block 1, Address 0, • Bits[5:0] are shadowed in Register Block 1, Address 0, bits[D5:D0]	R/W	R/W	VTR Only	VTR Only
CR18	CIRCC2 IRQ/DMA Select Register • Bits[7:4] CIRCC2 IRQ Select • Bits[3:0] CIRCC2 DMA Select	SCE: Register Block 3, Address 4, • Bits[7:4] CIRCC2 IRQ Select • Bits[3:0] CIRCC2 DMA Select	R/W	Read-Only	VCC	-
CR19	CIRCC2 Software Select A	SCE: Register Block 3, Address 5	R/W	Read-Only	VCC	-
CR1A	CIRCC2 Software Select B	SCE: Register Block 3, Address 6	R/W	Read-Only	VCC	-
CR1B	CIRCC2 Half Duplex Timeout (Note 10-2)	SCE: Register Block 5, Address 1	Yes	Yes	VCC	VTR Only

Note 10-2 The CIRCC2 Half Duplex Timeout register (shaded in the table below) is reset on a VCC POR in Config space, which overrides the SCE condition to reset on VTR POR only

Note 10-3 The CIRCC2 SCE registers are implemented as blocks of registers that are directly addressable at the programmed CIRCC2 Base I/O Address plus an offset.

10.4.4 GENERATING CIRCC2 INTERRUPT EVENTS

The CIRCC2 block generates two types of interrupt events: a wake event and a runtime event.

The wake event, if enabled, can be used to generate a PME event to wake the system. The CIRCC2 block can be used to generate a wake event for an NEC PPM and RC5 event. To generate a wake event, the CIRCC2 block must first be powered and enabled (see CIRCC2 Operational Power States on page 38). The CIR mode, NEC PPM and RC5, is configured directly in the SCE registers. The PME event is reported in bit[1] of the PME_STS2 register at offset 03h of the Runtime Register block. This status event can be used to generate a PME interrupt if bit[2] of the PME_EN2 register is enabled and PMEs are enabled in the PME_EN register at offset 01h. See Section 17.0, "Runtime Registers," on page 53.

The runtime event (if enabled) may be reported as an SMI event or a Serial IRQ event. The following diagram shows the interrupt event (INT) that is used to generate a runtime event. To have a runtime event, the individual status events must be enabled. In addition to the individual interrupt enables, the Master Interrupt Enable located in the SCE Master Block Control Register must also be enabled. These interrupt status and enable bits are defined in the Consumer Infrared Communications Controller 2 (CIRCC2) specification. If a runtime event occurs bit[3] of the SMI_STS2 register at offset 09h of the Runtime register block will be set. If bit[3] of the SMI_EN2 register is one and if SMI's are enabled on the IO_SMI# pin an SMI event will be generated.

This runtime event can also be routed to the Serial IRQs. To enable Serial IRQs for the CIRCC2 runtime events software must select an IRQ channel in the CIRCC2 IRQ/DMA Select register. See CR18 on page 68.

11.0 POWER MANAGEMENT

Power management capabilities are provided for the following logical devices: UART 1, and UART 2. For each logical device, two types of power management are provided: direct powerdown and auto powerdown.

11.1 UART Power Management

Direct power management is controlled by CR02. Refer to the Configuration section for more information.

Auto Power Management is enabled by the UART1 and UART2 enable bits in CR07. When set, these bits allow the following auto power management operations:

1. The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2. The receiver enters powerdown when the following conditions are all met:
   a) Receive FIFO is empty
   b) The receiver is waiting for a start bit.

Note:	While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

11.1.1 EXIT AUTO POWERDOWN

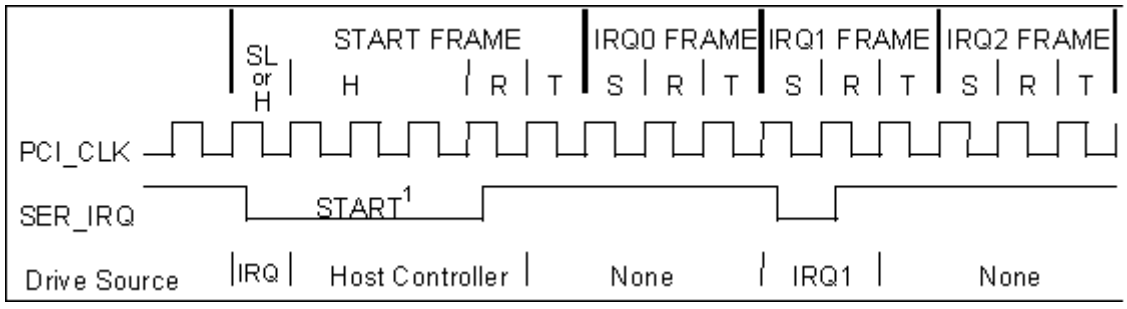
The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.

12.0 SERIAL IRQ

The SIO1007 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0. The PCI_CLK, SER_IRQ and nCLKRUN pins are used for this interface. The Serial IRQ/CLKRUN Enable bit D7 in CR29 activates the serial interrupt interface.

12.1 Timing Diagrams for SER_IRQ Cycle

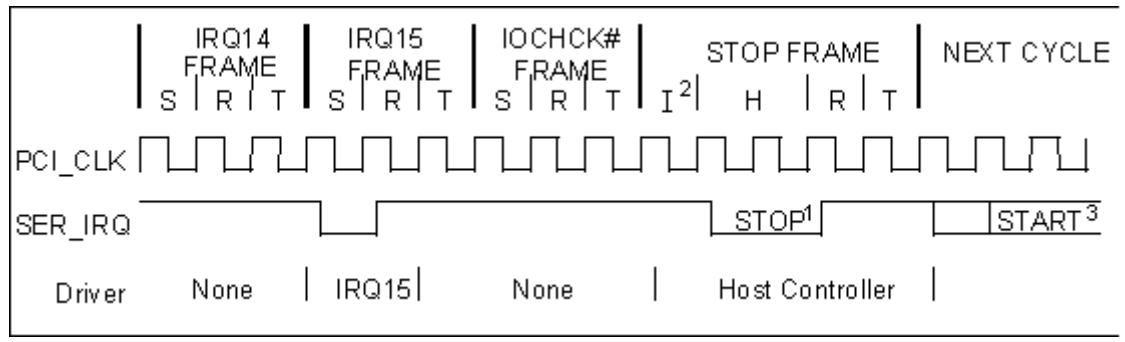
a) Start Frame timing with source sampled a low pulse on IRQ1



Note: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample

1. Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

b) Stop Frame Timing with Host using 17 SER_IRQ sampling period



Note: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle

1. Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
2. There may be none, one or more Idle states during the Stop Frame.
3. The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

12.1.1 SER_IRQ CYCLE CONTROL

There are two modes of operation for the SER_IRQ Start Frame.

1) **Quiet (Active) Mode**: Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ is immediately tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated, the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The SIO1007) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle.

2) **Continuous (Idle) Mode**: Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.

12.1.2 SER_IRQ DATA FRAME

Once a Start Frame has been initiated, the SIO1007 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase, the SIO1007 drives the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ is left tri-stated. During the Recovery phase, the SIO1007 drives the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase, the SIO1007 tri-states the SER_IRQ. The SIO1007 will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

TABLE 12-1: SER_IRQ SAMPLING PERIODS

SER_IRQ Period	Signal Sampled	# of Clocks Past Start
1	Not Used	2
2	IRQ1	5
3	nIO_SMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame supports IRQ2 from a logical device on Period 3, which can be used for the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices Serial Port 1, Serial Port 2 have IRQ13 as a choice for their primary interrupt.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the nIO_SMI pin via bit 7 of the SMI Enable Register 2.

12.1.3 STOP CYCLE CONTROL

Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuous mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

12.1.4 LATENCY

Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

12.1.5 EOI/ISR READ LATENCY

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

12.1.6 AC/DC SPECIFICATION ISSUE

All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

12.1.7 RESET AND INITIALIZATION

The SER_IRQ bus uses PCI_RESET# as its reset signal. The SER_IRQ pin is tri-stated by all agents while PCI_RESET# is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to ensure SER_IRQ bus is in IDLE state before the system configuration changes.

12.2 Routable IRQ Inputs

The routable IRQ input (IRQINx) functions are muxed onto GP13 and GP14 respectively as inputs. The IRQINx pin's IRQ time slot in the Serial IRQ stream is selected via a 4-bit control register for each IRQIN function (CR29 for IRQIN1, CR2A for IRQIN2). A value of 0000 disables the IRQ function.

The part is able to generate a PME and an SMI from both of the IRQ inputs through the GPIO bits in the PME and SMI status and enable registers. The edge is programmable through the polarity bit of the GPIO control register.

User Note: In order to use an IRQ for one of the IRQINx inputs that are muxed on the GPIO pins, the corresponding IRQ must not be used for any of the devices in the SIO1007. Otherwise contention may occur.

APPLICATION NOTE: If GPIO function is selected on GP13/IRQIN1/CLKI32 and GP14/IRQIN2 pins and if IRQ is selected using the routing registers (CR29 for IRQIN1 and CR2A for IRQIN2), IRQs will be generated on the Serial IRQ stream. The state of the GPIO pins will be reflected on the serial IRQ stream. The IRQ selection bits should be ‘0000’ in the IRQ routing registers when GPIO functions are used. These IRQ selection bits default to ‘0000’ on VCC POR.

13.0 PCI CLKRUN SUPPORT

13.1 Overview

The SIO1007 supports the PCI nCLKRUN signal. nCLKRUN is used to indicate the PCI clock status as well as to request that a stopped clock be started. See Figure 13-1 for an example of a typical system implementation using nCLKRUN.

If the SIO1007 SIRQ_CLKRUN_EN signal is disabled, it will disable the nCLKRUN support related to LDRQ# in addition to disabling the SER_IRQ and the nCLKRUN associated with SER_IRQ.

nCLKRUN is an open drain output and an input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the nCLKRUN function.

13.2 nCLKRUN for Serial IRQ

The SIO1007 supports the PCI CLKRUN# signal for the Serial IRQs. If an SIO interrupt occurs while the PCI clock is stopped, nCLKRUN is asserted before the serial interrupt signal is driven active.

See Using nCLKRUN section below for more details.

13.3 nCLKRUN for LDRQ#

CLKRUN# support is also provided in the SIO1007 for the LDRQ# signal. If a device requests DMA service while the PCI clock is stopped, CLKRUN# is asserted to restart the PCI clock. This is required to drive the LDRQ# signal active.

See Using nCLKRUN section for more details.

13.4 Using nCLKRUN

If nCLKRUN is sampled “high”, the PCI clock is stopped or stopping. If nCLKRUN is sampled “low”, the PCI clock is starting or started (running). If a device in the SIO1007 asserts or de-asserts an interrupt or asserts a DMA request, and nCLKRUN is sampled “high”, the SIO1007 requests the restoration of the clock by asserting the nCLKRUN signal asynchronously (Table 13-1). The SIO1007 holds nCLKRUN low until it detects two rising edges of the clock. After the second clock edge, the SIO1007 disables the open drain driver (Figure 13-2).

The SIO1007 will not assert nCLKRUN under any conditions if SIRQ_CLKRUN_EN is inactive (“0”). The SIRQ_CLKRUN_EN bit is D7 in CR29.

The SIO1007 will not assert nCLKRUN if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in Figure 13-1. The SIO1007 will not assert nCLKRUN unless the line has been deasserted for two successive clocks; i.e., before the clock was stopped (Figure 13-2).

TABLE 13-1: SIO1007 NCLKRUN FUNCTION

SIRQ_CLKRUN_EN	Internal Interrupts/ DMA Requests	nCLKRUN	Action
0	X	X	None
1	NO CHANGE	X	None
	CHANGE/ASSERTION (Note 13-1)	0	None
		1	Assert nCLKRUN (Note 13-2)

Note 13-1 “Change/Assertion” means either-edge change on any internal IRQs routed to the SIRQ block or assertion of an internal DMA request by a device in SIO1007. The “assertion” detection logic runs asynchronously to the PCI Clock and regardless of the Serial IRQ mode; i.e., “continuous” or “quiet”.

Note 13-2 The nCLKRUN signal is ‘1’ for at least two consecutive clocks before SIO1007 asserts (‘0’) it.

FIGURE 13-1: NCLKRUN SYSTEM IMPLEMENTATION EXAMPLE

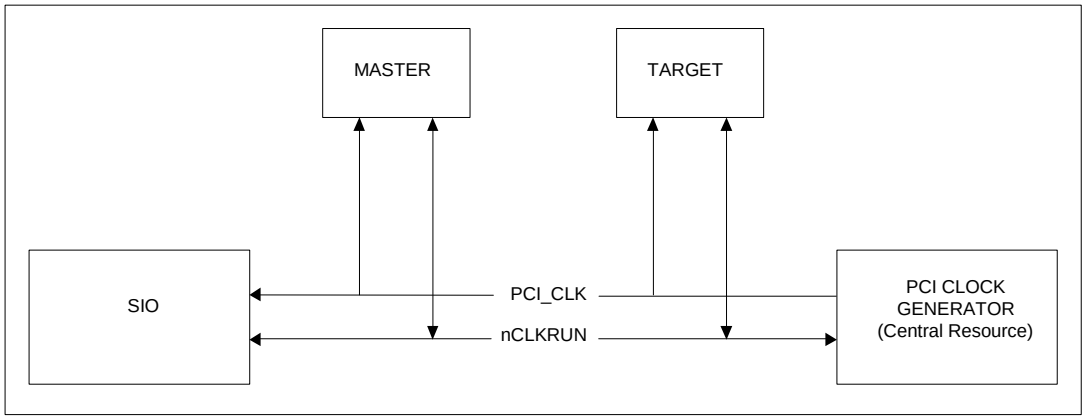
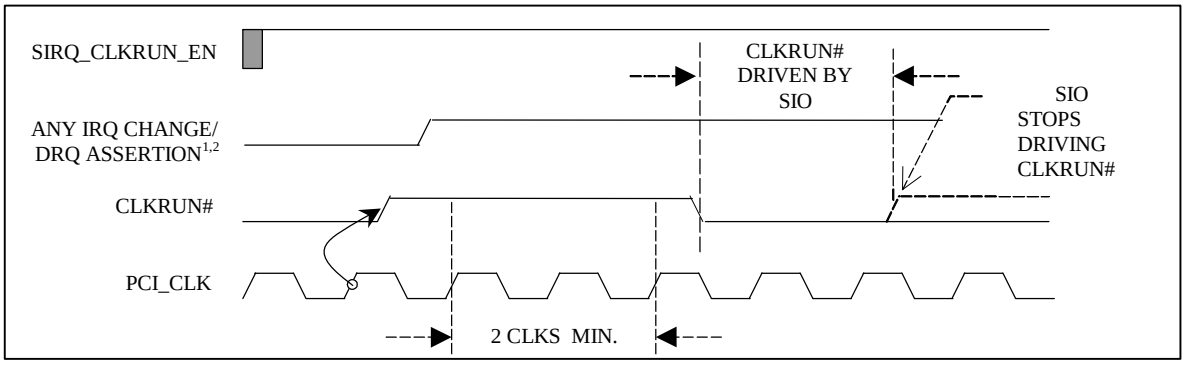


FIGURE 13-2: CLOCK START ILLUSTRATION



Note 1: The signal “ANY IRQ CHANGE/DRQ ASSERTION” is the same as “CHANGE/ASSERTION” in Table 13-1.

2: The SIO1007 continually monitors the state of nCLKRUN to maintain the PCI Clock until an active “ANY IRQ CHANGE/DRQ ASSERTION” condition has been transferred to the host in a SER_IRQ/DMA cycle. For example, if “ANY IRQ CHANGE/DRQ ASSERTION” is asserted before nCLKRUN is de-asserted (not shown in Figure 13-2), the SIO1007 must assert nCLKRUN as needed until the SER_IRQ/DMA cycle has completed.

14.0 GENERAL PURPOSE I/O

The SIO1007 provides a set of flexible Input/Output control functions to the system designer through the 16 independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

14.1 GPIO Pins

The following pins include GPIO functionality as defined in the table below.

TABLE 14-1: GPIO PIN FUNCTIONALITY

Name	Power Well	Default On VTR POR	PME/SMI Function
GP10	VCC (Note 14-1)	Input	PME/SMI
GP11	VCC (Note 14-1)	Input	PME/SMI
GP12/IO_SMI#	VCC (Note 14-1)	Input	IO_SMI#/ PME/SMI
GP13/IRQIN1/CLKI32	VCC (Note 14-1)	Input	PME/SMI
GP14/IRQIN2	VCC (Note 14-1)	Input	PME/SMI
GP15 / CIRRX	VCC (Note 14-1)	Input	PME/SMI
GP16 / CIRTX	VCC (Note 14-1)	Input	PME/SMI
GP17	VCC (Note 14-1)	Input	PME/SMI
GP30	VCC (Note 14-1)	Input	PME
GP31	VCC (Note 14-1)	Input	PME
GP32	VCC (Note 14-1)	Input	PME
GP33	VCC (Note 14-1)	Input	PME
GP34	VCC (Note 14-1)	Input	PME
GP35	VCC (Note 14-1)	Input	PME
GP36	VCC (Note 14-1)	Input	PME
GP37	VCC (Note 14-1)	Input	PME

Note 14-1 These pins have input buffers into the wakeup logic that are powered by VTR.

14.2 Description

Each GPIO port has a 1-bit data register. GPIOs are controlled by GPIO control registers located in the Configuration section. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 and GP3. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. The value is latched on reads and writes.

Although the bits in GP1 and GP3 default to 0x00 at VTR POR, the value read is affected by the GPIO pin state. Each GPIO pin's state at VCC POR is controlled by the pin's programmed configuration and the external interface (e.g. input driven low by external device.) Each GPIO pin has programmable configuration bits in CR31-CR39 which control direction, output types, polarity, and internal pull-ups. For example, the GPIO internal pull-ups are controlled by CR37 and CR38 and default at VTR POR to pull-up enabled (logic '1'.) If not reprogrammed any open input will have logic '1' at VCC POR. This will affect the corresponding bit in the GP1 and GP3 runtime register.

The GPIO data registers are located in the Runtime Register block; see the Runtime Registers section. The GPIO ports with their alternate functions and configuration state register addresses are listed in Table 14-2.

TABLE 14-2: GENERAL PURPOSE I/O PORT ASSIGNMENTS

Default Function	Alternate Function	Data Register	Data Register Bit No.	Register Offset (HEX)	Pullup Control Register Control (Note 14-2)	Pullup Register Bit No.
GPIO10		GP1	0	0C	CR38	0
GPIO11			1			1
GPIO12	IO_SMI#		2			2
GPIO13	IRQIN1		3			3
GPIO14	IRQIN2		4			4
GPIO15			5			5
GPIO16			6			6
GPIO17			7			7
GPIO 30		GP3	0	0E	CR37	0
GPIO 31			1			1
GPIO 32			2			2
GPIO33			3			3
GPIO34			4			4
GPIO35			5			5
GPIO36			6			6
GPIO37			7			7

Note 14-2 The GPIO Data Registers are located at the offset shown from the RUNTIME REGISTERS BLOCK address.

14.3 GPIO Control

Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in the Configuration section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. GPIO Direction Registers determine the port direction, GPIO Polarity Registers determine the signal polarity, and GPIO Output Type Register determines the output driver type select. The GPIO Output Type Register applies all GPIOs. The GPIO Direction, Polarity and Output Type Registers control the GPIO pin when the pin is configured for the GPIO function and when the pin is configured for the alternate function for all pins.

The basic GPIO configuration options are summarized in Table 14-3.

TABLE 14-3: GPIO CONFIGURATION SUMMARY

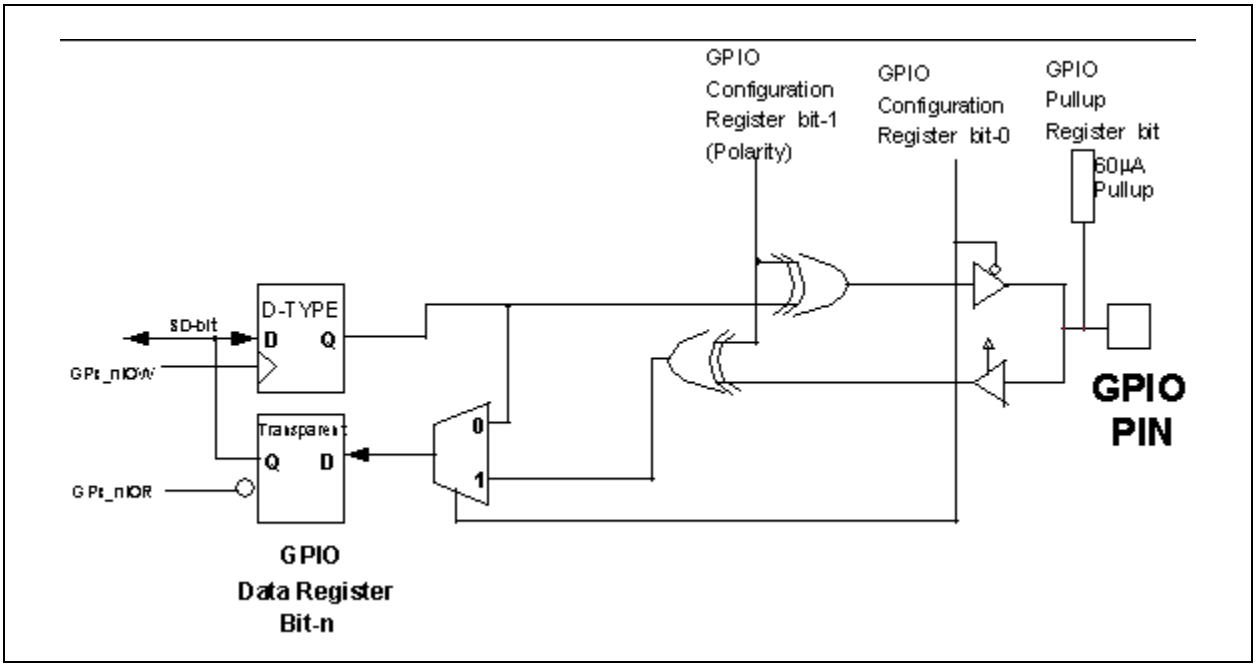
Selected Function	Direction Bit	Polarity Bit	Description
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

In addition, each GPIO pin has a programmable weak pull-up (45 µA) to VCC. The Pull-up control is independent of GPIO direction, buffer type, and Alternate Function selection. Each GPIO pin has a bit in a GPIO PULLUP Register, which enables the pin's pull-up.

14.4 GPIO Operation

The operation of the GPIO ports is illustrated in Figure 14-1.

FIGURE 14-1: GPIO FUNCTION ILLUSTRATION



Note: Figure 14-1 is for illustration purposes only and in not intended to suggest specific implementation details.

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect (Table 14-4).

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register (Table 14-4).

TABLE 14-4: GPIO READ/WRITE BEHAVIOR

Host Operation	GPIO Input Port	GPIO Output Port
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

The SIO1007 provides 16 GPIOs that can directly generate a PME. See the table in the next section. The GPIO Polarity Registers in the Configuration section select the edge on these GPIO pins that will set the associated status bit in the PME_STS1 – PME_STS3 registers. The default is the low-to-high edge. If the corresponding enable bit in the PME_EN1 – PME_EN3 registers and the PME_EN bit in the PME_EN register is set, a PME will be generated. These registers are located in the Runtime Registers Block, which is located at the address contained in the configuration registers CR30. The PME status bits for the GPIOs are cleared on a write of '1'. In addition, the SIO1007 provides 10 GPIOs that can directly generate an SMI. See the table in the next section.

14.5 GPIO PME and SMI Functionality

The provides SIO1007 provides 16 GPIOs that can directly generate a PME. See the table in the next section. The GPIO Polarity Registers in the Configuration section select the edge on these GPIO pins that will set the associated status bit in the PME_STS1 – PME_STS3 registers. The default is the low-to-high edge. If the corresponding enable bit in the PME_EN1 – PME_EN3 registers and the PME_EN bit in the PME_EN register is set, a PME will be generated. These registers are located in the Runtime Registers Block, which is located at the address contained in the configuration registers CR30. The PME status bits for the GPIOs are cleared on a write of '1'. In addition, the SIO1007 provides 8 GPIOs that can directly generate an SMI.

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP10-GP17

GP30-GP37

This following is the list of PME status and enable registers for their corresponding GPIOs:

PME_STS1 and PME_EN1 for GP10-GP17

PME_STS3 and PME_EN3 for GP30-GP37

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

GP10-GP17

The following SMI status and enable registers for these GPIOs:

SMI_STS1 and SMI_EN1 for GP10-17

The following table summarizes the PME and SMI functionality for each GPIO.

TABLE 14-5: PME AND SMI FUNCTIONALITY

GPIO	PME Status and Enable Registers	SMI Status and Enable Registers	Output Buffer Power
GP10-GP11	PME_STS1 & PME_EN1	SMI_STS1 and SMI_EN1	VCC
GP12 (See Note 14-3)			VCC
GP13-GP17			VCC
GP30-GP37	PME_STS1 & PME_EN1	None	VCC

Note 14-3 Since GP12 can be used to generate an SMI and as the IO_SMI# output, do not enable GP12 to generate an SMI (by setting bit 2 of the SMI Enable Register 1) if the IO_SMI# function is selected on the GP12 pin. Use GP12 to generate an SMI event only if the SMI output is enabled on the Serial IRQ stream.

15.0 SYSTEM MANAGEMENT INTERRUPT (SMI)

The SIO1007 implements a “group” nIO_SMI output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from Super I/O Device Interrupts (Serial Port 1 and 2) and many of the GPIOs pins. The GP12/nIO_SMI pin, when selected for the nIO_SMI function, can be programmed to be active high or active low via bit 2 in the GPIO Polarity Register 1 (CR32). The nIO_SMI pin function defaults to active low. The output buffer type of the pin can be programmed to be open-drain or push-pull via GPIO Output Type Register (CR39).

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1 and 2. The nSMI output is then enabled onto the nIO_SMI output pin via bit[7] in the SMI Enable Register 2. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 2.

15.1 SMI Registers

The SMI event bits for the GPIOs events are located in the SMI status and Enable registers 1 and 2. The polarity of the edge used to set the status bit and generate an SMI is controlled by the GPIO Polarity Registers located in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits for the GPIOs are cleared on a write of ‘1’.

The SMI logic for the GPIO events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The SMI event bits for the super I/O devices are located in the SMI status and enable register 1 and 2. All of these status bits are cleared at the source; these status bits are not cleared by a write of ‘1’. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See the Runtime Registers section for the definition of the SMI status and enable registers.

16.0 PME SUPPORT

The SIO1007 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events in an ACPI system. A power management event is indicated to the chipset via the assertion of the IO_PME# signal. In the SIO1007, the IO_PME# is asserted by active transitions on the ring indicator inputs nRI1 and nRI2, and programmable edges on GPIO pins. The nIO_PME pin can be programmed to be active high or active low via bit 5 in the GPIO Polarity Register 2 (CR34). The nIO_PME pin function defaults to active low, open-drain output. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 in the GPIO Output Type Register (CR39). This pin is powered by VTR. See the Configuration section for description on these registers.

PME functionality is controlled by the PME status and enable registers in the runtime registers block, which is located at the address programmed in register 0x30 in the Configuration section. The PME Enable bit, PME_EN, globally controls PME Wake-up events. When PME_EN is inactive, the IO_PME# signal can not be asserted. When PME_EN is asserted, any wake source whose individual PME Wake Enable register bit is asserted can cause IO_PME# to become asserted.

The PME Status register indicates that an enabled wake source has occurred and if the PME_EN bit is set, asserted the IO_PME# signal. The PME Status bit is asserted by active transitions of PME wake sources. PME_STS will become asserted independent of the state of the global PME enable, PME_EN.

The following pertains to the PME status bits for each event:

- The output of the status bit for each event is combined with the corresponding enable bit to set the PME status bit.
- The status bit for any pending events must be cleared in order to clear the PME_STS bit. Status bits are cleared on a write of ‘1’.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the GPIO Polarity Registers in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits are cleared on a write of ‘1’.

In the SIO1007 the IO_PME# pin can be programmed to be an open drain, active low, driver. The SIO1007 IO_PME# pin is fully isolated from other external devices that might pull the IO_PME# signal low; i.e., the IO_PME# signal is capable of being driven high externally by another active device or pullup even when the SIO1007 VCC is grounded, providing VTR power is active.

16.1 PME Registers

The PME registers are run-time registers as follows. These registers are located in system I/O space at an offset from Runtime Registers Block, the address programmed at register 0x30 in the Configuration section.

The following registers are for GPIO PME events:

- PME Wake Status 1 (PME_STS1), PME Wake Enable 1 (PME_EN1)
- PME Wake Status 2 (PME_STS2), PME Wake Enable 2 (PME_EN2)
- PME Wake Status 3 (PME_STS3), PME Wake Enable 3 (PME_EN3)

See PME register description in the Runtime Registers Section.

17.0 RUNTIME REGISTERS

17.1 Runtime Registers Block Summary

The runtime registers are located at the address programmed in the Runtime Register Block Base Address configuration registers (high and low byte) located in CR30 & CR21. The part performs 16-bit address qualification on the Runtime Register Base Address (bits[15:0] are decoded). The runtime register block may be located within the range 0x0100-0xFFFF on 16-byte boundaries. Decodes are disabled if the Runtime Register Base Address is located below 0x100. These registers are powered by VTR.

TABLE 17-1: RUNTIME REGISTER BLOCK SUMMARY

Register Offset (HEX)	Type	PCI Reset	VCC POR	VTR POR	Register
00	R/W	-	-	0x00	PME_STS
01	R/W	-	-	0x00	PME_EN
02	R/W	-	Note 17-1	0x00	PME_STS1
03	R/W	-	-	0x00	PME_STS2
04	R/W	-	Note 17-1	0x00	PME_STS3
05	R/W	-	-	0x00	PME_EN1
06	R/W	-	-	0x00	PME_EN2
07	R/W	-	-	0x00	PME_EN3
08	R/W	-	Note 17-1	0x00	SMI_STS1
09	R/W	-	-	0x00	SMI_STS2
0A	R/W	-	-	0x00	SMI_EN1
0B	R/W	-	-	0x00	SMI_EN2
0C	R/W	-	Note 17-1	0x00	GP1
0D	R	-	-	0x00	Reserved
0E	R/W	-	Note 17-1	0x00	GP3
0F	R	-	-	0x00	Reserved

Note 17-1 Reserved bits return 0 on read.

17.2 Runtime Registers Block Description

TABLE 17-2: RUNTIME REGISTERS BLOCK DESCRIPTION

Name/Default	Register Offset	Description
PME_STS Default = 0x00 on VTR POR	00 (R/W)	Bit[0] PME_Status = 0 (default) = 1 Set when SIO1007 would normally assert the IO_PME# signal, independent of the state of the PME_En bit. Bit[7:1] Reserved **Note:** PME_Status is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a “1” to PME_Status will clear it and cause the SIO1007 to stop asserting IO_PME#, in enabled. Writing a “0” to PME_Status has no effect.
PME_EN Default = 0x00 on VTR POR	01 (R/W)	Bit[0] PME_En = 0 IO_PME# signal assertion is disabled (default) = 1 Enables SIO1007 to assert IO_PME# signal Bit[7:1] Reserved PME_EN is not affected by Vcc POR, SOFT RESET or PCI RESET

TABLE 17-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
PME_STS1 Default = 0x00 on VTR POR See Note 17-2	02 (R/W)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
PME_STS2 Default = 0x00 on VTR POR	03 (R/W)	PME Wake Status Register 2 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] RI1 Bit[1] IRRX2 Bit[2] CIRCC2 Bit[7:3] Reserved The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
PME_STS3 Default = 0x00 on VTR POR See Note 17-2	04 (R/W)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_EN bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or PCI RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
PME_EN1 Default = 0x00 on VTR POR	05 (R/W)	PME Wake Enable Register 1 This register is used to enable individual SIO1007 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.

TABLE 17-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
PME_EN2 Default = 0x00 on VTR POR	06 (R/W)	PME Wake Enable Register 2 This register is used to enable individual SIO1007 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] RI1 Bit[1] IRRX2 Bit[2] CIRCC2 Bit[7:3] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
PME_EN3 Default = 0x00 on VTR POR	07 (R/W)	PME Wake Enable Register 3 This register is used to enable individual SIO1007 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or PCI RESET.
SMI_STS1 Default = 0x00 on VTR POR See Note 17-2	08 (R/W)	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of ‘1’. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
SMI_STS2 0x00 on VTR POR	09 (R/W)	SMI Status Register 2 This register is used to read the status of the SMI inputs. The bits[3:0] must be cleared at their source. Bits[5:4] are cleared on a write of ‘1’. Bit[0] Reserved Bit[1] U2INT Bit[2] U1INT Bit[3] CIRCC2 Bit[7:4] Reserved

TABLE 17-2: RUNTIME REGISTERS BLOCK DESCRIPTION (CONTINUED)

Name/Default	Register Offset	Description
SMI_EN1 Default = 0x00 on VTR POR	0A (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the internal group nSMI signal. 1=Enable 0=Disable Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
SMI_EN2 Default = 0x00 on VTR POR	0B (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the internal group nSMI signal, and the internal group nSMI signal onto the nIO_SMI GPI/O pin or the serial IRQ stream on IRQ2. 1=Enable 0=Disable Bit[0] Reserved Bit[1] EN_U2INT Bit[2] EN_U1INT Bit[3] EN_CIRCC2 Bit[5:4] Reserved Bit[6] EN_SMI_S (Enable group nSMI signal onto serial IRQ2) Bit[7] EN_SMI (Enable group nSMI signal onto IO_SMI# pin)
GP1 Default = 0x00 on VTR POR See Note 17-2	0C R/W	General Purpose I/O Data Register 1 Bit[0]GP10 Bit[1]GP11 Bit[2]GP12 Bit[3]GP13 Bit[4]GP14 Bit[5]GP15 Bit[6]GP16 Bit[7]GP17
GP2 Default = 0x00 on VTR POR	0D R	Bit[7:0]Reserved
GP3 Default = 0x00 on VTR POR See Note 17-2	0E R/W	General Purpose I/O Data Register 3 Bit[0]GP30 Bit[1]GP31 Bit[2]GP32 Bit[3]GP33 Bit[4]GP34 Bit[5]GP35 Bit[6]GP36 Bit[7]GP37
GP4 Default = 0x00 on VTR POR	0F R	Bit[7:0]Reserved

Note: Reserved bits return 0 on read.

Note 17-2 Although the bits in this runtime register default at VTR POR to ‘0’, the value read is affected by the GPIO pin state. Each GPIO pin’s state at VCC POR is controlled by the pin’s programmed configuration and the external interface (e.g. input driven low by external device.) Each GPIO pin has programmable configuration bits in CR31-CR39 which control direction, output types, polarity, and internal pull-ups. For example, the GPIO internal pull-ups are controlled by CR37 and CR38 and default at VTR POR to pull-up enabled (logic ‘1’). If not reprogrammed any open input will have logic ‘1’ at VCC POR. This will affect this runtime register.

18.0 CONFIGURATION

The configuration of the SIO1007 is programmed through hardware selectable Configuration Access Ports that appear when the chip is placed into the configuration state. The SIO1007 logical device blocks, if enabled, will operate normally in the configuration state.

18.1 Configuration Access Ports

The Configuration Access Ports are the CONFIG PORT, the INDEX PORT, and the DATA PORT (Table 18-2). The base address of these registers is controlled by the nRTS/SYSOPT0 and nDTS/SYSOPT1 pins and by the Configuration Port Base Address registers CR12 and CR13. The configuration base address at power-up is determined by the SYSOPT strap option. The SYSOPT strap option is latched state of the nRTS/SYSOPT0 and nDTS/SYSOPT1 pins at the deasserting edge of PCIRST#. The nRTS/SYSOPT0 pin determines the lower byte of the Base Address and the nDTS/SYSOPT1 pin determines the upper byte of the Base Address. See Table 18-1 Default Configuration Access Ports Base Address Decoded from the SYSOPT Strap Option.

APPLICATION NOTE: The nRTS1/SYSOPT0 and the nDTS1/SYSOPT1 pins require external pullup/pull-down resistors to set the default base I/O address for configuration to 0x002E, 0x004E, 0x162E, or 0x164E.

TABLE 18-1: DEFAULT CONFIGURATION ACCESS PORTS BASE ADDRESS DECODED FROM THE SYSOPT STRAP OPTION

SYSOPT1	SYSOPT0	Default CONFIG Port/ Index Port Address
0	0	0x002E
0	1	0x004E
1	0	0x162E
1	1	0x164E

TABLE 18-2: CONFIGURATION ACCESS PORTS

Port Name	Relative Address	Type
CONFIG PORT	Configuration Access Ports Base Address + 0	WRITE
INDEX PORT	Configuration Access Ports Base Address + 0	READ/WRITE (Note 18-1, Note 18-2)
DATA PORT	Configuration Access Ports Base Address + 1	READ/WRITE (Note 18-2)

Note 18-1 The INDEX and DATA ports are active only when the SIO1007 is in the configuration state.

Note 18-2 The INDEX PORT is only readable in the configuration state.

18.2 Configuration State

The configuration registers are used to select programmable chip options. The SIO1007 operates in two possible states: the run state and the configuration state. After power up by default the chip is in the run state. To program the configuration registers, the configuration state must be explicitly enabled. Programming the configuration registers typically follows this sequence:

1. Enter the Configuration State,
2. Program the Configuration Register(s),
3. Exit the Configuration State.

18.2.1 ENTERING THE CONFIGURATION STATE

To enter the configuration state write the Configuration Access Key to the CONFIG PORT. The Configuration Access Key is one byte of 55H data. The SIO1007 will automatically activate the Configuration Access Ports following this procedure.

18.2.2 CONFIGURATION REGISTER PROGRAMMING

The SIO1007 contains configuration registers CR00-CR39. After the SIO1007 enters the configuration state, configuration registers can be programmed by first writing the register index number (00 - 39H) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or reading the configuration register contents through the DATA PORT. Configuration register access remains enabled until the configuration state is explicitly exited.

18.2.3 EXITING THE CONFIGURATION STATE

To exit the configuration state, write one byte of AAH data to the CONFIG PORT. The SIO1007 will automatically deactivate the Configuration Access Ports following this procedure, at which point configuration register access cannot occur until the configuration state is explicitly re-enabled.

18.2.4 PROGRAMMING EXAMPLE

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;----------------------------.
; ENTER CONFIGURATION STATE  |
;----------------------------'
MOVDX,02EH;SYSOPT = 0
MOVAX,055H
OUTDX,AL
;----------------------------.
; CONFIGURE REGISTER CR0-CRx |
;----------------------------'
MOVDX,02EH
MOVAL,00H
OUTDX,AL ;Point to CR0
MOVDX,02FH
MOVAL,3FH
OUTDX,AL ;Update CR0
;
MOVDX,02EH
MOVAL,01H
OUTDX,AL ;Point to CR1
MOVDX,02FH
MOVAL,9FH
OUTDX,AL ;Update CR1
;
; Repeat for all CRx registers
;
;----------------------------.
; EXIT CONFIGURATION STATE    |
;----------------------------'
MOVDX,02EH
MOVAX,AAH
OUTDX,AL
```

18.2.5 CONFIGURATION SELECT REGISTER (CSR)

The Configuration Select Register can only be accessed when the SIO1007 is in the configuration state. The CSR is located at the INDEX PORT address and must be initialized with configuration register index before the register can be accessed using the DATA PORT.

18.3 Configuration Registers Summary

The configuration registers are set to their default values at power up (Table 18-3) and are RESET as indicated in Table 18-3 and the register descriptions that follow.

TABLE 18-3: CONFIGURATION REGISTERS SUMMARY

Register Index	Type	PCI Reset (Note 18-3)	VCC POR	VTR POR	Register
CR00	R	-	0x00		Valid Config Cycle
CR01	R/W	bit[7]=1		-	CR Lock
CR02	R/W	bit[7]=0	0x08	-	UART AND IR POWER
CR03	R	-	-	-	Reserved
CR04	R/W	-	0x00	-	UART Miscellaneous
CR05	R	-	0x00	-	Reserved
CR06	R	-	0x00	-	Reserved
CR07	R/W	bit[6:5]=0	0x00	-	Auto Power Mgt
CR08	R	-	0x00	-	Reserved
CR09	R/W	-	0x00	-	Test 4
CR0A	R/W	bit[7:6]=0	0x00	0x00	IR MUX
CR0B	R	-	0x00	-	Reserved
CR0C	R/W	0x02	0x02	-	UART Mode
CR0D	R	-	0x20	-	Device ID
CR0E	R	-	Revision	-	Revision ID
CR0F	R/W	-	0x00	-	Test 1
CR10	R/W	-	0x00	-	Test 2
CR11	R/W	-	0x00	-	Test 3
CR12	R/W	SYSOPT0=0:0x2E SYSOPT0=1:0x4E		-	Configuration Base Address 0
CR13	R/W	SYSOPT1=0:0x00 SYSOPT1=1:0x16		-	Configuration Base Address 1
CR14	R	-	-	-	Reserved
CR15	R	-	-	-	UART1 FCR Shadow
CR16	R	-	-	-	UART2 FCR Shadow
CR17	R	-	0x00	-	Reserved
CR18	R/W	-	0x00	-	CIRCC2 Interrupt/DMA Selection
CR19	R/W	-	0x00	-	CIRCC2 Software Select A
CR1A	R/W	-	0x00	-	CIRCC2 Software Select B
CR1B	R/W	-	0x03	-	CIRCC2 Half Duplex Timeout
CR1C	R	-	0x00	-	Reserved
CR1D	R/W	-	0x00	-	Test 5
CR1E	R/W	-	0x00	-	SCE (FIR) Base Address - High Byte
CR1F	R/W	-	0x00	-	CIRCC2 Base Address Register (Low Byte)
CR20	R/W	-	0x00	-	CIRCC2 Base Address Register (High Byte)
CR21	R/W	-	0x00	-	Runtime Register Base Address - High Byte
CR22	R	-	0x00	-	Reserved
CR23	R	-	0x00	-	Reserved
CR24	R/W	-	0x00	-	UART1 Base Address
CR25	R/W	-	0x00	-	UART2 Base Address
CR26	R	-	0x00	-	Reserved

TABLE 18-3: CONFIGURATION REGISTERS SUMMARY (CONTINUED)

Register Index	Type	PCI Reset (Note 18-3)	VCC POR	VTR POR	Register
CR27	R	-	0x00	-	Reserved
CR28	R/W	-	0x00	-	UART IRQ Select
CR29	R/W	-	0x80	-	IRQIN1/HPMODE/SIRQ_CLKRUN_En
CR2A	R/W	-	0x00	-	IRQIN2
CR2B	R/W	-	0x00	-	SCE (FIR) Base Address - Low Byte
CR2C	R/W	-	0x0F	-	SCE (FIR) DMA Select
CR2D	R/W	-	0x03	-	IR Half Duplex Timeout
CR2E	R/W	-	0x00	-	Software Select A
CR2F	R/W	-	0x00	-	Software Select B
CR30	R/W	-	0x00	-	Runtime Register Base Address - Low Byte
CR31	R/W	-	-	0x00	GPIO Direction Register 1
CR32	R/W	-	-	0x00	GPIO Polarity Register 1
CR33	R/W	-		0xFF-	GPIO Output Type Register 1
CR34	R/W	-	-	0x01	Alternate Function Register
CR35	R/W	-	-	0x00	GPIO Direction Register 3
CR36	R/W	-	-	0x00	GPIO Polarity Register 3
CR37	R/W	-	-	0xFF	GPIO PULLUP Register 3
CR38	R/W	-	-	0xFF	GPIO PULLUP Register 1
CR39	R/W	-	-	0xFF	GPIO Output Type Register 3
CR3A	R/W		0x00		Logical Device Activate Register
CR3B	R/W		0x00		LPC Docking Base Address Register High Byte
CR3C	R/W		0x00		LPC Docking Base Address Register Low Byte

Note 18-3 The bits that control the direction, polarity and output buffer type of each GPIO also affect the alternate function on the GPIO.

18.4 Configuration Register Detailed Description

18.4.1 CR00

CR00 can only be accessed in the configuration state and after the CSR has been initialized to 00H.

TABLE 18-4: CR00

Valid Configuration Cycle		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
6:0	Reserved	Read Only. A read returns 0
7	Valid	A high level on this software-controlled bit can be used to indicate that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. This bit has no effect on any other hardware in the chip.

18.4.2 CR01

CR01 can only be accessed in the configuration state and after the CSR has been initialized to 01H.

TABLE 18-5: CR01

CR Lock		
Type: R/W		**Default: 0X80 ON VCC POR; BIT[7] = 1 ON PCI RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
6:0	Reserved	Read Only. A read returns “0”.
7	Lock CRx	A high level on this bit enables the reading and writing of CR00 –CR39 (Default). A low level on this bit disables the reading and writing of CR00 – CR39. **Note:** Once the Lock CRx bit is set to “0”, this bit can only be set to “1” by a PCI reset or power-up reset.

18.4.3 CR02

CR02 can only be accessed in the configuration state and after the CSR has been initialized to 02H.

TABLE 18-6: CR02

UART and IR Power		
Type: R/W		**Default: 0x20 on VTR POR; 0xx00000VCC POR; Bit[7] = 0 on PCI Reset**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-2	Reserved	Read Only. A read returns “0”.
3	UART1 Power Control Note 18-4	0= Primary Serial Port are in Power Down Mode. (default) 1= Enables normal operation of the Primary Serial Port
4	Reserved	Read Only. A read returns “0”.
5	CIRCC2 PLL Power Down	CIRCC PLL Power (Note: This bit is reset on VTR POR only) = 0 The 32.768kHz clock PLL is running and can replace the 14.318MHz clock source for the CIRCC2 Wake Event. PLL selected by internal PWRGOOD signal. = 1 The 32.768kHz clock PLL is unpowered (default)
6	CIRCC2 Power Control Note 18-4	0= SCE/FIR block is in Power Down Mode. (default) 1= Enables normal operation of the SCE/CIR block **Note:** This bit is reset on VTR POR only.
7	UART2 Power Control Note 18-4	0= Secondary Serial Port including the SCE/FIR block are in Power Down Mode. (default on VCC POR and PCI Reset) 1=Enables normal operation of the Secondary Serial Port, including the SCE/FIR block.

Note 18-4 Power Control bits disable the respective logical device and associated pins, however the power control bit does not disable the selected address range for the logical device. To disable the host address registers software must clear the activate bits in CR3A, the Logical Device Activate Register. Devices that are powered down and still activated will participate in Plug-and-Play range checking.

18.4.4 CR03

Register CR03 is reserved. The default value of this register after power up is 00H.

18.4.5 CR04

CR04 can only be accessed in the configuration state and after the CSR has been initialized to 04H.

TABLE 18-7: CR04

UART Miscellaneous		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0		Read Only. A read returns “0”.
4	MIDI 1 (Note 18-5)	Serial Clock Select Port 1: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
5	MIDI 2 (Note 18-5)	Serial Clock Select Port 2: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
7:6		Read Only. A read returns “0”.

Note 18-5 MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%).

18.4.6 CR05

Register CR05 is reserved. The default value of this register after power up is 00H.

18.4.7 CR06

Register CR06 is reserved. The default value of this register after power up is 00H.

18.4.8 CR07

CR07 can only be accessed in the configuration state and after the CSR has been initialized to 07H. CR07 controls auto power management.

TABLE 18-8: CR07

Auto Power Management and Boot Drive Select		
Type: R/W		**Default: 0X00 ON VCC POR; BITS[6:5] = 00 ON PCI RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
4:0	Reserved	Read Only. A read returns 0.
5	UART 2 Enable	This bit controls the AUTOPOWER DOWN feature of the UART2. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
6	UART 1 Enable	This bit controls the AUTOPOWER DOWN feature of the UART1. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
7	Reserved	Read Only. A read returns 0.

18.4.9 CR08

Register CR08 is reserved. The default value of this register after power up is 00H.

18.4.10 CR09

CR09 can only be accessed in the configuration state and after the CSR has been initialized to 09H. CR09 is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 18-9: CR09

Test 4		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 24	RESERVED FOR MICROCHIP USE
1	Test 25	
2	Test 26	
3	Test 27	
4	Test 28	
5	Test 29	
6	Test 30	
7	Test 31	

18.4.11 CR0A

CR0A can only be accessed in the configuration state and after the CSR has been initialized to 0AH. CR0A Bits [5:4] are CIRCC2 OUTPUT MUX bits and are reset to the default state by a VTR POR. CR0A Bits [7:6] control the IRCC2 OUTPUT MUX and are reset to the default state by a VTR POR, VCC POR and PCI Reset.

TABLE 18-10: CR0A

IR MUX				
Type: R/W		**Default: 0x00 on VTR POR; 00xx0000b VCC POR; Bits[7:6] = 00 on PCI RESET**		
BIT NO.	**BIT NAME**	**DESCRIPTION**		
3:0	Reserved	Read Only. A read returns 0.		
4,5	CIRCC2 Output Mux	These bits are used to select CIRCC Output Mux Mode.		
		BIT5	**BIT4**	**MUX MODE**
		0	0	Default tristate (Note 18-6)
		0	1	Active device to CIRCC2 port. That is, use CIRRX, CIRTX (pins 23, 24). When CIRCC2 is inactive (Power Down bit = 0), then CIRTX pin is low.
		1	0	Reserved.(Note 18-6)
		1	1	Reserved.(Note 18-6)

TABLE 18-10: CR0A (CONTINUED)

IR MUX				
Type: R/W			**Default: 0x00 on VTR POR; 00xx0000b VCC POR; Bits[7:6] = 00 on PCI RESET**	
BIT NO.	**BIT NAME**	**DESCRIPTION**		
6,7	IRCC2 Output Mux	These bits are used to select IRCC2 Output Mux Mode.		
		BIT7	**BIT6**	**MUX MODE**
		0	0	Active device to COM port (Default). This port in not connected. When Serial Port 2 is inactive (Power Control bit = 0), then the IRTX2 pin is low.
		0	1	Active device to IR port. is the IRRX2, IRTX2 are selected. When Serial Port 2 is inactive (Power Down bit = 0), then IRTX2 pin is low.
		1	0	Reserved.
		1	1	Outputs Inactive: IRTX2 is High-Z, regardless of mode of UART2 and state of UART2 Power Control bit.

Note 18-6 The CIRTX pin will tristate when this combination is selected. Outputs Inactive: CIRTX is High-Z, regardless of mode of CIRCC2 and state of CIRCC2 Power Control bit.

18.4.12 CR0B

Register CR0B is reserved. The default value of this register after power up is 00H.

18.4.13 CR0C

CR0C can only be accessed in the configuration state and after the CSR has been initialized to 0CH. CR0C controls the operating mode of the UART. This register is reset to the default state by a POR or a hardware reset.

TABLE 18-11: CR0C

UART Mode			
Type: R/W		**Default: 0X02 ON VCC POR AND PCI RESET**	
BIT NO.	**BIT NAME**	**DESCRIPTION**	
0	UART 2 RCV Polarity	0 = RX input active high (default). 1 = RX input active low.	
1	UART 2 XMIT Polarity	0 = TX output active high. 1 = TX output active low (default).	
2	UART 2 Duplex	This bit is used to define the FULL/HALF DUPLEX operation of UART 2. 1 = Half duplex 0 = Full duplex (default)	
3, 4, 5	UART 2 MODE	UART 2 Mode 5 4 3 0 0 0 Standard COM Functionality (default) 0 0 1 IrDA (HPSIR) 0 1 0 Amplitude Shift Keyed IR 0 1 1 Reserved 1 x x Reserved	
6	UART 1 Speed	This bit enables the high speed mode of UART 1. 1 = High speed enabled 0 = Standard (default)	
7	UART 2 Speed	This bit enables the high speed mode of UART 2. 1 = High speed enabled 0 = Standard (default)	

18.4.14 CR0D

CR0D can only be accessed in the configuration state and after the CSR has been initialized to 0DH. This register is read only. CR0D contains the SIO1007 Device ID. The default value of this register after power up is 0x20 on VCC POR.

18.4.15 CR0E

CR0E can only be accessed in the configuration state and after the CSR has been initialized to 0EH. This register is read only. CR0E contains the current SIO1007 Chip. Revision Level starting at 00H.

18.4.16 CR0F

CR0F can only be accessed in the configuration state and after the CSR has been initialized to 0FH. CR0F is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 18-12: CR0F

Test 1		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 0	RESERVED FOR MICROCHIP USE
1	Test 1	
2	Test 2	
3	Test 3	
4	Test 4	
5	Test 5	
6	Test 6	
7	Test 7	

18.4.17 CR10

CR10 can only be accessed in the configuration state and after the CSR has been initialized to 10H. CR10 is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 18-13: CR10

Test 2		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 8	RESERVED FOR MICROCHIP USE
1	Test 9	
2	Test 10	
3	Test 11	

TABLE 18-13: CR10 (CONTINUED)

Test 2		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
4	Test 12	
5	Test 13	
6	Test 14	
7	Test 15	

18.4.18 CR11

CR11 can only be accessed in the configuration state and after the CSR has been initialized to 11H. CR11 is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 18-14: CR11

Test 3		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 16	RESERVED FOR MICROCHIP USE
1	Test 17	
2	Test 18	
3	Test 19	
4	Test 20	
5	Test 21	
6	Test 22	
7	Test 23	

18.4.19 CR12 - CR13

CR12 and CR13 are the SIO1007 Configuration Ports base address registers (Table 18-15 and Table 18-16). These registers are used to relocate the Configuration Ports base address beyond the power-up defaults determined by the SYSOPT[1:0] pin strap options.

CR12 contains the Configuration Ports base address bits A[7:0]. CR13 contains the Configuration Ports base address bits A[15:8].

The Configuration Ports base address is relocatable on even-byte boundaries; i.e., A0 = ‘0’.

At power-up the Configuration Ports base address is determined by the SYSOPT[1:0] pin strap options. To relocate the Configuration Ports base address after power-up, first write the lower address bits of the new base address to CR12 and then write the upper address bits to CR13.

Note:	Writing CR13 changes the Configuration Ports base address.

TABLE 18-15: CR12

Configuration Ports Base Address Byte 0 (Note 18-7)		
Type: R/W		**Default: 0X2E (SYSOPT0=0) 0X4E (SYSOPT0=1) ON VCC POR AND PCI RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	A1	Configuration Ports Base Address Byte 0 for decoder.
2	A2	
3	A3	
4	A4	
5	A5	
6	A6	
7	A7	

Note 18-7 The Configuration Ports Base Address is relocatable on even-byte boundaries; i.e., A0 = “0”.

TABLE 18-16: CR13

Configuration Ports Base Address Byte 1 (Note 18-8)		
Type: R/W		**Default: 0X00 (SYSOPT1=0) 0X16 (SYSOPT1=1) ON VCC POR AND PCI RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	A8	Configuration Ports Base Address Byte 1 for decoder.
1	A9	
2	A10	
3	A11	
4	A12	
5	A13	
6	A14	
7	A15	

Note 18-8 Writing CR13 changes the Configuration Ports base address.

18.4.20 CR14

Register CR14 is reserved. The default value of this register after power up is 00H.

18.4.21 CR15

CR15 can only be accessed in the configuration state and after the CSR has been initialized to 15H. CR15 shadows the bits in the write-only UART1 run-time FCR register.

TABLE 18-17: CR15

UART1 FCR Shadow Register				
Type: R		**Default: N/A**		
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs		
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.		
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.		
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.		
4,5	Reserved	Read Only. A read returns 0.		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO TRIGGER LEVEL (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

18.4.22 CR16

CR16 can only be accessed in the configuration state and after the CSR has been initialized to 16H. CR16 shadows the bits in the write-only UART2 run-time FCR register. See CR15 for register description.

18.4.23 CR17

Register CR17 is reserved. The default value of this register after power up is 00H.

18.4.24 CR18

CR18 can only be accessed in the configuration state and after the CSR has been initialized to 18h. CR18 is used to select the IRQ channel for CIRCC2 and the DMA channel for the CIRCC2 port. Any unselected IRQ output is in tristate. Shared IRQs are not supported in the SIO1007.

TABLE 18-18: CR18

CIRCC2 Interrupt/DMA Selection		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	CIRCC2 DMA Select	These bits are used to select DMA for CIRCC2 port. See DMA encoding for CR18 (see Table 18-20).
7:4	CIRCC2 IRQ Select	These bits are used to select IRQ for CIRCC2 port. See IRQ encoding for CR18 (see Table 18-19). **Note:** A CIRCC2 IRQ event will only be generated if an SCE event is active and enabled and the CIRCC2 Base I/O Address is in the active range (i.e., greater than 100h)

TABLE 18-19: IRQ ENCODING

Bits [7:4]	IRQ Selected
0000	NONE
0001	IRQ_1
0010	IRQ_2
0011	IRQ_3
0100	IRQ_4
0101	IRQ_5
0110	IRQ_6
0111	IRQ_7
1000	IRQ_8
1001	IRQ_9
1010	IRQ_10
1011	IRQ_11
1100	IRQ_12
1101	IRQ_13
1110	IRQ_14
1111	IRQ_15

TABLE 18-20: DMA SELECTION

Bits [3:0]	DMA Selected
0000	RESERVED
0001	DMA1
0010	DMA2
0011	DMA3
0100	RESERVED
....	…. ….
1110	RESERVED
1111	NONE

18.4.25 CR19

CR19 can only be accessed in the configuration state and after the CSR has been initialized to 19h. CR19 is directly connected to the SCE Register Block Three, Address 0x05 in the CIRCC2 block

.

TABLE 18-21: CR19

CIRCC2 Software Select A		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select A	These bits are directly connected to SCE Register Block Three, Address 0x05 in the CIRCC2 block.

18.4.26 CR1A

CR1A can only be accessed in the configuration state and after the CSR has been initialized to1Ah. CR1A is directly connected to SCE Register Block Three, Address 0x05 in the CIRCC2 block.

TABLE 18-22: CR1A

CIRCC2 Software Select B		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select B	These bits are directly connected to SCE Register Block Three, Address 0x06 in the CIRCC2 block.

18.4.27 CR1B

CR1B can only be accessed in the configuration state and after the CSR has been initialized to 1Bh. CR1B is used to set the CIRCC2 Half Duplex Turnaround Delay Time for the CIRCC2 port. This value is 0 to 25.5msec in 100µsec increments.

The CIRCC2 block includes an 8 bit IR Half Duplex Time-out register in SCE Register Block 5, Address 1 that interacts with configuration register CR1B. These two registers behave like the other CIRCC2 Legacy controls where either source uniformly updates the value of both registers when either register is explicitly written using IOW or following a device-level POR. CIRCC2 software resets do not affect these registers.

The IR Half Duplex Time-out is programmable from 0 to 25.5mS in 100µS increments, as follows:

IR HALF DUPLEX TIME-OUT = (CR1B) x 100µS

TABLE 18-23: CR1B

CIRCC2 Half Duplex Timeout		
Type: R/W		**Default: 0x03 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	IR Half Duplex Time Out	These bits are used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

18.4.28 CR1D

CR1D can only be accessed in the configuration state and after the CSR has been initialized to 09H. CR1D is a test control register and all bits must be treated as Reserved.

Note:	All test modes are reserved for Microchip use. Activating test mode registers may produce undesired results.

TABLE 18-24: CR1D

Test 5		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 32	RESERVED FOR MICROCHIP USE
1	Test 33	
2	Test 34	
3	Test 35	
4	Test 36	
5	Test 37	
6	Test 38	
7	Test 39	

18.4.29 CR1E

CR1E can only be accessed in the configuration state and after the CSR has been initialized to 1EH. CR1E is used to set the SCE (FIR) base address - High Byte ADR[15:11].

The SCE (FIR) logical device base address is initialized using the base address bits located in two configuration registers: CR2B-low byte and CR1E-high byte. The SCE base address can be set to 8160 locations on 8-byte boundaries from 0000H - FFF8H.

The SCE (FIR) base address bits A[2:0] are decoded as 000b. The SCE (FIR) block uses full 16-bit addressing decoding. An address matching the SCE (FIR) base address bits A[15:3] is decoded using the specific address bits A[2:0] to target registers in SCE (FIR).

When the SCE (FIR) logical device activate bit in CR3A-bit0 is cleared to 0, no address decoding takes place for the SCE (FIR) logical device.

TABLE 18-25: CR1E

SCE (FIR) Base Address Register - High Byte		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR11	FIR Base Address bits for decoder.
1	ADR12	
2	ADR13	
3	ADR14	
4	ADR15	
5	RESERVED	Reads return 0. Writes have no effect.
6	RESERVED	Reads return 0. Writes have no effect.
7	RESERVED	Reads return 0. Writes have no effect.

18.4.30 CR1F

CR1F can only be accessed in the configuration state and after the CSR has been initialized to 1Fh. CR1F is used to select the low byte of the base address (ADR[9:3] bits of CIrCC2 Logical Device.

The CIRCC2 logical device base address is initialized using the base address bits located in two configuration registers: CR1F-low byte and CR20-high byte. The CIRCC2 base address can be set to 8,192 locations on 8-byte boundaries from 0000H - FFF8H.

The CIRCC2 base address bits A[2:0] are decoded as 000b. The CIRCC2 block uses full 16-bit addressing decoding. An address matching the CIRCC2 base address bits A[15:3] is decoded using the specific address bits A[2:0] to target registers in CIRCC2.

When the activate bit in CR3A-bit2 is cleared to 0, no address decoding takes place for the CIRCC2 logical device.

To disable CIRCC2 Port, set Bit[2] of the Activate register located at CR3A.

TABLE 18-26: CR1F

CIRCC2 Base Address Register (Low Byte)		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	CIRCC2 Port Base Address bits[9:3] for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

18.4.31 CR20

CR20 can only be accessed in the configuration state and after the CSR has been initialized to 20h. CR20 is used to select the high byte of the base address ADR[15:10] bits of CIrCC2 Logical Device.

The CIRCC2 logical device base address is initialized using the base address bits located in two configuration registers: CR1F-low byte and CR20-high byte. The CIRCC2 base address can be set to 8,192 locations on 8-byte boundaries from 0000H - FFF8H.

The CIRCC2 base address bits A[2:0] are decoded as 000b. The CIRCC2 block uses full 16-bit addressing decoding. An address matching the CIRCC2 base address bits A[15:3] is decoded using the specific address bits A[2:0] to target registers in CIRCC2.

When the activate bit in CR3A-bit2 is cleared to 0, no address decoding takes place for the CIRCC2 logical device.

To disable CIRCC2 Port, set Bit[2] of the Activate register located at CR3A.

TABLE 18-27: CR20

CIRCC2 Base Address Register (High Byte)		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR10	CIRCC2 Port Base Address bits[15:10] for decoder.
1	ADR11	
2	ADR12	
3	ADR13	
4	ADR14	
5	ADR15	
6	Reserved	Read Only. A read returns 0.
7	Reserved	Read Only. A read returns 0.

18.4.32 CR21

CR21 can only be accessed in the configuration state and after the CSR has been initialized to 21H. CR21 is used to select the high byte of the base address ADR[15:12] bits of Runtime Register Logical Device.

Runtime Register Address Decoding: address bits A[11:4] are programmable in CR30. The Runtime register base address bits A[3:0] are decoded as 0000b. An address matching the Runtime register base address bits A[15:4] decodes the specific address bits A[3:0] for the registers in Section 17.0, "Runtime Registers," on page 53.

The Runtime Register logical device base address is initialized using the base address bits located in two configuration registers: CR30-low byte and CR21-high byte. The Runtime Register base address can be set to 4080 locations on 16-byte boundaries from 0000H - FFF0H.

The Runtime Register base address bits A[3:0] are decoded as 0000b. The Runtime Register block uses full 16-bit addressing decoding. An address matching the Runtime Register base address bits A[15:4] is decoded using the specific address bits A[3:0] to target registers in Section 17.0.

When the activate bit in CR3A-bit1 is cleared to 0, no address decoding takes place for the Runtime Register block logical device.

TABLE 18-28: CR21

Runtime Register Base Address Register - High Byte		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR12	Runtime Register Base Address bits for decoder.
1	ADR13	
2	ADR14	
3	ADR15	
4	RESERVED	Reads return 0. Writes have no effect.
5	RESERVED	Reads return 0. Writes have no effect.
6	RESERVED	Reads return 0. Writes have no effect.
7	RESERVED	Reads return 0. Writes have no effect.

18.4.33 CR22

Register CR22 is reserved. The default value of this register after power up is 00H.

18.4.34 CR23

Register CR23 is reserved. The default value of this register after power up is 00H.

18.4.35 CR24

CR24 can only be accessed in the configuration state and after the CSR has been initialized to 24H. CR24 is used to select the base address of Serial Port 1 (UART1). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 1, set ADR9 and ADR8 to zero. Set CR24.0 to 0 when writing the UART1 Base Address.

Serial Port 1 Address Decoding: address bits A[15:10] must be '000000' to access UART1 registers. A[2:0] are decoded as XXXb.

TABLE 18-29: CR24

UART1 Base Address Register		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 1 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

18.4.36 CR25

CR25 can only be accessed in the configuration state and after the CSR has been initialized to 25H. CR25 is used to select the base address of Serial Port 2 (UART2). Serial Port 2 can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 2, set ADR9 and ADR8 to zero. Set CR25.0 to 0 when writing the UART2 Base Address.

Serial Port 2 Address Decoding: address bits A[15:10] must be '000000' to access UART2 registers. A[2:0] are decoded as XXXb.

TABLE 18-30: CR25

UART2 Base Address Register		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 2 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

18.4.37 CR26

Register CR26 is reserved. The default value of this register after power up is 00H.

18.4.38 CR27

Register CR27 is reserved. The default value of this register after power up is 00H.

18.4.39 CR28

CR28 can only be accessed in the configuration state and after the CSR has been initialized to 28H. CR28 is used to select the IRQ for Serial Port 1 (bits 7 - 4) and for Serial Port 2 (bits 3 - 0). The four bit IRQ encoding field is defined in Table 18-32, "IRQ Encoding". Any unselected IRQ output (registers CR28 - CR2A) is in tristate. Shared IRQs are not supported in the SIO1007.

TABLE 18-31: CR28

UART Interrupt Selection		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	UART2 IRQ Select	These bits are used to select IRQ for Serial Port 2. See Table 18-32.
7:4	UART1 IRQ Select	These bits are used to select IRQ for Serial Port 1. See Table 18-32.

TABLE 18-32: IRQ ENCODING

Bits [3:0] Or Bits [7:4]	IRQ Selected
0000	NONE
0001	IRQ_1
0010	IRQ_2
0011	IRQ_3
0100	IRQ_4
0101	IRQ_5

TABLE 18-32: IRQ ENCODING (CONTINUED)

Bits [3:0] Or Bits [7:4]	IRQ Selected
0110	IRQ_6
0111	IRQ_7
1000	IRQ_8
1001	IRQ_9
1010	IRQ_10
1011	IRQ_11
1100	IRQ_12
1101	IRQ_13
1110	IRQ_14
1111	IRQ_15

TABLE 18-33: UART INTERRUPT OPERATION

UART1		UART2		IRQ Pins	
UART1 OUT2 Bit	UART1 IRQ Output State	UART2 OUT2 Bit	UART2 IRQ Output State	UART1 Pin State	UART2 Pin State
0	Z	0	Z	Z	Z
1	asserted	0	Z	1	Z
1	de-asserted	0	Z	0	Z
0	Z	1	asserted	Z	1
0	Z	1	de-asserted	Z	0
1	asserted	1	asserted	1	1
1	asserted	1	de-asserted	1	0
1	de-asserted	1	asserted	0	1
1	de-asserted	1	de-asserted	0	0
Note: It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result. Note: Z = Don't Care.					

18.4.40 CR29

CR29 can only be accessed in the configuration state and after the CSR has been initialized to 29H. CR29 controls the HPMODE bit and is used to select the IRQ mapping (bits 0 - 3) for the IRQIN1 pin. The four bit IRQ encoding field is defined in Table 18-32, "IRQ Encoding". Any unselected IRQ output (registers CR28 - CR2A) is in tristate. Shared IRQs are not supported in the SIO1007.

TABLE 18-34: CR29

IRQIN1/HPMODE/SIRQ_CLKRUN_EN			
Type: R/W		**Default: 0X80 ON VCC POR**	
BIT NO.	**BIT NAME**	**DESCRIPTION**	
0-3	IRQIN1	Selects the IRQ for IRQIN1. (See Application Note in the Routable IRQ Inputs Section 12.2.)	
4	HPMODE	See Figure 10-1– Infrared Interface Block Diagram	
		0	Select IRMODE (default)
		1	Select IRRX3
5-6	RESERVED	Not Writeable, Reads Return "0"	
7	SIRQ_CLKRUN_EN	Serial IRQ and CLKRUN enable bit. 0 = Disable 1 = Enable (default)	

18.4.41 CR2A

CR2A can only be accessed in the configuration state and after the CSR has been initialized to 2AH. CR2A is used to select the IRQ mapping (bits 0 - 3) for the IRQIN2 pin. The four bit IRQ encoding field is defined in Table 18-32 on page 74. Any unselected IRQ output (registers CR28 - CR2A) is in tristate. Shared IRQs are not supported in the SIO1007.

TABLE 18-35: CR2A

IRQIN2		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	IRQIN2	Selects the IRQ for IRQIN2. (See Application Note in the Routable IRQ Inputs Section 12.2.)
7:4	Reserved	Read Only. A read returns 0.

18.4.42 CR2B

CR2B can only be accessed in the configuration state and after the CSR has been initialized to 2BH. CR2B is used to set the SCE (FIR) base address ADR[10:3].

The SCE (FIR) logical device base address is initialized using the base address bits located in two configuration registers: CR2B-low byte and CR1E-high byte. The SCE base address can be set to 8160 locations on 8-byte boundaries from 0000H - FFF8H.

The SCE (FIR) base address bits A[2:0] are decoded as 000b. The SCE (FIR) block uses full 16-bit addressing decoding. An address matching the SCE (FIR) base address bits A[15:3] is decoded using the specific address bits A[2:0] to target registers in SCE (FIR).

When the SCE (FIR) logical device activate bit CR3A-bit0 is cleared to 0, no address decoding takes place for the SCE (FIR) logical device.

TABLE 18-36: CR2B

SCE (FIR) Base Address Register - Low Byte		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR3	FIR Base Address bits for decoder.
1	ADR4	
2	ADR5	
3	ADR6	
4	ADR7	
5	ADR8	
6	ADR9	
7	ADR10	

18.4.43 CR2C

CR2C can only be accessed in the configuration state and after the CSR has been initialized to 2CH. Bits D[3:0] of this register are used to select the DMA for the SCE (FIR). Bits D[7:4] are Reserved. Reserved bits cannot be written and return 0 when read. Any unselected DMA Request output (DRQ) is in tristate.

TABLE 18-37: CR2C

SCE (FIR) DMA Select Register						
Type: R/W					**Default: 0X0F ON VCC POR**	
BIT NO.	**BIT NAME**	**DESCRIPTION**				
3:0	DMA Select	BIT3	BIT2	BIT1	BIT0	DMA SELECTED
		0	0	0	0	RESERVED
		0	0	0	1	DMA1
		0	0	1	0	DMA2
		0	0	1	1	DMA3
		0	1	0	0	RESERVED
		. .	. .	. .	. .	. .
		1	1	1	0	RESERVED
		1	1	1	1	NONE
7:4	Reserved	Read Only. A read returns 0.				

18.4.44 CR2D

CR2D can only be accessed in the configuration state and after the CSR has been initialized to 2DH. CR2D is used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

The IRCC v2.0 block includes an 8-bit IR Half Duplex Time-out register in SCE Register Block 5, Address 1 that interacts with configuration register CR2D. These two registers behave like the other IRCC Legacy controls where either source uniformly updates the value of both registers when either register is explicitly written using IOW or following a device-level POR. IRCC software resets do not affect these registers.

The IR Half Duplex Time-out is programmable from 0 to 25.5mS in 100µS increments, as follows:

IR HALF DUPLEX TIME-OUT = (CR2D) x 100µS

TABLE 18-38: CR2D

IR Half Duplex Timeout		
Type: R/W		**Default: 0X03 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	IR Half Duplex Time Out	These bits are used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

18.4.45 CR2E

CR2E can only be accessed in the configuration state and after the CSR has been initialized to 2EH. CR2E is directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

TABLE 18-39: CR2E

Software Select A		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select A	These bits are directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

18.4.46 CR2F

CR2F can only be accessed in the configuration state and after the CSR has been initialized to 2FH. CR2F is directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

TABLE 18-40: CR2F

Software Select B		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select B	These bits are directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

18.4.47 CR30

CR30 can only be accessed in the configuration state and after the CSR has been initialized to 21H. CR30 is used to select the low byte of the base address (ADR[11:4] bits of Runtime Register Logical Device.

The Runtime Register logical device base address is initialized using the base address bits located in two configuration registers: CR30-low byte and CR21-high byte. The Runtime Register base address can be set to 4080 locations on 16-byte boundaries from 0000H - FFF0H.

The Runtime Register base address bits A[3:0] are decoded as 0000b. The Runtime Register block uses full 16-bit addressing decoding. An address matching the Runtime Register base address bits A[15:4] is decoded using the specific address bits A[3:0] to target registers in Section 17.0, "Runtime Registers," on page 53.

When the activate bit in CR3A-bit1 is cleared to 0, no address decoding takes place for the Runtime Register block logical device.

TABLE 18-41: CR30

Runtime Registers Block Base Address-Low Byte		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR4	The bits in this register are used to program the location of the Runtime Register Block Base Address.
1	ADR5	
2	ADR6	
3	ADR7	
4	ADR8	
5	ADR9	
6	ADR10	
7	ADR11	

18.4.48 CR31

CR31 can only be accessed in the configuration state and after the CSR has been initialized to 31H. CR31 is GPIO Direction Register 1 and is used to select the direction of GP10-GP17 pins.

TABLE 18-42: CR31

GPIO Direction Register 1		
Type: R/W		**Default: 0X00 ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP10	The bits in this register are used to select the direction of the GP10-GP17 pins. 0=Input 1=Output
1	GP11	
2	GP12	
3	GP13	
4	GP14	
5	GP15	
6	GP16	
7	GP17	

18.4.49 CR32

CR32 can only be accessed in the configuration state and after the CSR has been initialized to 32H. CR32 is GPIO Polarity Register 1 and is used to select the polarity of GP10-GP17 pins.

TABLE 18-43: CR32

GPIO Polarity Register 1		
Type: R/W		**Default: 0X00 ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP10	The bits in this register are used to select the polarity of the GP10-GP17 pins. 0=Non-Inverted 1=Inverted
1	GP11	
2	GP12	
3	GP13	
4	GP14	
5	GP15	
6	GP16	
7	GP17	

18.4.50 CR33

CR33 can only be accessed in the configuration state and after the CSR has been initialized to 33H. CR33 is GPIO Output Register and is used to select the output buffer of GP10-GP17.

TABLE 18-44: CR33

GPIO Output Type Register 1		
Type: R/W		**Default: 0XFF ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP10	The bits in this register are used to select the output buffer type of the GP10-GP17 pins. 0=Push-pull 1=Open Drain
1	GP11	
2	GP12	
3	GP13	
4	GP14	
5	GP15	
6	GP16	
7	GP17	

18.4.51 CR34

CR34 can only be accessed in the configuration state and after the CSR has been initialized to 34H. CR34 is Alternate Function Register 1. It is used to select the polarity IO_PME pin, and select alternate function on GP13 and GP14 pins.

TABLE 18-45: CR34

Alternate Function and IO_PME# Configuration Register		
Type: R/W		**Default: 0x01 on VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	IO_PME# Buffer Select	The bits in this register are used to select the output buffer type of the IO_PME# pin 0=Push-pull 1=Open Drain (default)
1	IO_PME# Polarity select	This bit is used to select the polarity of the IO_PME# pin. 0=Non-Inverted 1=Inverted **Note:** Configuring this pin function with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. (See Bit 4).
2	CLKI32 Alternate Function Select	0= The alternate function is determined by Bit[6] of this register (Bit[6] is the GP13 Alternate Function Select bit). (default) 1=CLKI32
3	GP15 Alternate Function Select	0=GPIO 1=CIRRX
4	GP16 Alternate Function Select	0=GPIO 1=CIRTX
5	GP12 Alternate. Function Select	0=GPIO 1=nIO_SMI **Note:** Selecting the nIO_SMI function with GP12 configured with non-inverted polarity will give an active low output signal. The output type can be programmed for open drain via CR33.

TABLE 18-45: CR34 (CONTINUED)

Alternate Function and IO_PME# Configuration Register		
Type: R/W		**Default: 0x01 on VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
6	GP13 Alternate Function Select	If Bit[2] of this register is 1 then the GP13 pin is configured as the CLKI32 input and bit[6] has no effect. If Bit[2] of this register is 0 then the alternate function enabled on the GP13 pin is determined by the setting of bit[6] as shown. **Bit [2] / Bit [6] / Definition** 1 / x / CLKI32 0 / 0 / GPIO (default) 0 / 1 / IRQIN1
7	GP14 Alternate Function Select	0=GPIO (See Application Note in the Routable IRQ Inputs section 13.2.) 1=IRQIN2

18.4.52 CR35

CR35 can only be accessed in the configuration state and after the CSR has been initialized to 35H. CR35 is GPIO Direction Register 3 and is used to select the direction of GP30-GP37 pins.

TABLE 18-46: CR35

GPIO Direction Register 3		
Type: R/W		**Default: 0X00 ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the direction of the GP30-GP37 pins. 0=Input 1=Output
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

18.4.53 CR36

CR36 can only be accessed in the configuration state and after the CSR has been initialized to 36H. CR36 is GPIO Polarity Register 3 and is used to select the polarity of GP30-GP37 pins.

TABLE 18-47: CR36

GPIO Polarity Register 3		
Type: R/W		**Default: 0X00 ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the polarity of the GP30-GP37 pins. 0=Non-Inverted 1=Inverted
1	GP31	
2	GP32	
3	GP33	

TABLE 18-47: CR36 (CONTINUED)

GPIO Polarity Register 3		
Type: R/W		**Default: 0X00 ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
4	GP34	
5	GP35	
6	GP36	
7	GP37	

18.4.54 CR37

CR37 can only be accessed in the configuration state and after the CSR has been initialized to 37H. CR37 is GPIO Pull-up Register 3 and is used to select the weak pull-up (45µ A) for GP30-GP37 pins.

TABLE 18-48: CR37

GPIO Pullup Register 3		
Type: R/W		**Default: 0XFF ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the pull-up of the GP30-GP37 pins. 0=No pull-up 1=Pull-up enabled
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

18.4.55 CR38

CR38 can only be accessed in the configuration state and after the CSR has been initialized to 38H. CR38 is GPIO Pull-up Register 1 and is used to select the weak pull-up (45µ A) for GP10-GP17 pins.

TABLE 18-49: CR38

GPIO Pullup Register 1		
Type: R/W		**Default: 0XFF ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP10	The bits in this register are used to select the pull-up of the GP10-GP17 pins. 0=No pull-up 1=Pull-up enabled
1	GP11	
2	GP12	
3	GP13	
4	GP14	

TABLE 18-49: CR38 (CONTINUED)

GPIO Pullup Register 1		
Type: R/W		**Default: 0XFF ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
5	GP15	
6	GP16	
7	GP17	

18.4.56 CR39

CR39 can only be accessed in the configuration state and after the CSR has been initialized to 39H. CR39 is GPIO Output Register and is used to select the output buffer of GP30-GP37pins.

TABLE 18-50: CR39

GPIO Output Register 3		
Type: R/W		**Default: 0XFF ON VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the output buffer type of the GP30-GP37 pins. 0=Push-pull 1=Open Drain
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

18.4.57 CR3A

CR3A can only be accessed in the configuration state and after the CSR has been initialized to 3AH.

TABLE 18-51: CR3A

Logical Device Activate Register		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	SCE(FIR)	0 = Disables the host access to SCE (FIR) logical device (default). 1 = Enables the host access to SCE (FIR) logical device's I/O runtime register space for the IRCC2.0 block. The I/O address is selected by the SCE(FIR) Base Address Registers.
1	Runtime Register	0 = Disables the host access to Runtime Register logical device (default). 1 = Enables the host access to Runtime Register logical device's I/O register space for the Runtime Register block. The I/O address is selected by the Runtime Register Base Address Registers.
2	CIRCC2	0 = Disables the host access to CIRCC2 logical device (default). 1 = Enables the host access to CIRCC2 logical device's I/O runtime register space for the CIRCC2 block. The I/O address is selected by the CIRCC2 Base Address Registers.

TABLE 18-51: CR3A (CONTINUED)

Logical Device Activate Register		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
3	LPC Dock Note 18-9	A high level on this bit, enables the host access to LPC Docking logical device's I/O runtime register space. The I/O address is selected by the LPC Docking Base Address Registers. A low level on this bit disables the host access to LPC Docking logical device (default).
4,5,6, 7	Reserved	Read Only. A read returns 0

Note 18-9 The Activate bit disables the selected address range for the logical device. When the Activate bit is set and the corresponding Logical Device resides at a valid I/O base address, the Logical Device will participate in Plug-and-Play range checking.

APPLICATION NOTE: When the Activate bit (CR3A bit 3 to '1'), the values in CR3B and CR3C must be valid; otherwise, an undefined state and undesired behavior may result.

18.4.58 CR3B-3C

CR3B can only be accessed in the configuration state and after the CSR has been initialized to 3BH. CR3C can only be accessed in the configuration state and after the CSR has been initialized to 3CH. CR3B and CR3C are used to select the base address of LPC Docking. Valid addresses for LPC Docking runtime register space can be set to locations on single -byte boundaries from 0000H - FFFFH. To disable LPC Docking runtime register decoding, set the Activate bit (CR3A-bit 3 to '0').

Set CR3A-bit 3 to '0' (to disable LPC Docking runtime register decoding) when writing the LPC Docking Base Address registers CR3B and CR3C.

The LPC Docking runtime register uses full 16-bit addressing decoding.

TABLE 18-52: CR3B

LPC Docking Base Address Register High Byte		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR8	LPC Docking Base Address bits for decoder.
1	ADR9	
2	ADR10	
3	ADR11	
4	ADR12	
5	ADR13	
6	ADR14	
7	ADR15	

TABLE 18-53: CR3C

LPC Docking Base Address Register Low Byte		
Type: R/W		**Default: 0X00 ON VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR0	LPC Docking Base Address bits for decoder.
1	ADR1	
2	ADR2	
3	ADR3	
4	ADR4	
5	ADR5	
6	ADR6	
7	ADR7	

18.5 Logical Device Base I/O Address and Range

TABLE 18-54: I/O BASE ADDRESS CONFIGURATION REGISTER DESCRIPTION

Logical Device	Register Index	Base I/O Range	Fixed Base Ofsets
Serial Port 1	CR24 See Note 18-11	[0x0100:0x03F8] On 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
Serial Port 2 (Async. Comm Engine)	CR25 See Note 18-11	[0x0100:0x03F8] On 8-byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
Serial Port 2 (Sync. Comm Engine)	CR2B, CR1E (FIR/CIR) See Note 18-9 on page 84 and Note 18-11	[0x0000:0x07F8] On 8-byte boundaries	+0 : DR/SCEA/CIRC/IDH/(IRDACR/BOFH) +1 : INTID/SCEB/CIRCR/IDL/BOFL +2 : IER/FIFOT/CIRBR/CID/BWCL +3 : LSR/LSA/VERN/(BWCH/TDSH) +4 : LCA/(IRQL/DMAC)/TDSL +5 : LCB/RDSH +6 : BS/RDSL +7 : MCR
CIRCC2	CR1F, CR20 See Note 18-9 on page 84 and Note 18-11	[0x0000:0x07F8] On 8-byte boundaries	+0 : DR/SCEA/CIRC/IDH/(IRDACR/BOFH) +1 : INTID/SCEB/CIRCR/IDL/BOFL +2 : IER/FIFOT/CIRBR/CID/BWCL +3 : LSR/LSA/VERN/(BWCH/TDSH) +4 : LCA/(IRQL/DMAC)/TDSL +5 : LCB/RDSH +6 : BS/RDSL +7 : MCR
Runtime Register Block	CR30, CR21 See Note 18-9 on page 84	[0x0000:0x0FF0] On 16-byte boundaries	+00 : PME_STS +0F : GP4 (See Table 17-1in the Runtime Registers section for Full List)

TABLE 18-54: I/O BASE ADDRESS CONFIGURATION REGISTER DESCRIPTION (CONTINUED)

Logical Device	Register Index	Base I/O Range	Fixed Base Ofsets
Config. Port	CR12 - CR13 See Note 18-10	[0x0000:0x07FE] On 2-byte boundaries	See Configuration Registers in Table 18-3. They are accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.
LPC Docking	CR3B-3C See Note 18-9 on page 84	[0x0000:0x0FFF] On single byte boundaries	+0 : Docking LPC Switch Register

Note 18-10 The Configuration Port is at either 0x002E, 0x004E, 0x162E or 0x164E (controlled by the SYSOPT[1:0] Strap options) at power up and can be relocated via CR12 and CR13.

Note 18-11 The UART and IR Power Register at CR02 Power Control bits disable the respective logical device and associated pins, however the power control bit does not disable the selected address range for the logical device. To disable the host address registers software must clear the activate bits in CR3A, the Logical Device Activate Register. Devices that are powered down and still activated will participate in Plug-and-Play range checking.

19.0 OPERATIONAL DESCRIPTION

19.1 Maximum Ratings

Operating Temperature Range ..... 0^oC to $+70^oC$

Storage Temperature Range ..... -55^o to $+150^oC$

Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020

Positive Voltage on any pin, with respect to Ground ..... V_{CC}+0.3V

Negative Voltage on any pin, with respect to Ground ..... -0.3V

Maximum V_{CC} ..... +5.5V

Note:

- Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.
- When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

19.2 DC Electrical Characteristics

($T_A = 0^0C – 70^0C$, V_{CC} = +3.3 V ± 10%)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
Input Leakage, I and IS Buffers						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	$V_{IN} = V_{CC}$
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 19-1)

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 19-1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 19-1)
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 19-1)
Progammable Pullup current	I_{pu}	18	34.5	60	µA	(Note 19-7)
Backdrive Protect/ChiProtect (Note 19-5)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
5V Tolerant Pins (Note 19-5)	I_{IL}			± 10	µA	V_{CC} = 3.3V V_{IN} = 5.5V Max
LPC Bus Pins (Note 19-5 and Note 19-6)	I_{IL}			± 10	µA	V_{CC} = 0V and V_{CC} = 3.3V V_{IN} = 3.6V Max
VCC Supply Current Active	I_{CC}			10 (Note 19-2)	mA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V

Parameter	Symbol	MIN	TYP	MAX	Units	Comments
Trickle Supply Voltage (Note 19-4)	V_{TR}	V_{CC} min -.5V		V_{CC} max	V	V_{CC} must not be greater than .5V above V_{TR}
VTR Supply Current Active (Note 19-2 and Note 19-3)	I_{TR}			7	mA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V

Note 19-1 All output leakage's are measured with all pins in high impedance

Note 19-2 These values are estimated. They will be updated after characterization. Contact Microchip for the latest values.

Note 19-3 Max I_{TR} with V_{CC} = 3.3V (nominal) is 0.2mA.

Max I_{TR} with V_{CC} = 0V (nominal) is 60µA.

Note 19-4 The minimum value given for V_{TR} applies when V_{CC} is active. When V_{CC} is 0V, the minimum V_{TR} is 0V.

Note 19-5 See Section 5.1, "3.3 Volt Operation / 5 Volt Tolerance".

Note 19-6 Table 4-1and the associated Note 4-5 identify the non-5V tolerant pins.

Note 19-7 Programmable pullup resistance on GPIO are controlled by CR37 and CR38.

CAPACITANCE $T_A = 25^0C$; fc = 1MHz; V_{CC} = 3.3V ±10%

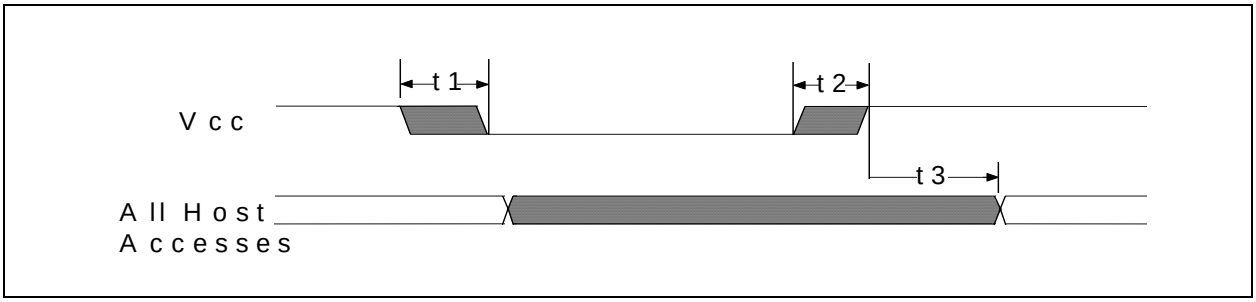
Parameter	Symbol	Limits			Unit	Test Condition
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

20.0 TIMING DIAGRAMS

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

Name	Capacitance Total (pF)
SER_IRQ	50
nLAD[3:0]	50
nLDRQ	50
TXD1	50
nCLKRUN	50

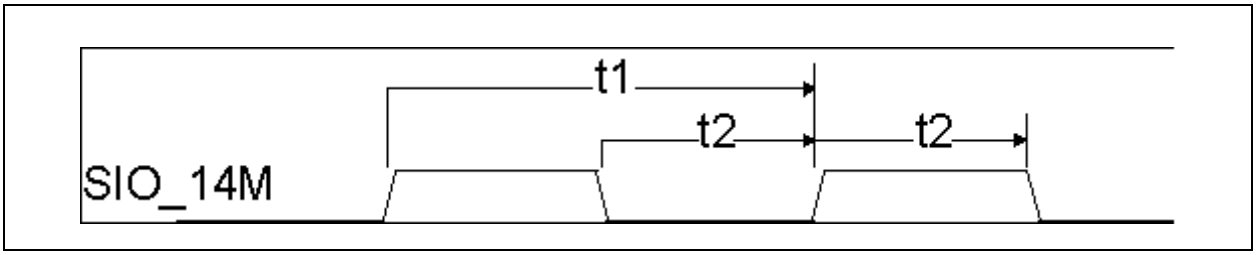
FIGURE 20-1: POWER-UP TIMING



Name	Description	MIN	TYP	MAX	Units
t1	Vcc Slew from 2.7V to 0V	300			s
t2	Vcc Slew from 0V to 2.7V	100			s
t3	All Host Accesses After Powerup (Note 20-1)	125		500	s

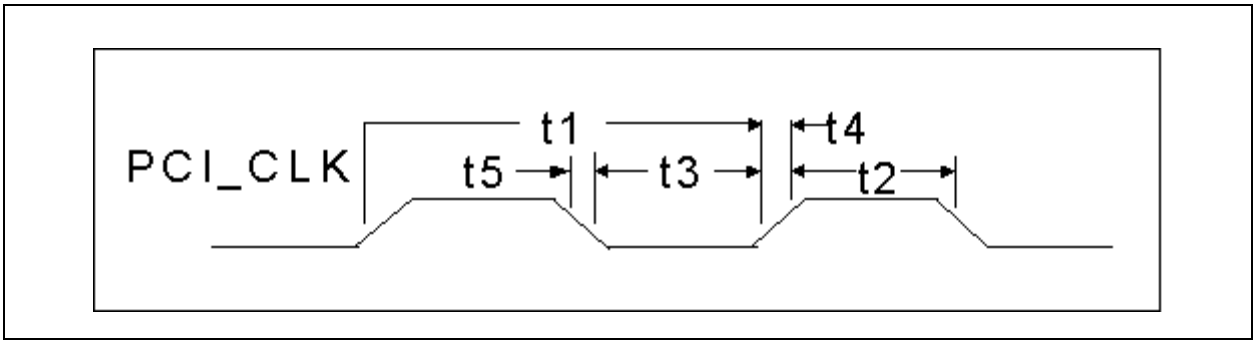
Note 20-1 Internal write-protection period after Vcc passes 2.7 volts on power-up.

FIGURE 20-2: INPUT CLOCK TIMING



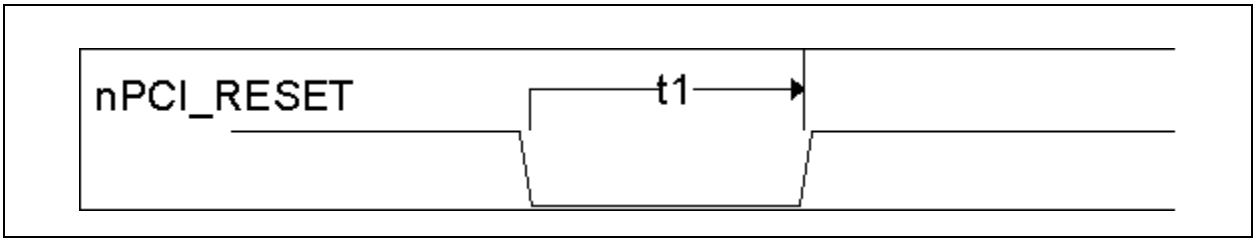
Name	Description	MIN	TYP	MAX	Units
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
	Clock Rise Time/Fall Time (not shown)			5	ns

FIGURE 20-3: PCI CLOCK TIMING



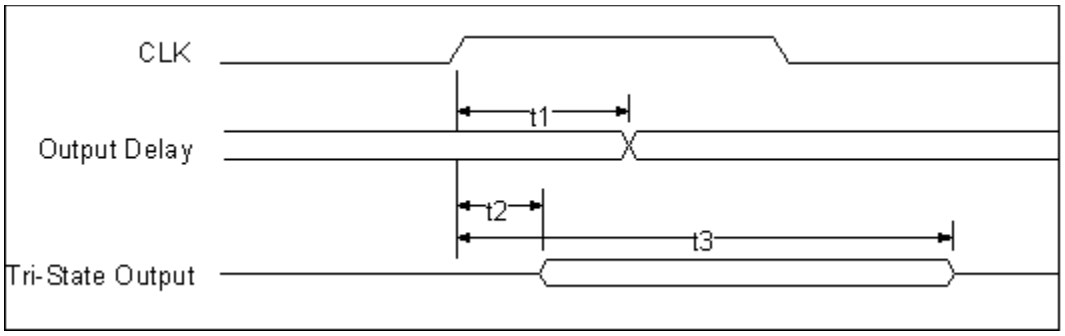
Name	Description	MIN	TYP	MAX	Units
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

FIGURE 20-4: RESET TIMING



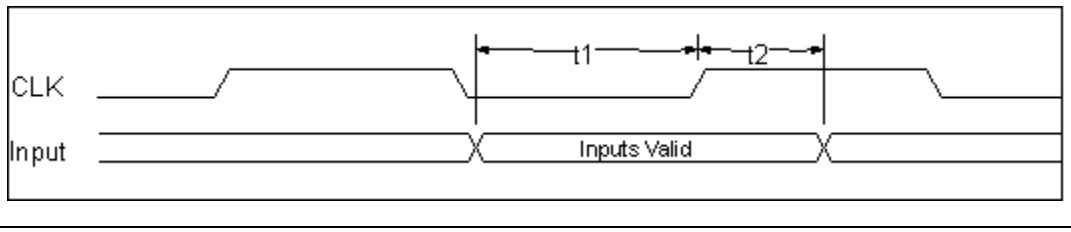
Name	Description	MIN	TYP	MAX	Units
t1	PCI_RESET# width	1			ms

FIGURE 20-5: OUTPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS



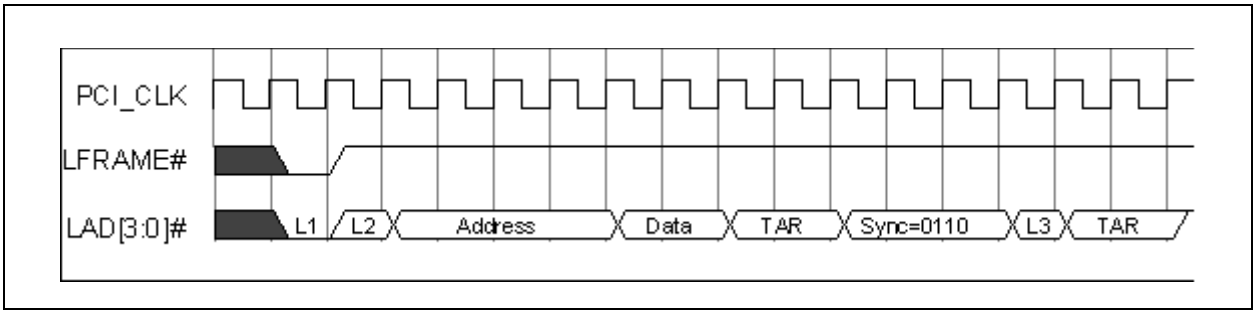
Name	Description	MIN	TYP	MAX	Units
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

FIGURE 20-6: INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS



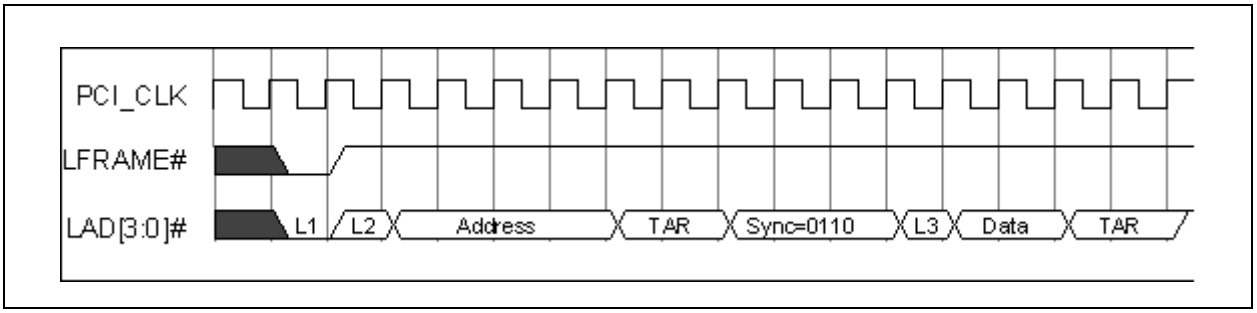
Name	Description	MIN	TYP	MAX	Units
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns

FIGURE 20-7: I/O WRITE



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 20-8: I/O READ



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 20-9: DMA REQUEST ASSERTION THROUGH LDRQ#

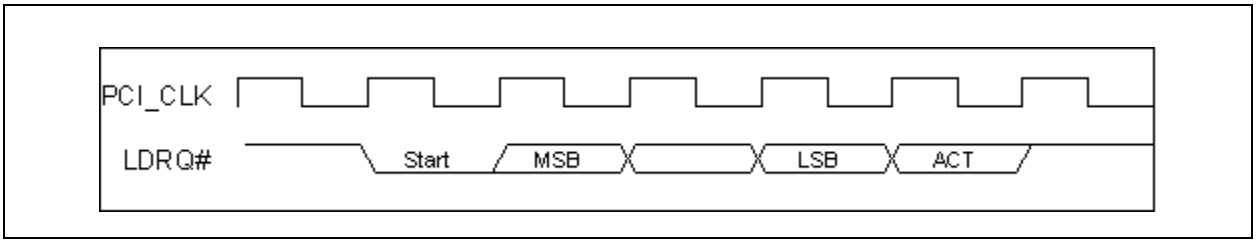
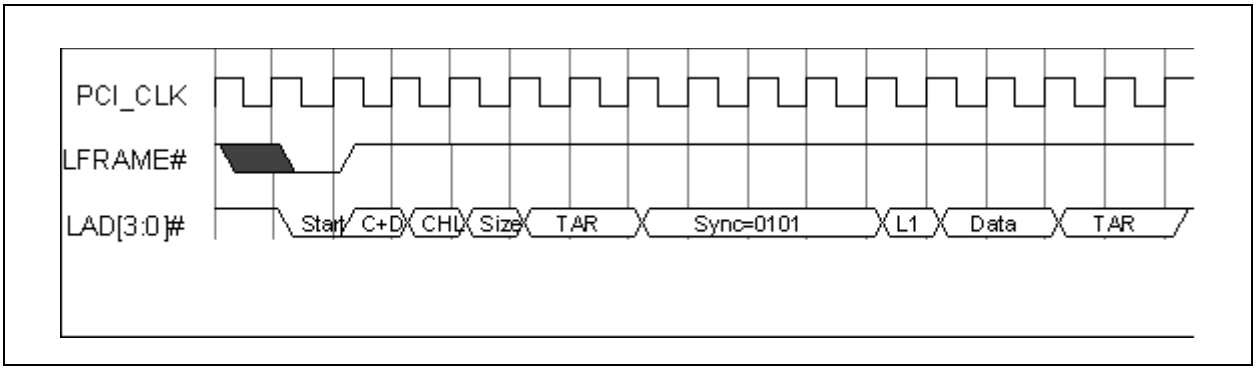
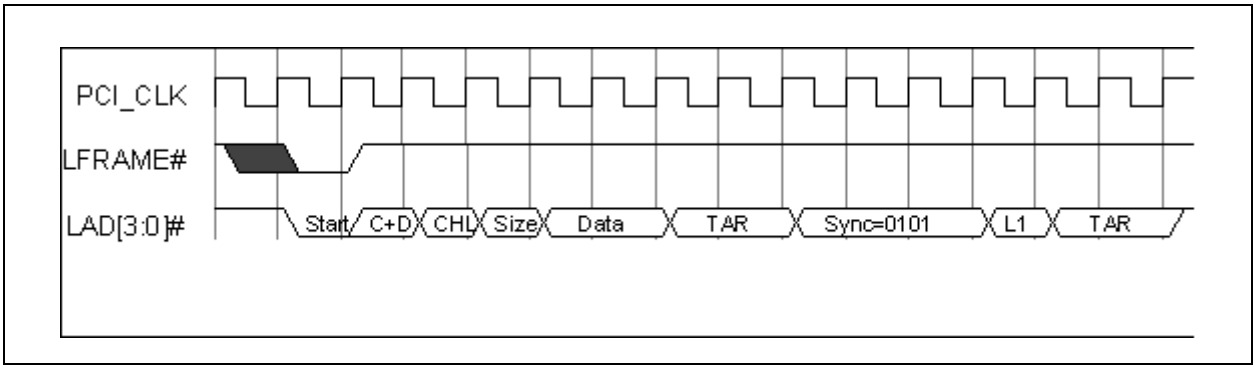


FIGURE 20-10: DMA WRITE (FIRST BYTE)



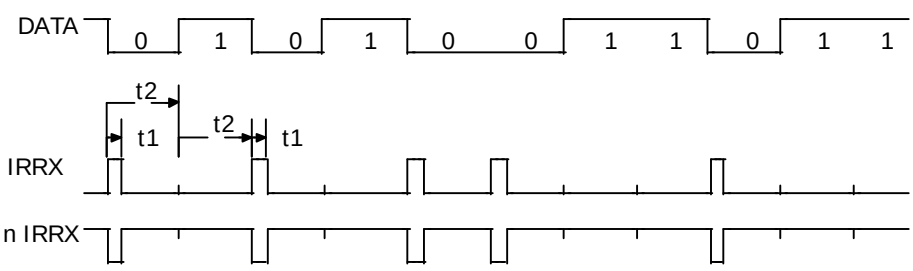
Note: L1=Sync of 0000

FIGURE 20-11: DMA READ (FIRST BYTE)



Note: L1=Sync of 0000

FIGURE 20-12: IRDA RECIEVE TIMING

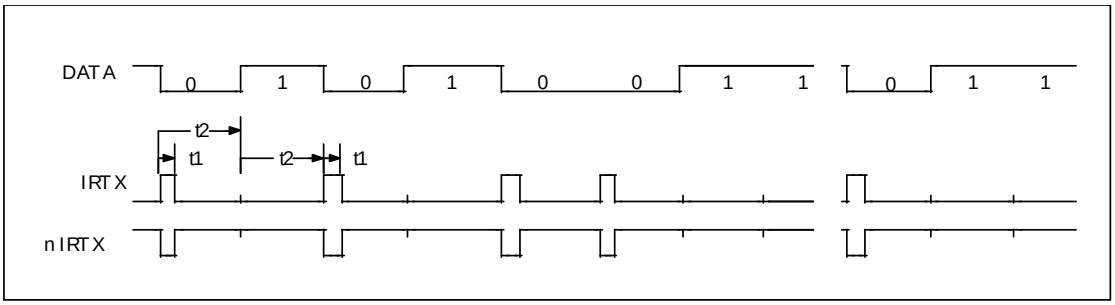


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

FIGURE 20-13: IRDA TRANSMIT TIMING

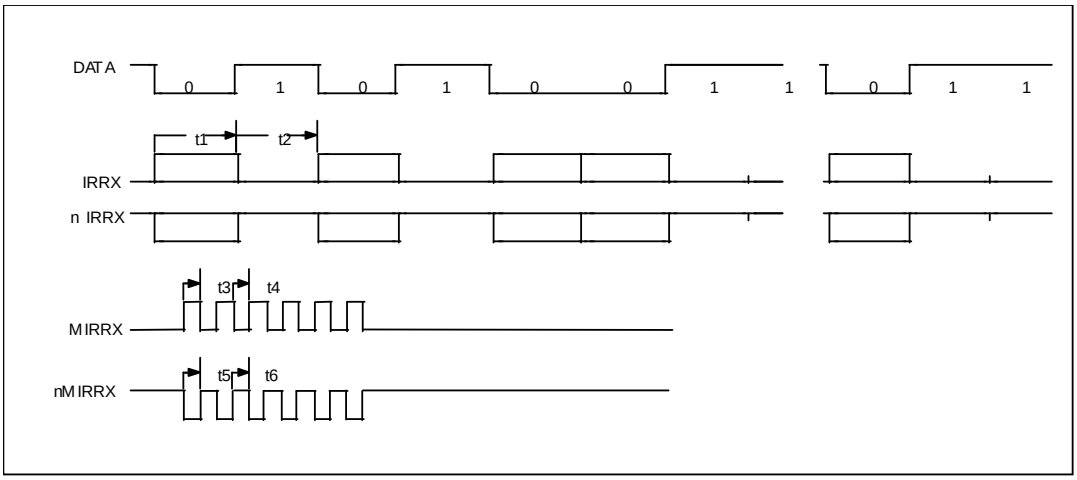


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP 95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0

FIGURE 20-14: AMPLITUDE SHIFT KEYED IR RECEIVE TIMING

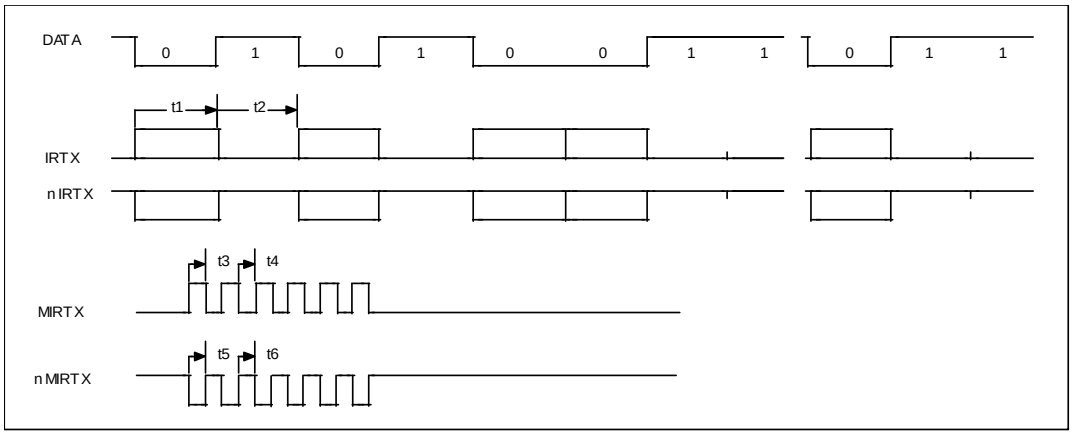


	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

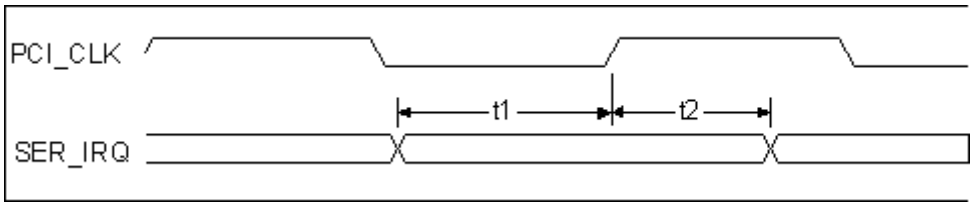
FIGURE 20-15: AMPLITUDE SHIFT KEYED IR TRANSMIT TIMING



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

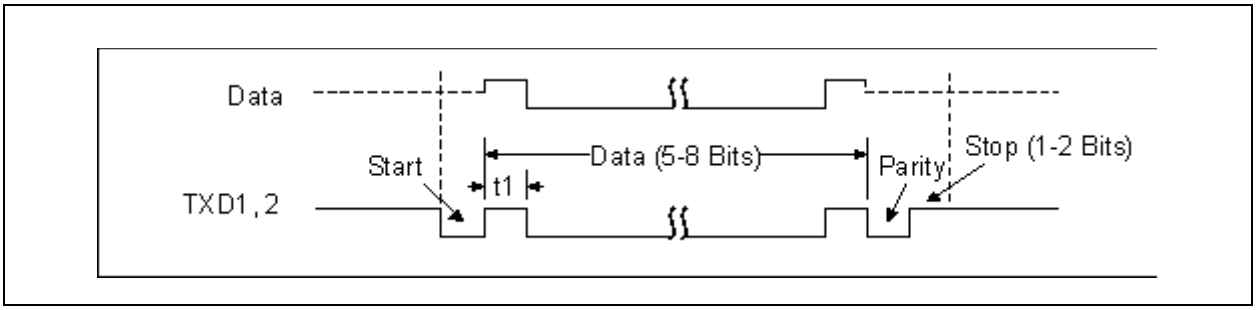
Notes:
1. IRTX L5, CRF1 Bit 1 = 1 (default)
nIRTX: L5, CRF1 Bit 1 = 0
MIRTX, nMIRTX are the modulated outputs

FIGURE 20-16: SETUP AND HOLD TIME



Name	Description	MIN	TYP	MAX	Units
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

FIGURE 20-17: SERIAL PORT DATA



Name	Description	MIN	TYP	MAX	Units
t1	Serial Port Data Bit Time		t_{BR} (Note 20-2)		nsec

Note 20-2 t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

21.0 XNOR-CHAIN TEST MODE

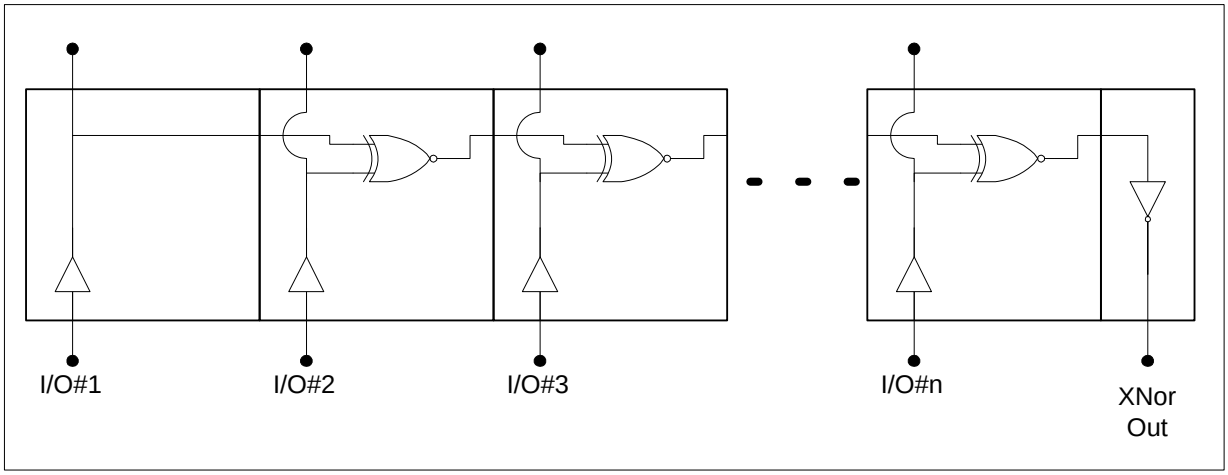
The SIO1007 provides board test capability through the implementation of XNOR chain. See following sub-sections.

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See Figure 21-1 below. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the SIO1007 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

FIGURE 21-1: XNOR-CHAIN TEST STRUCTURE



21.1 Entering and Exiting Test Mode

XNOR-Chain test mode can be entered as follows:

On the rising (deasserting) edge of nPCI_RESET, drive nLFRAME low and drive LAD[0] low.

Exit XNOR-Chain test mode as follows:

On the rising (deasserting) edge of nPCI_RESET, drive either nLFRAME or LAD[0] high.

The nPCI_RESET pin is not included in the XNOR-Chain. The XNOR-Chain output is on the nIO_PME pin. See the following subsections for more details.

21.2 Pin List of XNOR Chain

All pins on the chip are inputs to the first XNOR chain, with the exception of the following:

1. VCC (5 pins) and VTR (1 pin).
2. VSS (6 pins).
3. nPCI_RESET
4. nIO_PME This is the chain output.

To put the chip in the first XNOR chain test mode, tie LAD0 and nLFRAME low. Then toggle nPCI_RESET from a low to a high state. Once the chip is put into XNOR chain test mode, LAD0 and nLFRAME become part of the chain.

To exit the first XNOR chain test mode tie LAD0 or nLFRAME high. Then toggle nPCI_RESET from a low to a high state. A VCC POR will also cause the XNOR chain test mode to be exited. To verify the test mode has been exited, observe the output at nIO_PME. Toggling any of the input pins in the chain should not cause its state to change.

21.3 Setup of XNOR Chain

Warning: Ensure power supply is off during setup.

1. Connect VSS pins to ground.
2. Connect VCC pins and VTR pin to VCC (3.3V).
3. Connect an oscilloscope, voltmeter, or other measurement device to the nIO_PME pin.
4. All other pins should be tied to ground.

21.4 Testing Procedure

1. Turn power on.
2. With LAD0 pin and nLFRAME pin, low, bring nPCI_RESET pin high. The chip is now in XNOR chain test mode. At this point, all inputs to the first XNOR chain are low. The output, on nIO_PME (pin 17), should also be low. Refer to INITIAL CONFIG on Table 21-1.
3. Bring pin 64 high. The output on the nIO_PME pin should go high. Refer to STEP ONE on Table 21-1.
4. In descending pin order, bring each input high. The output should switch states each time an input is toggled. Continue until all inputs are high. The output on nIO_PME should now be low. Refer to END CONFIG on Table 21-1.
5. The current state of the chip is now represented by INITIAL CONFIG in Table 21-2.
6. Each input should now be brought low, starting at pin one and continuing in ascending order. Continue until all inputs are low. The nIO_PME output should now be low. Refer to Table 21-2.
7. To exit test mode, tie LAD0 (pin 20) OR nLFRAME (pin 24) high, and toggle nPCI_RESET from a low to a high state.An odd number of inputs (all grounded) yield a logic high on the chain output pin. If all the inputs are held high the value on the chain output should be low.

TABLE 21-1: TOGGLING INPUTS IN DESCENDING ORDER

	Pin 64	Pin 63	Pin 62	Pin 61	Pin 60	PIN ...	PIN 1	Output Pin nIO_PME
INITIAL CONFIG	L	L	L	L	L	L	L	L
STEP 1	H	L	L	L	L	L	L	H
STEP 2	H	H	L	L	L	L	L	L
STEP 3	H	H	H	L	L	L	L	H
STEP 4	H	H	H	H	L	L	L	L
STEP 5	H	H	H	H	H	L	L	H
…	…	…	…	…	…	…	…	…
STEP N-1	H	H	H	H	H	H	L	H
END CONFIG	H	H	H	H	H	H	H	L

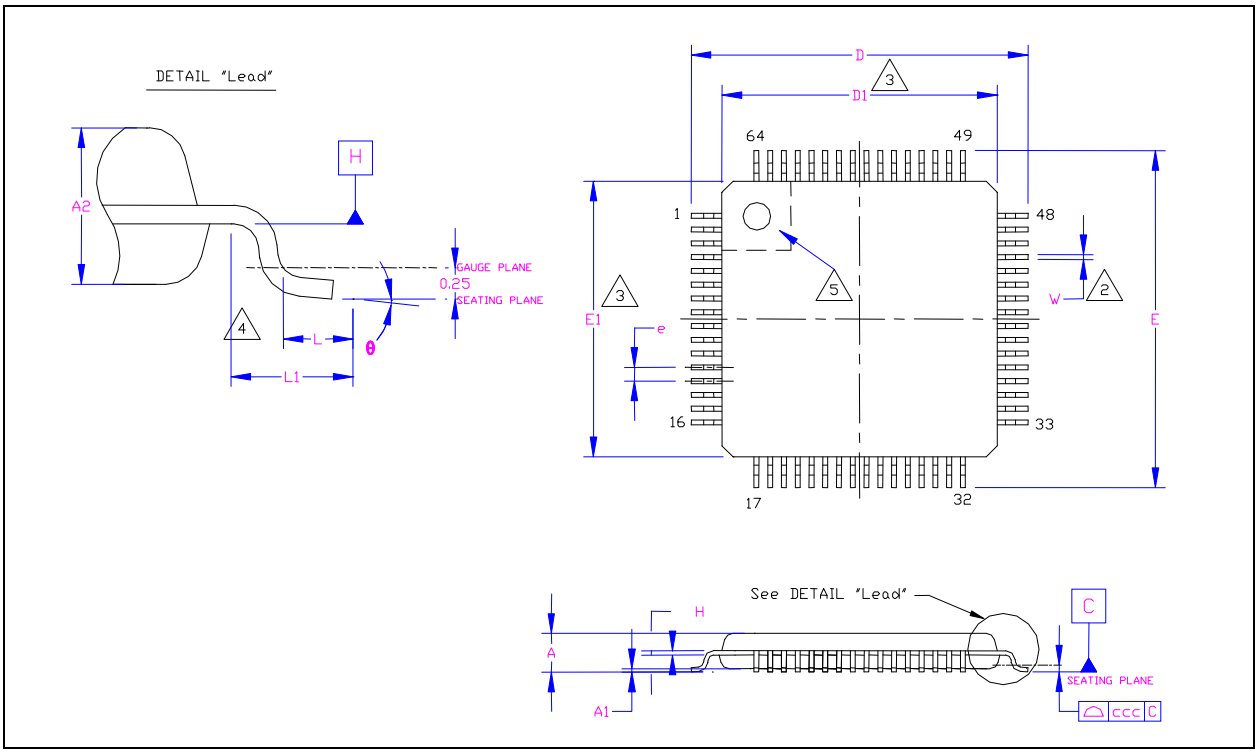
TABLE 21-2: TOGGLING INPUTS IN ASCENDING ORDER

	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin ...	Pin 64	Output Pin nIO_PME
INITIAL CONFIG	H	H	H	H	H	H	H	L
STEP 1	L	H	H	H	H	H	H	H
STEP 2	L	L	H	H	H	H	H	L
STEP 3	L	L	L	H	H	H	H	H
STEP 4	L	L	L	L	H	H	H	L
STEP 5	L	L	L	L	L	H	H	H
	…	…	…	…	…	…	…	…
STEP N-1	L	L	L	L	L	L	H	H
END CONFIG	L	L	L	L	L	L	L	L

22.0 PACKAGE OUTLINE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

FIGURE 22-1: 64-PIN STQFP PACKAGE



	Min	Nominal	Max	Remarks
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	8.80	9.00	9.20	X Span
D1	6.80	7.00	7.20	X body Size
E	8.80	9.00	9.20	Y Span
E1	6.80	7.00	7.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00 REF.	~	Lead Length
e	0.40 Basic			Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
ccc	~	~	0.08	Coplanarity

Note 1: Controlling Unit: millimeter.

2: Tolerance on the true position of the leads is ± 0.035 mm maximum.

3: Package body dimensions D1 and E1 do not include the mold protrusion.

4: Maximum mold protrusion is 0.25 mm per side. D1 and E1 dimensions determined at datum plane H.

5: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

6: Details of pin 1 identifier are optional but must be located within the zone indicated.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002020A (10-09-15)	Replaces previous SMSC version Rev. 0.11 (03-03-05)	

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PART NO.[1] - XXX[2] - [X][3]	Example:
Device / Package / Tape and Reel Option	SIO1007-JV = 64-pin STQFP

Device:	SIO1007 [1]		
Package:	JV	=	64-pin STQFP [2]
Tape and Reel Option:	Blank	=	Tray packaging
	TR	=	Tape and Reel [3]

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html .

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ISBN: 9781632778765

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