

STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	BU2092F/BU2092FV
FUNCTION	12bit Serial IN / Parallel Out Driver
FEATURES	1) Nch open drain, capable of driving a maximum of 25mA 2) 25V high voltage output can be used. 3) This product can be operated on low voltage. (2.7V)

● ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V _{DD}	7.0	V
Power Dissipation1	Pd1	450/400(F/FV)	mW
Power Dissipation2	Pd2	550/650*(F/FV)	mW
Operating Temperature Range	T _{opr}	-25~+75	°C
Storage Temperature Range	T _{stg}	-55~+125	°C
Input Voltage	V _{IN}	-0.3~V _{DD} +0.3	V

* Output (Q0~Q11) are 25V (Max.)

* 50mm×50mm×1.6mm/70mm×70mm×1.6mm glass epoxy (F/FV)

• Status of this document

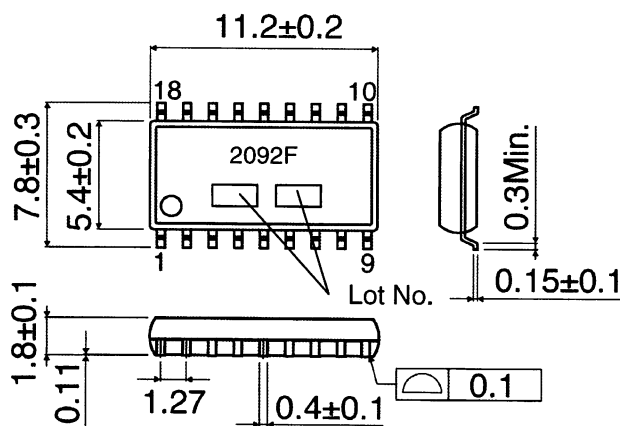
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any difference in translation version of this document, formal version takes priority.

● ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25°C, VCC=5.0V)

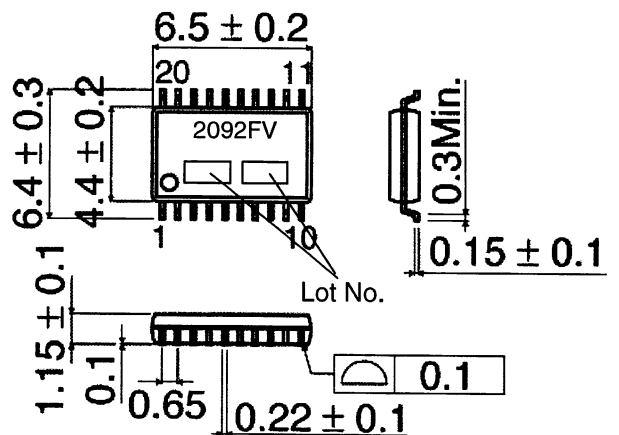
Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Power Supply Voltage range	V _{DD}	2.7	-	5.5	V	VDD pin
Output Voltage range	V _o	0	-	25.0	V	
Supply current1	I _{cc1}	-	-	5.0	μA	V _{in} =VSS or VDD, Output=OPEN, VDD=5V
Supply current2	I _{cc2}	-	-	3.0	μA	V _{in} =VSS or VDD, Output=OPEN, VDD=3V
Input "H" voltage1	V _{IH1}	3.5	-	-	V	VDD=5V
Input "H" voltage2	V _{IH2}	2.5	-	-	V	VDD=3V
Input "L" voltage1	V _{IL1}	-	-	1.5	V	VDD=5V
Input "L" voltage2	V _{IL2}	-	-	0.4	V	VDD=3V
Output "L" voltage1	V _{OL1}	-	-	2.0	V	VDD=5V, 20mA
Output "L" voltage2	V _{OL2}	-	-	1.0	V	VDD=3V, 5mA
Output Leakage current1	I _{IH}	-	-	10.0	μA	External resistance 10kΩ, V _{out} =25V
Output Leakage current2	I _{IL}	-	-	-5.0	μA	External resistance 10kΩ, V _{out} =0V
Data Minimum set up time1	t _{su1}	200	-	-	nS	VDD=5V
Data Minimum set up time2	t _{su2}	400	-	-	nS	VDD=3V
Data hold time1	t _{h1}	200	-	-	nS	VDD=5V
Data hold time2	t _{h2}	400	-	-	nS	VDD=3V
Minimum shift pulse width1	t _{w1}	500	-	-	nS	VDD=5V
Minimum shift pulse width2	t _{w2}	1000	-	-	nS	VDD=3V

This product is not assessed whether to be strategic materials in foreign exchange and trade law or not, so please confirm at trading. This product is not deigned against radioactive ray.

● PHYSICAL DIMENSIONS



SOP18 (UNIT : mm)

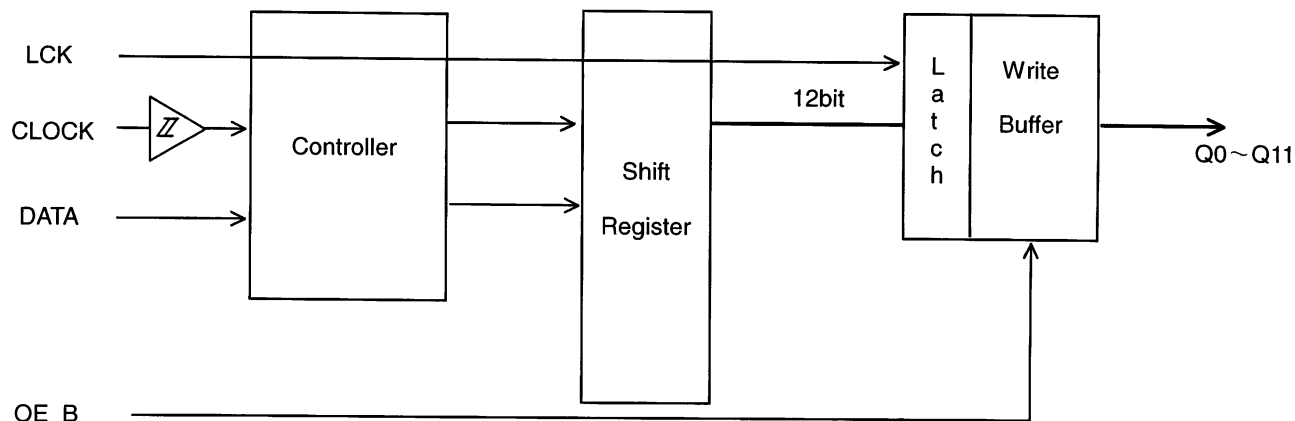


SSOP-B20 (UNIT : mm)

● Pin Description

Pin. No (F/FV)	Terminal	Symbol	Function
3/3	CLOCK	C	Shift pulse for shift register
2/2	DATA	S _I	Data input for shift register, data is set at rising edge of shift pulse
4/4	LCK	L _C	Latch signal input, output is renewable out "1" and reserved at "0".
17/19	OE_B	O _{EB}	Enable signal input, data can be shifted to output.
5/5	Q0	O ₀	1st bit output, it becomes "1" when data in register is "1"
6/6	Q1	O ₁	2nd bit output, it becomes "1" when data in register is "1"
7/7	Q2	O ₂	3rd bit output, it becomes "1" when data in register is "1"
8/8	Q3	O ₃	4th bit output, it becomes "1" when data in register is "1"
9/9	Q4	O ₄	5th bit output, it becomes "1" when data in register is "1"
10/10	Q5	O ₅	6th bit output, it becomes "1" when data in register is "1"
11/11	Q6	O ₆	7th bit output, it becomes "1" when data in register is "1"
12/14	Q7	O ₇	8th bit output, it becomes "1" when data in register is "1"
13/15	Q8	O ₈	9th bit output, it becomes "1" when data in register is "1"
14/16	Q9	O ₉	10th bit output, it becomes "1" when data in register is "1"
15/17	Q10	O ₁₀	11th bit output, it becomes "1" when data in register is "1"
16/18	Q11	O ₁₁	12th bit output, it becomes "1" when data in register is "1"
1/1	VSS	GND	GND
18/20	VDD	VDD	Power supply
-/12	NC	NC	NC pin
-/13	NC	NC	NC pin

● BLOCK DIAGRAM



● NOTES FOR USE

- (1) Absolute maximum ratings
Exceeding the absolute maximum ratings, including applied voltage and operating temperature range, may damage or destroy the IC. Since the cause of the damage cannot be conclusively identified (as, for example, a short or open mode), be sure to take appropriate physical safety measures, such as incorporating fuses, whenever a special mode anticipated to exceed absolute maximum ratings is employed.
- (2) Ground Potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode.
- (3) Thermal design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.
- (4) Electromagnetic fields
Use in strong electromagnetic fields may cause malfunctions. Be careful operating in electromagnetic fields.
- (5) Ground wiring pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

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Japan /
(Internal Sales)

Tokyo	2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082	TEL : +81(3)5203-0321	FAX : +81(3)5203-0300
Yokohama	2-4-8, Shin Yokohama, Kohoku-ku, Yokohama, Kanagawa 222-8575	TEL : +81(45)476-2131	FAX : +81(45)476-2128
Nagoya	Dainagayo Building 9F 3-28-12, Meieki, Nakamura-ku, Nagoya, Aichi 450-0002	TEL : +81(52)581-8521	FAX : +81(52)561-2173
Kyoto	579-32 Higashi Shiokouji-cho, Karasuma Nishi-iru, Shiokoujidori, Shimogyo-ku, Kyoto 600-8216	TEL : +81(75)311-2121	FAX : +81(75)314-6559

(Contact address for overseas customers in Japan)

Yokohama	TEL : +81(45)476-9270	FAX : +81(045)476-9271
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