SONY

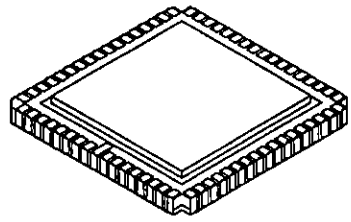
CXA1276K

8-bit 500 MSPS Flash A/D Converter

Description

The CXA1276K is an 8-bit ultrahigh-speed flash A/D converter IC capable of digitizing analog signals at a maximum rate of 500 MSPS. The digital I/O level of this A/D converter is compatible with the ECL 100K/10KH/10K.

68 pin LCC (Ceramic)



Features

- Differential linearity error: ±0.5 LSB or less
- Integral linearity error: ±0.7 LSB or less
- Built-in integral linearity compensation circuit
- Ultrahigh-speed operation with maximum conversion rate of 500 MSPS
- Low input capacitance: 20pF
- Wide analog input bandwidth: 300MHz
- Single power supply: –5.2V
- Low power consumption: 2.8W (Typ.)
- Low error rate
- Good temperature characteristics
- Capable of driving 50Ω loads

Structure

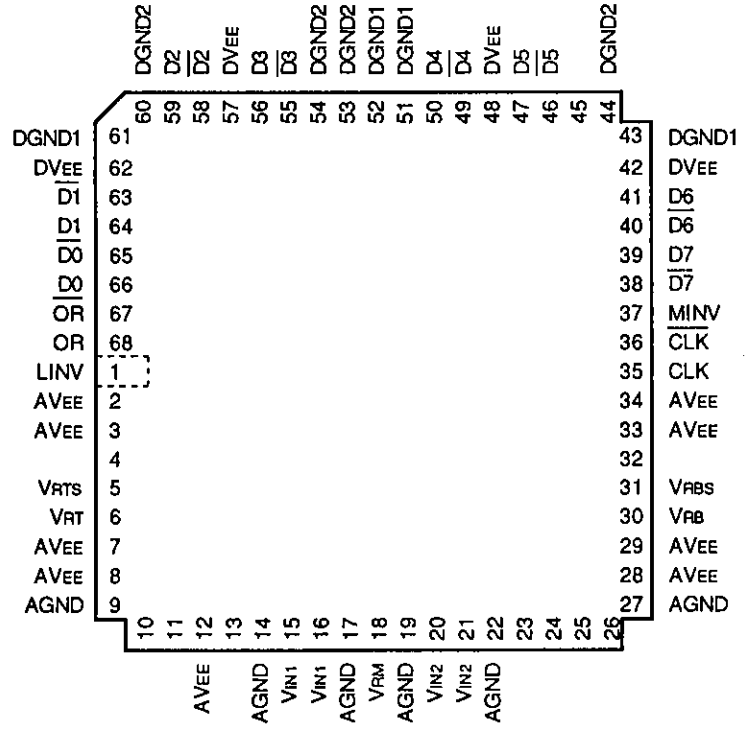
Bipolar silicon monolithic IC

Applications

- Digital oscilloscopes
- Other apparatus requiring ultrahigh-speed A/D conversion

Pin Configuration

Pins without name are NC pins (not connected internally).



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E94710—ST

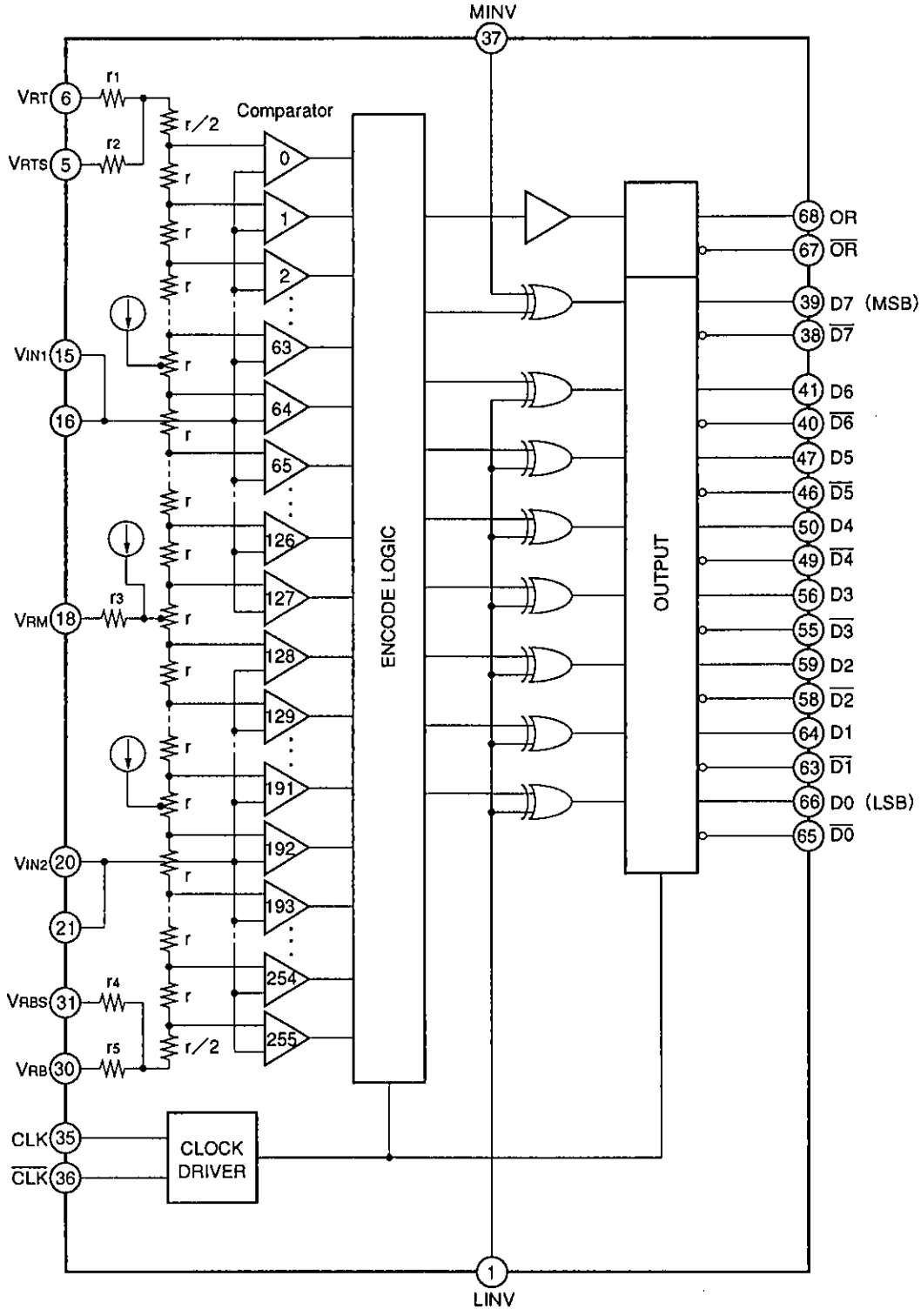
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	AV_{EE}, DV_{EE}	−7 to +0.5	V
• Analog input voltage	V_{IN}	−2.7 to +0.5	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	AV_{EE} to +0.5	V
	$\lvert V_{RT}-V_{RB} \rvert$	2.5	V
• Digital input voltage	MINV, LINV	−4 to +0.5	V
	CLK, $\overline{CLK}$	DV_{EE} to +0.5	V
	$\lvert CLK-\overline{CLK} \rvert$	2.7	V
• V_{RM} pin input current	I_{VRM}	−3 to +3	mA
• Digital output current	ID_0 to ID_7, IOR, $\overline{ID_0}$ to $\overline{ID_7}$, $\overline{IOR}$	−30 to 0	mA
• Storage temperature	Tstg	−65 to +150	°C

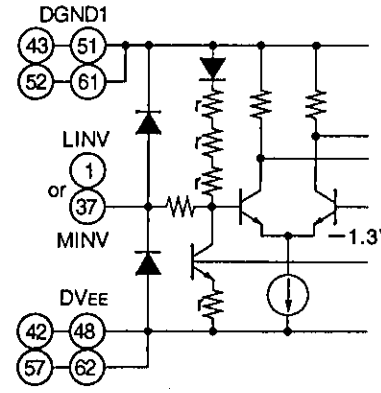
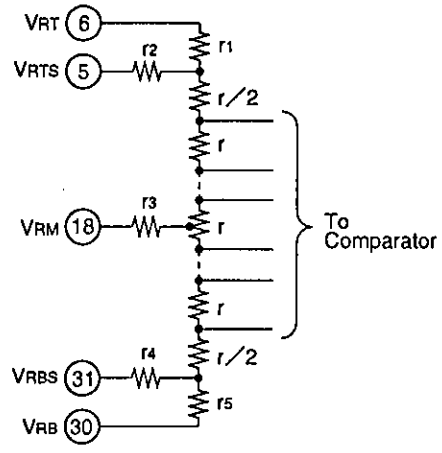
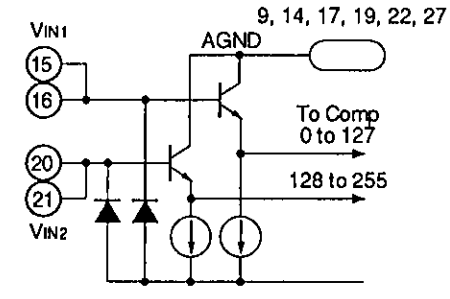
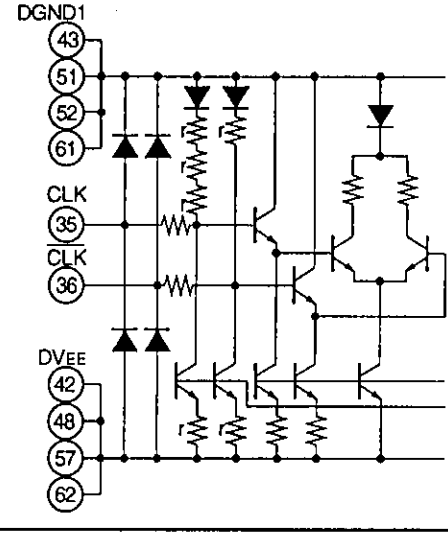
Operating Conditions

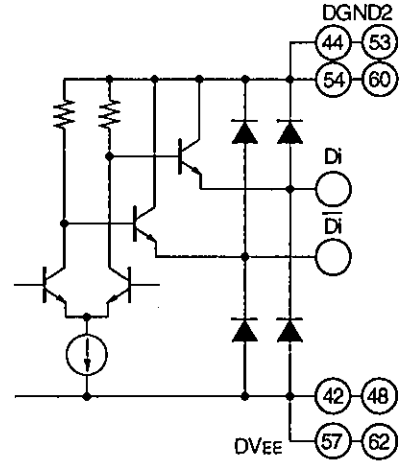
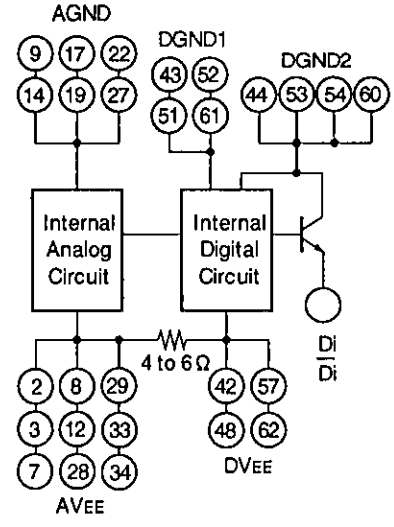
		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.5	−5.2	−4.95	V
	$AV_{EE}-DV_{EE}$	−0.05	0	0.05	V
	AGND−DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2.0	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Operating temperature	Tc	−20		100	°C

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	LINV	I	ECL		Polarity selection for LSBs. (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
37	MINV	I	ECL		Polarity selection for MSB (Refer to the table of Input voltage vs. Digital output) L level is maintained with left open.
6	V_{RT}	I	0V		Analog reference voltage (Top) (0V Typ.)
5	V_{RTS}	O	0V		Reference voltage sense (Top)
18	V_{RM}	I	$V_{RB}/2$		Reference voltage mid-point If can be used for linearity compensation.
31	V_{RBS}	O	−2V		Reference voltage sense (Bottom)
30	V_{RB}	I	−2V		Analog reference voltage (Bottom)
15 16	V_{IN1}	I	V_{RTS} to V_{RBS}		Analog input All of the pins must be wired externally.
20 21	V_{IN2}				
35	CLK	I	ECL		CLK input
36	$\overline{CLK}$	I	ECL		Complementary CLK input V_{BB} (−1.3V) is maintained with left open.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
39 38	D_7 $\overline{D_7}$	O	ECL		MSB and complementary MSB output
41 40	D_6 $\overline{D_6}$	O			D_1 to D_6: Output $\overline{D_1}$ to $\overline{D_6}$: Complementary output
47 46	D_5 $\overline{D_5}$	O			
50 49	D_4 $\overline{D_4}$	O			
56 55	D_3 $\overline{D_3}$	O			
59 58	D_2 $\overline{D_2}$	O			
64 63	D_1 $\overline{D_1}$	O			
66 65	D_0 $\overline{D_0}$	O			LSB and complementary LSB output
68 67	OR $\overline{OR}$	O			Overrange and complementary Overrange output
2, 3, 7, 8, 12, 28, 29, 33, 34	AVEE*		–5.2V		Analog supply Internally connected with DVEE (resistance: 4 to 6Ω).
9, 14, 17, 19, 22, 27	AGND*		0V		Analog ground
42, 48, 57, 62	DVEE*		–5.2V		Digital supply Internally connected with AVEE (resistance: 4 to 6Ω).
43, 51, 52, 62	DGND1*		0V		Digital ground
44, 53, 54, 60	DGND2*		0V		Digital ground for output drive
4, 10, 11, 13, 23, 24, 25, 26, 32	NC		—		No connect pins It is recommended to wire these pins to AGND.
45	NC		—		No connect pins It is recommended to wire these pins to DGND.

* All of these pins must be wired to the respective external circuit.

Electrical Characteristics (AV_{EE} = DV_{EE} = –5.2V, V_{RT}, V_{RTS} = 0V, V_{RB}, V_{RBS} = –2V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution				8		bits
DC characteristics						
Integral linearity error	E_{IL}				±0.7	LSB
Differential linearity error	E_{DL}				±0.5	LSB
Analog input						
Analog input capacitance	C_{IN}	V_{IN} = –1V		20		pF
Analog input resistance	R_{IN}		30	70		kΩ
Input bias current	I_{IN}	V_{IN} = –1V			850	μA
Reference inputs						
Reference resistance	R_{REF}		70	110	160	Ω
Residual resistance*1 r_1	r_1		0.1	0.5	2.0	Ω
r_2	r_2		0.5	5.2	10	Ω
r_3	r_3		0.5	1.6	5.0	Ω
r_4	r_4		0.5	8.7	20	Ω
r_5	r_5		0.1	0.5	2.0	Ω
Digital inputs						
Logic H level	V_{IH}		–1.10			V
Logic L level	V_{IL}				–1.55	V
Logic H current	I_{IH}	Input connected to –0.8V	0		70	μA
Logic L current	I_{IL}	Input connected to –1.6V	–50		60	μA
Input capacitance				6		pF
Switching characteristics						
Maximum conversion rate	Fc		500			MSPS
Aperture jitter	Taj	150MHz		11		ps
Sampling delay	Tds	150MHz	0.2	0.8	1.5	ns
Output delay	Tdo		1.5	1.9	2.3	ns
Clock duty cycle			45	50	55	%
Digital output						
Logic H level	V_{OH}	R_L = 50Ω to –2V	–1.03			V
Logic L level	V_{OL}	R_L = 50Ω to –2V			–1.58	V
Output rising time	Tr	R_L = 50Ω to –2V, 20% to 80%	0.5	0.7	1.0	ns
Output falling time	Tf	R_L = 50Ω to –2V, 80% to 20%	0.5	0.7	1.0	ns
Dynamic characteristics						
Bandwidth		V_{IN}=2Vp-p	300			MHz
SNR		Input = 1kHz, FS, Clock = 500MHz	44	46		dB
		Input = 125MHz, FS, Clock = 500MHz	30	34		dB
Error rate		Input = 100MHz, FS, Error>16LSB, Clock = 400MHz		10^{-11}	10^{-9}	TPS*2
		Input = 125MHz, FS, Error>16LSB, Clock = 500MHz		10^{-8}	10^{-6}	TPS*2
Differential gain error	DG	NTSC 40IRE mod. ramp, Fc = 500MSPS		1.0		%
Differential phase error	DP			0.5		deg
Power supply						
Supply current	I_{EE}		–680	–520		mA
Power consumption*3	Pd			2.8	3.6	W

*1 See Block Diagram

*2 TPS: Times Per Sample

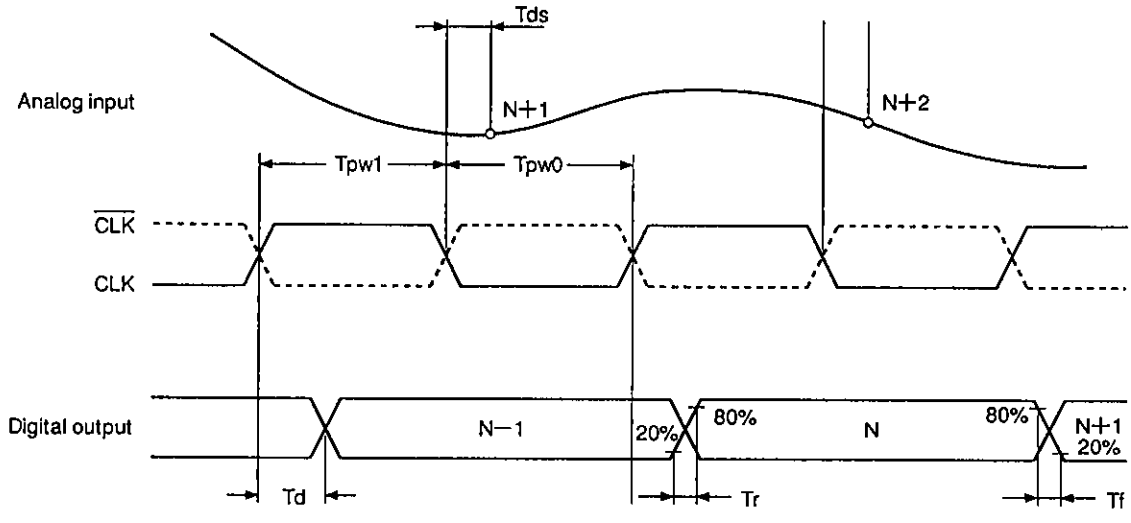
*3 $Pd = I_{EE} \cdot V_{EE} + \frac{(V_{RT}-V_{RB})^2}{R_{REF}}$

Input Voltage vs. Digital Output

V_{IN}*	Step	MINV 1 LINV 1		0 1		1 0		0 0	
		OR	D7 D0	OR	D7 D0	OR	D7 D0	OR	D7 D0
0V		1	000……00	1	100……00	1	011……11	1	111……11
	0	0	000……00	0	100……00	0	011……11	0	111……11
	1	0	000……01	0	100……01	0	011……10	0	111……10
			⋮		⋮		⋮		⋮
–1V	127	0	011……11	0	111……11	0	000……00	0	100……00
	128	0	100……00	0	000……00	0	111……11	0	011……11
		⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	254	0	111……10	0	011……10	0	100……01	0	000……01
	255	0	111……11	0	011……11	0	100……00	0	000……00
–2V		0	111……11	0	011……11	0	100……00	0	000……00

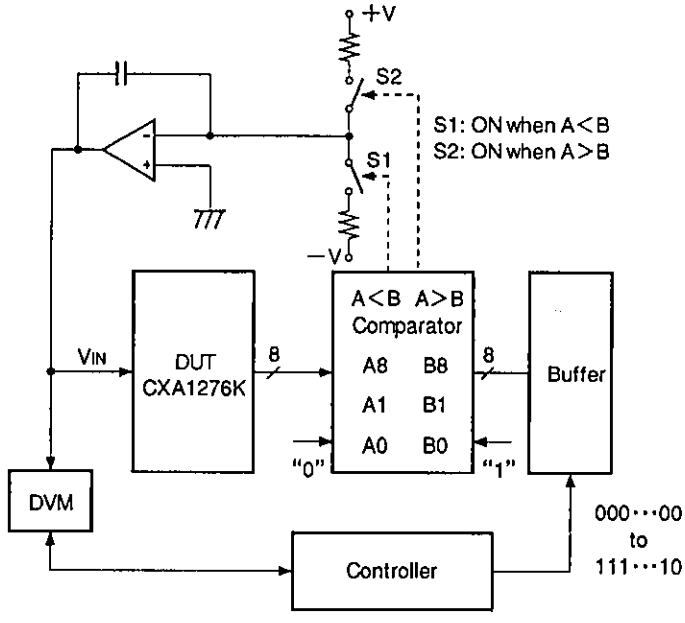
* V_{RT} = 0V, V_{RTS} Open, V_{RM} Open, V_{RBS} Open, V_{RB} = –2V

Timing Diagram

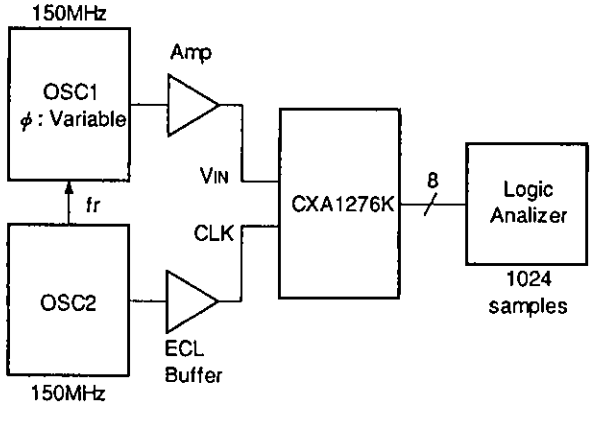


Electrical Characteristics Test Circuit

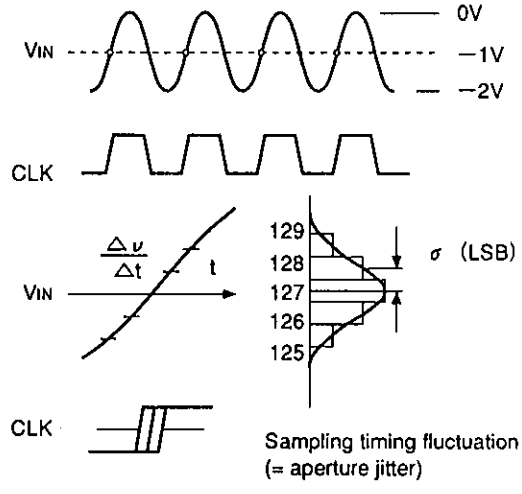
Integral Linearity Error Test Circuit
Differential Linearity Error Test Circuit



Sampling Delay Test circuit
Aperture Jitters Test circuit



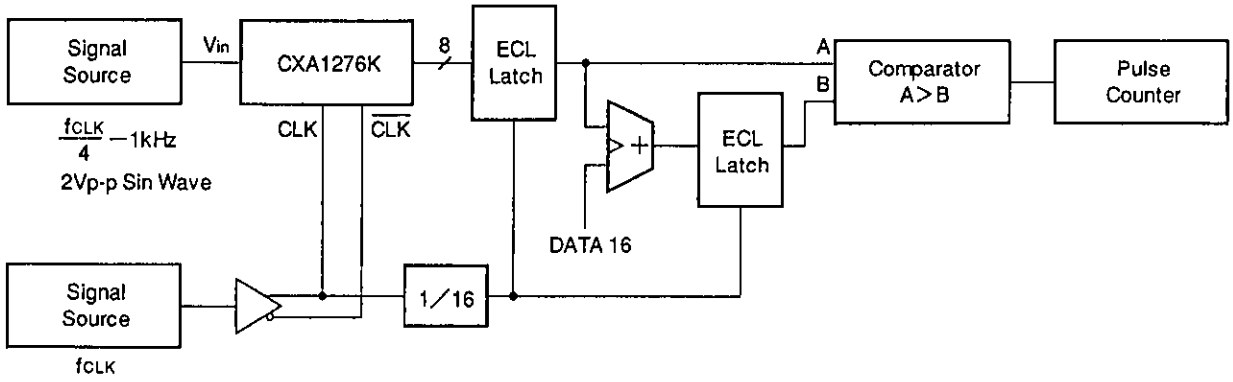
Aperture Jitters Test Method



Where (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

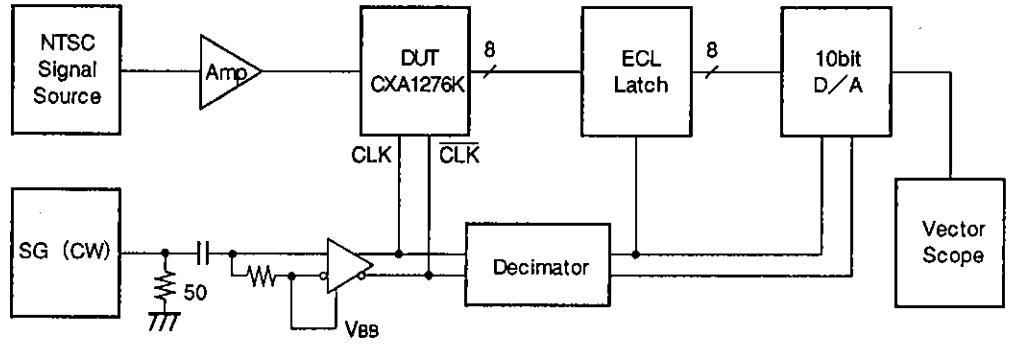
$$Taj = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right)$$

Error Rate Test Circuit



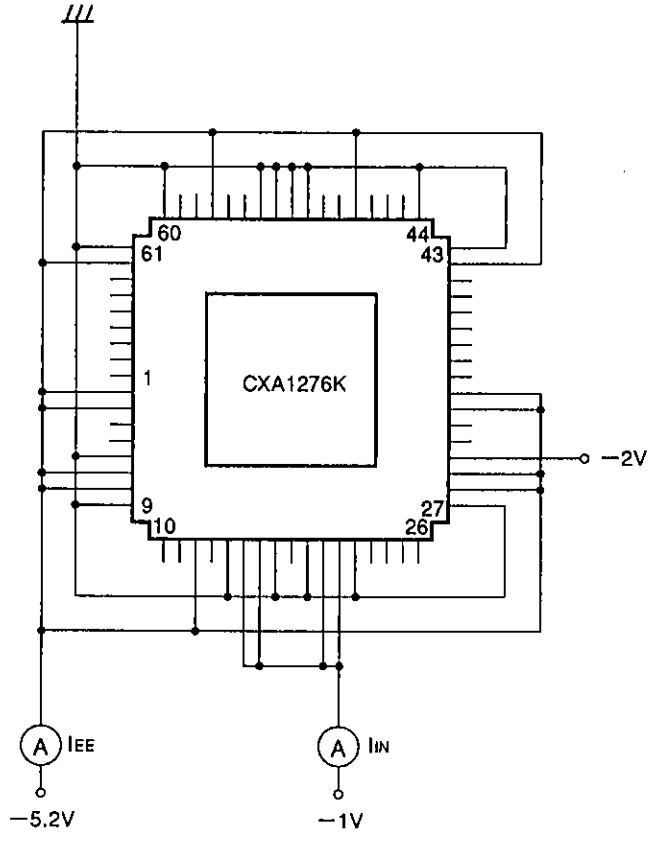
Differential Gain Error Test Circuit

Differential Phase Error Test Circuit



Power Supply Current Test Circuit

Analog Input Bias Current Test Circuit



Notes on Operation

- The CXA1276K is an ultra-high speed AD converter with ECL level I/O. As the high-speed digital signal is next to analog signal, the following precautions must be taken in order to obtain optimum performance.

- Properly match the impedance (using micro strip line) to prevent distortion of waveform by the digital signal circuit (clock/data output). The CXA1276K is designed to use line with characteristic impedance of 50Ω.

- The CXA1276K operates on single –5.2V power supply. However, AGND and DGND, and AV_{EE} and DV_{EE} are separated to prevent the noise from the digital circuit leaking to the analog circuit. The board also should be a multi-layer board separated analog region and digital region. Avoid overlapping signal lines and power supply GND in the two regions. Connect AGND and DGND at one location (using a ferrite-bead) to avoid DC offset. The same processing is also necessary for AV_{EE} and DV_{EE}.

- Connect all power supply pins and GND pins, not leaving them open.

- Bypass capacitors (approx. 0.1μF) with high frequency characteristics should be used to bypass between AV_{EE}—AGND and DV_{EE}—DGND.

- Make complimentary use of clock input and data output as much as possible in order to obtain stable high performance. The SPECL standard logic series D flip-flop (CXB1109) is suitable for receiving complimentary signals.

- When mounting ADC in a socket, use the one with shortest leads. The QFP type socket IC61-0684-048 manufactured by YAMAICHI ELECTRONICS CO., LTD. is recommended.

- The analog input pin V_{IN}'s have relatively large input capacitance (approx. 20pF) for high frequency circuit. The input bandwidth of the CXA1276K is determined mainly by how much the driver can drive this capacitance rather than the characteristics of the IC.

- All four V_{IN} pins should be connected directly at shortest distance as possible. The difference in delay between pins causes the distortion at high frequency input signals.

- The voltages at V_{RT} and V_{RB} pins and the internal reference voltages are slightly different due to residual resistance. Therefore, V_{RTS} and V_{RBS} are provided to increase their precision. The reference voltage for over range is at 1/2 LSB below V_{RTS} and the lowest input voltage at which the output code changes is at 1/2 LSB above V_{RBS}.

- V_{RM} is originally provided to reduce integral linearity error, but there is no need for this. It should simply be kept open.

- OR and $\overline{OR}$ pins are outputs indicating that the input is over range. These pins do not invert at MINV nor LINV.

- When there is noise in the MINV or LINV pins, it is difficult to find the cause from the resulting error. Therefore, provide sufficient margins for the High/Low voltage levels and connect as close to DGND as possible through bypass capacitor (approx. 0.1μF) with high frequency characteristics. Stable Low level can be obtained. The recommended high level input voltage is between –0.5V and –1.0V and the low level input voltage is between –1.6V and –2.5V.

- Although the electrical characteristics of the CXA1276K depends on the clock duty cycle, this is not significant. Therefore, the electrical characteristics are defined at 50% duty cycle taking the ease of generating the clock signal into consideration. An example of dependence on the clock duty cycle is shown in the characteristics graph "Error rate vs. Clock duty cycle characteristics".

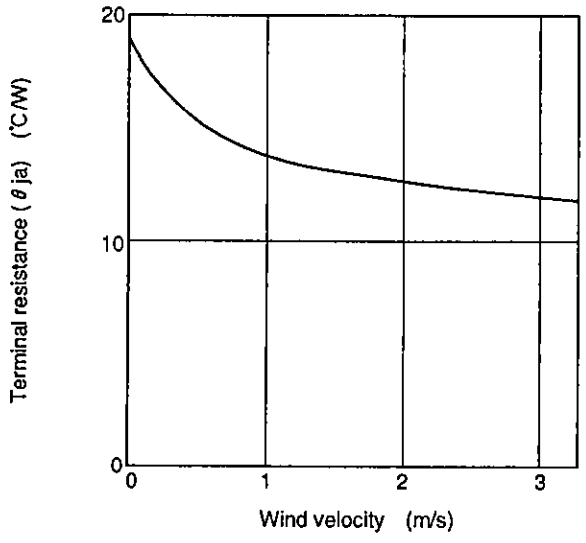
- The horizontal axis of the characteristics graph "Error rate vs. Threshold level characteristics" indicates the change in error rate when the error detection threshold level is changed. The increase in error below 5 LSBs is due to the fluctuation detected at the AD converter output. The mechanism of this error differs from those detected at higher threshold levels. The fact that there is only small change in the error rate when the threshold level is increased indicates that the most of the CXA1276K errors are large. The electrical characteristics of error rate are defined at 16 LSBs where the error rate is stable.

- Error rate changes with input frequency and input amplitude. The error rate, at the electrical characteristics specific condition which is full scale sine wave input at 1/4 the clock frequency, can be considered close to the upper limit during actual use (when the input signal is below Nyquist frequency).

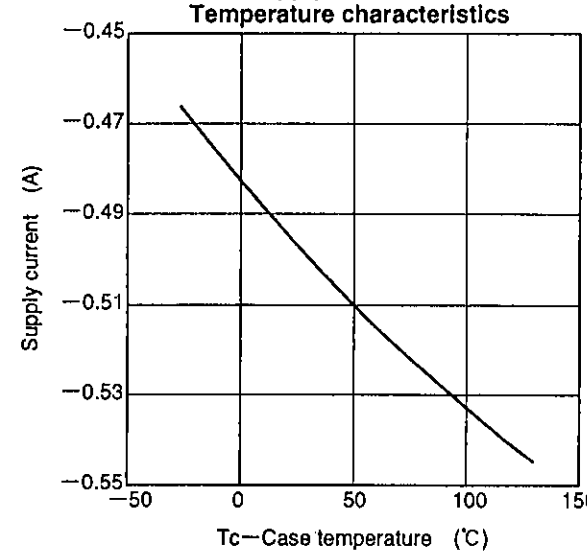
- When the chip temperature rises, current dissipation increases and the error rate also increases. Sufficient cooling is necessary in order to prolong product life.

Example of Representative Characteristics

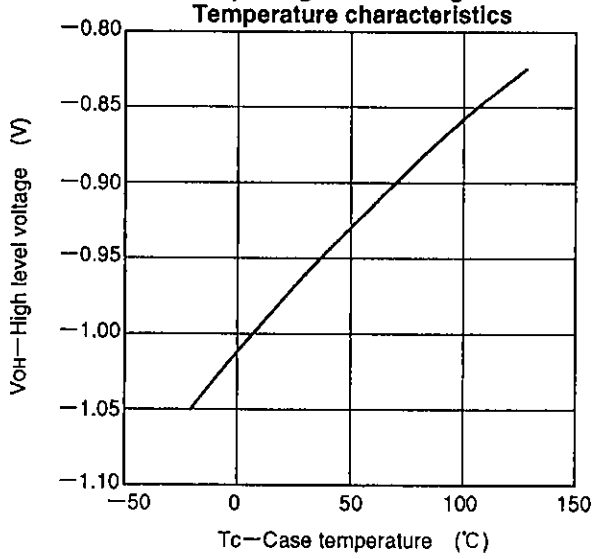
Terminal resistance at on-board condition



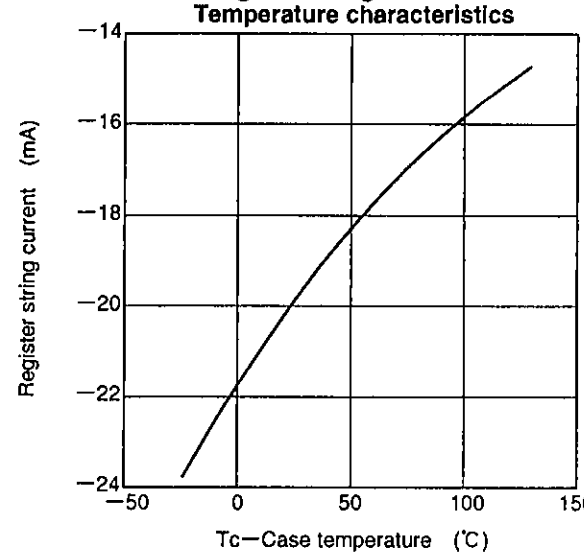
Supply current vs. Temperature characteristics



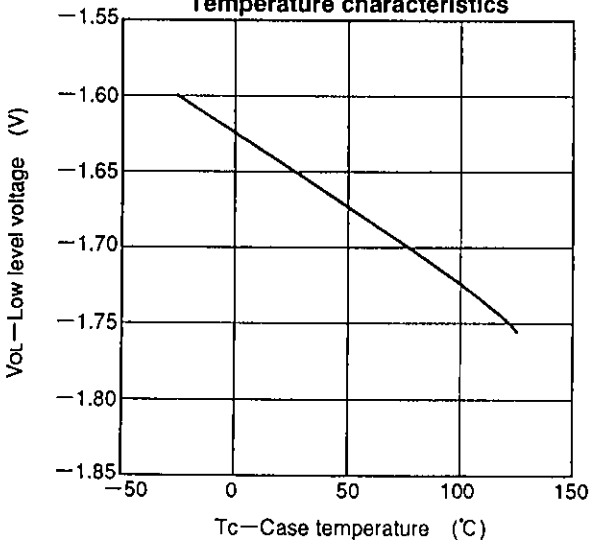
DO pin High level voltage vs. Temperature characteristics



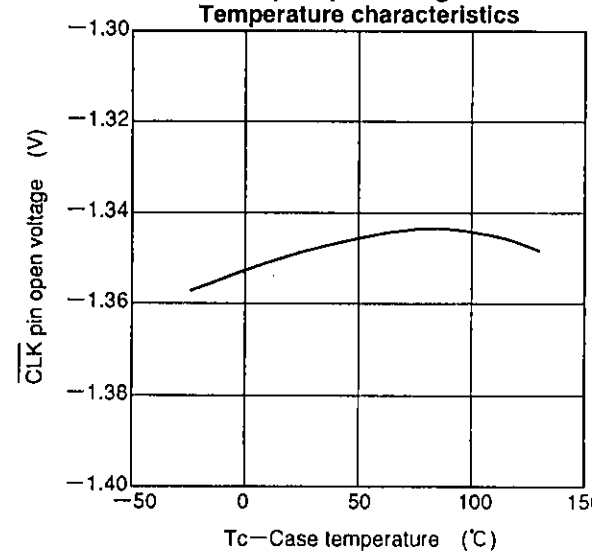
Register string current vs. Temperature characteristics



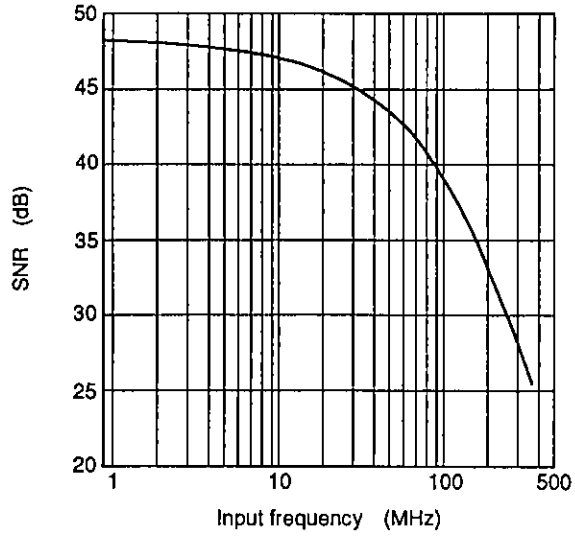
DO pin Low level voltage vs. Temperature characteristics



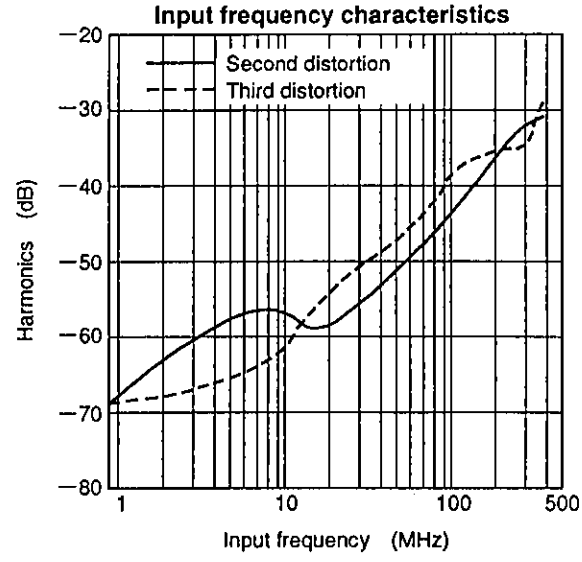
$\overline{CLK}$ pin open voltage vs. Temperature characteristics



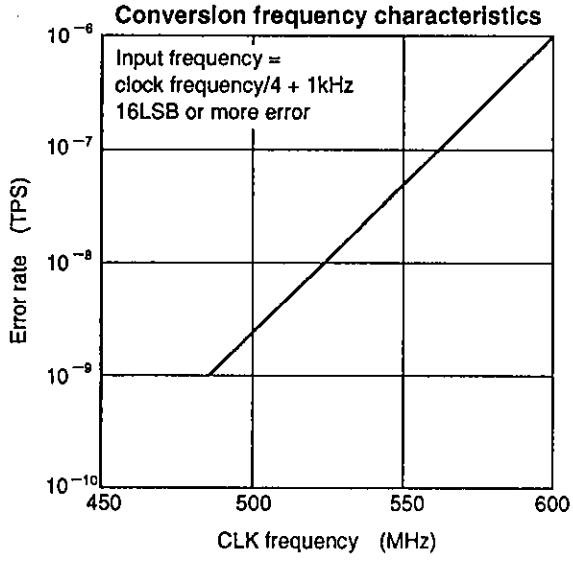
SNR vs. Input frequency characteristics



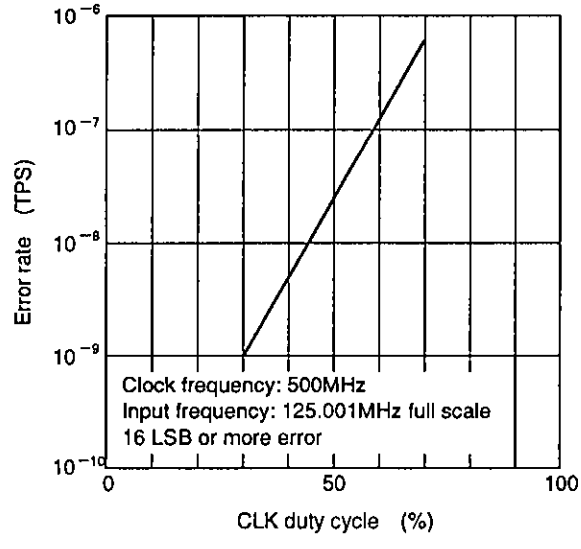
Harmonic distortion vs. Input frequency characteristics



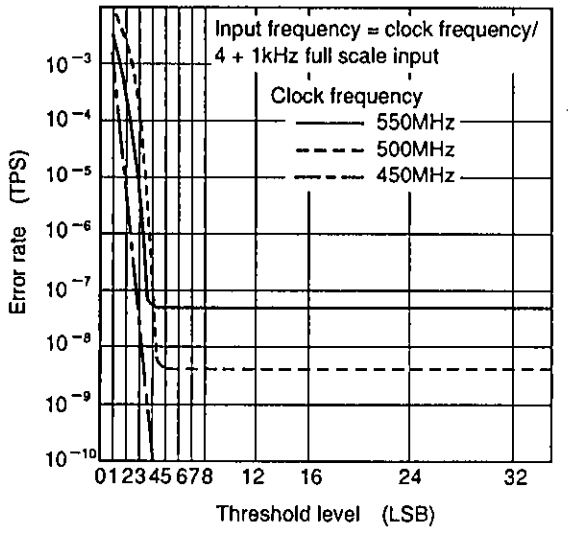
Error rate vs. Conversion frequency characteristics



Error rate vs. Clock duty cycle characteristics



Error rate vs. Threshold level characteristics



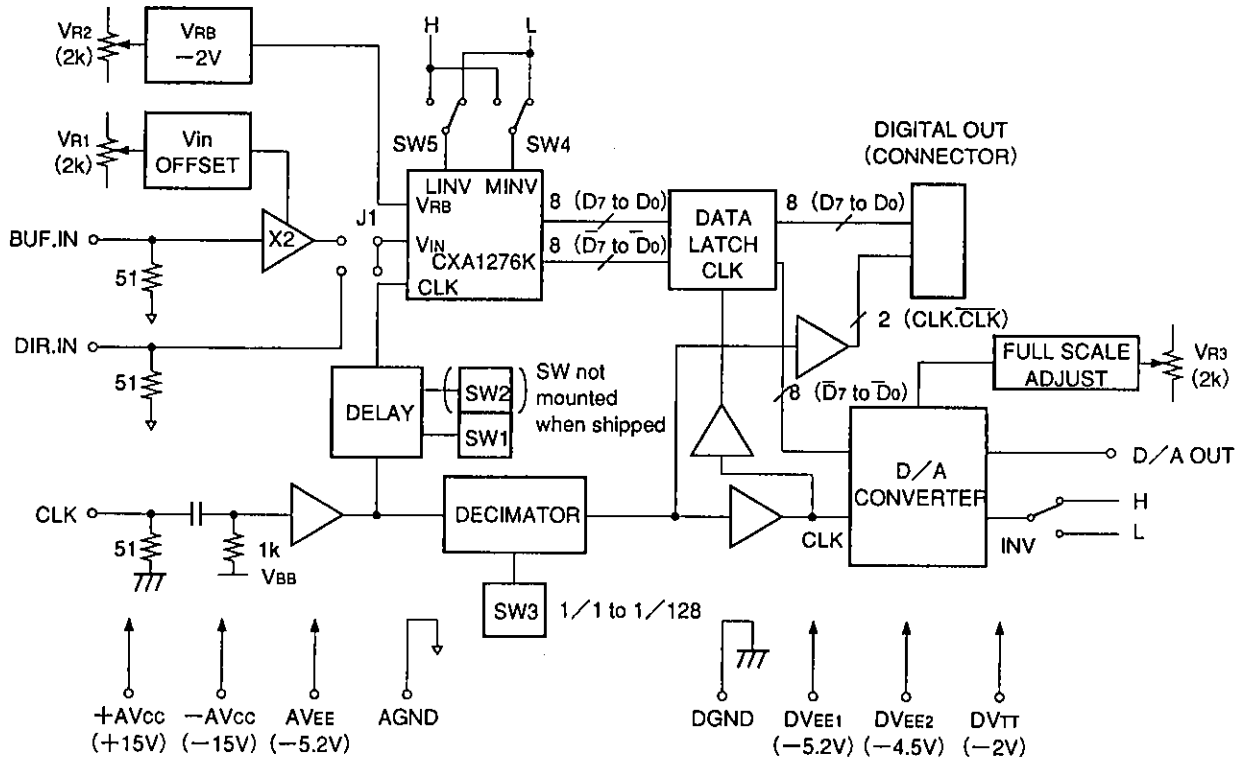
8-bit, 500 MSPS ADC Evaluation Board

The CXA1276K PCB is a tool for customers to evaluate the performance of the CXA1276K (8-bit, 500MHz, high-speed A/D converter). In addition to indispensable features such as the reference voltage generator, this tool equips the input voltage offset generator, the clock decimator, the output date latches, the 10-bit high-speed DAC, and the 20-pin cable connector for digital outputs. This evaluation board is designed to facilitate evaluation.

Features

- Resolution: 8 bits
- Maximum conversion rate: 500 MSPS
- Supply voltage: –5.2V, –4.5V, –2.0V, +15V, –15V
- Clock level converter: Sine wave to ECL level signal
- Reference voltage adjustment circuit for A/D converter
- Built-in clock frequency decimation circuit: 1/1 to 1/128

Fig. 1. Block Diagram



Supply Current

Item	Min.	Typ.	Max.	Unit
AV_{EE}+DV_{EE1} (–5.2V)		0.6	0.9	A
DV_{EE2} (–4.5V)		1.0	1.5	A
DV_{TT} (–2.0V)		0.75	1.2	A
–AVcc (–15.0V)		60	100	mA
+AVcc (+15.0V)		50	100	mA

Analog Input

Item	Min.	Typ.	Max.	Unit
Input voltage (BUF. IN)	–0.5		+0.5	V
(DIR. IN)	–2.0		0	V
Input impedance		50		Ω

* For the analog input method, see Section 3 of "Adjustment Methods and Notes on Operation."

Clock input (CLK)

Item	Min.	Typ.	Max.	Unit
Input voltage (Peak to Peak)		1.0		Vp-p
Input impedance		50		Ω

Digital output (Digital OUT)

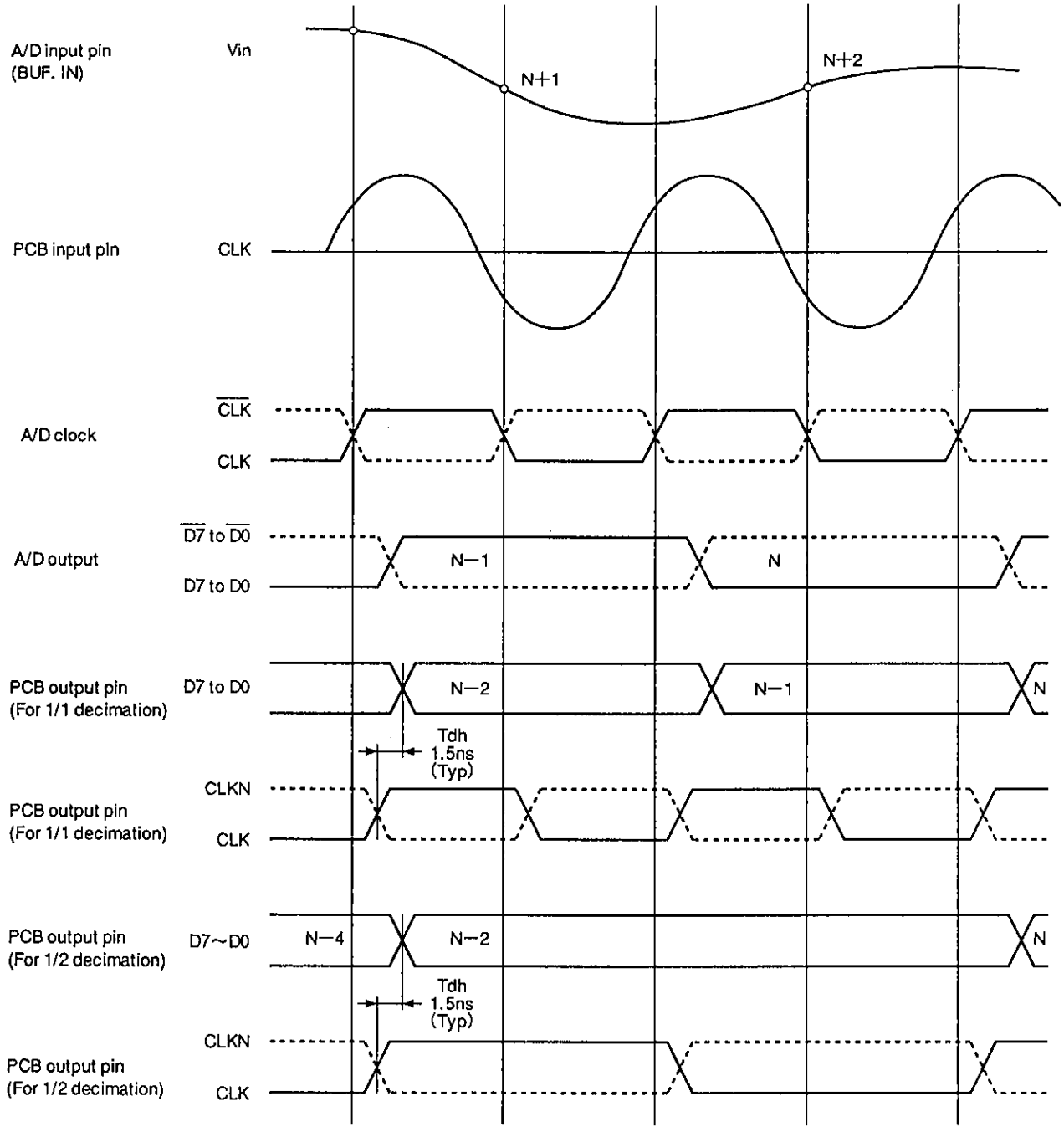
ECL level

Output Code Table

1: ECL High level, 0: ECL Low level

	MINV (SW4) / LINV (SW5)	0 / 0	0 / 1	1 / 0	1 / 1
V_{IN}	0V	111 …… 11	100 …… 00	011 …… 11	000 …… 00
		111 …… 10	100 …… 01	011 …… 10	000 …… 01
		⋮	⋮	⋮	⋮
		100 …… 00	111 …… 11	000 …… 00	011 …… 11
		011 …… 11	000 …… 00	111 …… 11	100 …… 00
		⋮	⋮	⋮	⋮
		000 …… 01	011 …… 10	100 …… 01	111 …… 10
	–2V	000 …… 00	011 …… 11	100 …… 00	111 …… 11

Fig. 2. Timing Diagram



Adjustment Methods and Notes on Operation

1) V_{IN} Offset (VR1)

The volume to adjust the BUF. IN signal range (0V center assumed) with the A/D converter input range.

2) A/D Full Scale (VR2)

The volume to adjust A/D converter V_{RB} voltage (–2V typ.)

3) J1 jumper wire is used to select the analog input pins BUF. IN and DIR. IN.

Analog input method	A	B	Offset
When using BUF. IN input	Shorted	Open	Adjusted by VR1
When using DC-coupled DIR. IN input	Open	Shorted	Input offset signal
When using AC-coupled DIR. IN input	1kΩ	0.1μF	Adjusted by VR1

4) D/A Full Scale (VR3)
The volume to adjust the bottom of D/A output full scale voltage (–1V typ.)

5) SW1 and SW2
Selection switches to adjust the clock delay. These switches enable clock delay to be stepped to any one of 23 settings through binary input. Binary input from 00001 to 00110 increments the clock delay at approximately 125 ps intervals, and binary input from 00111 to 10111 increments the clock delay at approximately 190 ps intervals. The switches are designed such that, when SW1 is normally set to 1010 or A in hexadecimal, and SW2 is either set to L or not mounted, good timing margin can be kept at any clock frequency.

6) SW3 (Decimation)
The switch to select clock frequency decimation. Selection settings are as follows.

No.	Decimation ratio
0	1/1
1	1/2
2	1/4
3	1/8
4	1/16
5	1/32
6	1/64
7	1/128

7) SW4
The switch for MINV High/Low

8) SW5
The switch for LINV High/Low

9) SW6 (D/A INV)
The switch for D/A converter output inversion

10) Waveform probe pins P4 to P33 are devised to facilitate GND connection in order to reduce the distortion. As shown in the diagram below, the distance between the probe point and the GND is 300 mils, and there is ϕ 1.2mm throughhole at each. The signal and GND locations are suit for a Tektronix GND tip (part number 013-1185-00).

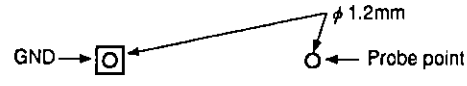


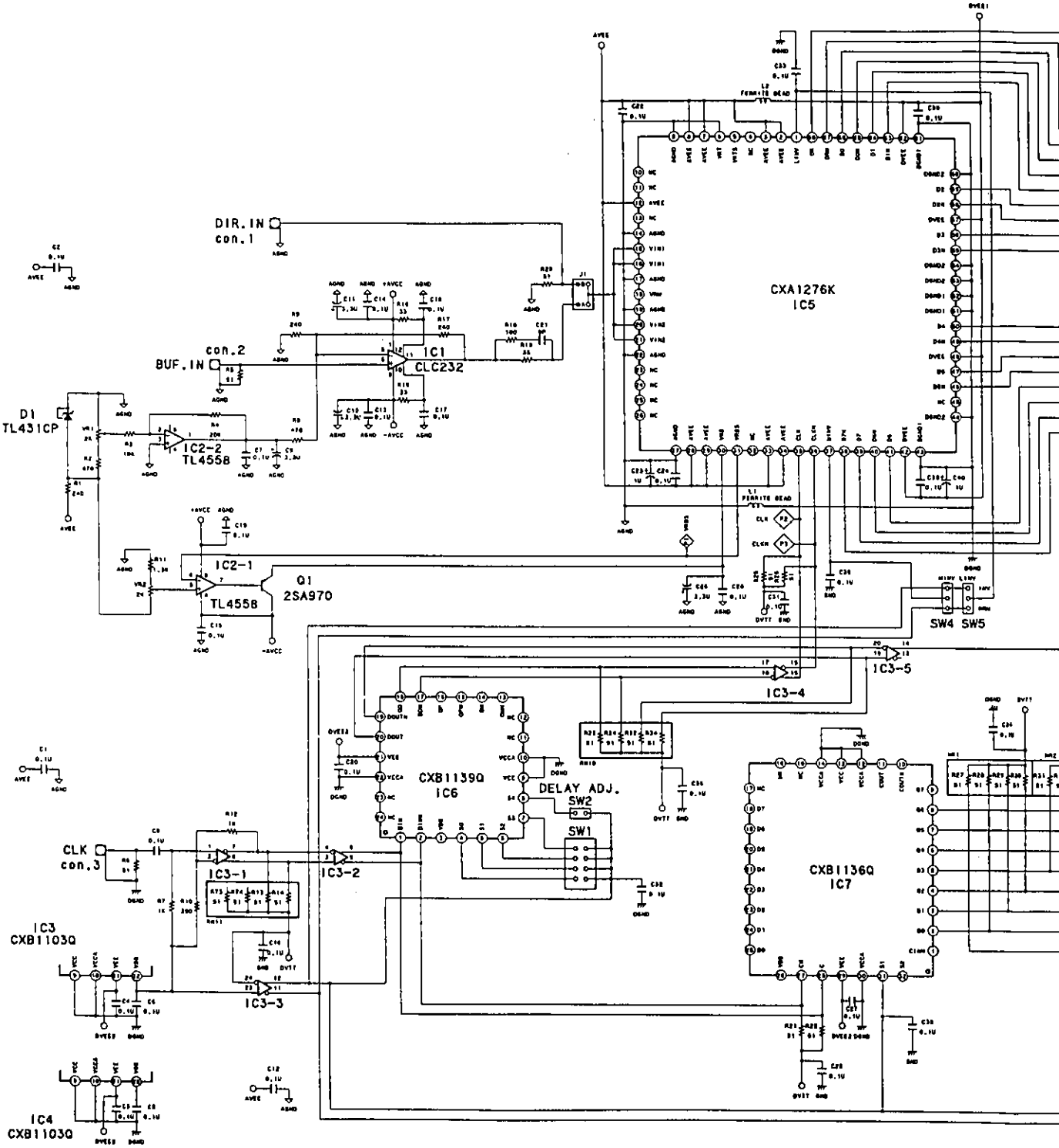
Fig. 3.

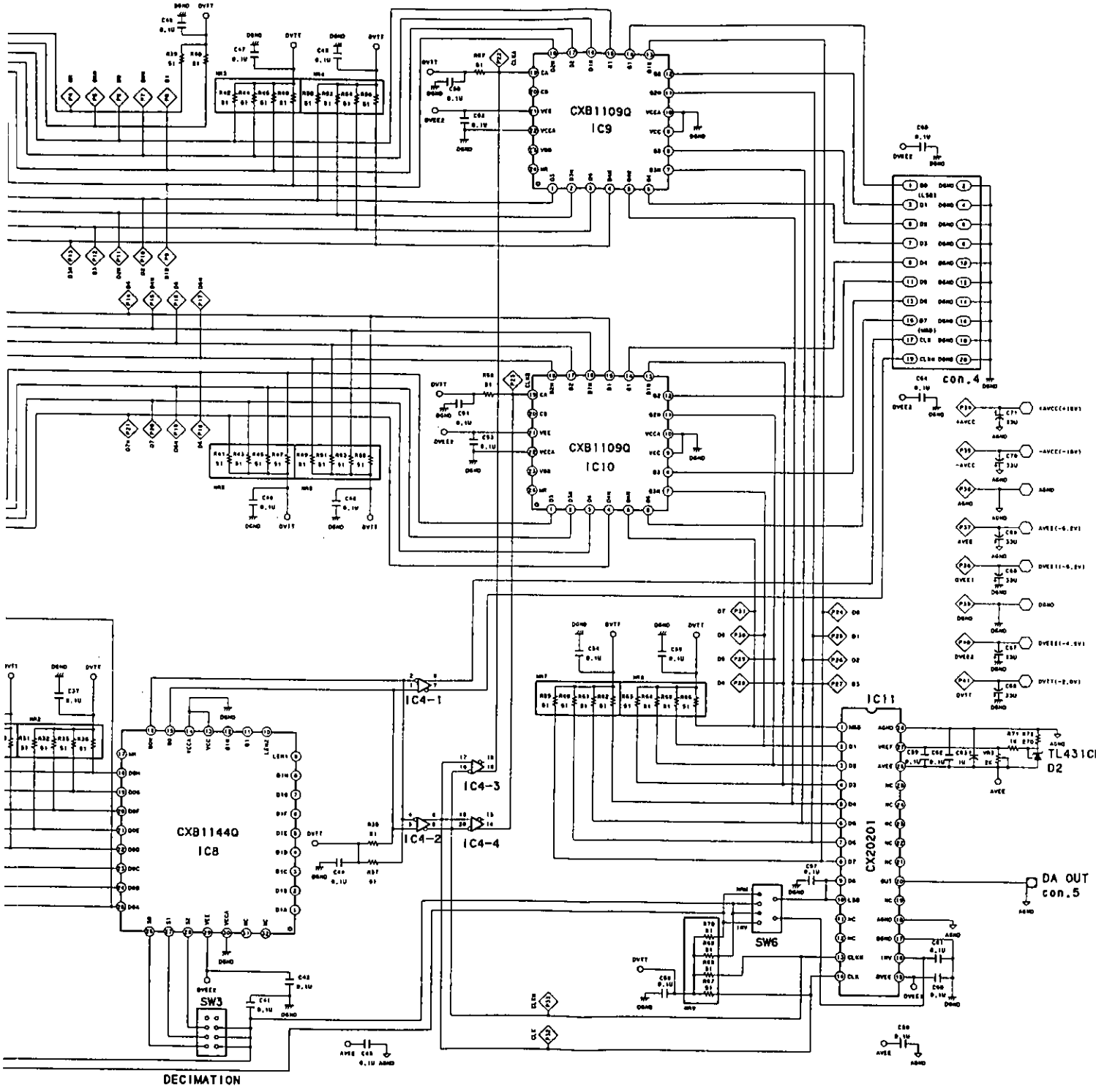
11) D/A converter (IC11) input data (waveform probe pins P24 to P31) are the complementary signals of the decimated A/D converter outputs. Those are inverted again in the D/A converter so that the direction (rise/fall) of reproduced waveform can agree with the A/D input signal's.

12) When observing the reproduced waveform (DA OUT output), set the decimator such that the clock frequency of the D/A converter (IC11: CX20201A-1) is less than 100MHz.

13) The part number of the digital output connector is KEL 8830E-020-170S. A corresponding connector and cable assembly is JUNKOSHA KB0020MCG50B1.

Schematic Diagram




CXB1109Q
IC9
CXB1109Q
IC10
CXB1144Q
IC8
IC4-1
IC4-2
IC4-3
IC4-4
IC11
CX20201
TL431CP
D2
con.4
DA OUT
con.5
SW3
SW6
DECIMATION

Characteristics

Fig. 5. Gain vs. Input Frequency

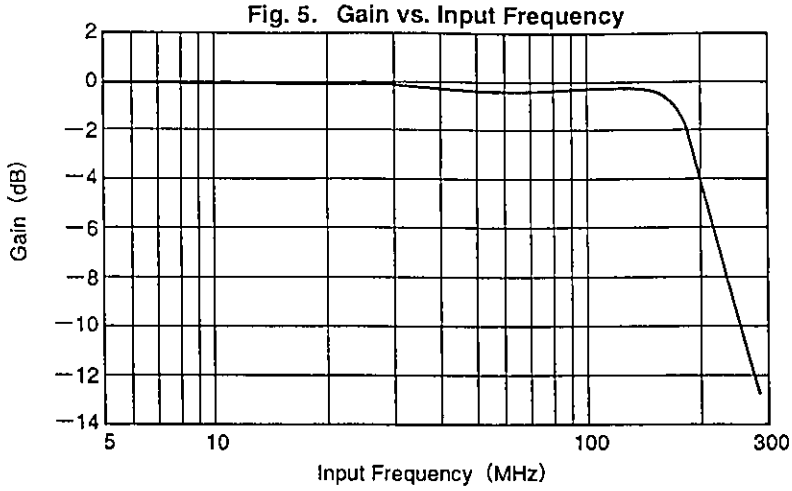


Fig. 6. SNR vs. Input Frequency

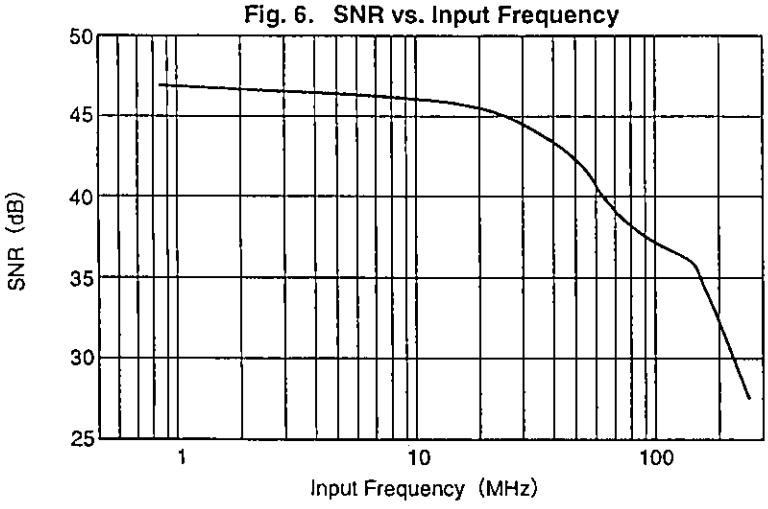
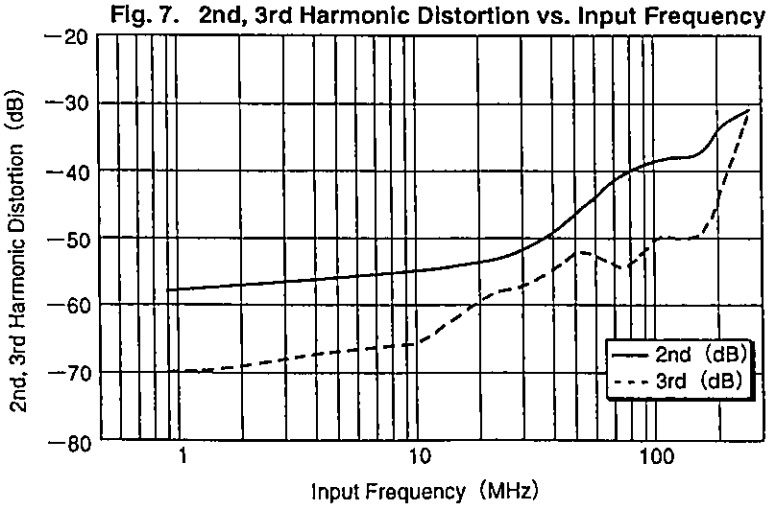
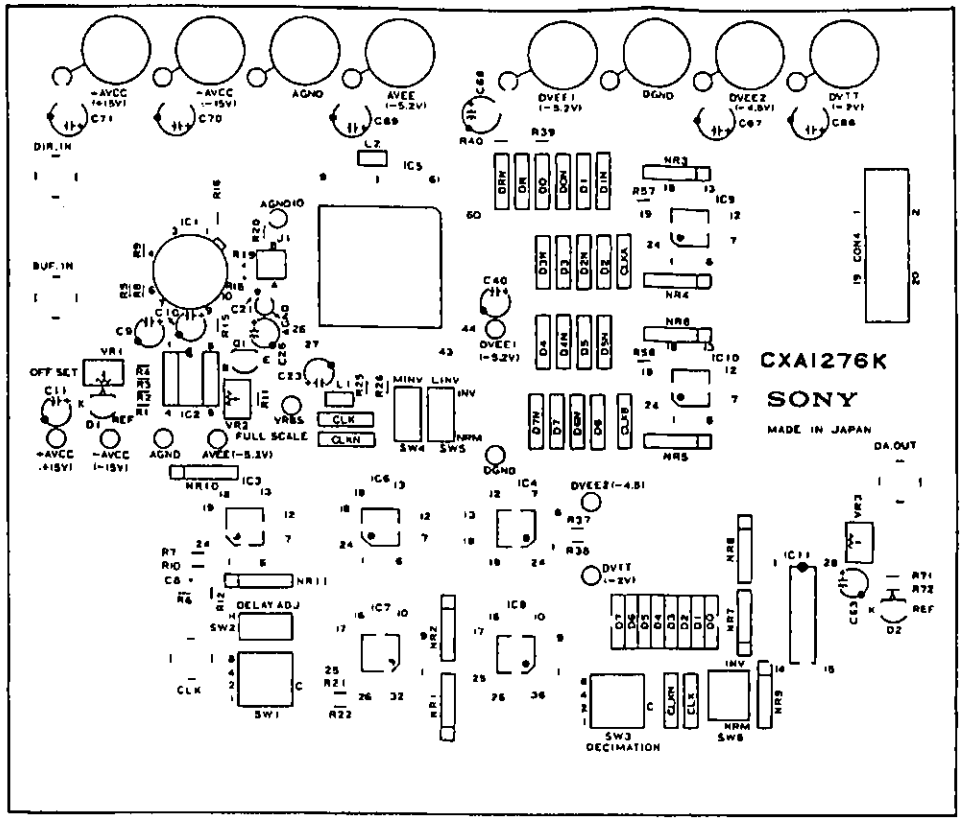


Fig. 7. 2nd, 3rd Harmonic Distortion vs. Input Frequency

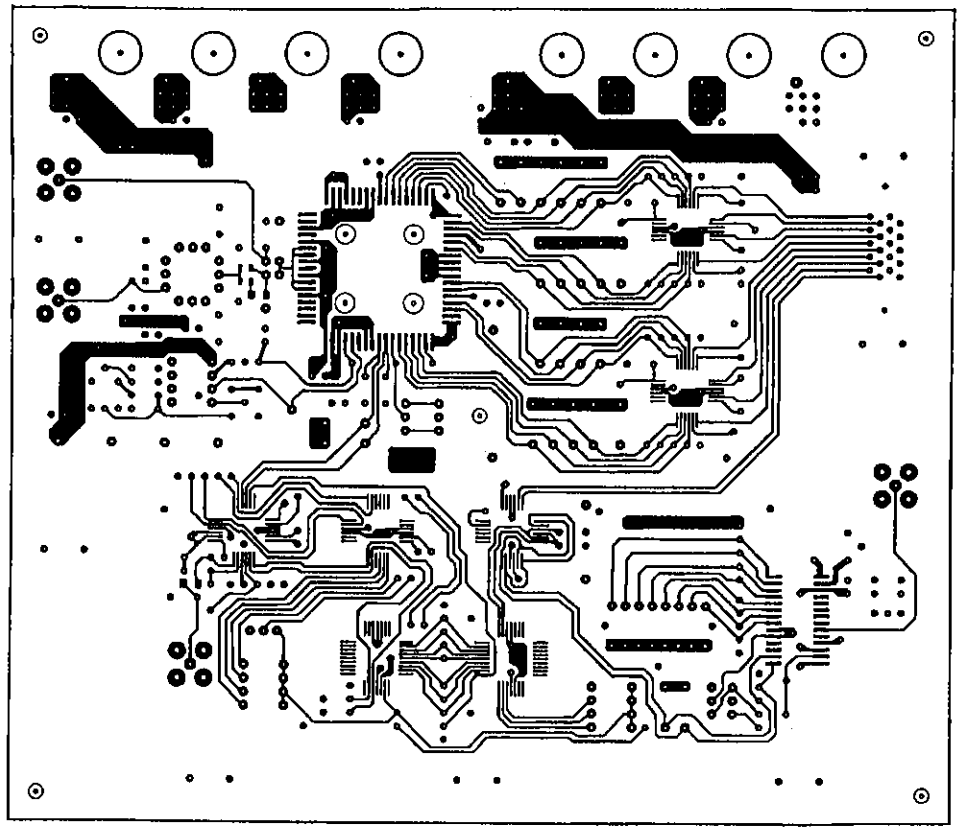


Parts Layout

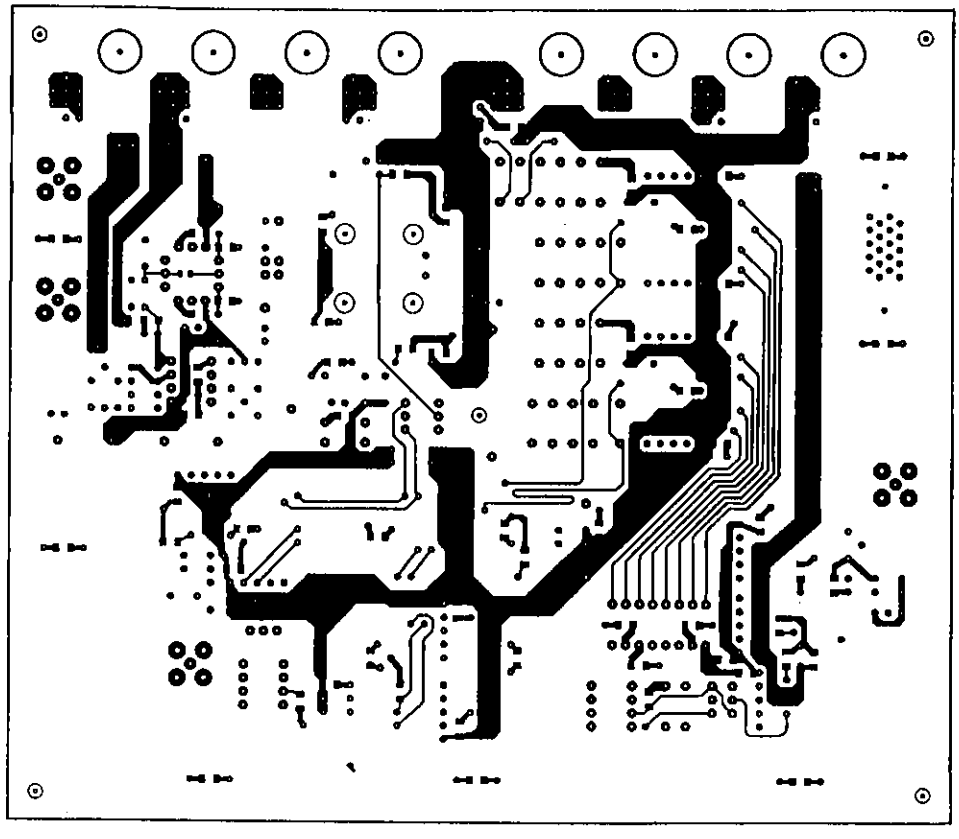


Component plane

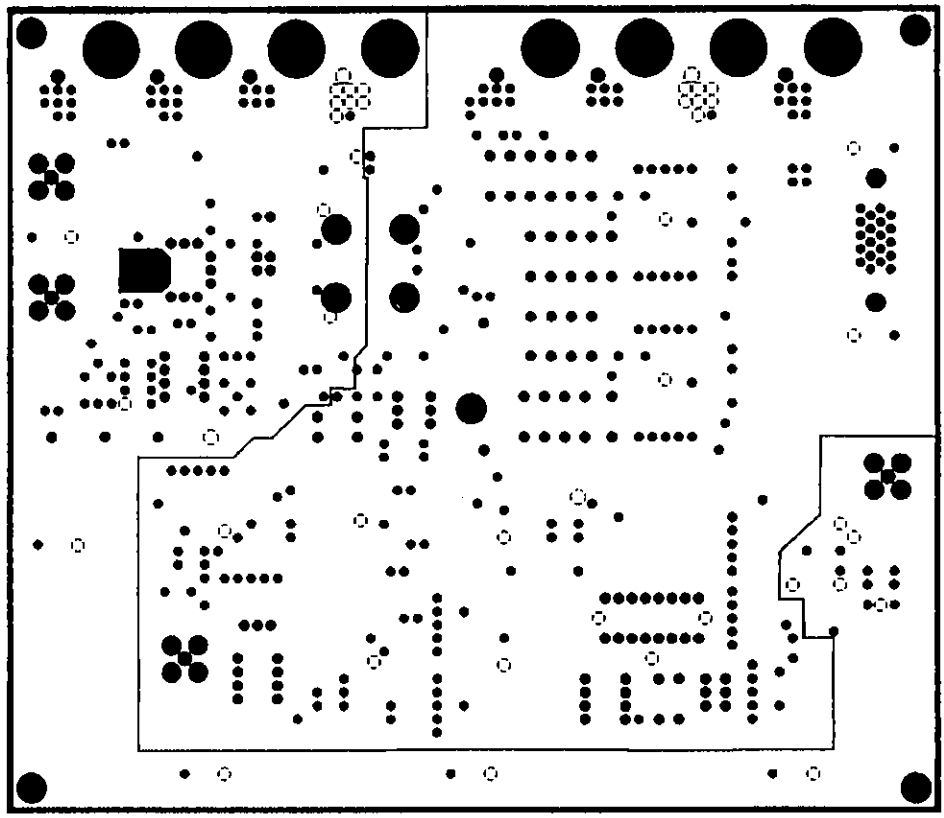
Printed Pattern



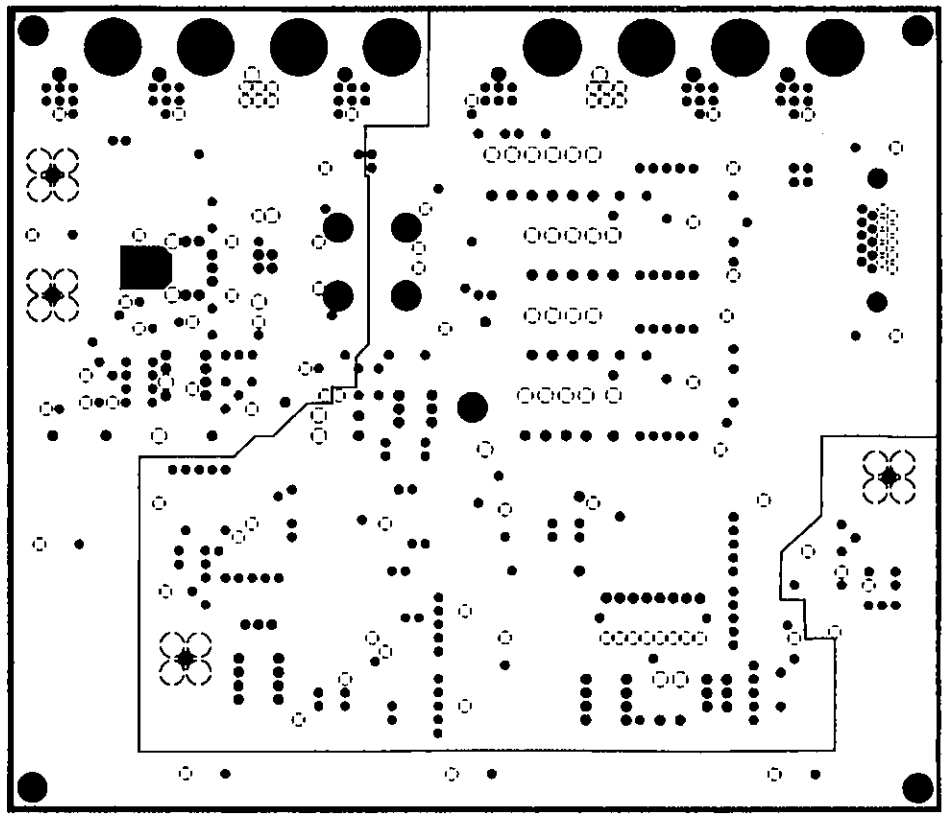
Component plane



Solder plane



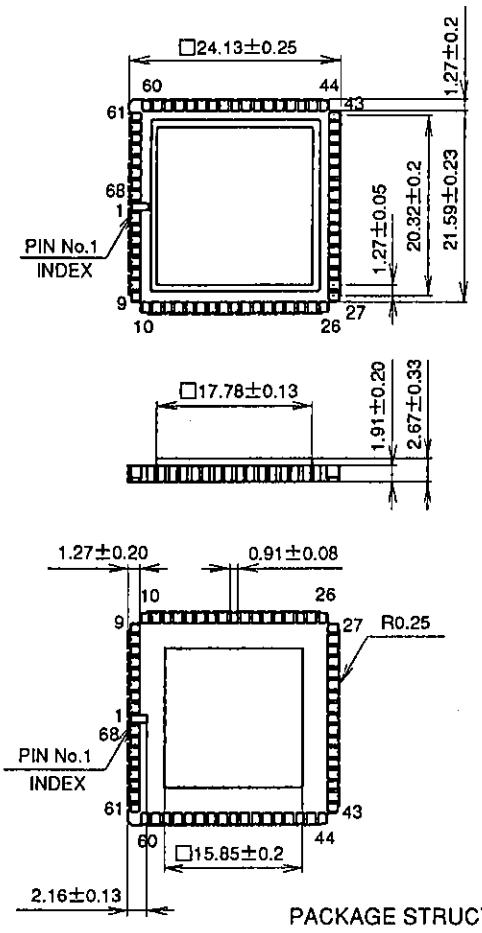
GND plane (inner layer)



VEE plane (inner layer)

Package Outline Unit : mm

68PIN LCC (CERAMIC)



SONY CODE	LCC-68C-02
EIAJ CODE	HQFN068-C-S950-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	
PACKAGE WEIGHT	3.7g