YAMAHA® LSI

YMZ705

SSGS

SSG & ADPCM Playback with Sequencer

■OVERVIEW

YMZ705(SSGS) is an automatic play LSI with synthesizer equivalent to two YM2149(SSG) and ADPCM playback function. By two internal sequencers, YMZ705 plays two different music simultaneously with up to six square wave plus two noise plus eight ADPCM voices at a time.

All the parameters for the synthesizer can be controlled directly by CPU even when the sequencers are in operation.

■FEATURES

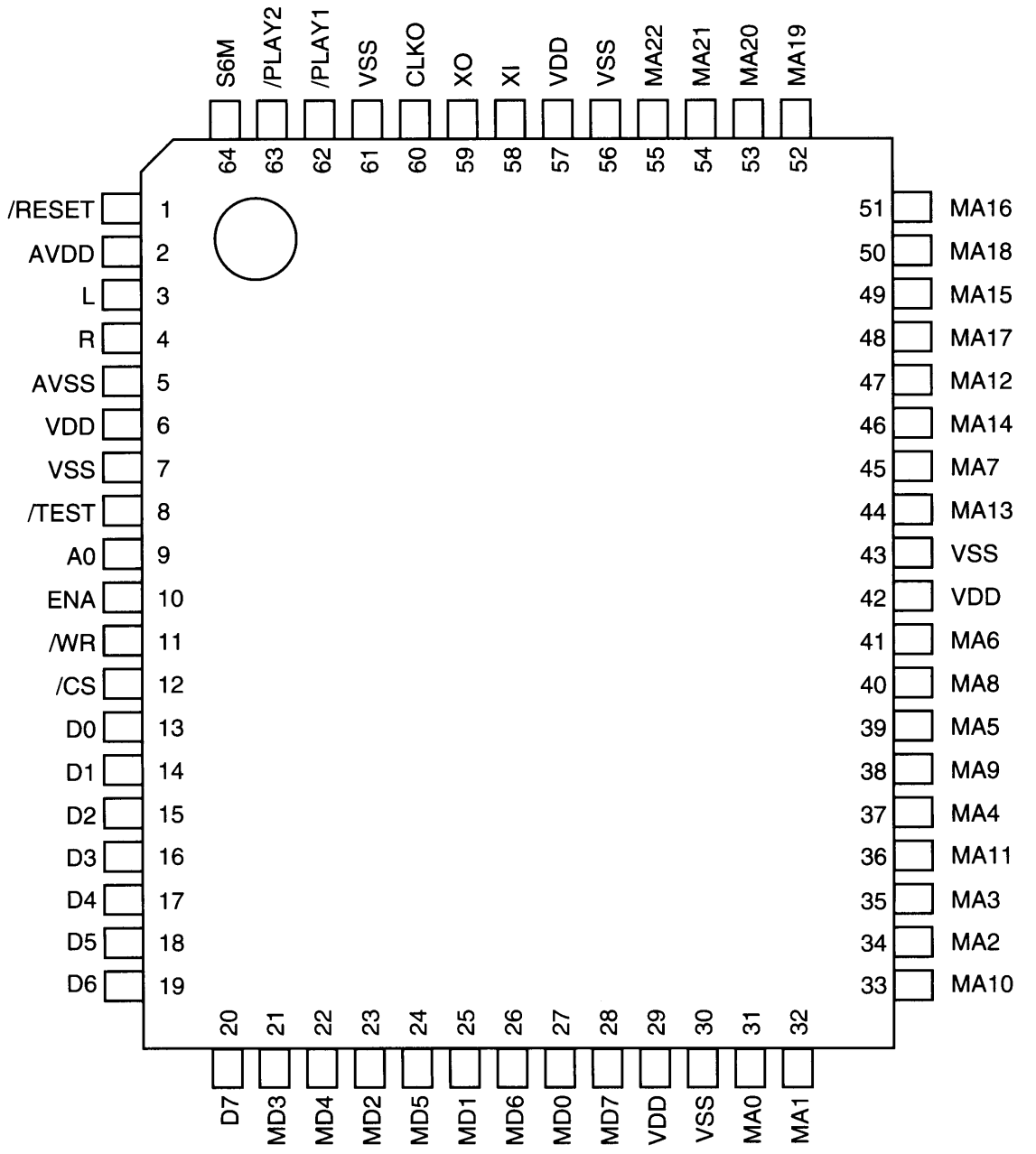
- ●YMZ705 includes two systems of SSG synthesizer, each of which generates three square wave plus one noise so that it can generate up to six square wave plus two noise plus eight ADPCM voices simultaneously.
  The voice data that is made by digital mixing is outputted as analog signals from the built-in 12-bit floating D/A converter.
- ●With its sequencer function, YMZ705 is able to playback two songs at the same time from up to 64 songs stored in the external memory.
- ●With its 4-bit ADPCM playback function, YMZ705 is able to playback maximum eight voices at the same time from voice data of up to 64 voices stored in the external memory.
  A sampling frequency can be selected from 32kHz, 16kHz, 8kHz and 4kHz for each channel.
- ●An external memory up to 8 Mbytes can be connected to YMZ705 for storing music data and ADPCM data.
- ●For both SSG and ADPCM, the data can be controlled directly by CPU.
- ●For SSG, pan-pot can be set for six voices independently. For ADPCM, it can be set for eight voice sindependently.
- ●+5V single power supply, silicon gate CMOS process.
- ●64 pin plastic QFP(YMZ705-F).

YAMAHA CORPORATION

YMZ705 CATALOG
CATALOG No. : -LSI4MZ705A2
1996. 10

■PIN OUT DIAGRAM

YMZ705-F



<64pin QFP Top View>

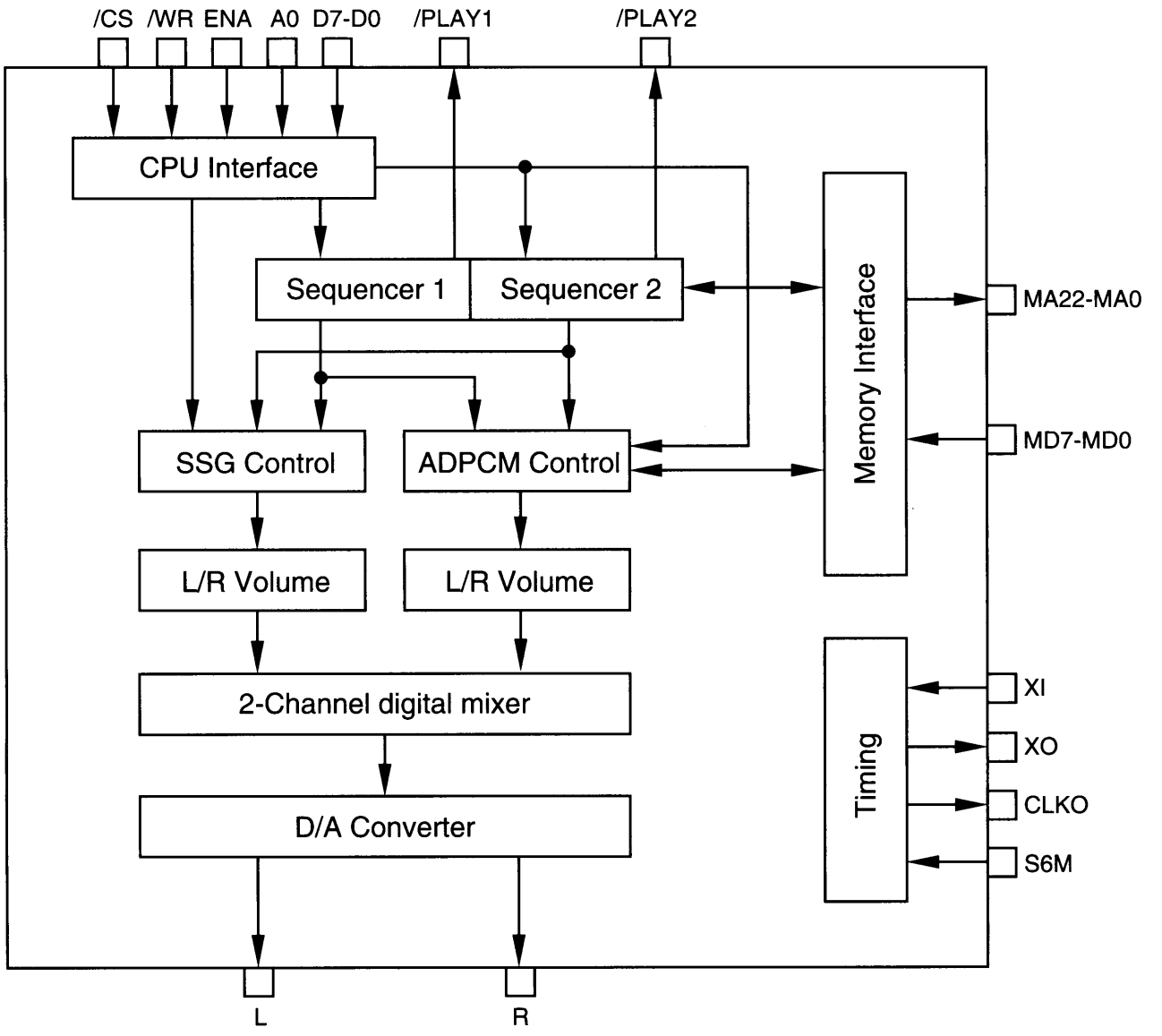
■PIN FUNCTION

No.	Name	I/O	Function
1	/RESET	I+	Reset input
2	AVDD	—	+5V power supply (Analog)
3	L	OA	Analog output (Left channel)
4	R	OA	Analog output (Right channel)
5	AVSS	—	Ground (Analog)
6	VDD	—	+5V power supply
7	VSS	—	Ground
8	/TEST	I+	LSI test pin
9	AO	I	CPU interface Address select signal input
10	ENA	I	CPU interface Enable signal input
11	/WR	I	CPU interface Write enable signal input
12	/CS	I	CPU interface Chip select signal input
13	D0	I	CPU interface Data bus
14	D1	I	Data bus
15	D2	I	Data bus
16	D3	I	Data bus
17	D4	I	Data bus
18	D5	I	Data bus
19	D6	I	Data bus
20	D7	I	Data bus
21	MD3	I+	External memory interface Data bus
22	MD4	I+	Data bus
23	MD2	I+	Data bus
24	MD5	I+	Data bus
25	MD1	I+	Data bus
26	MD6	I+	Data bus
27	MD0	I+	Data bus
28	MD7	I+	Data bus
29	VDD	—	+5V power supply
30	VSS	—	Ground
31	MA0	O	External memory interface Address bus
32	MA1	O	Address bus
33	MA10	O	Address bus
34	MA2	O	Address bus
35	MA3	O	Address bus
36	MA11	O	Address bus
37	MA4	O	Address bus
38	MA9	O	Address bus
39	MA5	O	Address bus
40	MA8	O	Address bus
41	MA6	O	Address bus

No.	Name	I/O	Function
42	VDD	—	+5V power supply
43	VSS	—	Ground
44	MA13	O	External memory interface Address bus
45	MA7	O	Address bus
46	MA14	O	Address bus
47	MA12	O	Address bus
48	MA17	O	Address bus
49	MA15	O	Address bus
50	MA18	O	Address bus
51	MA16	O	Address bus
52	MA19	O	Address bus
53	MA20	O	Address bus
54	MA21	O	Address bus
55	MA22	O	Address bus
56	VSS	—	Ground
57	VDD	—	+5V power supply
58	XI	I	Crystal oscillator connection or external clock input pin (4.096MHz or 6.144MHz)
59	XO	O	Crystal oscillator connection pin
60	CLKO	O	Master clock output
61	VSS	—	Ground
62	/PLAY1	O	Sequencer 1 'Play in progress' flag
63	/PLAY2	O	Sequencer 2 'Play in progress' flag
64	S6M	I+	Master clock frequency select signal ('H'=6.144MHz, 'L'=4.096MHz)

Note: I+: Pin with built-in pull-up resistor
OA: Analog output pin
/TEST: To be open

■BLOCK DIAGRAM



■FUNCTIONS

1. Clock signal oscillation XI, XO, CLKO

XI and XO pins are used to form a crystal oscillation circuit. The circuit generates either 4.096MHz or 6.144MHz.
External clock signal can be inputted through XI pin. At this time, XO pin must be open.
CLKO pin outputs the same frequency.

2. Clock signal selection S6M

Set this pin to 'L' when the clock frequency is 4.096MHz, or to 'H' when 6.144MHz.

3. CPU interface /CS, /WR, ENA, A0, D7 to D0, /PLAY1, /PLAY2

Pins D7 to D0 accept command data from CPU.
Each of /CS, /WR, ENA and A0 controls writing of command data.
The mode varies according to the clock frequency selected with S6M pin.

S6M	/CS	/WR	ENA	A0	Function
L	L	L	H	L	Address write mode
L	L	L	H	H	Data write mode
L	*	*	L	*	Inactive mode
H	L	L	*	L	Address write mode
H	L	L	*	H	Data write mode
*	H	*	*	*	Inactive mode
*	*	H	*	*	Inactive mode

*: Don't care

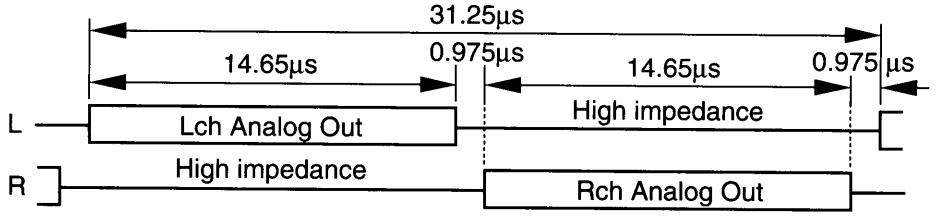
/PLAY1 and /PLAY2 are 'L' when the sequencer 1 and sequencer 2 are in play respectively.

4. External memory interface MA22 to MA0, MD7 to MD0

When reading data from external memory, address is outputted from MA22 to MA0 pins and data is inputted through MD7 to MD0 pins. MD7 to MD0 pins have built-in pull-up resisters.

5. DAC output L, R

Output of SSG synthesizer and playback voices of ADPCM are mixed at the digital mixer. The mixed digital signals are converted to analog signals with 12-bit 2-channel time sharing system, and then distributed to the L and R channels by analog switch.



6. System reset /RESET

YMZ705 requires the system reset at turn on. When the pin is 'L', internal registers to "0" and generation of voice are stopped compulsorily.

■SSG synthesis control register map

ADRS	Function	D7	D6	D5	D4	D3	D2	D1	D0
$00	Channel-1A Frequency	8-bit fine tone adjustment							
$01						4-bit rough tone adjustment			
$02	Channel-1B Frequency	8-bit fine tone adjustment							
$03						4-bit rough tone adjustment			
$04	Channel-1C Frequency	8-bit fine tone adjustment							
$05						4-bit rough tone adjustment			
$06	Noise-1 Frequency				5-bit Noise frequency				
$07	Mixer-1 Setting			Noise			Tone		
				C	B	A	C	B	A
$08	Channel-1A Volume				M	L3	L2	L1	L0
$09	Channel-1B Volume				M	L3	L2	L1	L0
$0A	Channel-1C Volume				M	L3	L2	L1	L0
$0B	Envelope-1 Frequency	8-bit fine adjustment							
$0C		8-bit rough adjustment							
$0D	Envelope-1 Shape					CONT	ATT	ALT	HOLD
$10	Channel-1A Pan-pot					P3	P2	P1	P0
$11	Channel-1B Pan-pot					P3	P2	P1	P0
$12	Channel-1C Pan-pot					P3	P2	P1	P0
$20	Channel-2A Frequency	8-bit fine tone adjustment							
$21						4-bit rough tone adjustment			
$22	Channel-2B Frequency	8-bit fine tone adjustment							
$23						4-bit rough tone adjustment			
$24	Channel-2C Frequency	8-bit fine tone adjustment							
$25						4-bit rough tone adjustment			
$26	Noise-2 Frequency				5-bit Noise frequency				
$27	Mixer-2 Setting			Noise			Tone		
				C	B	A	C	B	A
$28	Channel-2A Pan-pot				M	L3	L2	L1	L0
$29	Channel-2B Pan-pot				M	L3	L2	L1	L0
$2A	Channel-2C Pan-pot				M	L3	L2	L1	L0
$2B	Envelope-2 Frequency	8-bit fine adjustment							
$2C		8-bit rough adjustment							
$2D	Envelope-2 Shape					CONT	ATT	ALT	HOLD
$30	Channel-2A Frequency					P3	P2	P1	P0
$31	Channel-2B Frequency					P3	P2	P1	P0
$32	Channel-2C Frequency					P3	P2	P1	P0

Note: Contents of address $00 to $0D and $20 to 2D are register compatible with those of YM2149(SSG).
is don't care.

■ADPCM control register map

ADRS	Function	D7	D6	D5	D4	D3	D2	D1	D0
$40	Channel-1 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$41	Channel-1 Volume					L3	L2	L1	L0
$42	Channel-1 Pan-pot					P2	P1	P0	
$43	Channel-1 KEY ON, LOOP							KON	LOOP
$50	Channel-2 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$51	Channel-2 Volume					L3	L2	L1	L0
$52	Channel-2 Pan pot					P3	P2	P1	P0
$53	Channel-2 KEY ON, LOOP							KON	LOOP
$60	Channel-3 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$61	Channel-3 Volume					L3	L2	L1	L0
$62	Channel-3 Pan-pot					P3	P2	P1	P0
$63	Channel-3 KEY ON, LOOP							KON	LOOP
$70	Channel-4 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$71	Channel-4 Volume					L3	L2	L1	L0
$72	Channel-4 Pan-pot					P3	P2	P1	P0
$73	Channel-4 KEY ON, LOOP							KON	LOOP
$80	Channel-5 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$81	Channel-5 Volume					L3	L2	L1	L0
$82	Channel-5 Pan-pot					P3	P2	P1	P0
$83	Channel-5 KEY ON, LOOP							KON	LOOP
$90	Channel-6 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$91	Channel-6 Volume					L3	L2	L1	L0
$92	Channel-6 Pan-pot					P3	P2	P1	P0
$93	Channel-6 KEY ON, LOOP							KON	LOOP
$A0	Channel-7 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$A1	Channel-7 Volume					L3	L2	L1	L0
$A2	Channel-7 Pan-pot					P3	P2	P1	P0
$A3	Channel-7 KEY ON, LOOP							KON	LOOP
$B0	Channel-8 Voice designation	Sampling F		ADPCM Voice number					
	Sampling frequency	S1	S0	N5	N4	N3	N2	N1	N0
$B1	Channel-8 Volume					L3	L2	L1	L0
$B2	Channel-8 Pan-pot					P3	P2	P1	P0
$B3	Channel-8 KEY ON, LOOP							KON	LOOP

Note: ▒▒ is don't care.

■Sequencer and mix level control register map

ADRS	Function	D7	D6	D5	D4	D3	D2	D1	D0
$F0	Sequencer-1			Music number					
	Music designation, PLAY, REPEAT	PLAY	REP	PD5	PD4	PD3	PD2	PD1	PD0
$F1	Sequencer-1 Tempo			6-bit tempo adjustment					
$F2	Sequencer-2			Music number					
	Music designation, PLAY, REPEAT	PLAY	REP	PD5	PD4	PD3	PD2	PD1	PD0
$F3	Sequencer-2 Tempo			6-bit tempo adjustment					
$F4	Sequencer-1	ADPCM channel							
	Occupation channel(ADPCM)	8	7	6	5	4	3	2	1
$F5	Sequencer-2	ADPCM channel							
	Occupation channel(ADPCM)	8	7	6	5	4	3	2	1
$F6	Sequencer-1			SSG2 channel			SSG1 channel		
	Occupation channel(SSG)			C	B	A	C	B	A
$F7	Sequencer-2			SSG2 channel			SSG1 channel		
	Occupation channel(SSG)			C	B	A	C	B	A
$F8	SSG-ADPCM Mix level					4-bit SSG level adjustment			

Note: ▨ is don't care.

■8M byte Play data ROM address map

ADDRESS	DATA(8bit)
$000000～ $00003F	ADPCM Voice No.0～63 Data start address(L)
$000040～ $00007F	ADPCM Voice No.0～63 Data start address(M)
$000080～ $0000BF	ADPCM Voice No.0～63 Data start address(H)
$0000C0～ $0000FF	ADPCM Voice No.0～63 Data end address(L)
$000100～ $00013F	ADPCM Voice No.0～63 Data end address(M)
$000140～ $00017F	ADPCM Voice No.0～63 Data end address(H)
$000180～ $0001BF	Music No.0～63 Data start address(L)
$0001C0～ $0001FF	Music No.0～63 Data start address(M)
$000200～ $00023F	Music No.0～63 Data start address(H)
$000240～ $7FFFFF	ADPCM Voice data and music data area

■ELECTRICAL CHARACTERISTICS

1.Absolute maximum ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.5～7.0	V
Input voltage	V_I	−0.5～V_{DD}+0.5	V
Output voltage	V_O	−0.5～V_{DD}+0.5	V
Operating ambient temperature	T_{OP}	0～70	℃
Storage temperature	T_{STG}	−50～125	℃

2.Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating ambient temperature	T_{OP}	0	25	70	℃
Clock frequency	f_{MCLK}		4.096 or 6.144		MHz

3.DC characteristics (under recommended operating conditions)

Item	Symbol	Condition	Min.	Max.	Unit
Consumed current	I_{DD}	f_{MCLK}=4.096MHz		20	mA
Input voltage H level (1)	V_{IH1}	XI	3.5	V_{DD}+0.3	V
Input voltage L level (1)	V_{IL1}		−0.3	1.0	V
Input voltage H level (2)	V_{IH2}	All input pins except XI	2.2	V_{DD}+0.3	V
Input voltage L level (2)	V_{IL2}		−0.3	0.8	V
Output voltage H level	V_{OH}	I_{OH}=-0.1 mA	V_{DD}−1.0		V
Output voltage L level	V_{OL}	I_{OL}=2.0mA *1		0.4	V
Input leakage current	I_{LI}	V_I=0～5.0V *2	−10	10	μA
Pull-up resistor	R_U	*3	30	300	kΩ

Note: *1: Applied to all output pins except L, R, and XO.
*2: Applied to D7 to D0 (in case of input status), A0, /WR, XI, /CS and ENA pins.
*3: Applied to MD7 to MD0, /RESET, /TEST and S6M pins.

4. Analog characteristics (under recommended operating conditions)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog output voltage	V_{OA}	L, R *1		4.96		V

Note*1: AV_{DD}=5.0V, maximum volume, no load, peak to peak.

5.AC characteristics (under recommended operating conditions)

Item	Symbol	Min.	Typ.	Max.	Unit
Master clock frequency (4.096MHz)	tCK		tVCK/2 *1		ns
(6.144MHz)			tVCK/3		ns
Input clock rise time	tRCK			10	ns
Input clock fall time	tFCK			10	ns
Input clock duty	D	40	50	60	%
Reset pulse width	tRW	75*tVCK			ns
A0 set-up time *2	tAS	5			ns
A0 hold time *3	tAH	5			ns
Chip select pulse width *4	tCSW	tCK+20			ns
Write pulse width *4	tWRW	tCK+20			ns
ENA pulse width *4	tEW	tCK+20			ns
Write wait time(1) *5	tWWW1	2*tVCK			ns
Write wait time(2) *5	tWWW2	65*tVCK			ns
Write data set-up time *6	tWDS	80			ns
Write data hold time *6	tWDH	−5			ns
Memory access time *7	tRAC			250	ns

Note: Output load capacitance CL=50(pF).

*1: tVCK=488.28ns. Internal operation clock cycle(2.048MHz).

*2: tAS is determined by the later timing of "both /CS and /WR turn 'L'" or "ENA turns 'H'".

*3: tAH is determined by the earlier timing of "both /CS and /WR turn 'H'" or "ENA turns 'L'".

*4: Overlapping time of each pulse width.

*5: twww1 and twww2 are determined by the longer period of "/CS and /WR are 'H'" or "ENA is 'L'".

*6: tWDS and tWDH are determined by the earlier timing of "both /CS and /WR turn 'H'" or "ENA turns 'L'".

*7: The time from the moment address has been settled to the moment data has been settled.

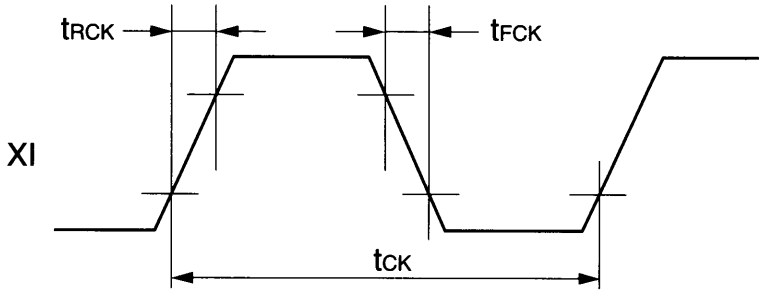


Fig.1 Master clock timing

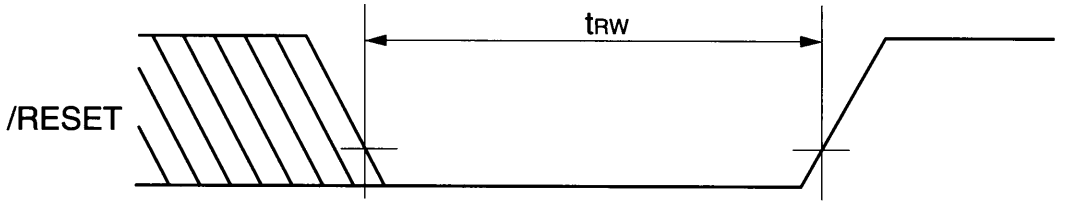


Fig.2 Reset timing

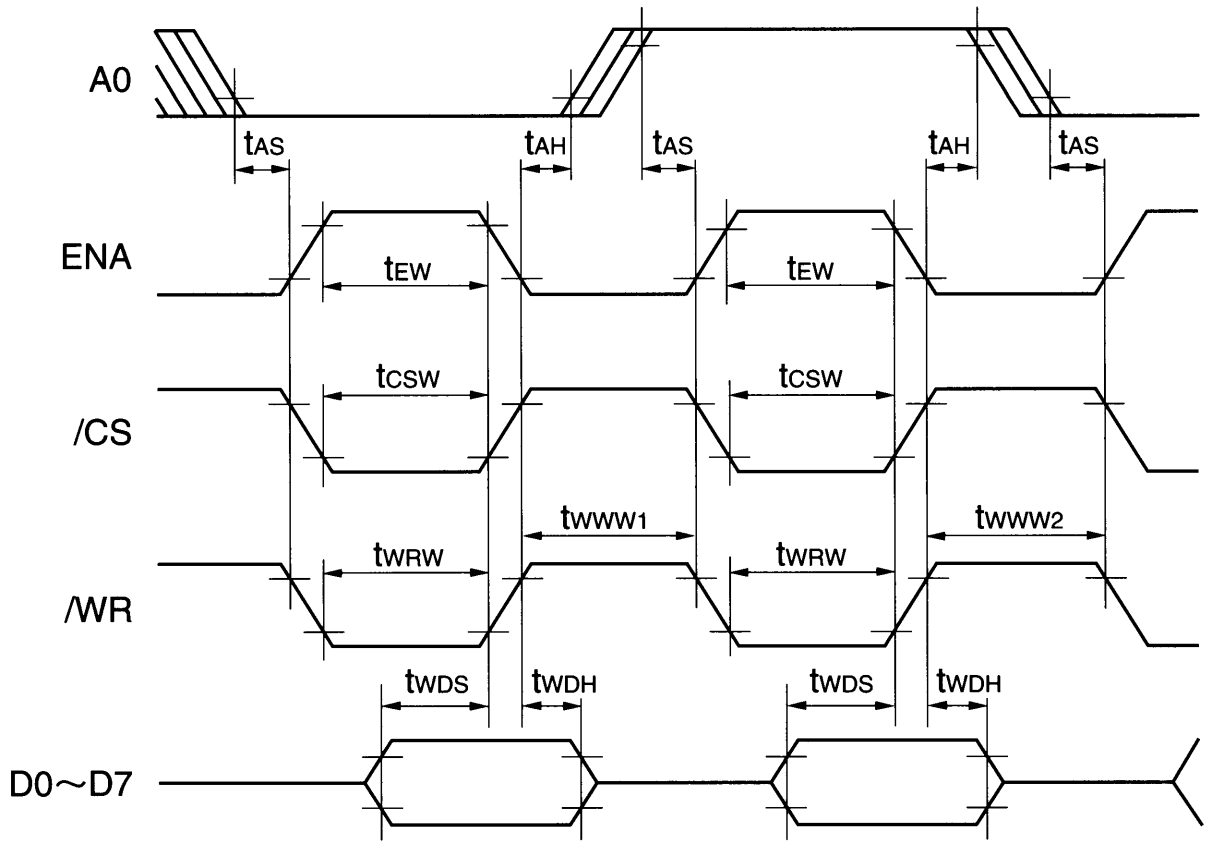
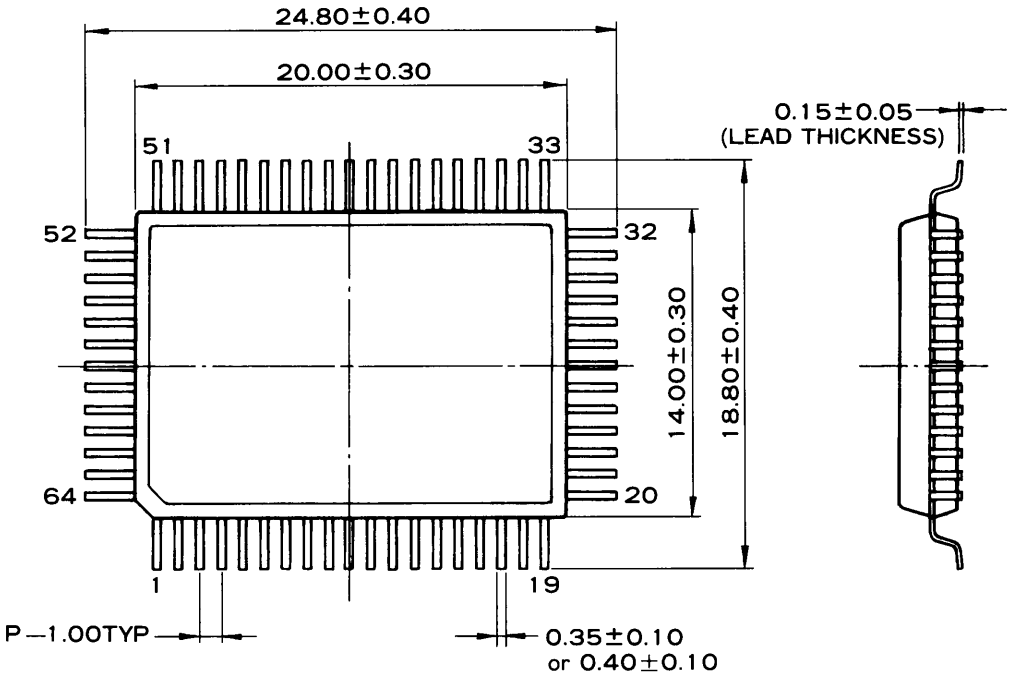
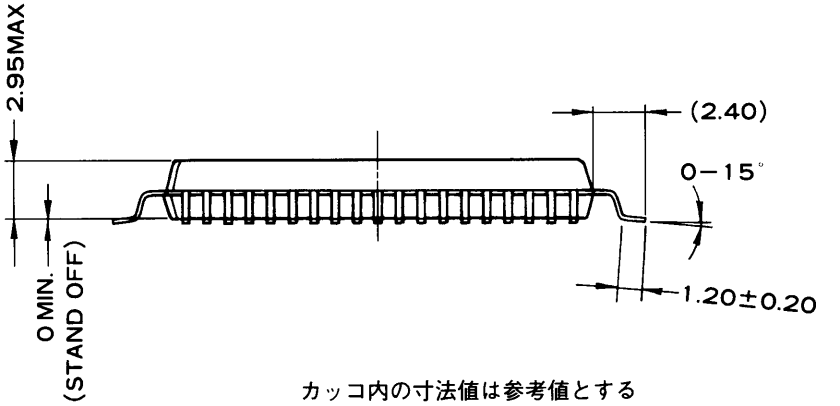


Fig.3 CPU interface timing

■EXTERNAL DIMENSIONS

YMZ705-F





カッコ内の寸法値は参考値とする
モールド外形寸法はバリを含まない
単位（UNIT）：mm

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

NOTE: The LSIs for surface mount need especial consideration on storage and soldering condisions. For derailed information, please contact your nearest agent of yamaha.

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