Errata on SAM3U Engineering Sample Devices

1. Scope

This document describes the known errata found on the SAM3U series engineering samples.

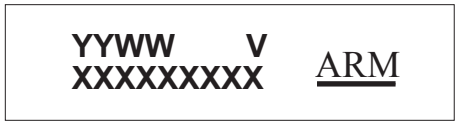
It applies to:

- AT91SAM3U4E (with Marking ES)
- AT91SAM3U2E (with Marking ES)
- AT91SAM3U1E (with Marking ES)
- AT91SAM3U4C (with Marking ES)
- AT91SAM3U2C (with Marking ES)
- AT91SAM3U1C (with Marking ES)

1.1 Marking

All devices are marked with the Atmel logo and the ordering code.

Additional marking is as follows:



where

- “YY”: manufactory year
- “WW”: manufactory week
- “V”: revision
- “XXXXXXXXX”: lot number

AT91 ARM Thumb-based Microcontrollers

ATSAM3U Series

Errata Sheet

6483A–ATARM–04-Aug-09

1.2 Errata

1.2.1 Flash Memory

1.2.1.1 *FLASH: Flash Reading in 64-bit mode*

Higher power consumption than expected can be seen when reading Flash in 64-bit mode.

Workaround

Use 128-bit mode instead.

Problem Fix

This issue will be fixed in the next revision.

1.2.1.2 *FLASH: Flash issue running at frequency lower than 2.5 MHz*

When the system clock (MCK) is lower then 2.5 MHz with 1 or 2 Wait State (WS) programmed in the EEFC_FMR, the Cortex fetches wrong instructions.

Workaround

Do not use 1 or 2 WS when running at a frequency lower than 2.5 MHz.

Problem Fix

This issue will be fixed in the next revision.

1.2.2 12-bit ADC (ADC12B)

1.2.2.1 *ADC12B: Single Ended Mode*

When enabling a channel in single ended mode, AD12B0 (CH0) for example, the associated channel in differential mode, AD12B1 and its associated pin are also activated. If the application is using the PIO pin multiplexed with AD12B1 input, the PIO pin will switch to input Analog Mode when the channel is enabled. However, the conversion result on AD12B0 channel is not impacted.

Workaround

None.

Problem Fix

This issue will be fixed in the next revision.

1.2.2.2 *ADC12B: Differential Mode*

When enabling a channel in differential mode, CH0 (AD12B0-AD12B1 inputs) for example, only the AD12B0 input will be set to input analog mode automatically by the ADC Controller.

Workaround

The associated differential input channel, AD12B1 must be enabled by the user's software, i.e., CH1.

Problem Fix

This issue will be fixed in the next revision.

1.2.2.3 *ADC12B: Wrong Mode after reset*

After reset the ADC is not in Off Mode, but in Standby Mode leading to current consumption on VDDANA (1.4 mA. instead of 0.1 µA).

Workaround

Configure the ADC in Off Mode in the ADC Extended Mode Register (ADC_EMR) after reset.

Problem Fix

This issue will be fixed in the next revision.

1.2.2.4 ADC12B: Current Consumption in Backup Mode on VDDANA

In Backup mode, the ADC is not in Off Mode, but in Standby Mode (even if the software has previously put it in Off mode) leading to current consumption on VDDANA (1.4 mA instead of 0.1µA).

Workaround

None.

Problem Fix

This issue will be fixed in the next revision.

1.2.3 Serial Wire and JTAG Debug Port (SWJ-DP)

1.2.3.1 SWJ-DP: Asynchronous Trace (TRACESWO)

Asynchronous Trace *(TRACESWO)* does not work.

Workaround

None.

Problem Fix

This issue will be fixed in the next revision.

1.2.3.2 SWJ-DP: Processor Reset

A processor reset also asserts *SWJ-DP*. Connection issue in debug mode.

Workaround

Workaround applied by Segger on SAM-ICE Firmware.

Problem Fix

This issue will be fixed in the next revision.

1.2.4 Supply Controller (SUPC)

1.2.4.1 SUPC: Bad behavior of SMS and SMOS bit in SUPC_SR in Sample mode

When the Supply Monitor is configured in sample mode (SMSMPL > 1), the SMS and SMOS bits of the supply controller status register (SUPC_SR) might not be reliable when polling SUPC_SR.

Workaround

Use the Supply Monitor Interrupt instead of polling the status register. In the interrupt handler, set the Supply Monitor in Continuos mode to check the bits SMA and SMOS.

Problem Fix

This issue will be fixed in the next revision.

1.2.5 Power Management Controller (PMC)

1.2.5.1 PMC: SysTick does not work properly if MCK/8 is selected as clock source

The System Tick (SysTick) of the Cortex®-M3 has two sources of clock, either MCK or MCK/8 and is configured by the CLKSOURCE bit of the SysTick CTRL register.

When setting CLKSOURCE to 0 (MCK/8), SysTick does not work properly.

Workaround

Set CLKSOURCE at 1 (MCK selected as SysTick source).

Problem Fix

This issue will be fixed in the next revision.

1.2.5.2 PMC: Main Oscillator Crystal Failure detection not functional

When the 32768 Hz Crystal Oscillator is selected as slow clock source and if the Main Oscillator Crystal Failure detection is enabled, the CFDEV, CFDS and FOS status bits in the PMC_SR register do not rise.

Workaround

Use the Embedded 32 kHz RC Oscillator as slow clock source.

Problem Fix

This issue will be fixed in the next revision.

1.2.5.3 PMC: Main Oscillator Frequency selection if the Main On Chip RC Oscillator is off

When the 4/8/12 MHz RC Oscillator is off, the frequency selection (MOSCRCF in CKGR_MOR) can not be changed. The register can be written but the modification on MOSCRCF will not be taken into account.

Workaround

Modify MOSCRCF when the 4/8/12 MHz RC Oscillator is on (MOSCRCEN =1).

Problem Fix

This issue will be fixed in the next revision.

1.2.6 SAM3U Matrix (MATRIX)

1.2.6.1 MATRIX: I/D default master for Flash after reset

The I/D Cortex-M3 bus is not set as default master for the Flash after reset. There is a minor impact in terms of performance when running the code from the Flash (about 5%).

Workaround

Configure by software the I/D Cortex-M3 bus as default Master for the Flash.

Problem Fix

This issue will be fixed in the next revision.

1.2.7 PIO

1.2.7.1 PIO: NCS1 on PA16

The chip select 1 (NCS1) of the SMC on PA16 (Peripheral B) does not work.

Workaround

Use NCS1 available on PC12 (Peripheral A) or use a another chip select or drive the chip select by software.

Problem Fix

This issue will be fixed in the next revision.

1.2.8 Backup Mode

1.2.8.1 Backup mode: VDDUTMI current consumption in Backup mode

In Backup mode, the current consumption measured on VDDUMTI can be around 500 µA instead of less than 0.1 µA.

Workaround

Disable externally the voltage on VDDUTMI in Backup mode.

Problem Fix

This issue will be fixed in the next revision.

1.2.8.2 Backup mode: the PIO states are not kept

When entering in Backup mode with WFE command, the PIO states are not kept. All the PIOs go into input with pull-up state in Backup mode.

Workaround

.Instead of using the WFE command to go into Backup mode, set the VROFF bit (SUPC_CR).

Problem Fix

This issue will be fixed in the next revision.

1.2.9 Wait Mode

1.2.9.1 Wait mode: VDDCORE current consumption

Some parts may show a higher current consumption than expected (50 µA instead of 5 µA) on VDDCORE.

Workaround

None.

Problem Fix

This issue will be fixed in the next revision.

Revision History

Doc. Rev	Comments	Change Request Ref.
6483A	First issue	

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