www.ti.com

SBVS068D–FEBRUARY 2006–REVISED OCTOBER 2007

Low Noise, High-Bandwidth PSRR Low-Dropout 150mA Linear Regulator

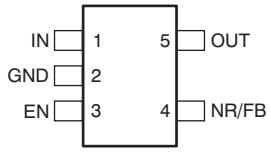
FEATURES

- **150mA Low-Dropout Regulator with Enable**
- **Low I_Q: 50μA (typical)**
- **Available in Multiple Output Versions:**
  - **Fixed Output with Voltages from 0.9V to 3.3V Using Innovative Factory EEPROM Programming**
  - **Adjustable Output Voltage from 0.9V to 6.2V**
- **Ultra-High PSRR:**
  - **70dB at 1kHz, 67dB at 100kHz and 45dB at 1MHz**
- **Low Noise: 30μV typical (100Hz to 100kHz)**
- **Stable with a 1.0μF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **3% Overall Accuracy (over Load/Line/Temp)**
- **Over-Current and Over-Temperature Protection**
- **Very Low Dropout: 170mV Typical at 150mA**
- **Small SC70-5, 2mm x 2mm SON-6, and 1.5mm × 1.5mm SON-6 Packages**

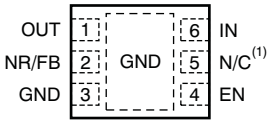
APPLICATIONS

- **Mobile Phone Handsets**
- **Wireless LAN, Bluetooth™**
- **PDAs and Smartphones**

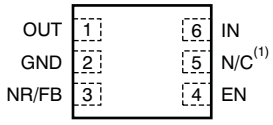
TPS717xx DCK SC70-5 PACKAGE (TOP VIEW)



TPS717xx DRV 2mm x 2mm SON (TOP VIEW)



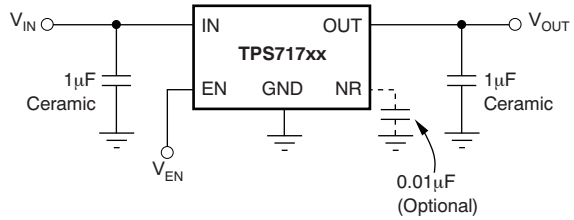
TPS717xx DSE 1.5mm x 1.5mm SON (TOP VIEW)



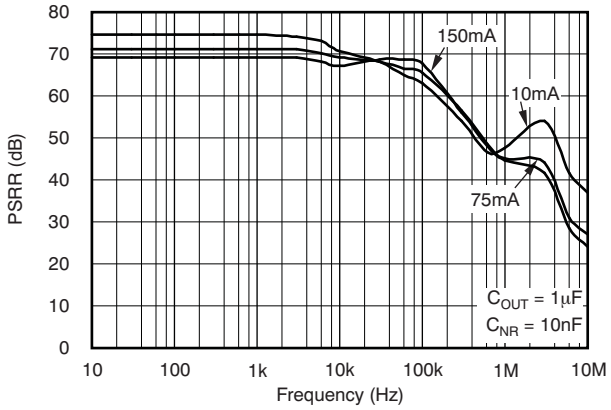
NOTE: (1) N/C = Not connected.

DESCRIPTION

The TPS717xx family of low-dropout (LDO), low-power linear regulators offers very high power supply rejection (PSRR) while maintaining very low 50μA ground current in an ultra-small, five-pin SC70 package. The family uses an advanced BiCMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717xx is stable with a 1.0μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. It is fully specified from T_J = –40°C to +125°C and is offered in a small SC70-5 package, a 2mm × 2mm SON-6 package with a thermal pad, and a 1.5mm × 1.5mm SON package, which are ideal for small form factor portable equipment such as wireless handsets and PDAs.



Typical Application Circuit for Fixed Voltage Versions



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS717**xxyyyz**	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Output voltages from 0.9V to 3.3V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted). All voltages are with respect to GND.

PARAMETER	TPS717xx	UNIT
Input voltage range, V_{IN}	–0.3 to +7.0	V
Feedback input voltage range, V_{FB}, V_{NR}	–0.3 to +3.6	V
Enable voltage range, V_{EN}	–0.3 to V_{IN} + 0.3V(2)	V
Output voltage range, V_{OUT}	–0.3 to +7.0	V
Maximum output current, I_{OUT}	Internally limited	
Continuous total power dissipation, P_{DISS}	See Dissipation Ratings Table	
Junction temperature range, T_J	–55 to +150	°C
Storage junction temperature range, T_{STG}	–55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{EN} absolute maximum rating is V_{IN} + 0.3V or +7.0V, whichever is greater.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
Low-K(1)	DCK	165°C/W	395°C/W	2.5mW/°C	250mW	140mW	100mW
High-K(2)	DCK	165°C/W	315°C/W	3.2mW/°C	320mW	175mW	130mW
Low-K(1)	DRV	20°C/W	140°C/W	7.1mW/°C	715mW	395mW	285mW
High-K(2)	DRV	20°C/W	65°C/W	15.4mW/°C	1540mW	845mW	615mW
High-K(2)	DSE	—	206°C/W	4.85mW/°C	485mW	269mW	194mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.5V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{IN}, C_{OUT} = 1.0µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS71701, V_{OUT} = 2.8V. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.5		6.5	V
V_{FB}	Internal reference (TPS71701)			0.790	0.800	0.810	V
V_{OUT}	Output voltage range (TPS71701)			0.9		6.5 – V_{DO}	V
V_{OUT}	Output accuracy(1)	Nominal	T_J = +25°C, 1.6V ≤ V_{IN} ≤ 6.5V	–0.05		+0.06	%
		Over V_{IN}, I_{OUT}, Temp(2)	V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.5V 0mA ≤ I_{OUT} ≤ 150mA	–3.0	±1.5	+3.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation (1)		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 6.5V, I_{OUT} = 5mA		125		µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		0mA ≤ I_{OUT} ≤ 150mA		120		µV/mA
V_{DO}	Dropout voltage(3) (V_{IN} = $V_{OUT(NOM)}$ – 0.1V)		I_{OUT} = 150mA		170	300	mV
I_{CL} (Fixed)	Output current limit (fixed output)		V_{OUT} = 0.9 × $V_{OUT(NOM)}$	200	325	500	mA
I_{CL} (Adjustable)	Output current limit (TPS71701)		V_{OUT} = 0.9 × $V_{OUT(NOM)}$	200	325	575	mA
I_{GND}	Ground pin current		I_{OUT} = 0.1mA		50	80	µA
			I_{OUT} = 150mA		100		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, 2.5V ≤ V_{IN} < 4.5V, T_J = –40°C to +85°C		0.20	1.5	µA
			V_{EN} ≤ 0.4V, 4.5V ≤ V_{IN} ≤ 6.5V, T_J = –40°C to +85°C		0.90		µA
I_{FB}	Feedback pin current (TPS71701)				0.02	1.0	µA
PSRR	Power-supply rejection ratio V_{IN} = 3.8V, V_{OUT} = 2.8V, I_{OUT} = 150mA		f = 100Hz		70		dB
			f = 1kHz		70		dB
			f = 10kHz		67		dB
			f = 100kHz		67		dB
			f = 1MHz		45		dB
V_N	Output noise voltage BW = 100Hz to 100kHz, V_{IN} = 3.8V, V_{OUT} = 2.8V, I_{OUT} = 10mA		C_{NR} = none (fixed output, TPS71701)		95 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.001µF		25 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.01µF		12.5 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.1µF		11.5 × V_{OUT}		μV_{RMS}
T_{STR}	Startup time V_{OUT} = 90% $V_{OUT(NOM)}$, R_L = 19Ω, C_{OUT} = 1.0µF		0.9V ≤ V_{OUT} ≤ 1.6V, C_{NR} = 0.001µF		0.700		ms
			1.6V < V_{OUT} < V_{MAX}, C_{NR} = 0.01µF		0.160		ms
$V_{EN(HI)}$	Enable high (enabled)		V_{IN} ≤ 5.5V	1.2		6.5	V
			5.5V < V_{IN} ≤ 6.5V	1.25		6.5	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled		EN = 6.5V		0.02	1.0	µA
UVLO	Under-voltage lockout		V_{IN} rising	2.41	2.45	2.49	V
	Hysteresis		V_{IN} falling		150		mV
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		+160		°C
			Reset, temperature decreasing		+140		°C
T_J	Operating junction temperature			–40		+125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.5V, whichever is greater.
(2) Does not include external resistor tolerances.
(3) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.6V because minimum V_{IN} = 2.5V.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS

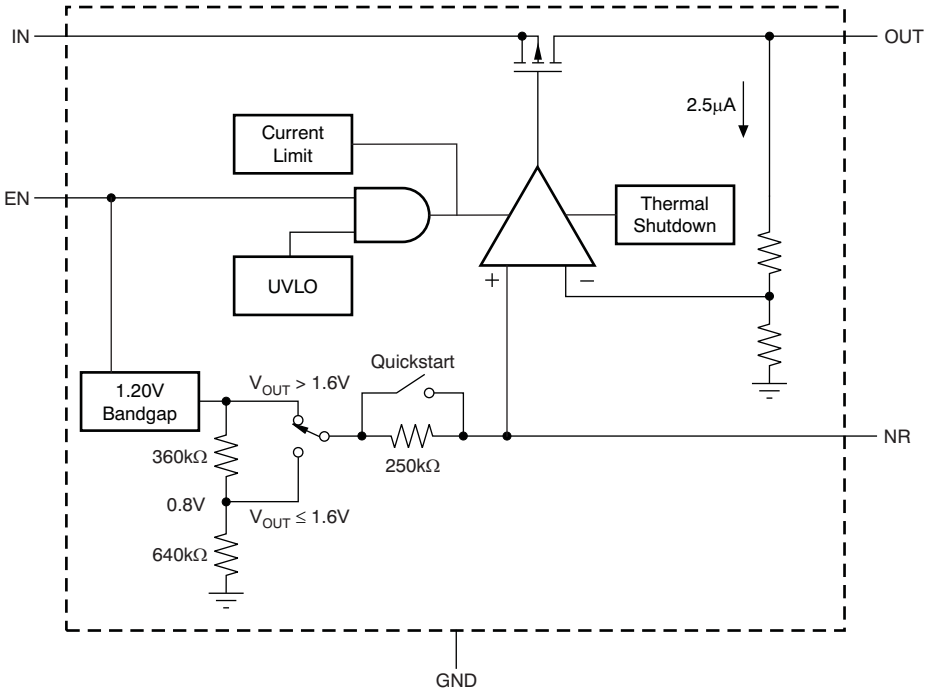


Figure 1. Fixed Voltage Versions

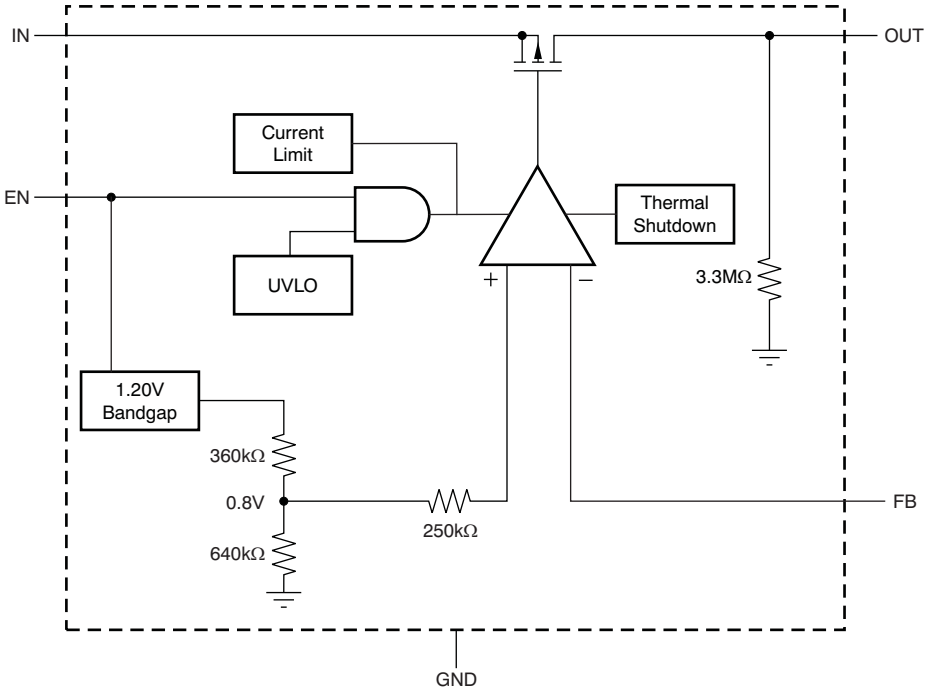
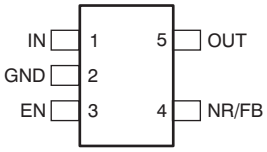


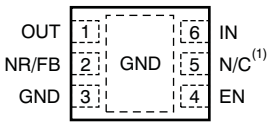
Figure 2. Adjustable Voltage Version

PIN CONFIGURATIONS

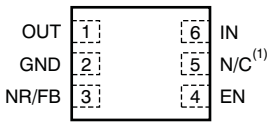
TPS717xx DCK
SC70-5 PACKAGE
(TOP VIEW)



TPS717xx DRV
2mm x 2mm SON
(TOP VIEW)



TPS717xx DSE
1.5mm x 1.5mm SON
(TOP VIEW)



NOTE: (1) N/C = Not connected.

Table 1. PIN DESCRIPTIONS

TPS717xx				DESCRIPTION
NAME	SC70 (DCK)	2×2 SON (DRV)	1.5×1.5 SON (DSE)	
IN	1	6	6	Input to the device.
GND	2	3	2	Ground.
EN	3	4	4	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into standby mode, thereby reducing operating current.
NR	4	2	3	Fixed voltage versions only. An external capacitor connected to this terminal bypasses noise generated by the internal bandgap, lowering output noise.
FB	4	2	3	Adjustable voltage version only. The voltage at this pin is fed to the error amplifier. A resistor divider from OUT to FB sets the output voltage when in regulation.
OUT	5	1	1	This is the regulated output voltage. A small capacitor is needed from this pin to ground to assure stability; a 1.0μF ceramic capacitor is adequate.
NC	–	5	5	Not connected. This pin can be tied to ground to improve thermal dissipation.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.5V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{IN}, C_{OUT} = 1.0µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS71701, V_{OUT} = 2.8V. Typical values are at T_J = +25°C.

LOAD REGULATION

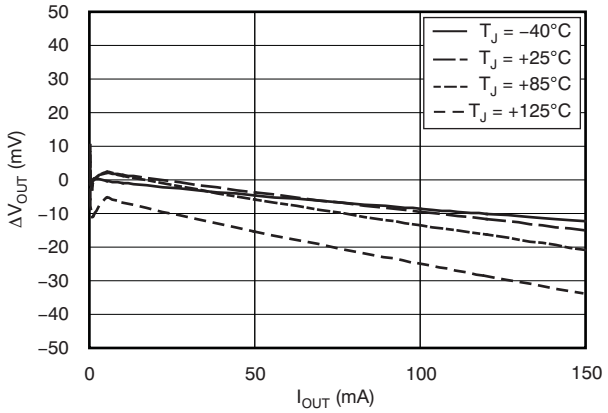


Figure 3.

LOAD REGULATION UNDER LIGHT LOADS

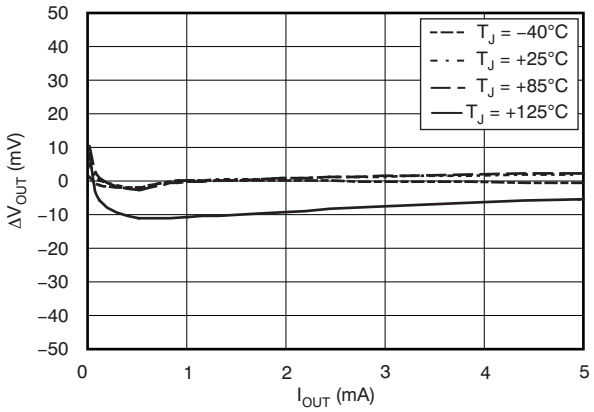


Figure 4.

LINE REGULATION
I_{OUT} = 5mA

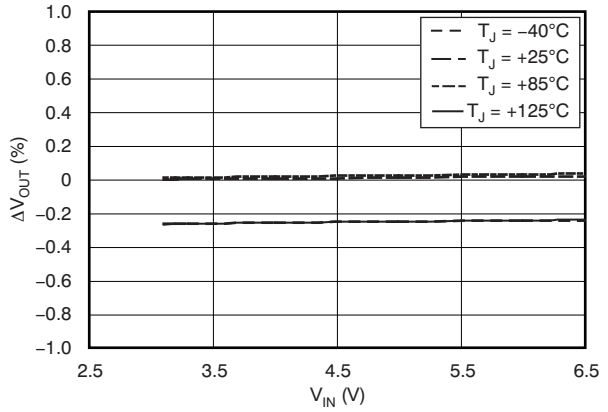


Figure 5.

LINE REGULATION
I_{OUT} = 150mA

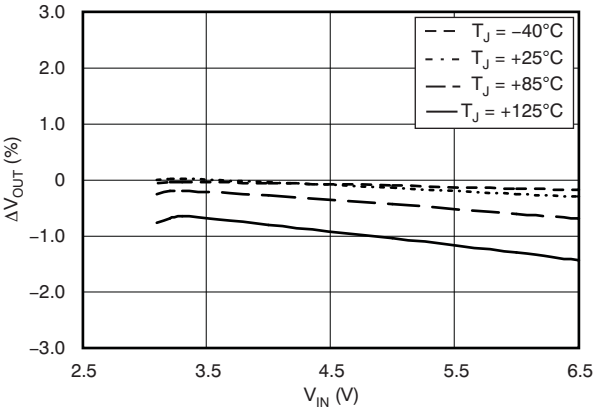


Figure 6.

OUTPUT VOLTAGE vs TEMPERATURE

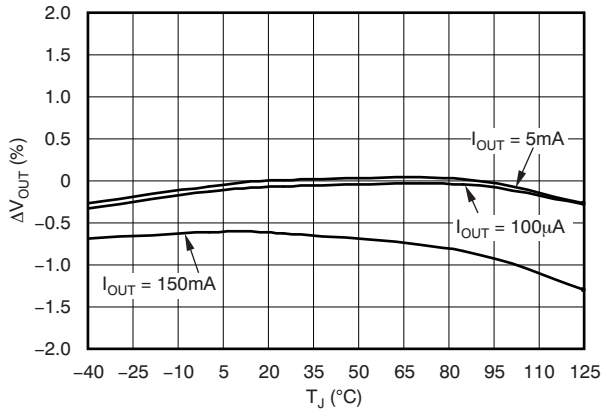


Figure 7.

DROPOUT VOLTAGE vs OUTPUT CURRENT

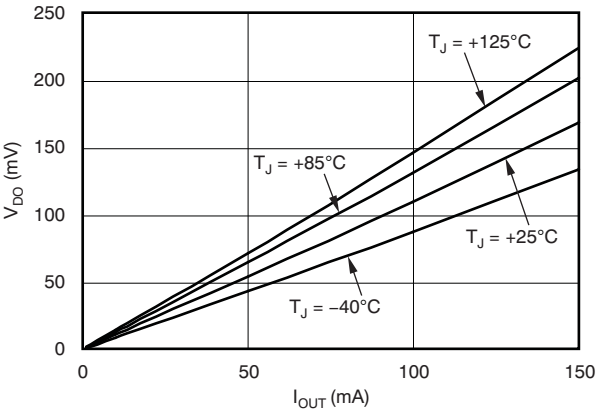


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.5V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{IN}, C_{OUT} = 1.0µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS71701, V_{OUT} = 2.8V.
Typical values are at T_J = +25°C.

DROPOUT VOLTAGE vs TEMPERATURE

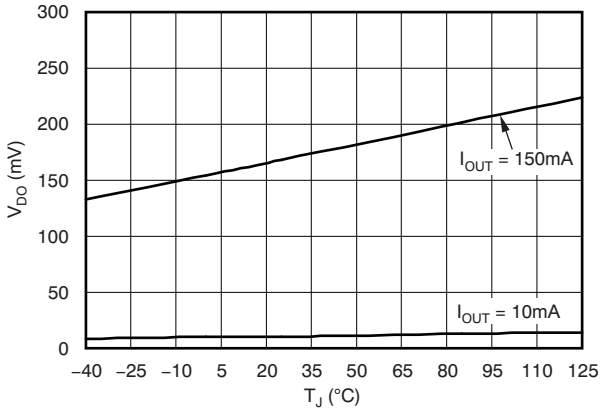


Figure 9.

GROUND PIN CURRENT vs INPUT VOLTAGE

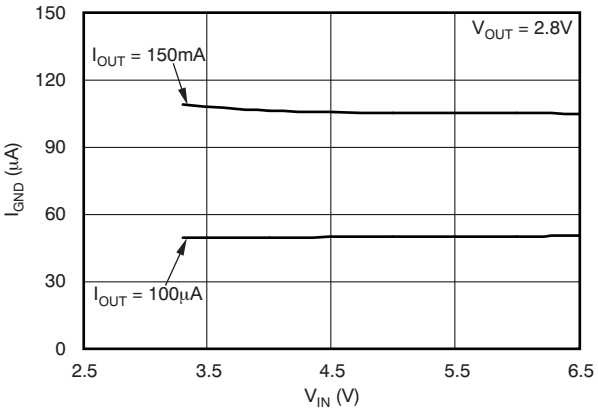


Figure 10.

GROUND PIN CURRENT vs OUTPUT CURRENT

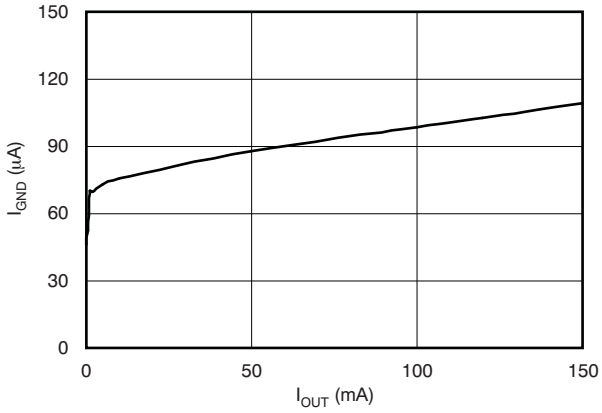


Figure 11.

GROUND PIN CURRENT vs TEMPERATURE (ENABLED)

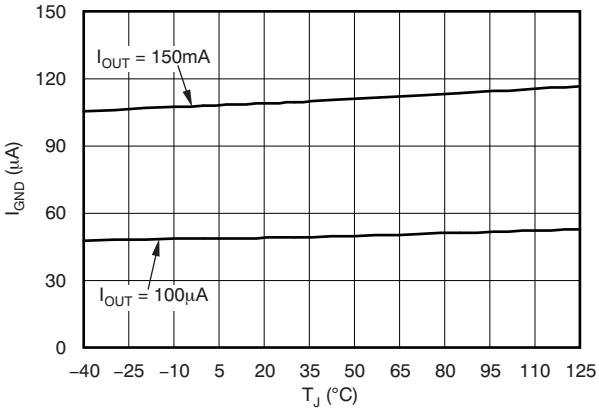


Figure 12.

GROUND PIN CURRENT vs TEMPERATURE (DISABLED)

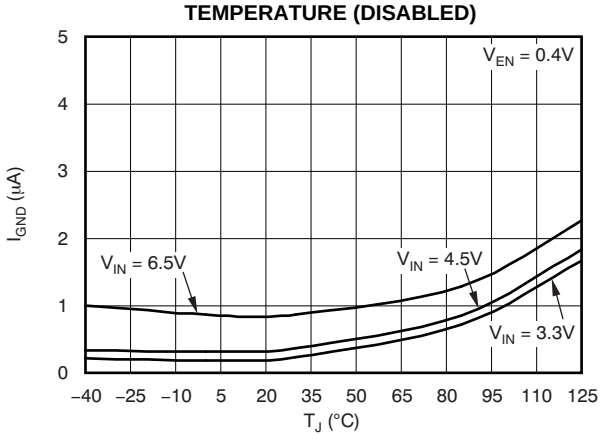


Figure 13.

CURRENT LIMIT vs INPUT VOLTAGE

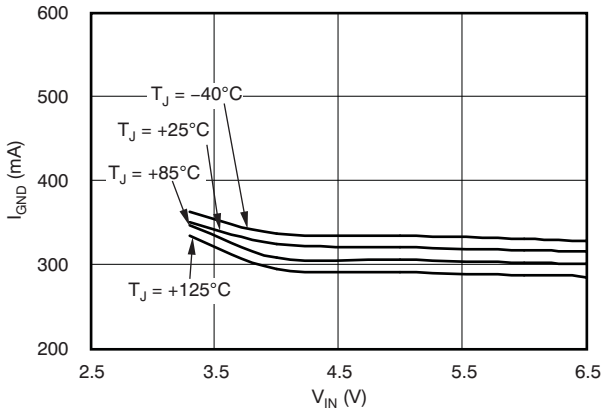


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.5V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{IN}, C_{OUT} = 1.0μF, C_{NR} = 0.01μF, unless otherwise noted. For TPS71701, V_{OUT} = 2.8V.
Typical values are at T_J = +25°C.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1V)

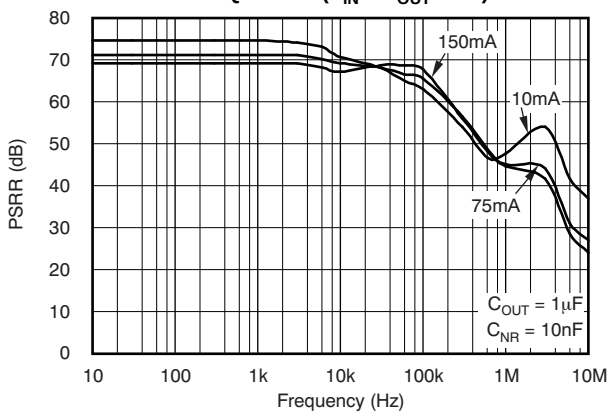


Figure 15.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.5V)

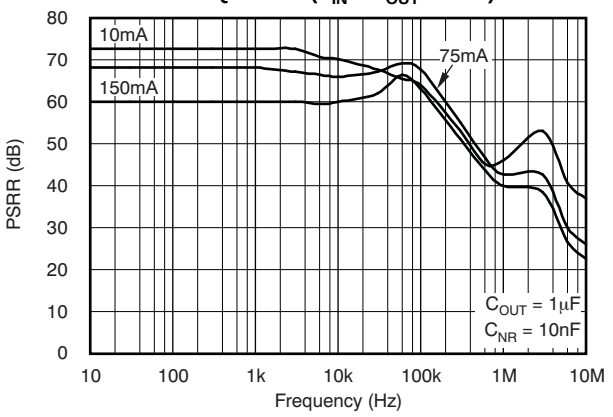


Figure 16.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.25V)

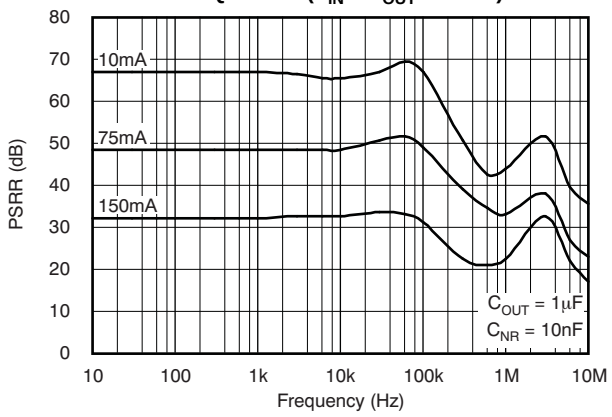


Figure 17.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1V)

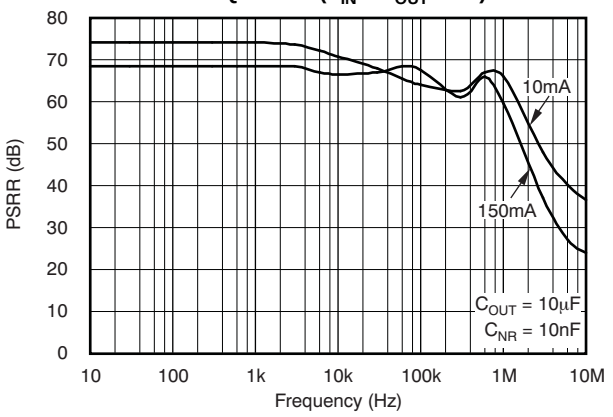


Figure 18.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.25V)

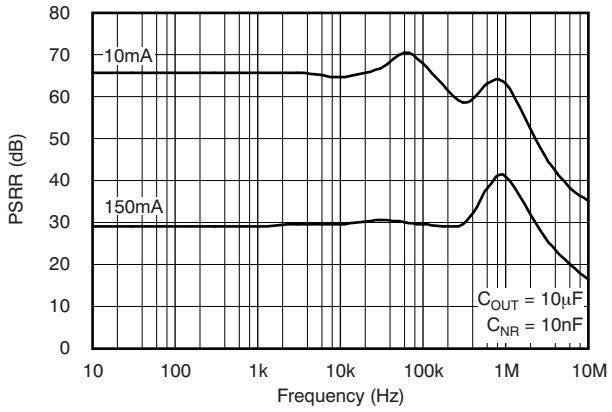


Figure 19.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1V)

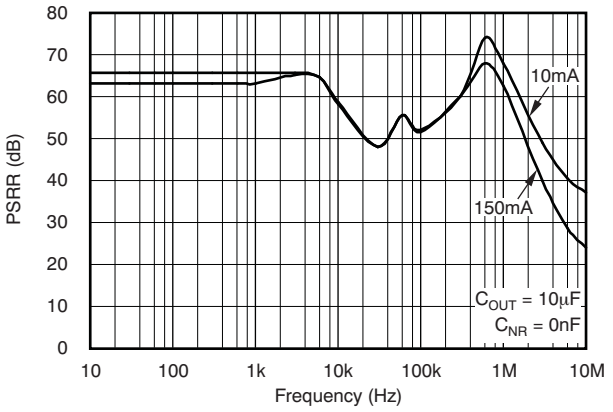


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.5V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{IN}, C_{OUT} = 1.0μF, C_{NR} = 0.01μF, unless otherwise noted. For TPS71701, V_{OUT} = 2.8V. Typical values are at T_J = +25°C.

POWER-SUPPLY RIPPLE REJECTION vs (V_{IN} – V_{OUT})

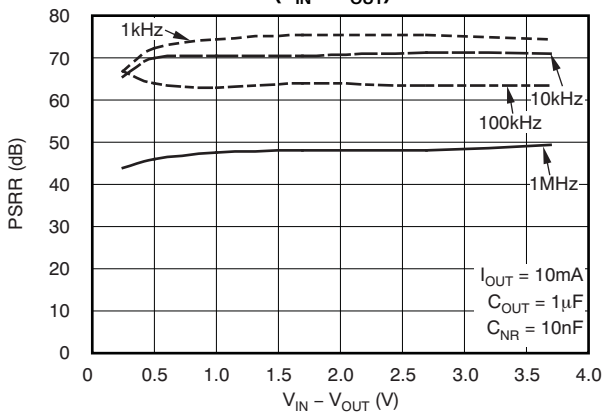


Figure 21.

POWER-SUPPLY RIPPLE REJECTION vs (V_{IN} – V_{OUT})

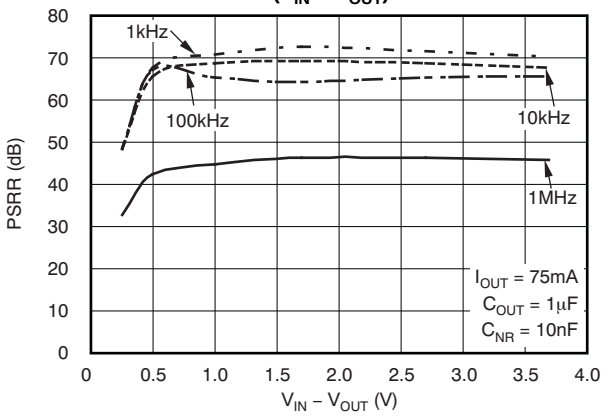


Figure 22.

POWER-SUPPLY RIPPLE REJECTION vs (V_{IN} – V_{OUT})

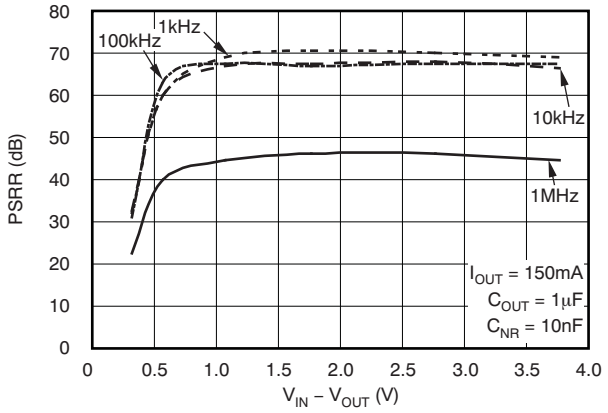


Figure 23.

OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CURRENT

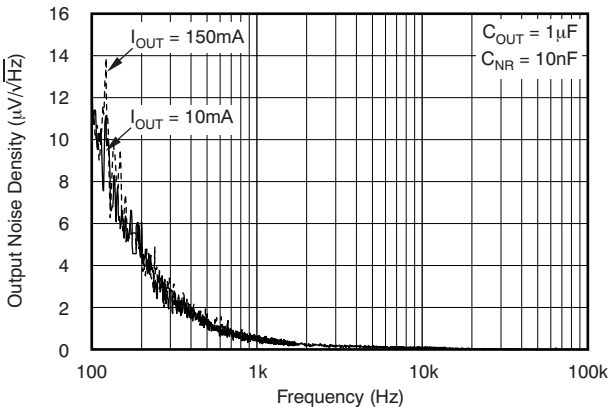


Figure 24.

OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT CAPACITANCE

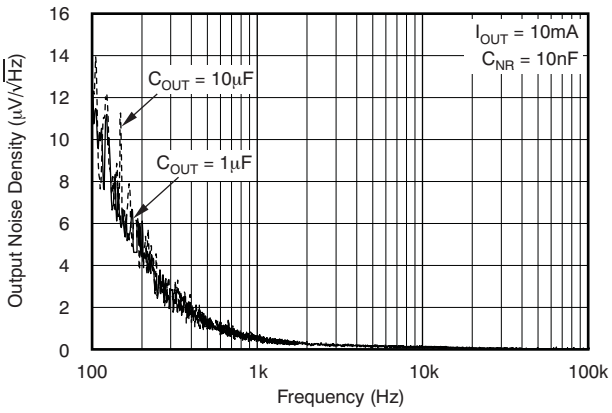


Figure 25.

OUTPUT SPECTRAL NOISE DENSITY vs NOISE REDUCTION

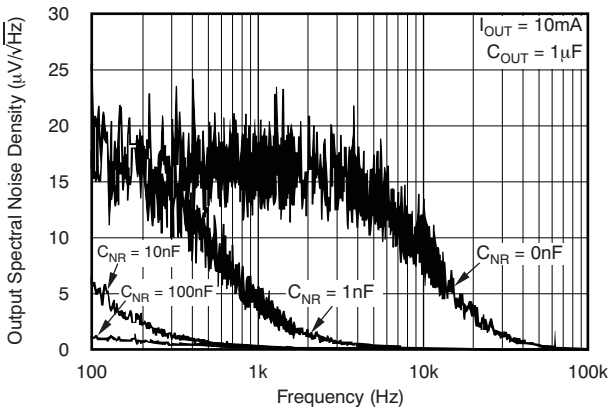


Figure 26.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.5V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{IN}, C_{OUT} = 1.0µF, C_{NR} = 0.01µF, unless otherwise noted. For TPS71701, V_{OUT} = 2.8V. Typical values are at T_J = +25°C.

TOTAL OUTPUT NOISE vs NOISE REDUCTION

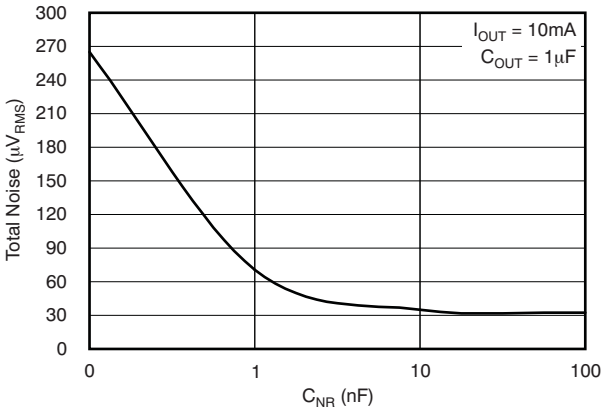


Figure 27.

TOTAL OUTPUT NOISE vs OUTPUT CAPACITANCE

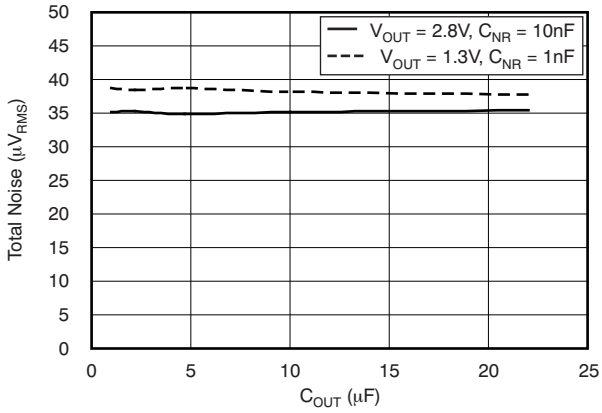


Figure 28.

LINE TRANSIENT RESPONSE

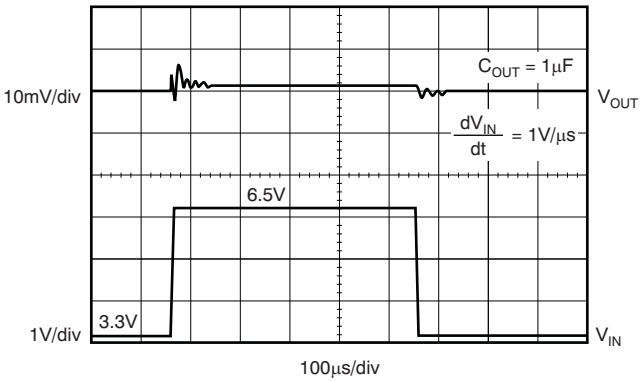


Figure 29.

LOAD TRANSIENT RESPONSE

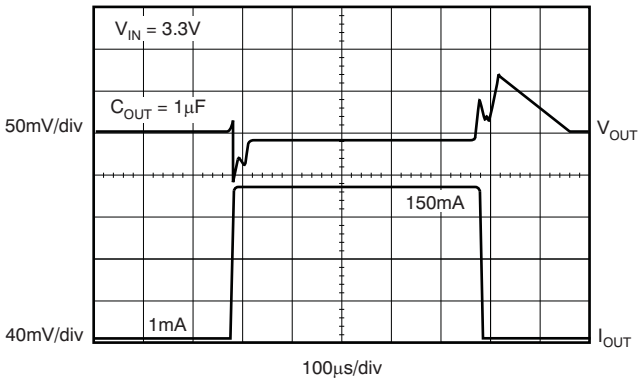


Figure 30.

TURN-ON RESPONSE

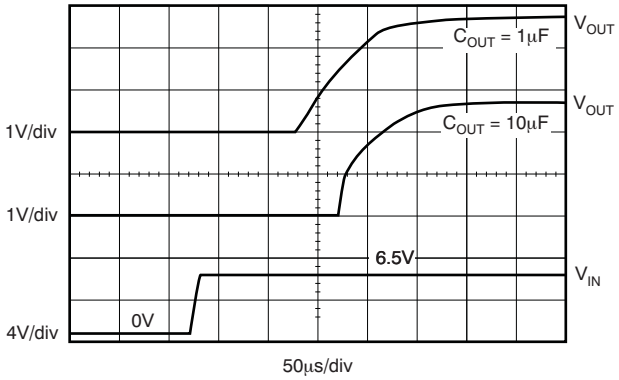


Figure 31.

POWER-UP/POWER-DOWN

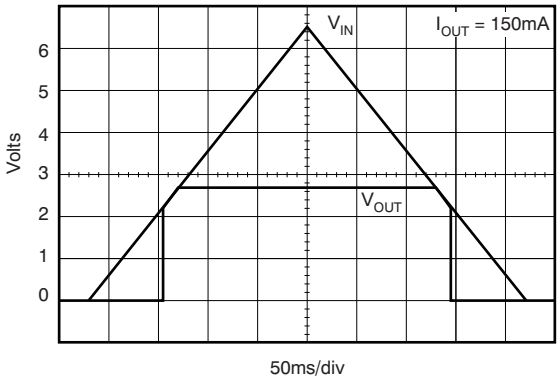


Figure 32.

APPLICATION INFORMATION

The TPS717xx belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1MHz) at very low headroom (V_{IN} – V_{OUT}). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor. These features, combined with low noise, enable, low ground pin current, and ultra-small packaging, make this part ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

Figure 33 shows the basic circuit connections for the fixed voltage options. Figure 34 gives the connections for the adjustable output version (TPS71701). **Note that the NR pin is not available on the adjustable version**.

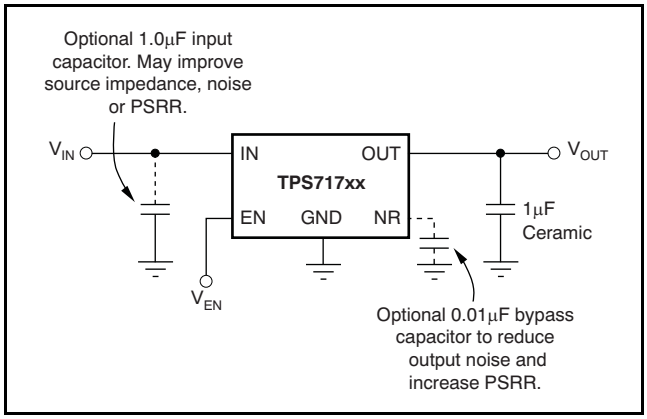


Figure 33. Typical Application Circuit (Fixed Voltage Versions)

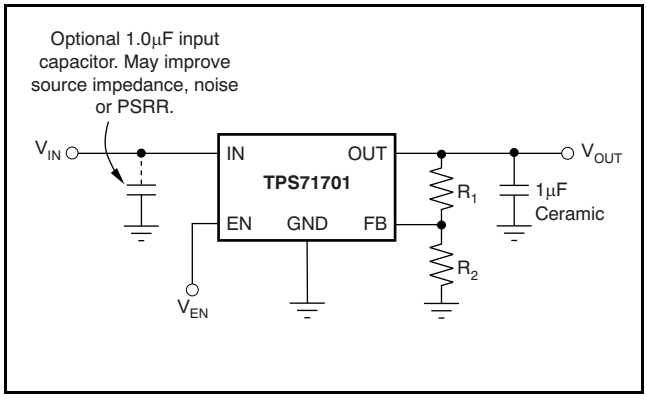


Figure 34. Typical Application Circuit (Adjustable Voltage Version)

For the adjustable version (TPS71701), the NR pin is replaced with a feedback (FB) pin. The voltage on this pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 1:

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.800,\ R_2 \sim 320k\Omega \quad (1)$$

The value of R_2 directly impacts the stability of the device and should be chosen at approximately 160kΩ or 320kΩ. Sample resistor values for common output voltages are shown in Table 2.

Table 2. Sample 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.0	80.6kΩ	324kΩ
1.2	162kΩ	324kΩ
1.5	294kΩ	332kΩ
1.8	402kΩ	324kΩ
2.5	665kΩ	316kΩ
3.3	1.02MΩ	324kΩ
5.0	1.74MΩ	332kΩ

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS717xx is designed to be stable with standard ceramic capacitors of values 1.0µF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be <1.0Ω.

The TPS717xx implements an innovative internal compensation circuit that does not require a feedback capacitor across R_2 for stability. A feedback capacitor should not be used for this device.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS717xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01µF (minimum) noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2.5µA of divider current has the same noise performance as a fixed voltage version.

Equation 2 approximates the total noise referred to the feedback point (FB pin) when C_{NR} = 0.01µF, total noise is approximately given by Equation 2:

$$V_N = 11.5 \frac{\mu V_{RMS}}{V} \times V_{OUT} \quad (2)$$

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS717xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS717xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS717xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 21 through Figure 23 in the Typical Characteristics section.

Startup

Fixed voltage versions of the TPS717xx use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see Functional Block Diagrams, Figure 1). This circuit allows the combination of very low output noise and fast start-up times. The NR pin is high impedance, so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup will be somewhat slower. Refer to Figure 31 in the Typical Characteristics section. The quick-start switch is closed for approximately 135µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01µF or smaller capacitor should be used.

For output voltages below 1.6V, a voltage divider on the bandgap reference voltage is employed to optimize output regulation performance for lower output voltages. This configuration results in an additional resistor in the quick-start path and combined with the noise reduction capacitor (C_{NR}) results in slower start-up times for output voltages below 1.6V.

Equation 3 approximates the start-up time as a function of C_{NR} for output voltages below 1.6V:

$$t_{START} = 160\mu s + \left(540 \frac{\mu s}{nF} \times C_{NR}nF\right)\mu s \quad (3)$$

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Under-Voltage Lock-Out (UVLO)

The TPS717xx utilizes an under-voltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50µs duration.

Minimum Load

The TPS717xx is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS717xx employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS717xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS717xx into thermal shutdown will degrade device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Package Mounting

Solder pad footprint recommendations for the TPS717xx are available from the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS71701DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71701DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71701DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71701DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71709DSER	ACTIVE	SON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71709DSERG4	ACTIVE	SON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71709DSET	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71709DSETG4	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71710DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71710DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71710DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71710DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71710DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71710DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71711DCKR	PREVIEW	SC70	DCK	5	3000	TBD	Call TI	Call TI
TPS71711DCKT	PREVIEW	SC70	DCK	5	250	TBD	Call TI	Call TI
TPS71712DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71712DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71712DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71712DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71713DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71713DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71713DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71713DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71715DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71715DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TPS71715DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71715DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DSER	ACTIVE	SON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DSERG4	ACTIVE	SON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DSET	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71718DSETG4	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71719DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71719DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71719DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71719DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71725DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71725DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71725DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71725DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71726DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71726DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71726DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71726DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71727DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71727DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71727DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS71727DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS717285DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS717285DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS717285DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS717285DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71728DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71728DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71728DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71728DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71728DSER	ACTIVE	SON	DSE	6	3000	TBD	Call TI	Call TI
TPS71728DSET	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71728DSETG4	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71729DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71729DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71729DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71729DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71730DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71730DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71730DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71730DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DRVRG4	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS71733DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DRVTG4	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DSER	ACTIVE	SON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DSERG4	ACTIVE	SON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DSET	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS71733DSETG4	ACTIVE	SON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

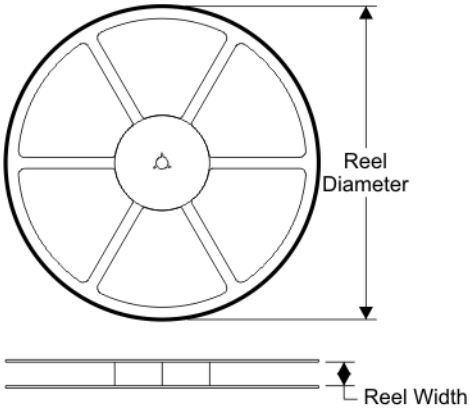
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

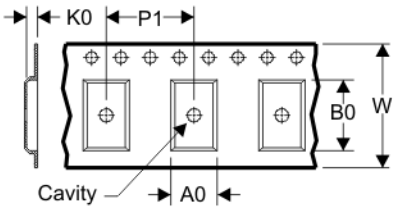
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

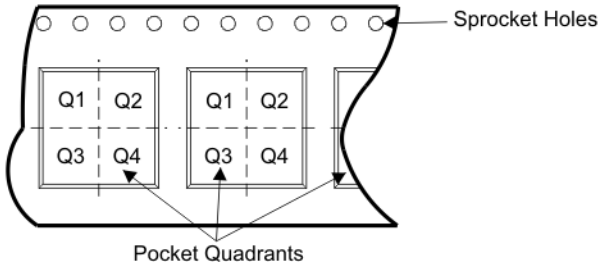


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

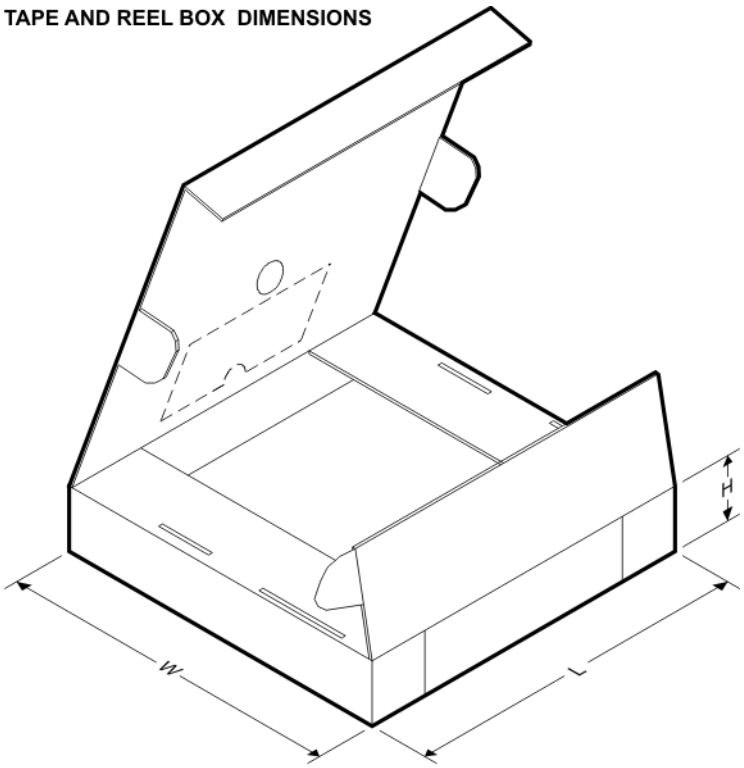
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71701DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71701DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71709DSER	DSE	6	SITE 48	179	8	1.8	1.8	1.0	4	8	Q2
TPS71709DSET	DSE	6	SITE 48	179	8	1.8	1.8	1.0	4	8	Q2
TPS71710DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71710DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71710DRVR	DRV	6	SITE 48	179	8	2.2	2.2	1.2	4	8	Q2
TPS71710DRVT	DRV	6	SITE 48	179	8	2.2	2.2	1.2	4	8	Q2
TPS71712DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71712DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71713DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71713DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71715DCKR	DCK	5	SITE 48	179	8	2.2	2.5	1.2	4	8	Q3
TPS71715DCKT	DCK	5	SITE 48	179	8	2.2	2.5	1.2	4	8	Q3
TPS71718DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71718DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71718DSER	DSE	6	SITE 48	179	8	1.8	1.8	1.0	4	8	Q2
TPS71718DSET	DSE	6	SITE 48	179	8	1.8	1.8	1.0	4	8	Q2
TPS71719DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71719DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71725DCKR	DCK	5	SITE 48	179	8	2.2	2.5	1.2	4	8	Q3
TPS71725DCKT	DCK	5	SITE 48	179	8	2.2	2.5	1.2	4	8	Q3
TPS71726DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71726DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71727DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71727DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS717285DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS717285DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71728DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71728DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71728DSET	DSE	6	SITE 48	179	8	1.8	1.8	1.0	4	8	Q2
TPS71729DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71729DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71730DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71730DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71733DCKR	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71733DCKT	DCK	5	SITE 48	179	8	2.25	2.4	1.22	4	8	Q3
TPS71733DRVR	DRV	6	SITE 48	179	8	2.2	2.2	1.2	4	8	Q2
TPS71733DRVT	DRV	6	SITE 48	179	8	2.2	2.2	1.2	4	8	Q2
TPS71733DSER	DSE	6	SITE 48	179	8	1.8	1.8	1.0	4	8	Q2
TPS71733DSET	DSE	6	SITE 48	179	8	1.8	1.8	1.0	4	8	Q2

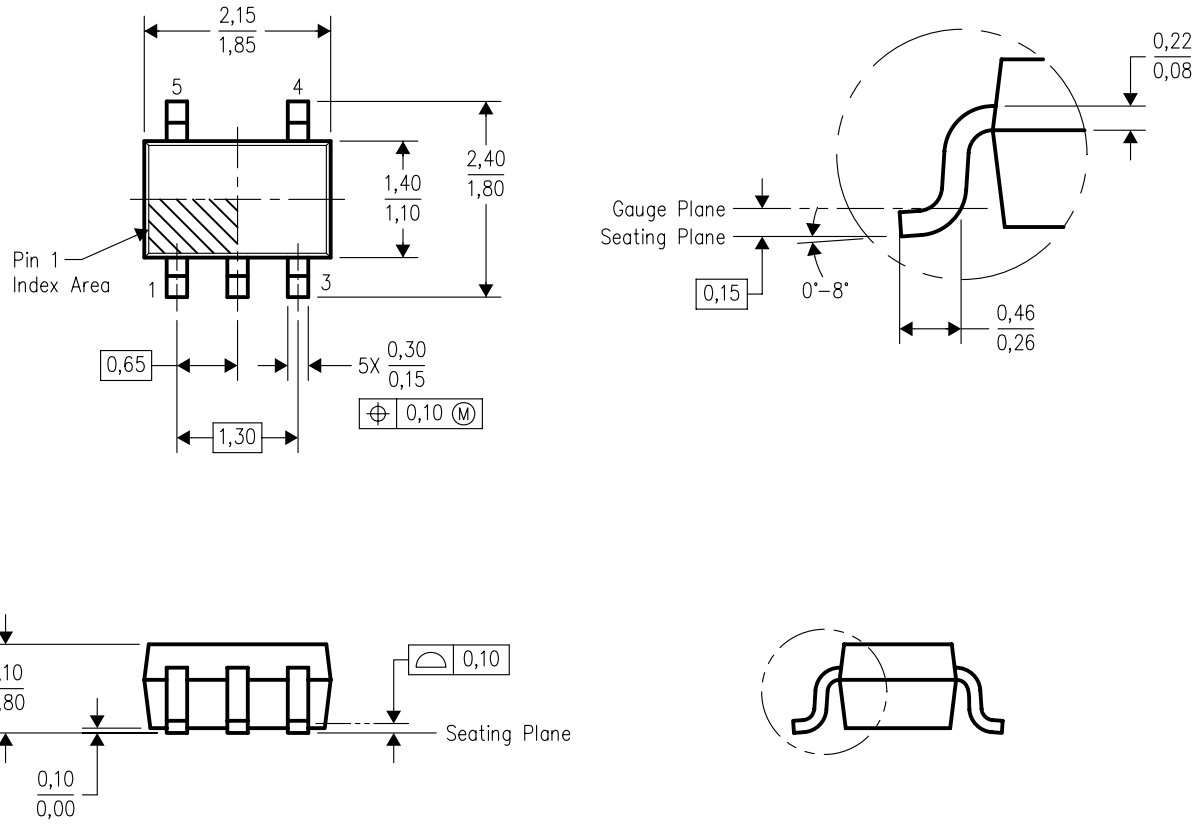
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS71701DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71701DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71709DSER	DSE	6	SITE 48	195.0	200.0	45.0
TPS71709DSET	DSE	6	SITE 48	195.0	200.0	45.0
TPS71710DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71710DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71710DRVR	DRV	6	SITE 48	195.0	200.0	45.0
TPS71710DRVT	DRV	6	SITE 48	195.0	200.0	45.0
TPS71712DCKR	DCK	5	SITE 48	0.0	0.0	0.0
TPS71712DCKT	DCK	5	SITE 48	0.0	0.0	0.0
TPS71713DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71713DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71715DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71715DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71718DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71718DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71718DSER	DSE	6	SITE 48	195.0	200.0	45.0
TPS71718DSET	DSE	6	SITE 48	195.0	200.0	45.0
TPS71719DCKR	DCK	5	SITE 48	0.0	0.0	0.0
TPS71719DCKT	DCK	5	SITE 48	0.0	0.0	0.0
TPS71725DCKR	DCK	5	SITE 48	195.0	200.0	45.0

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS71725DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71726DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71726DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71727DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71727DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS717285DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS717285DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71728DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71728DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71728DSET	DSE	6	SITE 48	195.0	200.0	45.0
TPS71729DCKR	DCK	5	SITE 48	0.0	0.0	0.0
TPS71729DCKT	DCK	5	SITE 48	0.0	0.0	0.0
TPS71730DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71730DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71733DCKR	DCK	5	SITE 48	195.0	200.0	45.0
TPS71733DCKT	DCK	5	SITE 48	195.0	200.0	45.0
TPS71733DRVR	DRV	6	SITE 48	195.0	200.0	45.0
TPS71733DRVT	DRV	6	SITE 48	195.0	200.0	45.0
TPS71733DSER	DSE	6	SITE 48	195.0	200.0	45.0
TPS71733DSET	DSE	6	SITE 48	195.0	200.0	45.0

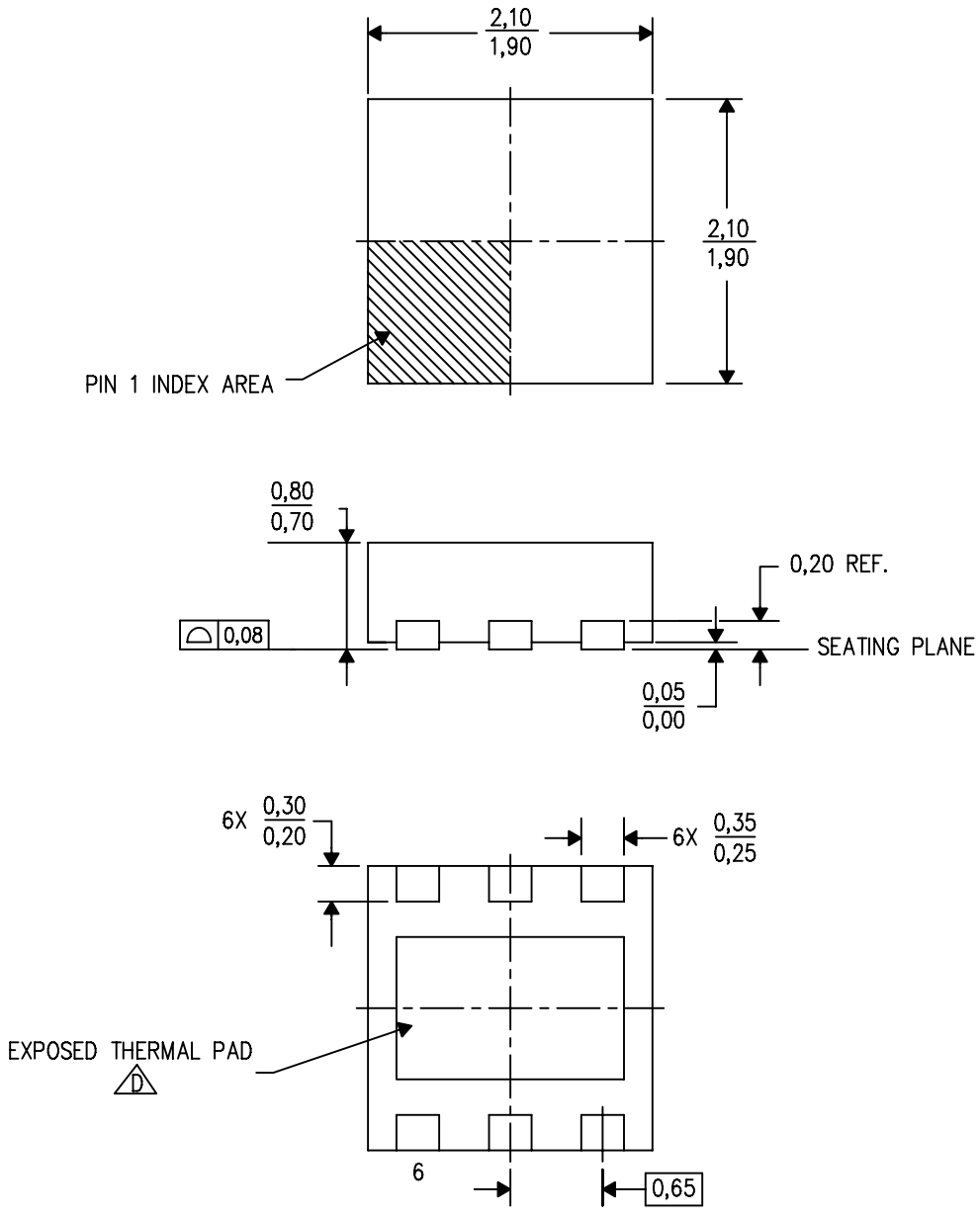
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DRV (S–PDSO–N6) PLASTIC SMALL OUTLINE



4206925/D 12/07

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

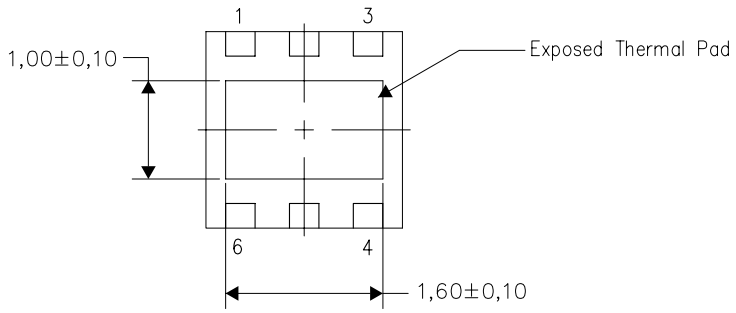
DRV (S–PDSO–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

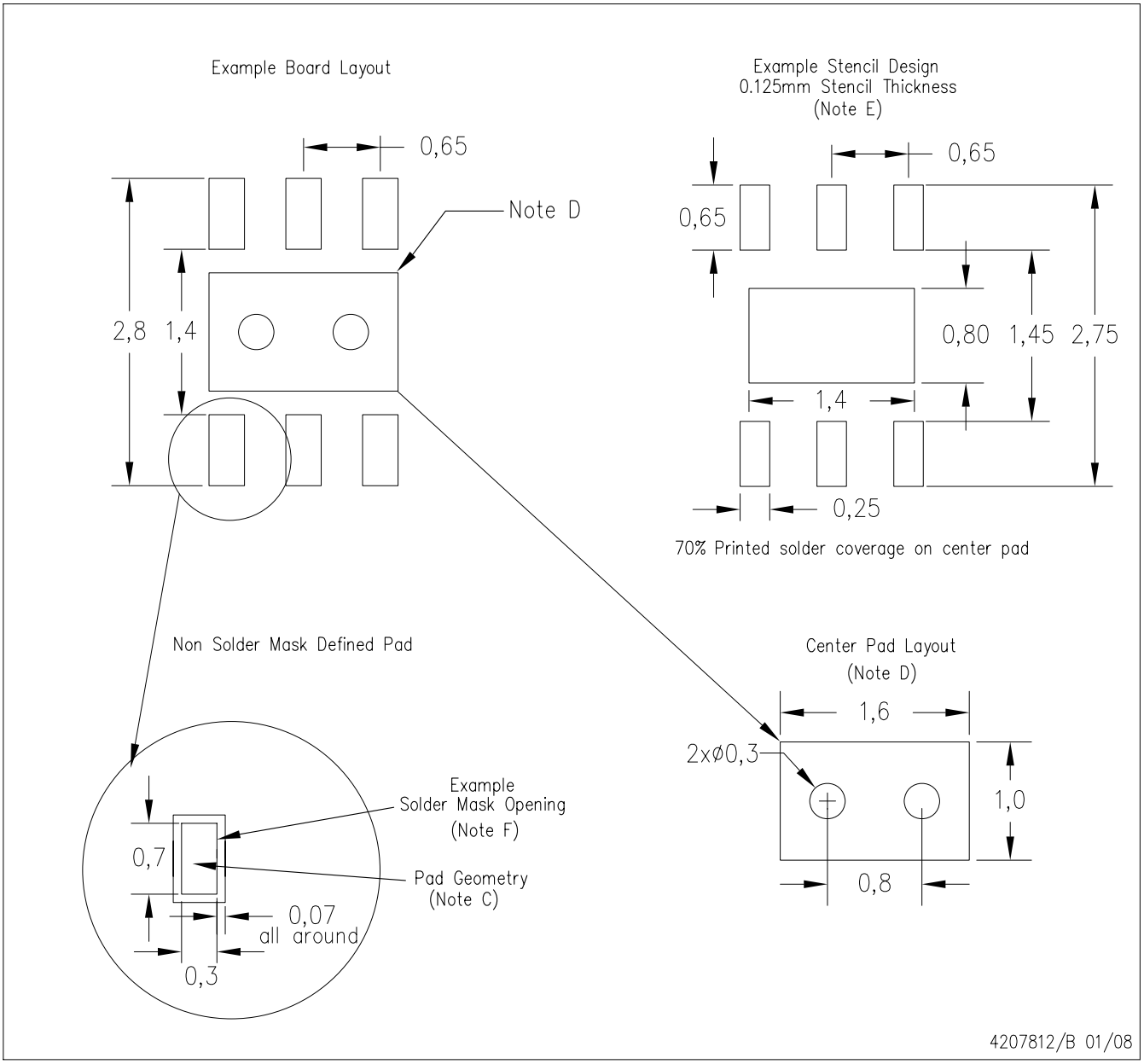


Bottom View

NOTE: All linear dimensions are in millimeters

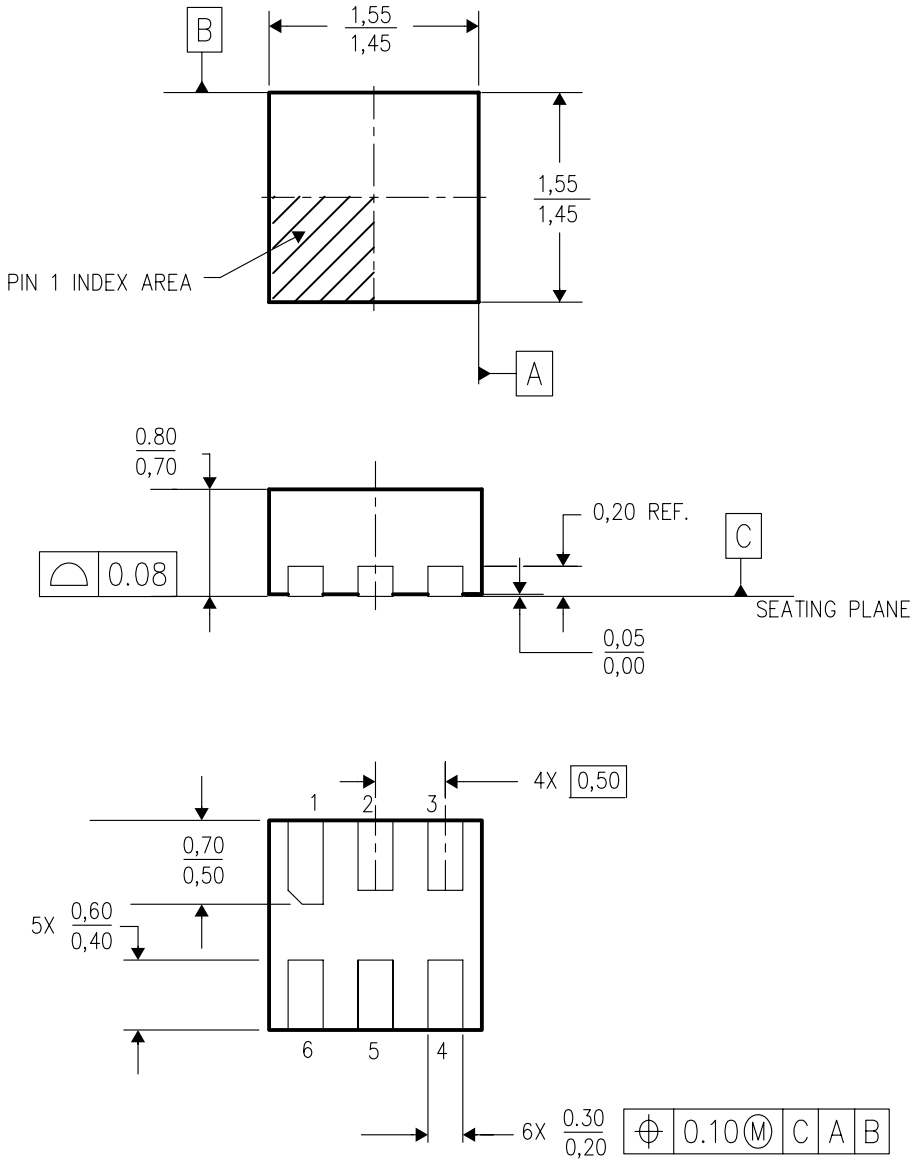
Exposed Thermal Pad Dimensions

DRV (S–PDSO–N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

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RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
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