LXP600A, LXP602 and LXP604

Low-Jitter Clock Adapters (CLADs)

General Description

The LXP600A, LXP602 and LXP604 Clock Adapters (CLADs) incorporate Level One's patented frequency conversion circuitry. The LXP600A and LXP602 convert a 1.544 MHz input clock to a 2.048 MHz output clock, or vice versa. The LXP604 converts between 1.544 MHz and 4.096 MHz. Each CLAD produces two different high frequency output (HFO) clocks for applications which require a higher-than-baud rate backplane or system clock.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock (CLKO) is as accurate as the input clock (CLKI), and the two clocks are frequency-locked together. When an input frame sync pulse (FSI) is provided, the CLAD also phase-locks CLKI and CLKO together, and locks the output frame sync pulse ($\overline{\text{FSO}}$) to 600.

Features

- Generates a 1.544 MHz clock and its frame sync from a 2.048 MHz or 4.096 MHz clock and its frame sync, or vice versa
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and ITU Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Available in 8-pin plastic DIP
- Pin-selectable operation mode
- Advanced CMOS device requires only a single +5 V power supply

Frequency Conversion

CLAD	CLKI	CLKO	HFO
LXP600A	1.544	2.048	6.144
	2.048	1.544	6.178
LXP602	1.544	2.048	8.192
	2.048	1.544	6.176
LXP604	1.544	4.096	8.192
	4.096	1.544	6.176

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, PBX, etc.
- Conversion between 2.048 MHz or 4.096 MHz backplane rates and 1.544 MHz T1 clock rate
- Conversion between North American and International standards (T1/E1 Converter)

LXT600 Block Diagram

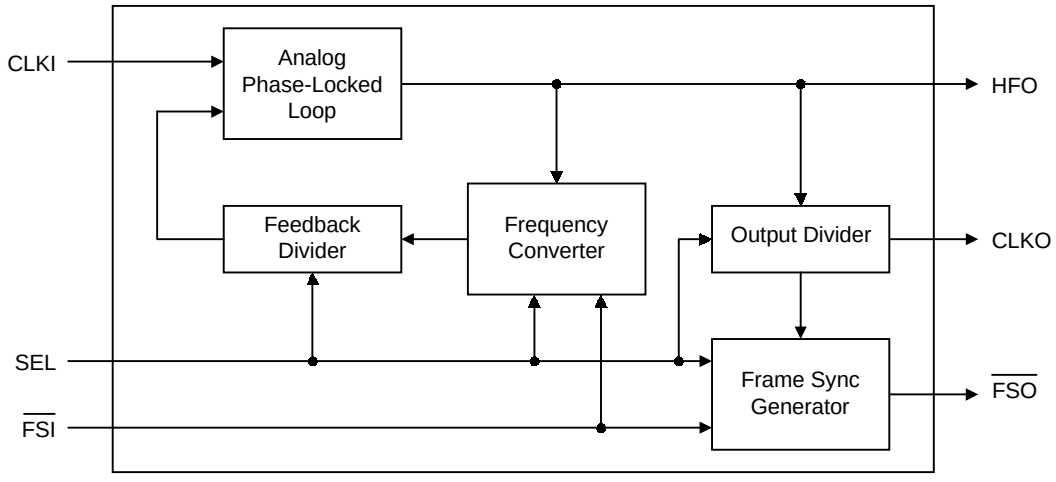


Figure 1: LXT600 Pin Assignments

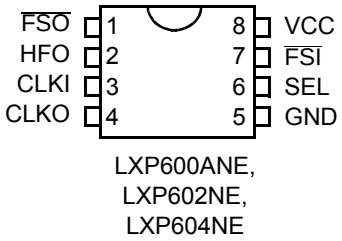


Table 1: Pin Descriptions

Pin #	Sym	I/O	Description
1	FSO	O	**Frame Sync Output.** Frame synchronization output at 8 kHz. $\overline{\text{FSO}}$ is synced to CLKO and to $\overline{\text{FSI}}$ (if $\overline{\text{FSI}}$ is provided).
2	HFO	O	**High Frequency Output.** HFO is used to derive CLKO. HFO can also clock external devices. HFO is always a multiple of CLKO (CLKO x2, x3, or x4). Actual frequencies are determined by device, CLKI and CLKO frequencies and Mode Select (SEL) input, as listed in Table 2.
3	CLKI	I	**Clock Input.** Input clock (1.544, 2.048 or 4.096 MHz) to be converted.
4	CLKO	O	**Clock Output.** Output clock (1.544, 2.048 or 4.096 MHz) derived from CLKI.
5	GND	–	**Ground.**
6	SEL	I	**Mode Select.** controls frequency conversion as listed in Table 2. When SEL = High, higher frequency CLKI (2.048 for LXP600A and LXP602, or 4.096 MHz for LXP604) is converted to 1.544 MHz CLKO. When SEL = Low, 1.544 MHz CLKI is converted to higher frequency CLKO (2.048 for LXP600A and LXP602, or 4.096 MHz for LXP604).
7	$\overline{\text{FSI}}$	I	**Frame Sync Input.** 8 kHz frame synchronization pulse. Tie High or Low if not used.
8	VCC	–	**Power Supply.** +5 V power supply input.

FUNCTIONAL DESCRIPTION

The CLADs convert an input clock (CLKI) at a particular frequency to an output clock (CLKO) at a different frequency. They also produce a frame sync output ($\overline{FSO}$) and a high frequency output (HFO) clock. The HFO is a multiple (2x, 3x, or 4x) of CLKO. The HFO and CLKI/CLKO conversion frequencies are different for each device, and controlled by the Mode Select input as listed in Table 2.

The LXP600A and LXP602 convert between 1.544 MHz and 2.048 MHz. When converting from 2.048 MHz to 1.544 MHz, both CLADs produce a 6.176 MHz HFO. However, when converting from 1.544 MHz to 2.048 MHz, the LXP600A produces a 6.144 MHz HFO and the LXP602 produces an 8.192 MHz HFO.

The LXP604 converts between 1.544 MHz and 4.096 MHz. When converting from 4.096 to 1.544 MHz the LXP604 HFO is 6.176. When converting from 1.544 MHz to 4.096 MHz, the LXP604 produces an 8.192 MHz HFO.

Mode Select

The Mode Select (SEL) input controls whether the device converts to a higher or lower frequency as described below:

- 2.048 or 4.096 to 1.544 MHz: To produce a 1.544 MHz output clock from a 2.048 MHz or 4.096 MHz input clock, SEL must be set High. In this mode HFO = 6.176 MHz for all CLADs.
- 1.544 to 2.048 MHz or 4.096 MHz: To produce a 2.048 MHz or 4.096 MHz output clock from a 1.544 MHz input clock, SEL must be set Low. In this mode the LXP600A HFO = 6.144 MHz, and the LXP602 and LXP604 HFO = 8.192 MHz.

In both frequency modes, CLKO is frequency-locked to CLKI. When $\overline{FSI}$ is applied, CLKO and CLKI are also phase- locked with $\overline{FSO}$ and $\overline{FSI}$ synchronized. Refer to Test Specifications for detailed timing.

When $\overline{FSI}$ is first asserted, the CLKI and CLKO rising edges will be aligned within a maximum of 500 ms.

If $\overline{FSI}$ is not provided, pin 7 should be tied High or Low. CLKO and $\overline{FSO}$ are still generated with the CLKO frequency-locked to CLKI.

Output Jitter

2.048 MHz or 4.096 MHz to 1.544 MHz

In this mode of operation, the CLADs meet the output jitter requirements of AT&T Publication 62411. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.020 UI pp with no bandlimiting, 0.010 UI pp over the range of 10 Hz to 40 kHz, and 0.012 UI pp in the 8 - 40 kHz band.

1.544 MHz to 2.048 MHz or 4.096 MHz

In this mode of operation, the CLADs meet the output jitter requirements of CCITT Recommendation G.823. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.035 UI pp over the range of 20 Hz to 100 kHz, and 0.025 UI pp in the 18 - 100 kHz band.

Jitter Transfer

The CLADs are sensitive to jitter on the input clock in certain frequency bands. The jitter transfer curve is determined by the frequency and amplitude of the input jitter. Test Specification Figures 4 and 5 show nominal jitter transfer measured in nanoseconds. These figures graph output jitter (less intrinsic jitter) divided by input jitter (0.25 UI). Jitter transfer from a 2.048 MHz CLKI to a 1.544 MHz CLKO is shown in Figure 4. In this mode, jitter in the critical 8 kHz band is slightly attenuated while jitter in the 18 - 70 kHz band is transferred with a small net gain. Jitter transfer from a 1.544 MHz CLKI to a 2.048 MHz CLKO is shown in Figure 5. In both modes, with an input jitter level of 0.25 UI, jitter transfer is held below a net gain of 1.110.

(Jitter transfer varies with input jitter. Performance in a specific application should be verified in the actual circuit.)

Table 2: CLAD Frequency Conversions

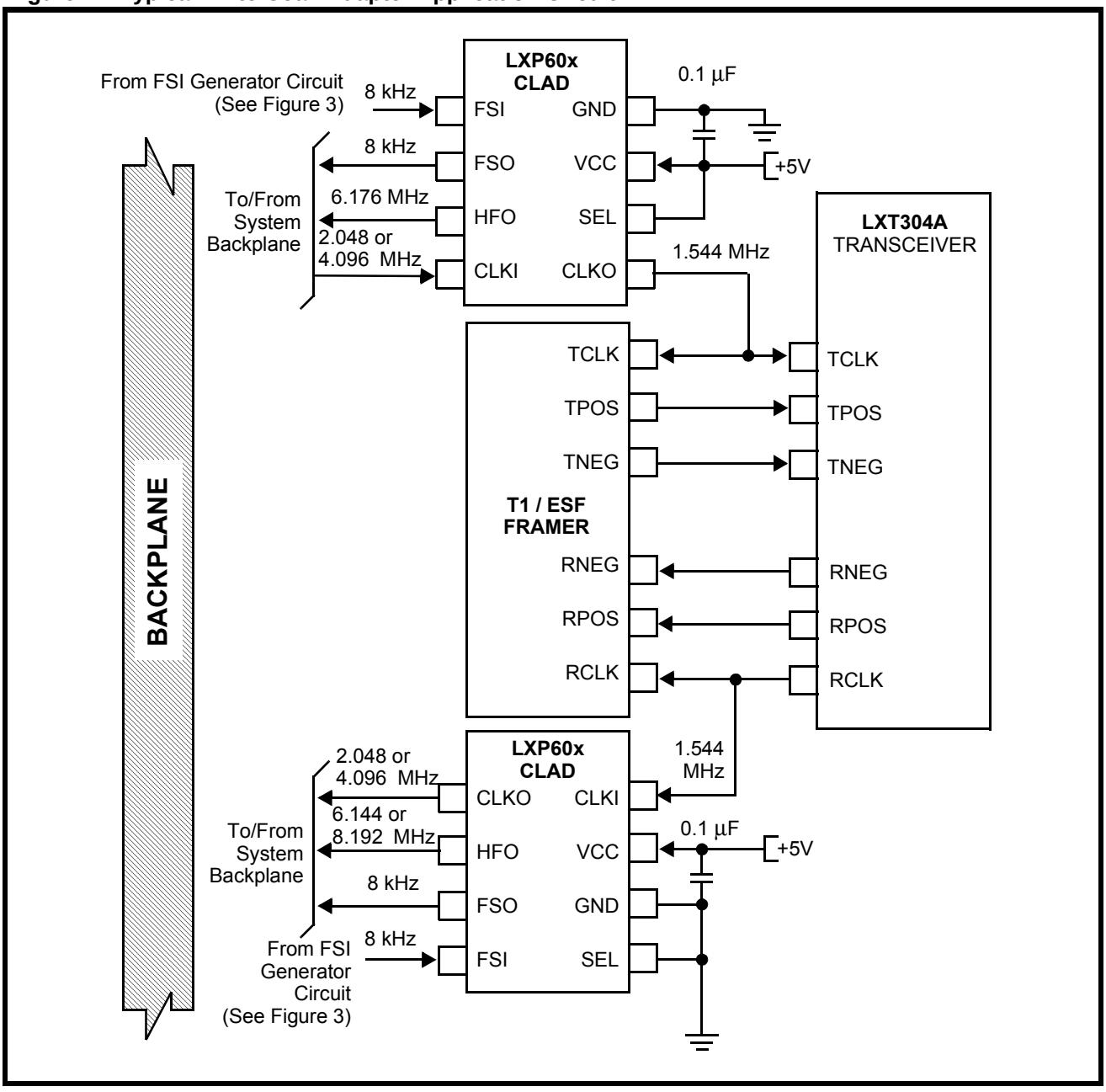
CLAD	CLKI	CLKO	HFO	SEL
LXP600A	1.544 2.048	2.048 1.544	6.144 6.178	0 1
LXP602	1.544 2.048	2.048 1.544	8.192 6.176	0 1
LXP604	1.544 4.096	4.096 1.544	8.192 6.176	0 1

APPLICATION INFORMATION

Power-up

Standard CMOS device precautions apply to the CLAD. Inputs must be applied either simultaneously with or after the power supply VCC. CLAD input signals include CLKI, $\overline{\text{FSI}}$ and SEL. The CLAD internal circuitry takes a maximum of 200 ms to stabilize. There is an additional delay of 500 ms maximum for CLKO to be phase-locked to the incoming clock CLKI during frame synchronization FSI.

Figure 2: Typical TP to Coax Adapter Application Circuit



Power Supply Decoupling and Filtering

The CLADs are designed to meet AT&T Publication 62411 specifications for jitter in the range from 10 Hz to 100 kHz. Proper power supply decoupling is critical for meeting these specifications. As shown in Figure 2, a typical application with a pair of CLADs for backplane frequency conversion, a standard 0.1 µF bypass capacitor is recommended.

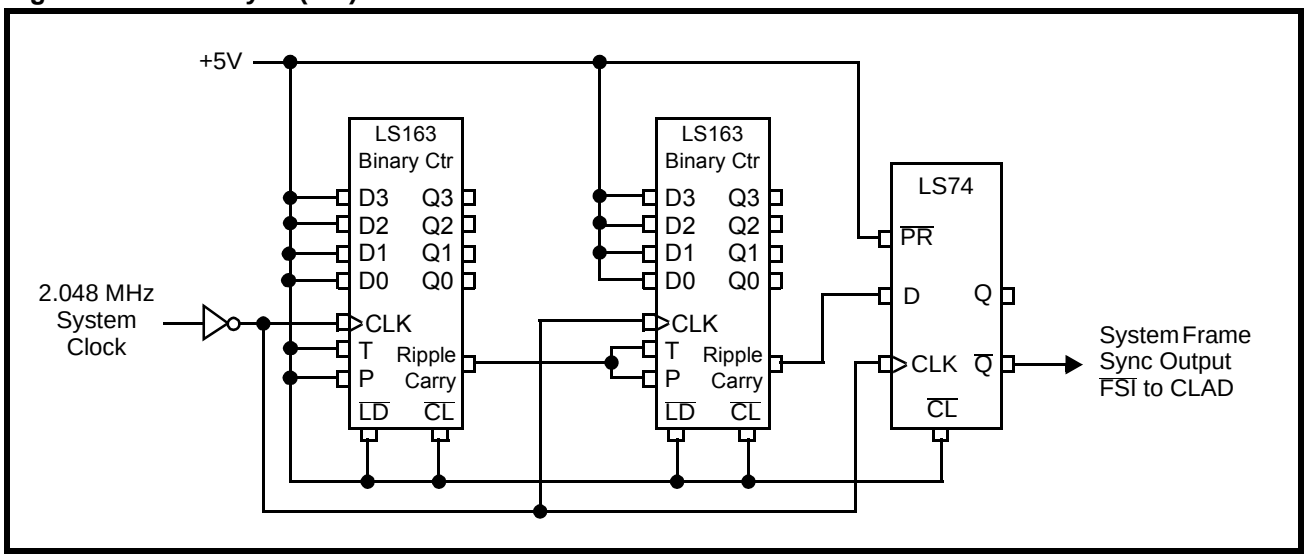
The CLADs are monolithic silicon devices which incorporate both analog and digital circuits. CLAD application circuit design may require closer attention to power supply filtering and bypassing than required for strictly digital devices.

Switching power supplies which operate below 100 kHz may produce noise spikes which can affect the analog sections of the CLAD. These spikes should be filtered with an RC network at the CLAD VCC pin.

Frame Sync Generation

A frame sync pulse is required to synchronize the input and output clocks. If a frame sync pulse is not provided on the backplane, one can be generated from the existing 2.048 MHz backplane clock. A typical FSI generation circuit is shown in Figure 3.

Figure 3: Frame Sync (FSI) Generation Circuit



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 8 and Figures 4 through 11 represent the performance specifications of the LXT600 and are guaranteed by test, except where noted by design.

Table 3: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply voltage	RV+, TV+	-0.3	7.0	V
Voltage, any I/O pin	V_{IO}	GND - 0.3	VCC + 0.3	V
Current, any I/O pin[1]	I_{IO}	-10	10	mA
Storage temperature	T_{STG}	-65	+150	ºC
Power dissipation	P_D	–	340	mW

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Transient currents of up to 100 mA will not cause SCR latch-up.

Table 4: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Supply voltage[1]	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}	–	–	8	mA	No TTL loading
	I_{CC}	–	–	14	mA	Full TTL loading
Operating temperature	T_{OP}	-40	–	85	ºC	

1. Voltages with respect to ground unless otherwise specified.

Table 5: Digital Electrical Characteristics (Over Recommended Range)

Parameter	Sym	Min	Max	Units
Input Low voltage	V_{IL}	–	0.8	V
Input High voltage	V_{IH}	2.0	–	V
Output Low voltage (I_{OL} = +1.6 mA)	V_{OL}	–	0.4	V
Output Low voltage (I_{OL} < +10µA)	V_{OL}	–	0.2	V
Output High voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	–	V
Output High voltage (I_{OH} < -10µA)	V_{OH}	4.5	–	V
Input leakage current	I_{LL}	-10	10	µA

Table 6: Output Jitter Specifications

Parameter	Sym	Frequency	Spec[1]	Typ[2]	Max	Units	Test Conditions
Output Jitter on CLKO CLKO=1.544 MHz (All CLADS)	TJ1	No Bandlimiting	0.050	0.010	0.20	UI pp	CLKI=2.048 or 4.096 MHz JI=0 $\overline{FSI}$ applied
		10 Hz to 40 kHz	0.025	0.005	0.010	UI pp	
		8 kHz to 40 kHz	0.025	0.006	0.012	UI pp	
Output Jitter on CLKO CLKO=2.048 Mhz (LXP600A and 602 only)	TJ2	20 Hz to 100 kHz	1.500	0.025	0.035	UI pp	CLKI=1.544 MHz, JI=0 $\overline{FSI}$ applied
		18 kHz to 100 kHz	0.200	0.015	0.025	UI pp	

1. Specifications from AT&T Publication 62411 and ITU Recommendations G.823 (for 1.544 MHz and 2.048 MHz, respectively).
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 4: Nominal Jitter Transfer - 2.048 MHz CLKI to 1.544 MHz CLKO (Input Jitter = 0.25 UI)

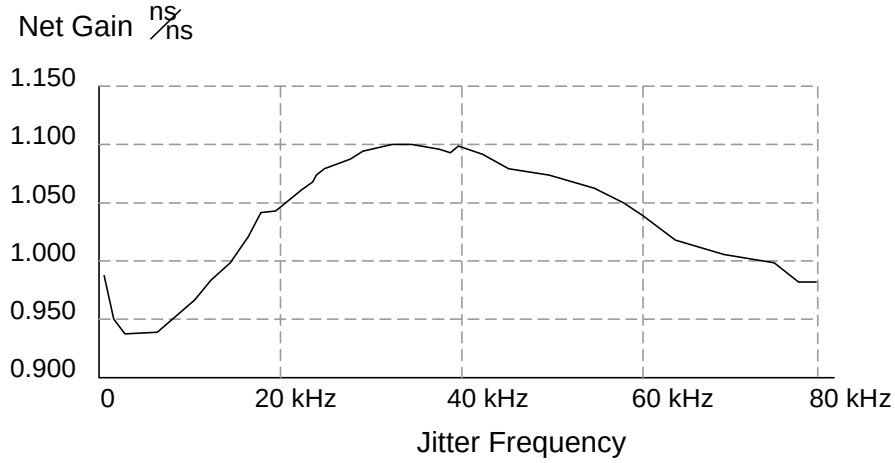


Figure 5: Nominal Jitter Transfer - 1.544 MHz CLKI to 2.048 MHz CLKO (Input Jitter = 0.25 UI)

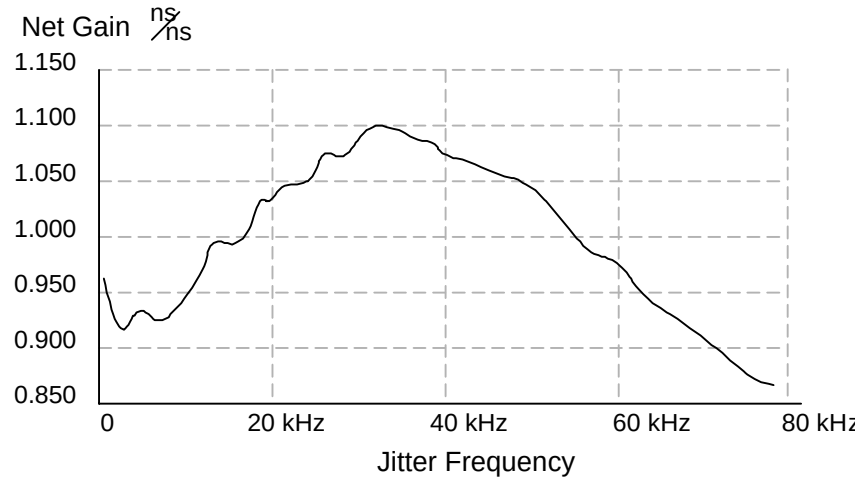


Table 7: Timing Values (see Figure 6)

Parameter	Sym	Minimum	Maximum	Units
Capture range on CLKI	–	±10000	–	ppm
Lock range on CLKI	–	±10000	–	ppm
Input clock duty cycle	–	35	65	%
Rise/fall time on CLKI, $\overline{FSI}$	Trf	–	40	ns
Rise/fall time on CLKO, $\overline{FSO}$, HFO with a 25 pF load	Trf	–	40	ns

Figure 6: Rise and Fall Times

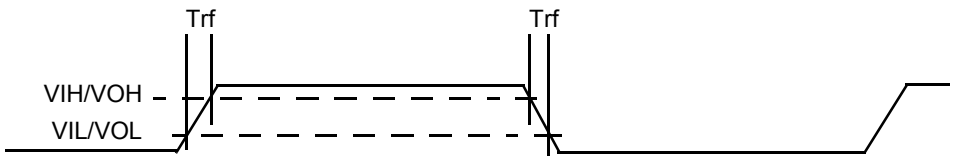


Table 8: Timing Values (see Figures 7 through 11)

Parameter	Sym	Minimum	Typ[1]	Maximum	Units
$\overline{FSI}$ setup time from CLKI rising	Tsui	46	–	–	ns
$\overline{FSI}$/CKLI hold time	Thi	30	–	–	ns
$\overline{FSI}$ pulse width (low)	Twi	76	–	TCLKI[2]	ns
CLKO delay from CLKI	TdC	-15	0	+15	ns
CLKO duty cycle	Cdc	49	–	51	%
$\overline{FSO}$ delay from HFO	TdF	-5	–	30	ns
$\overline{FSO}$ pulse width (low)	TWO	–	–	TCLKO[3]	ns
CLKO delay from HFO	TdH	-15	–	+15	ns

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. TCLKI is the period of CLKI.
3. TCLKO is the period of CLKO.

Figure 7: LXP600A and LXP602 High to Low Frequency Conversion Frame Sync Alignment)

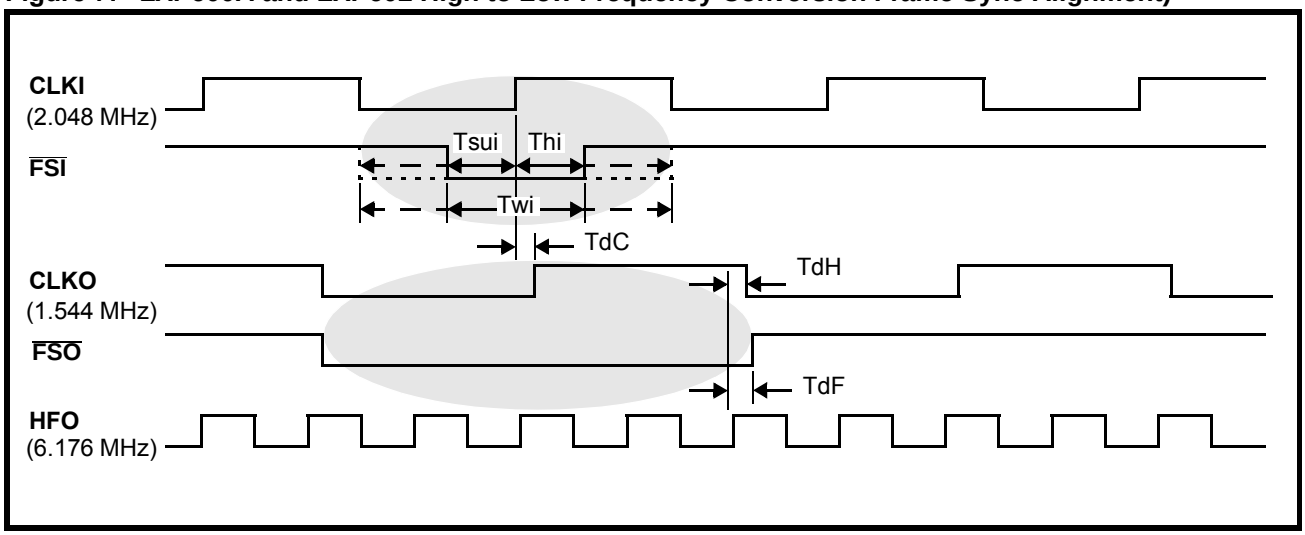


Figure 8: LXP604 High to Low Frequency Conversion Frame Sync Alignment)

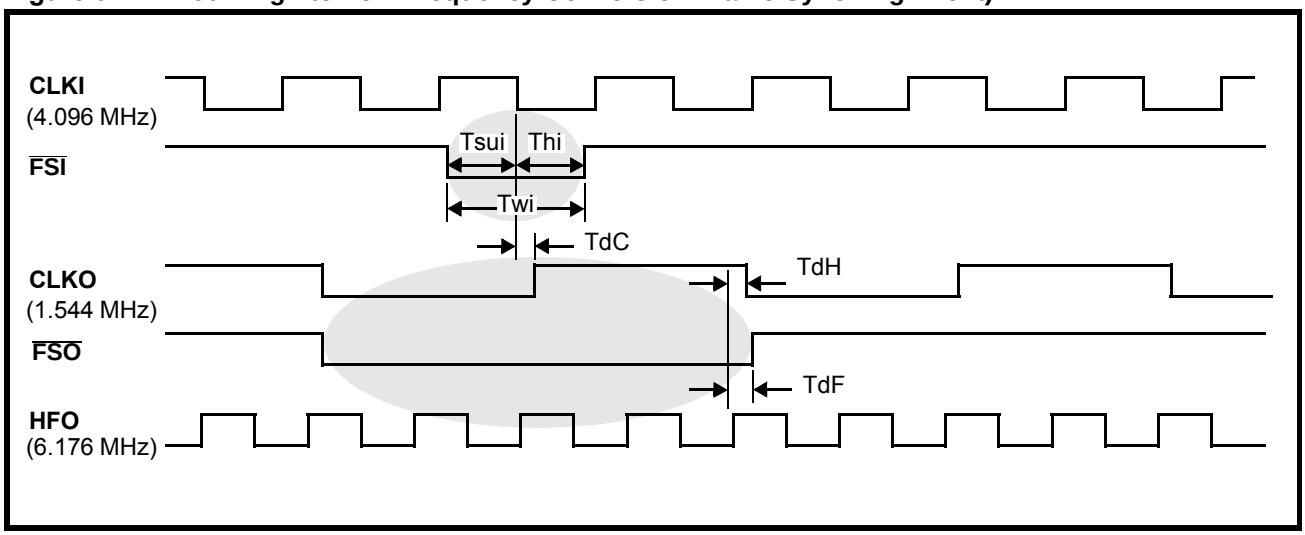


Figure 9: LXP600A Low to High Frequency Conversion Frame Sync Alignment

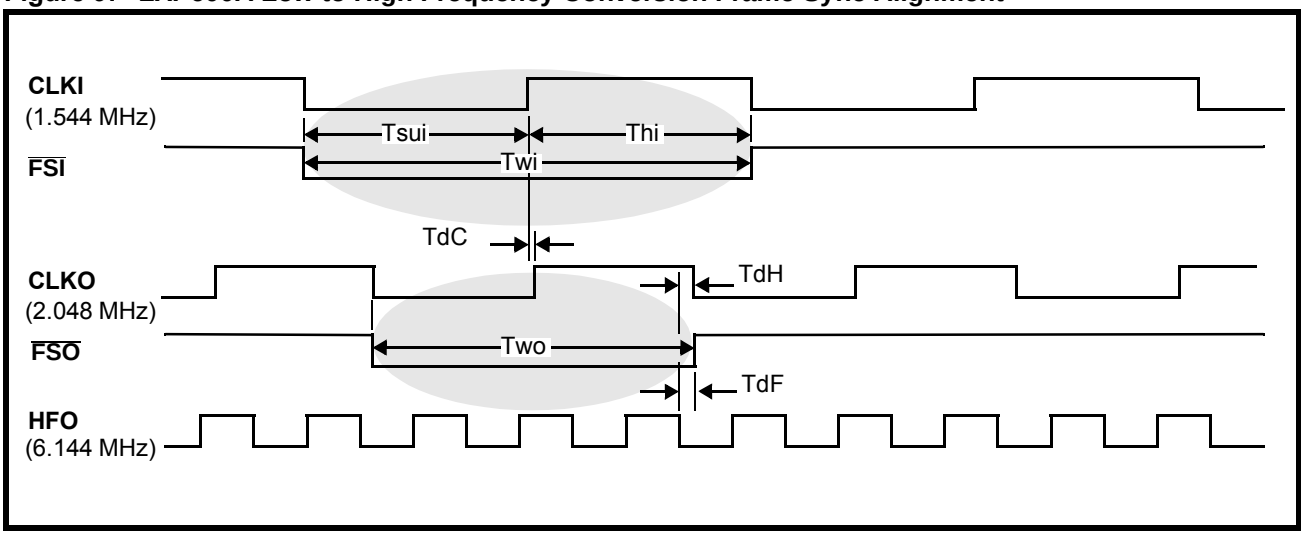


Figure 10: LXP602 Low to High Frequency Conversion Frame Sync Alignment)

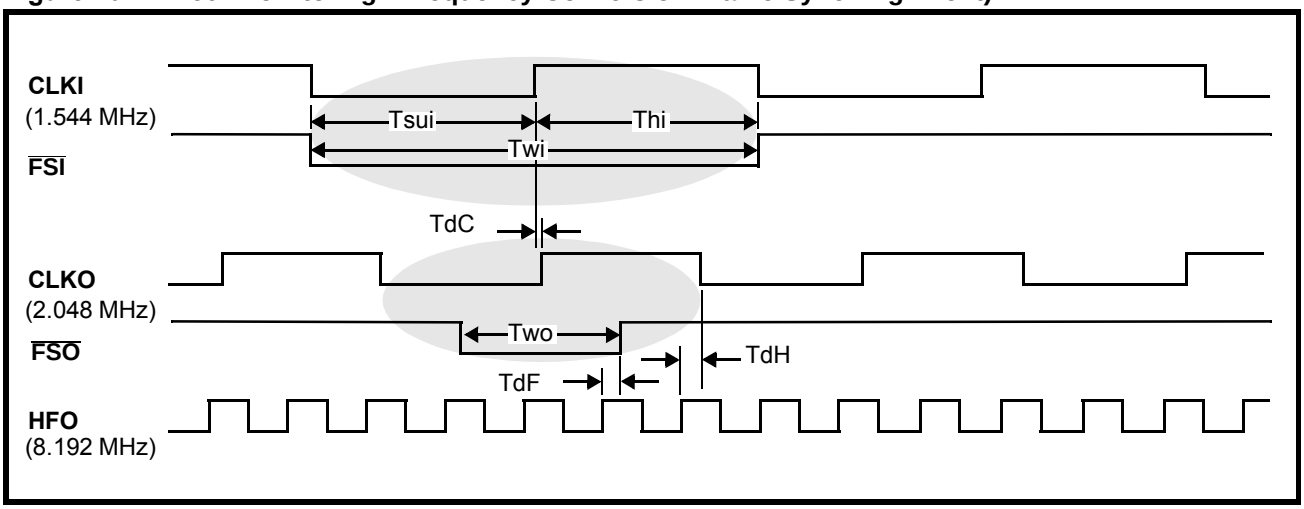


Figure 11: LXP604 Low to High Frequency Conversion Frame Sync Alignment)

