Quad/Octal Input Network Clock Generator/Synchronizer

AD9548

FEATURES

- Supports Stratum 2 stability in holdover mode
- Supports reference switchover with phase build-out
- Supports hitless reference switchover
- Auto/manual holdover and reference switchover
- 4 pairs of reference input pins with each pair configurable as a single differential input or as 2 independent single-ended inputs
- Input reference frequencies from 1 Hz to 750 MHz
- Reference validation and frequency monitoring (1 ppm)
- Programmable input reference switchover priority
- 30-bit programmable input reference divider
- 4 pairs of clock output pins with each pair configurable as a single differential LVDS/LVPECL output or as 2 single-ended CMOS outputs
- Output frequencies up to 450 MHz
- 30-bit integer and 10-bit fractional programmable feedback divider
- Programmable digital loop filter covering loop bandwidths from 0.001 Hz to 100 kHz
- Optional low noise LC-VCO system clock multiplier
- Optional crystal resonator for system clock input
- On-chip EEPROM to store multiple power-up profiles
- Software controlled power-down
- 88-lead LFCSP package

APPLICATIONS

- Network synchronization
- Cleanup of reference clock jitter
- GPS 1 pulse per second synchronization
- SONET/SDH clocks up to OC-192, including FEC
- Stratum 2 holdover, jitter cleanup, and phase transient control
- Stratum 3E and Stratum 3 reference clocks
- Wireless base station controllers
- Cable infrastructure
- Data communications

GENERAL DESCRIPTION

The AD9548 provides synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9548 generates an output clock synchronized to one of up to four differential or eight single-ended external input references. The digital PLL allows for reduction of input time jitter or phase noise associated with the external references. The AD9548 continuously generates a clean (low jitter), valid output clock even when all references have failed by means of a digitally controlled loop and holdover circuitry.

The AD9548 operates over an industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

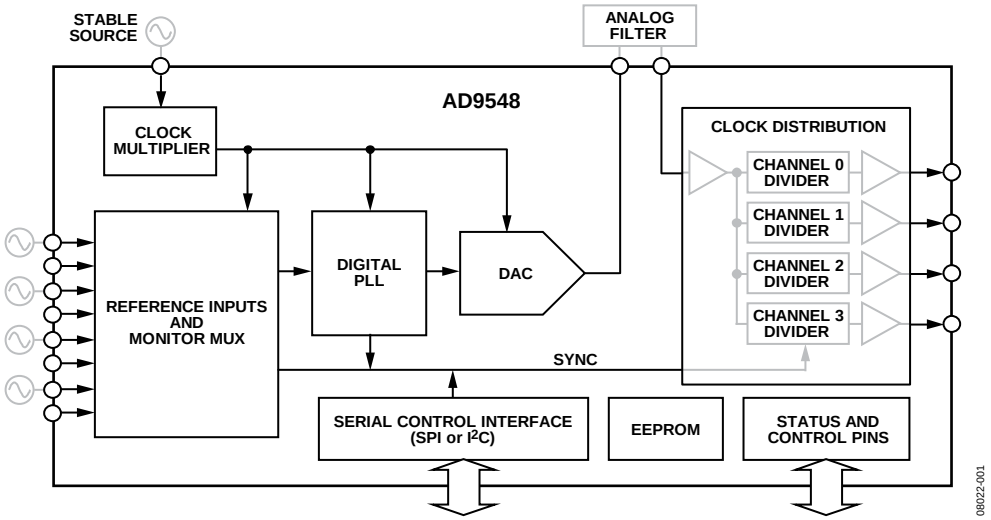


Figure 1.

Rev. 0
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
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REVISION HISTORY

5/09—Revision 0: Initial Version

SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for AVDD3 = DVDD_I/O = 3.3 V; AVDD = DVDD = 1.8 V; T_A = 25°C; I_{DAC} = 20 mA (full scale), unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD3	3.135	3.30	3.465	V	Pin 7, Pin 82
DVDD	1.71	1.80	1.89	V	Pin 1, Pin 6, Pin 12, Pin 14, Pin 15, Pin 77, Pin 83, Pin 88
AVDD3	3.135	3.30	3.465	V	Pin 21, Pin 22, Pin 47, Pin 60, Pin 66, Pin 67, Pin 73
3.3 V Supply (Typical)	3.135	3.30	3.465	V	Pin 31, Pin 37, Pin 38, Pin 44
1.8 V Supply (Alternative)	1.71	1.80	1.89	V	Pin 31, Pin 37, Pin 38, Pin 44
AVDD	1.71	1.80	1.89	V	Pin 23, Pin 24, Pin 29, Pin 34, Pin 41, Pin 50, Pin 55, Pin 59, Pin 63, Pin 70, Pin 74

SUPPLY CURRENT

The test conditions for the maximum (max) supply current are the same as the test conditions for the All Blocks Running parameter of Table 3. The test conditions for the typical (typ) supply current are the same as the test conditions for the Typical Configuration parameter of Table 3.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					
I_{DVDD3}		1.5	3	mA	Pin 7, Pin 82
I_{DVDD}		190	215	mA	Pin 1, Pin 6, Pin 12, Pin 14, Pin 15, Pin 77, Pin 83, Pin 88
I_{AVDD3}		52	75	mA	Pin 21, Pin 22, Pin 47, Pin 60, Pin 66, Pin 67, Pin 73
I_{AVDD3}					
3.3 V Supply (Typical)		24	110	mA	Pin 31, Pin 37, Pin 38, Pin 44
1.8 V Supply (Alternative)		24	110	mA	Pin 31, Pin 37, Pin 38, Pin 44
I_{AVDD}		135	163	mA	Pin 23, Pin 24, Pin 29, Pin 34, Pin 41, Pin 50, Pin 55, Pin 59, Pin 63, Pin 70, Pin 74

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration		800	1100	mW	f_{SYSCLK} = 20 MHz[1]; f_S = 1 GHz[2]; f_{DDS} = 122.88 MHz[3]; one LVPECL clock distribution output running at 122.88 MHz (all others powered down); one input reference running at 100 MHz (all others powered down)
All Blocks Running		900	1400	mW	f_{SYSCLK} = 20 MHz[1]; f_S = 1 GHz[2]; f_{DDS} = 399 MHz[3]; all clock distribution outputs configured as LVPECL at 399 MHz; all input references configured as differential at 100 MHz; fractional-N active (R = 10, S = 39, U = 9, V = 10)
Full Power-Down		13		mW	Conditions = typical configuration; no external pull-up or pull-down resistors

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Incremental Power Dissipation					Conditions = typical configuration; table values show the change in power due to the indicated operation.
SYSCLK PLL Off		−105		mW	f_{SYSCLK} = 1 GHz[1]; high frequency direct input mode.
Input Reference On					
Differential		7		mW	
Single-Ended		13		mW	
Output Distribution Driver On					
LVDS		70		mW	
LVPECL		75		mW	
CMOS		65		mW	A single 3.3 V CMOS output with a 10 pF load.

[1] f_{SYSCLK} is the frequency at the SYSCLKP and SYSCLKN pins.
[2] f_S is the sample rate of the output DAC.
[3] f_{DDS} is the output frequency of the DDS.

LOGIC INPUTS (M7 TO M0, RESET, TDI, TCLK, TMS)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (M7 to M0, RESET, TDI, TCLK, TMS)					
Input High Voltage (V_{IH})	2.1			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH}, I_{INL})		±80	±200	µA	
Input Capacitance (C_{IN})		3		pF	

LOGIC OUTPUTS (M7 TO M0, IRQ, TDO)

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M7 to M0, IRQ, TDO)					
Output High Voltage (V_{OH})	2.7			V	I_{OH} = 1 mA
Output Low Voltage (V_{OL})			0.4	V	I_{OL} = 1 mA
IRQ Leakage Current					Open-drain mode
Active Low Output Mode			1	µA	V_{OH} = 3.3 V
Active High Output Mode			1	µA	V_{OL} =-0 V

SYSTEM CLOCK INPUTS (SYSCLKP/SYSCLKN)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK PLL BYPASSED					
Input Frequency Range	500		1000	MHz	
Minimum Input Slew Rate	1000			V/µs	Minimum limit imposed for jitter performance
Duty Cycle	40		60	%	
Common-Mode Voltage		1.2		V	Internally generated
Differential Input Voltage Sensitivity	100			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding unused input
Input Capacitance		2		pF	Single-ended, each pin
Input Resistance		2.5		kΩ	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK PLL ENABLED					
PLL Output Frequency Range	900		1000	MHz	
Phase-Frequency Detector (PFD) Rate			150	MHz	
Frequency Multiplication Range	6		255		Assumes valid system clock and PFD rates
VCO Gain		70		MHz/V	
High Frequency Path					
Input Frequency Range	100.1		500	MHz	
Minimum Input Slew Rate	200			V/µs	Minimum limit imposed for jitter performance
Frequency Divider Range	1		8		Binary steps (M = 1, 2, 4, 8)
Common-Mode Voltage		1		V	Internally generated
Differential Input Voltage Sensitivity	100			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding unused input
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance		2.5		kΩ	
Low Frequency Path					
Input Frequency Range	3.5		100	MHz	
Minimum Input Slew Rate	50			V/µs	Minimum limit imposed for jitter performance
Common-Mode Voltage		1.2		V	Internally generated
Differential Input Voltage Sensitivity	100			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding unused input
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance		4		kΩ	
Crystal Resonator Path					
Crystal Resonator Frequency Range	10		50	MHz	Fundamental mode, AT cut
Maximum Crystal Motional Resistance			100	Ω	See the System Clock Inputs section for recommendations

DISTRIBUTION CLOCK INPUTS (CLKINP/CLKINN)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DISTRIBUTION CLOCK INPUTS (CLKINP/CLKINN)					
Input Frequency Range	62.5		500	MHz	
Minimum Slew Rate	75			V/µs	Minimum limit imposed for jitter performance.
Common-Mode Voltage		700		mV	Internally generated.
Differential Input Voltage Sensitivity	100			mV p-p	Capacitive coupling required; can accommodate single-ended input by ac grounding unused input; the instantaneous voltage on either pin must not exceed the supply rails.
Differential Input Power Sensitivity	−15			dBm	The same as voltage sensitivity but specified as power into a 50 Ω load.
Input Capacitance		3		pF	
Input Resistance		5		kΩ	Each pin has a 2.5 kΩ internal dc-bias resistance.

REFERENCE INPUTS (REFA/REFAA TO REFD/REFDD)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL OPERATION					
Frequency Range					
Sinusoidal Input	10		750	MHz	
LVPECL Input	1		750×10^6	Hz	
LVDS Input	1		750×10^6	Hz	
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Common-Mode Input Voltage		2		V	Internally generated
Differential Input Voltage Sensitivity		±65		mV	Minimum differential voltage across pins required to ensure switching between logic levels; the instantaneous voltage on either pin must not exceed the supply rails
Input Resistance		25		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High	620			ps	
Minimum Pulse Width Low	620			ps	
SINGLE-ENDED OPERATION					
Frequency Range (CMOS)	1		250×10^6	Hz	
Minimum Input Slew Rate	40			V/µs	Minimum limit imposed for jitter performance
Input Voltage High (V_{IH})					
1.2 V to 1.5 V Threshold Setting	0.9			V	
1.8 V to 2.5 V Threshold Setting	1.2			V	
3.0 V to 3.3 V Threshold Setting	1.9			V	
Input Voltage Low (V_{IL})					
1.2 V to 1.5 V Threshold Setting			0.27	V	
1.8 V to 2.5 V Threshold Setting			0.5	V	
3.0 V to 3.3 V Threshold Setting			1.0	V	
Input Resistance		45		kΩ	
Input Capacitance		3		pF	
Minimum Pulse Width High	1.5			ns	
Minimum Pulse Width Low	1.5			ns	

REFERENCE MONITORS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time			1.2	sec	Calculated using the nominal phase detector period (NPDP = R/f_{REF})[1]
Frequency Out-of Range Limits	9.54×10^{-7}		0.1	$\Delta f/f_{REF}$	Programmable (lower bound subject to quality of SYSCLK)
Validation Timer	0.001		65.535	sec	Programmable in 1 ms increments
Redetect Timer	0.001		65.535	sec	Programmable in 1 ms increments

[1] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R-divider.

REFERENCE SWITCHOVER SPECIFICATIONS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SWITCHOVER SPECIFICATIONS					
Maximum Output Phase Perturbation (Phase Build-Out Switchover)		40	200	ps	Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements
Maximum Time/Time Slope (Hitless Switchover)	315		65,535	ns/sec	Minimum/maximum values are programmable upper bounds; a minimum value ensures <10% error; satisfies Telcordia GR-1244-CORE requirements
Time Required to Switch to a New Reference					
Hitless Switchover		5		sec	Calculated using the nominal phase detector period (NPDP = R/f_{REF})[1]
Phase Build-Out Switchover		3		sec	Calculated using the nominal phase detector period (NPDP = R/f_{REF})[1]

[1] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R-divider.

DISTRIBUTION CLOCK OUTPUTS (OUT0 TO OUT3)

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL MODE					Using internal current setting resistor
Maximum Output Frequency		725		MHz	
Rise/Fall Time (20% to 80%)		180	315	ps	100 Ω termination across output pins
Duty Cycle	45		55	%	
Differential Output Voltage Swing	630	770	910	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	AVDD3 – 1.5	AVDD3 – 1.3	AVDD3 – 1.05	V	Output driver static
LVDS MODE					Using internal current setting resistor (nominal 3.12 kΩ)
Maximum Output Frequency		725		MHz	
Rise/Fall Time[1] (20% to 80%)		200	350	ps	100 Ω termination across the output pair
Duty Cycle	40		60	%	
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage swing between output pins; output driver static
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Offset Voltage					
Common-Mode, V_{OS}	1.125		1.375	V	Output driver static
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between pins; output driver static
Short-Circuit Output Current		13	24	mA	Output driver static
CMOS MODE					Weak drive option not supported for operating the CMOS drivers using a 1.8 V supply
Maximum Output Frequency					
3.3 V Supply					10 pF load
Strong Drive Strength Setting		250		MHz	
Weak Drive Strength Setting		25		MHz	
1.8 V Supply		150		MHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Rise/Fall Time[1] (20% to 80%)					10 pF load
3.3 V Supply					
Strong Drive Strength Setting		0.5	2	ns	
Weak Drive Strength Setting		8	14.5	ns	
1.8 V Supply		1.5	2.5	ns	
Duty Cycle	40		60	%	10 pF load
Output Voltage High (V_{OH})					Output driver static; strong drive strength setting
AVDD3 = 3.3 V, I_{OH} = 10 mA	2.6			V	
AVDD3 = 3.3 V, I_{OH} = 1 mA	2.9			V	
AVDD3 = 1.8 V, I_{OH} = 1 mA	1.5			V	
Output Voltage Low (V_{OL})					Output driver static; strong drive strength setting
AVDD3 = 3.3 V, I_{OL} = 10 mA			0.3	V	
AVDD3 = 3.3 V, I_{OL} = 1 mA			0.1	V	
AVDD3 = 1.8 V, I_{OL} = 1 mA			0.1	V	
OUTPUT TIMING SKEW					10 pF load
Between LVPECL Outputs		14	125	ps	Rising edge only; any divide value
Between LVDS Outputs		13	138	ps	Rising edge only; any divide value
Between CMOS 3.3 V Outputs					
Strong Drive Strength Setting		23	240	ps	
Weak Drive Strength Setting		24		ps	
Between CMOS 1.8 V Outputs		40		ps	Weak drive not supported at 1.8 V
Between LVPECL Outputs and LVDS Outputs		14	140	ps	
Between LVPECL Outputs and CMOS Outputs		19		ps	
ZERO-DELAY TIMING SKEW		±5		ns	Output relative to active input reference; output distribution synchronization to active reference feature enabled; assumes manual phase offset compensation of deterministic latency

[1] The listed values are for the slower edge (rise or fall).

DAC OUTPUT CHARACTERISTICS (DACOUTP/DACOUTN)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC OUTPUT CHARACTERISTICS (DACOUTP/DACOUTN)					
Frequency Range	62.5		450	MHz	
Output Offset Voltage			15	mV	This is the single-ended voltage at either DAC output pin (no external load) when the internal DAC code implies that no current is delivered to that pin.
Voltage Compliance Range	VSS − 0.5	0.5	VSS + 0.5	V	
Output Resistance		50		Ω	Single-ended, each pin has an internal 50 Ω termination to VSS.
Output Capacitance		5		pF	
Full-Scale Output Current		20		mA	Programmable (8 mA to 31 mA; see the DAC Output section).
Gain Error	−12		+12	% FS	

TIME DURATION OF DIGITAL FUNCTIONS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM-to-Register Download Time		25		ms	Using default EEPROM storage sequence (see Register 0E10 to Register 0E3F)
Register-to-EEPROM Upload Time		200		ms	Using default EEPROM storage sequence (see Register 0E10 to Register 0E3F
Minimum Power-Down Exit Time		10.5		µs	Dependent on loop-filter bandwidth
Maximum Time from Assertion of the RESET pin to the M0 to M7 Pins Entering High Impedance State		45		ns	

DIGITAL PLL

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Phase-Frequency Detector (PFD) Input Frequency Range	1		10^7	Hz	Maximum f_{PFD}[1]: $f_S/100$[2]
Loop Bandwidth	0.001		10^5	Hz	Programmable design parameter; maximum $f_{LOOP} = f_{REF}/(20R)$[3]
Phase Margin	30		89	Degrees	Programmable design parameter
Reference Input (R) Division Factor	1		2^{30}		1, 2, …, 1,073,741,824
Integer Feedback (S) Division Factor	8		2^{30}		8, 9, …, 1,073,741,824
Fractional Feedback Divide Ratio	0		0.999		Maximum value: 1022/1023.

[1] f_{PFD} is the frequency at the input to the phase-frequency detector.
[2] f_S is the sample rate of the output DAC.
[3] f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R-divider.

DIGITAL PLL LOCK DETECTION

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	0.001		65.5	ns	
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	0.001		16,700	ns	Reference-to-feedback period difference
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Frequency Accuracy		<0.01		ppm	Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover

SERIAL PORT SPECIFICATIONS—SPI MODE

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$					Internal 30 kΩ pull-up resistor
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		30		μA	
Input Logic 0 Current		110		μA	
Input Capacitance		2		pF	
SCLK					Internal 30 kΩ pull-down resistor
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
SDIO					
As an Input					
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
As an Output					
Output Logic 1 Voltage	2.7			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
SDO					
Output Logic 1 Voltage	2.7			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
TIMING					
SCLK					
Clock Rate, $1/t_{CLK}$			40	MHz	
Pulse Width High, t_{HI}	8			ns	
Pulse Width Low, t_{LO}	12			ns	
SDIO to SCLK Setup, t_{DS}	3			ns	
SCLK to SDIO Hold, t_{DH}	0			ns	
SCLK to Valid SDIO and SDO, t_{DV}			14	ns	
$\overline{CS}$ to SCLK Setup (t_S)	10			ns	
$\overline{CS}$ to SCLK Hold (t_C)	0			ns	
$\overline{CS}$ Minimum Pulse Width High	6			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUT)					No internal pull-up/down resistor.
Input Logic 1 Voltage	0.7 × DVDD3			V	
Input Logic 0 Voltage			0.3 × DVDD3	V	
Input Current	−10		+10	μA	For V_{IN} = 10% to 90% DVDD3
Hysteresis of Schmitt Trigger Inputs	0.015 × DVDD3				
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t_{SP}			50	ns	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.4	V	I_O = 3 mA.
Output Fall Time from V_{IHmin} to V_{ILmax}	20 + 0.1 C_b[1]		250	ns	10 pF ≤ C_b ≤ 400 pF.
TIMING					
SCL Clock Rate			400	kHz	
Bus-Free Time Between a Stop and Start Condition, t_{BUF}	1.3			µs	
Repeated Start Condition Setup Time, $t_{SU;STA}$	0.6			µs	
Repeated Hold Time Start Condition, $t_{HD;STA}$	0.6			µs	After this period, the first clock pulse is generated.
Stop Condition Setup Time, $t_{SU;STO}$	0.6			µs	
Low Period of the SCL Clock, t_{LO}	1.3			µs	
High Period of the SCL Clock, t_{HI}	0.6			µs	
SCL/SDA Rise Time, t_R	20 + 0.1 C_b[1]		300	ns	
SCL/SDA Fall Time, t_F	20 + 0.1 C_b[1]		300	ns	
Data Setup Time, $t_{SU;DAT}$	100			ns	
Data Hold Time, $t_{HD;DAT}$	100			ns	
Capacitive Load for Each Bus Line, C_b[1]			400	pF	

[1] C_b is the capacitance (pF) of a single bus line.

JITTER GENERATION

Table 19.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					
f_{REF} = 1 Hz[1]; f_{DDS} = 122.88 MHz[2]; f_{LOOP} = 0.01 Hz[3]					f_{SYSCLK} = 20 MHz[4] OCXO; f_S = 1 GHz[5]; Q-divider = 1; default SysClk PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 61 MHz		0.81		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.73		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.79		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.78		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.37		ps rms	Random jitter
f_{REF} = 8 kHz[1]; f_{DDS} = 155.52 MHz[2]; f_{LOOP} = 100 Hz[3]					f_{SYSCLK} = 50 MHz[4] crystal; f_S = 1 GHz[5]; Q-divider = 1; default SYSCLK PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 77 MHz		0.71		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.34		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.31		ps rms	Random jitter
f_{REF} = 19.44 MHz[1]; f_{DDS} = 155.52 MHz[2]; f_{LOOP} = 1 kHz[3]					f_{SYSCLK} = 50 MHz[4] crystal; f_S = 1 GHz[5]; Q-divider = 1; default SYSCLK PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 77 MHz		1.05		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.34		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.43		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.32		ps rms	Random jitter

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{REF} = 19.44 Hz[1]; f_{DDS} = 311.04 MHz[2]; f_{LOOP} = 1 kHz[3]					f_{SYSCLK} = 50 MHz[4] crystal; f_S = 1 GHz[5]; Q-divider = 1; default SYSCLK PLL charge pump current; results valid for LVPECL, LVDS, and CMOS output logic types
Bandwidth: 100 Hz to 100 MHz		0.67		ps rms	Random jitter
Bandwidth: 5 kHz to 20 MHz		0.31		ps rms	Random jitter
Bandwidth: 20 kHz to 80 MHz		0.33		ps rms	Random jitter
Bandwidth: 50 kHz to 80 MHz		0.33		ps rms	Random jitter
Bandwidth: 4 MHz to 80 MHz		0.16		ps rms	Random jitter

[1] f_{REF} is the frequency of the active reference.
[2] f_{DDS} is the output frequency of the DDS.
[3] f_{LOOP} is the DPLL digital loop filter bandwidth.
[4] f_{SYSCLK} is the frequency at the SYSCLKP and SYSCLKN pins.
[5] f_S is the sample rate of the output DAC.

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD3)	3.6 V
DAC Supply Voltage (AVDD3)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD3 + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

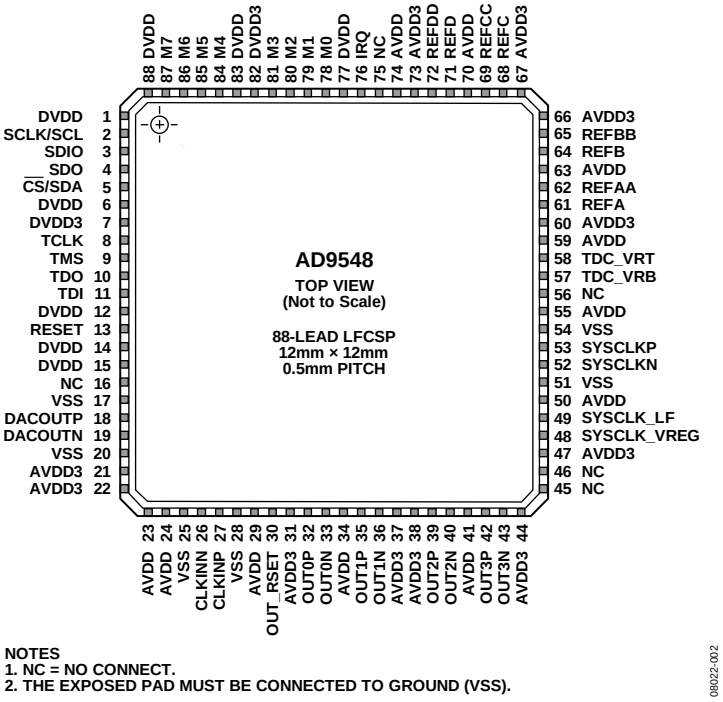


Figure 2. 88-Lead LFCSP Pin Configuration

Table 21. Pin Function Descriptions

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
1, 6, 12, 77, 83, 88	DVDD	I	Power	1.8 V Digital Supply.
2	SCLK/SCL	I	3.3 V CMOS	Serial Programming Clock. Data clock for serial programming.
3	SDIO	I/O	3.3 V CMOS	Serial Data Input/Output. When the device is in 4-wire mode, data is written via this pin. In 3-wire mode, both data reads and writes occur on this pin. There is no internal pull-up/pull-down resistor on this pin.
4	SDO	O	3.3 V CMOS	Serial Data Output. Use this pin to read data in 4-wire mode (high impedance in 3-wire mode). There is no internal pull-up/pull-down resistor on this pin.
5	$\overline{CS}$/SDA	I	3.3 V CMOS	Chip Select (SPI). Active low. When programming a device, this pin must be held low. In systems where more than one AD9548 is present, this pin enables individual programming of each AD9548 (in I^2C® mode, this is a serial data pin). This pin has an internal 10 kΩ pull-up resistor but only in SPI mode.
7, 82	DVDD3	I	Power	3.3 V I/O Digital Supply.
8	TCLK	I		JTAG Clock. Internal pull-down resistor; no connection if JTAG is not used.
9	TMS	I		JTAG Mode. Internal pull-up resistor; no connection if JTAG is not used.
10	TDO	O		JTAG Output. No connection if JTAG is not used
11	TDI	I		JTAG Input. Internal pull-up resistor; no connection if JTAG is not used.
13	RESET	I	3.3 V CMOS	Chip Reset. When this active high pin is asserted, the chip goes into reset. This pin has an internal 50 kΩ pull-down resistor.
14, 15	DVDD	I	Power	1.8 V DAC Decode Digital Supply. Keep isolated from the 1.8 V core digital supply.
16, 45, 46	NC			No Connect.
17, 20, 25, 28, 51, 54	VSS	O	Ground	Analog Ground. Connect to ground.
18	DACOUTP	O	Differential output	DAC Output. DACOUTP contains an internal 50 Ω pull-down resistor.
19	DACOUTN	O	Differential output	Complementary DAC Output. DACOUTN contains an internal 50 Ω pull-down resistor.
21, 22	AVDD3	I	Power	3.3 V Analog (DAC) Power Supply.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
23, 24	AVDD	I	Power	1.8 V Analog (DAC) Power Supply.
26	CLKINN	I	Differential input	Clock Distribution Input. In standard operating mode, this pin is connected to the filtered DACOUTN output. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal whose single-ended swing is at least 400 mV.
27	CLKINP	I	Differential input	Clock Distribution Input. In standard operating mode, this pin is connected to the filtered DACOUTP output
29	AVDD	I	Power	1.8 V Analog (Input Receiver) Power Supply.
30	OUT_RSET	O	Current set resistor	Connect an optional 3.12 kΩ resistor from this pin to ground (see the Output Current Control with an External Resistor section).
31, 37, 38, 44	AVDD3	I	Power	Analog Supply for Output Driver. These pins are normally 3.3 V but can be 1.8 V. Pin 31 powers Out0x. Pin 37 powers OUT1x. Pin 38 powers OUT2x. Pin 44 powers OUT3x. Apply power to these pins even if the corresponding outputs (OUT0P/ OUT0N, OUT1P/ OUT1N, OUT2P/ OUT2N, and OUT3P/ OUT3N) are not used. See the Power Supply Partitions section.
32	OUT0P	O	LVPECL, LVDS, or CMOS	Output 0. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
33	OUT0N	O	LVPECL, LVDS, or CMOS	Complementary Output 0. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
34, 41	AVDD	I	Power	1.8 V Analog (Output Divider) Power Supply.
35	OUT1P	O	LVPECL, LVDS, or CMOS	Output 1. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
36	OUT1N	O	LVPECL, LVDS, or CMOS	Complementary Output 1. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
39	OUT2P	O	LVPECL, LVDS, or CMOS	Output 2. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
40	OUT2N	O	LVPECL, LVDS, or CMOS	Complementary Output 2. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
42	OUT3P	O	LVPECL, LVDS, or CMOS	Output 3. This output can be configured as LVPECL, LVDS, or single-ended CMOS. LVPECL and LVDS operation require a 3.3 V output driver power supply. CMOS operation can be either 1.8 V or 3.3 V, depending on the output driver power supply.
43	OUT3N	O	LVPECL, LVDS, or CMOS	Complementary Output 3. This output can be configured as LVPECL, LVDS, or single-ended CMOS.
47	AVDD3	I	Power	3.3 V Analog (System Clock) Power Supply.
48	SYSCLK_VREG	I		System Clock Loop Filter Voltage Regulator. Connect a 0.1 µF capacitor from this pin to ground. This pin is also the ac ground reference for the integrated SYSCLK PLL multiplier's external loop filter (see the SYSCLK PLL Multiplier section).
49	SYSCLK_LF	O		System Clock Multiplier Loop Filter. When using the frequency multiplier to drive the system clock, an external loop filter can be attached to this pin.
50, 55	AVDD	I	Power	1.8 V Analog (System Clock) Power Supply.
52	SYSCLKN	I	Differential input	Complementary System Clock Input. Complementary signal to SYSCLKP. SYSCLKN contains internal dc biasing and should be ac-coupled with a 0.01 µF capacitor, except when using a crystal, in which case connect the crystal across SYSCLKP and SYSCLKN.

Pin No.	Mnemonic	Input/ Output	Pin Type	Description
53	SYSCLKP	I	Differential input	System Clock Input. SYSCLKP contains internal dc biasing and should be ac-coupled with a 0.01 µF capacitor, except when using a crystal, in which case connect the crystal across SYSCLKP and SYSCLKN. Single-ended 1.8 V CMOS is also an option but can introduce a spur if the duty cycle is not 50%. When using SYSCLKP as a single-ended input, connect a 0.01 µF capacitor from SYSCLKN to ground.
56, 75	NC	I		No Connection. These pins should be left floating.
59	AVDD	I	Power	1.8 V Analog Power Supply.
57, 58	TDC_VRB, TDC_VRT	I		Use capacitive decoupling on these pins (see Figure 38).
60, 66, 67, 73	AVDD3	I	Power	3.3 V Analog (Reference Input) Power Supply.
61	REFA	I	Differential input	Reference A Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
62	REFAA	I	Differential input	Complementary Reference A Input. Complementary signal to the input provided on Pin 61. The user can configure this pin as a separate single-ended input.
63, 70, 74	AVDD	I	Power	1.8 V Analog (Reference Input) Power Supply.
64	REFB	I	Differential input	Reference B Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
65	REFBB	I	Differential input	Complementary Reference B Input. Complementary signal to the input provided on Pin 64. The user can configure this pin as a separate single-ended input.
68	REFC	I	Differential input	Reference C Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
69	REFCC	I	Differential input	Complementary Reference C Input. Complementary signal to the input provided on Pin 68. The user can configure this pin as a separate single-ended input.
71	REFD	I	Differential input	Reference D Input. This internally biased input is typically ac-coupled and, when configured as such, can accept any differential signal with single-ended swing up to 3.3 V. If dc-coupled, input can be LVPECL, CMOS, or LVDS.
72	REFDD	I	Differential input	Complementary Reference D Input. Complementary signal to the input provided on Pin 71. The user can configure this pin as a separate single-ended input.
76	IRQ	O	Logic	Interrupt Request Line.
78, 79, 80, 81, 84, 85, 86, 87	M0, M1, M2, M3, M4, M5, M6, M7	I/O	3.3 V CMOS	Configurable I/O Pins. These pins are configured under program control.
EP	VSS	O	Exposed pad	The exposed pad must be connected to ground (VSS).

TYPICAL PERFORMANCE CHARACTERISTICS

f_R = input reference clock frequency; f_O = clock frequency; f_{SYS} = SYSCLK input frequency; f_S = internal system clock frequency; LBW = DPLL loop bandwidth; PLL off = SYSCLK PLL bypassed; PLL on = SYSCLK PLL enabled; I_{CP} = SYSCLK PLL charge pump current; LF = SYSCLK PLL loop filter. AVDD, AVDD3, and DVDD at nominal supply voltage, f_S = 1 GHz, I_{CP} = automatic mode, LF = internal, unless otherwise noted.

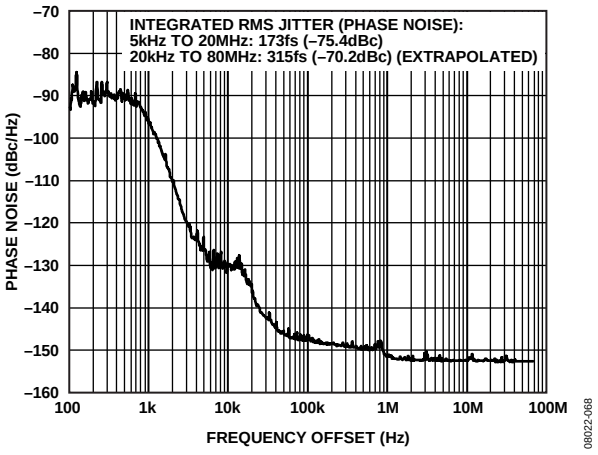


Figure 3. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 1 GHz, PLL Off

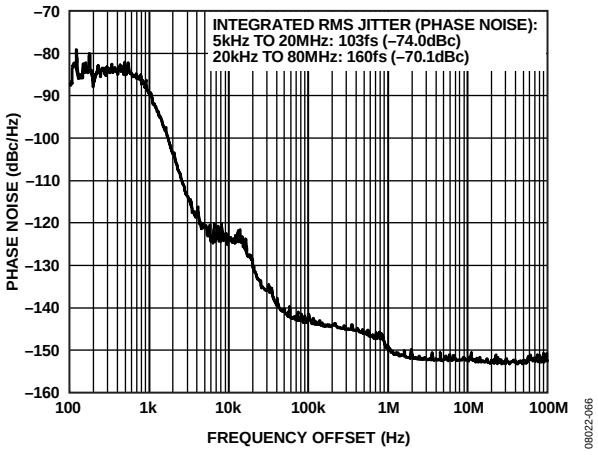


Figure 5. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 311.04 MHz, LBW = 1 kHz, f_{SYS} = 1 GHz, PLL Off

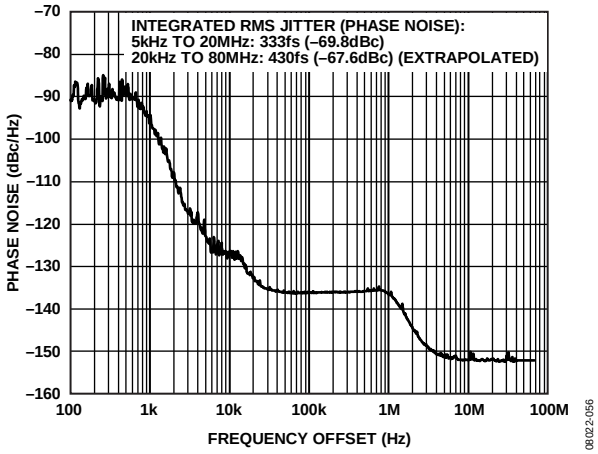


Figure 4. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz (Crystal), PLL On

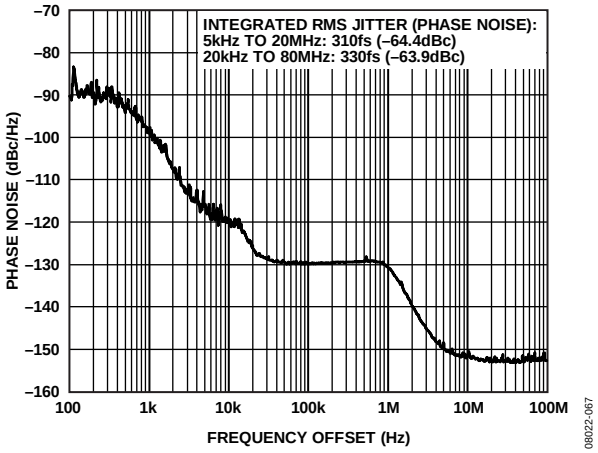


Figure 6. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 311.04 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz (Crystal), PLL On

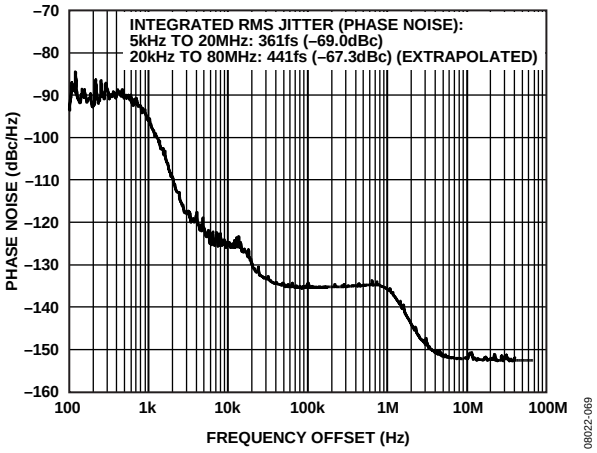


Figure 7. Additive Phase Noise (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz, PLL On

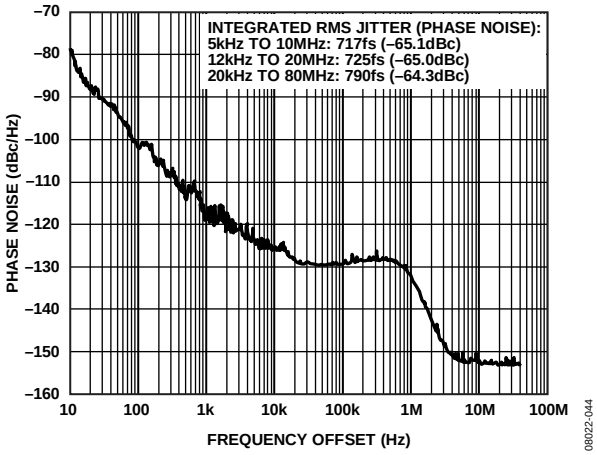


Figure 8. Additive Phase Noise (Output Driver = LVPECL), f_R = 1 Hz, f_O = 122.88 MHz, LBW = 0.05 Hz, f_{SYS} = 20 MHz (OCXO), PLL On

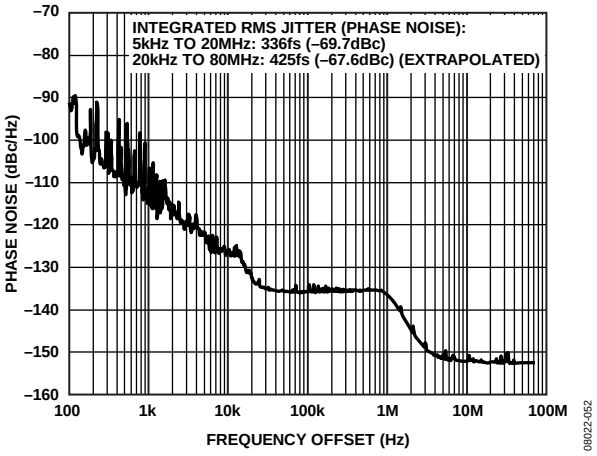


Figure 9. Additive Phase Noise (Output Driver = LVPECL), f_R = 8 kHz, f_O = 155.52 MHz, LBW = 100 Hz, f_{SYS} = 50 MHz (Crystal), PLL On

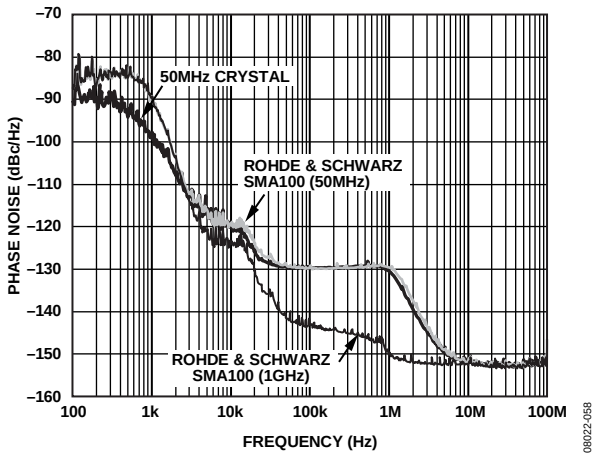


Figure 10. Additive Phase Noise Comparison of SYSCLK Input Options (Output Driver = LVPECL), f_R = 19.44 MHz, f_O = 311.04 MHz, LBW = 1 kHz

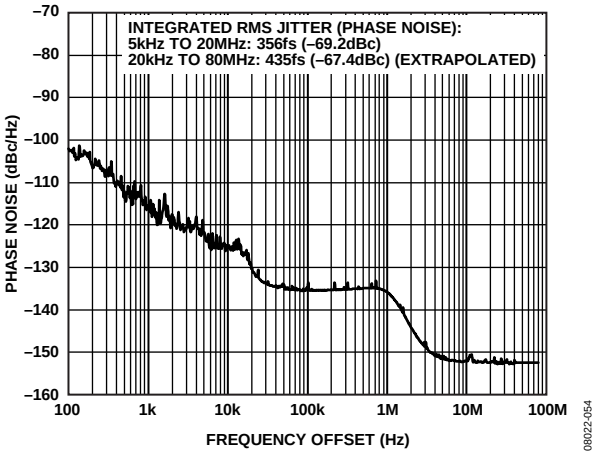


Figure 11. Additive Phase Noise (Output Driver = LVPECL), f_R = 1 Hz, f_O = 155.52 MHz, LBW = 0.05 Hz, f_{SYS} = 50 MHz, PLL On

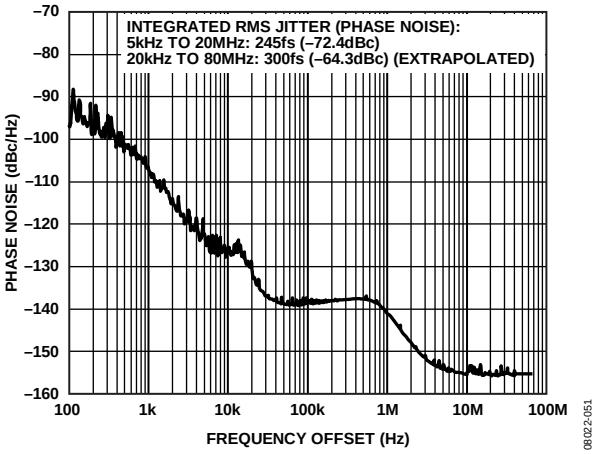


Figure 12. Additive Phase Noise (Output Driver = LVPECL) , f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 1 kHz, f_{SYS} = 50 MHz (Crystal), PLL On with 2x Frequency Multiplier, I_{CP} = 375 µA, LF = External (350 kHz)

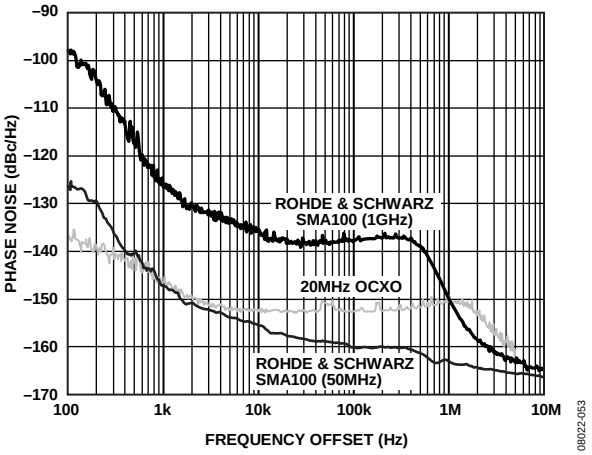


Figure 13. Phase Noise of SYSCLK Input Sources

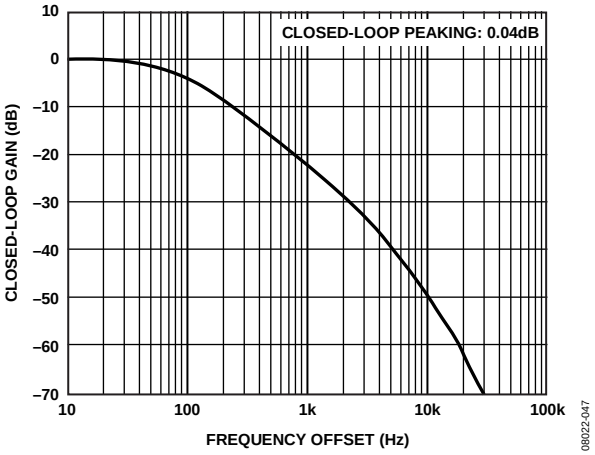


Figure 16. Jitter Transfer Bandwidth, Output Driver = LVPECL, f_R = 19.44 MHz, f_O = 155.52 MHz, LBW = 100 Hz (Phase Margin = 88°), f_{SYS} = 1 GHz, PLL Off

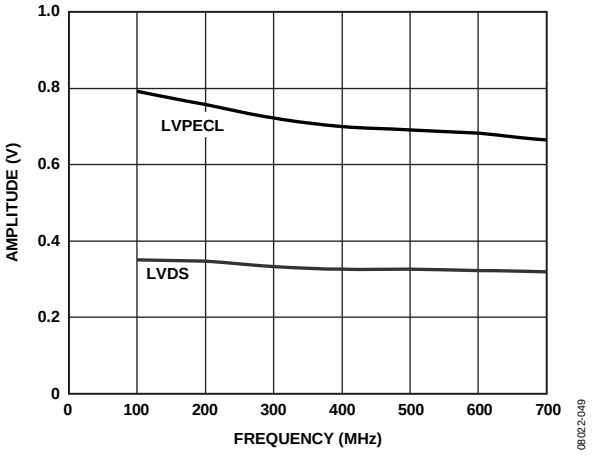


Figure 14. Amplitude vs. Toggle Rate, LVPECL and LVDS

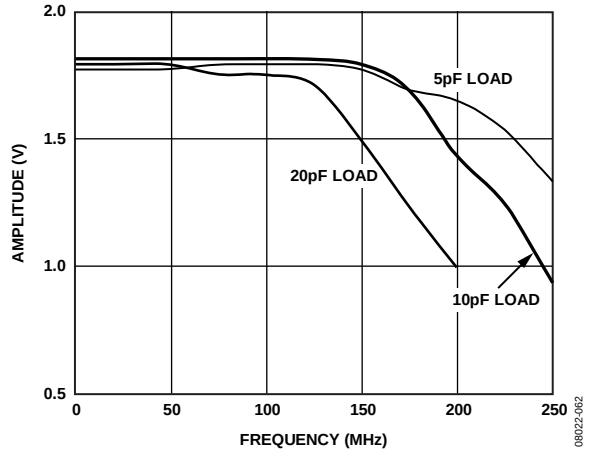


Figure 17. Amplitude vs. Toggle Rate, 1.8 V CMOS

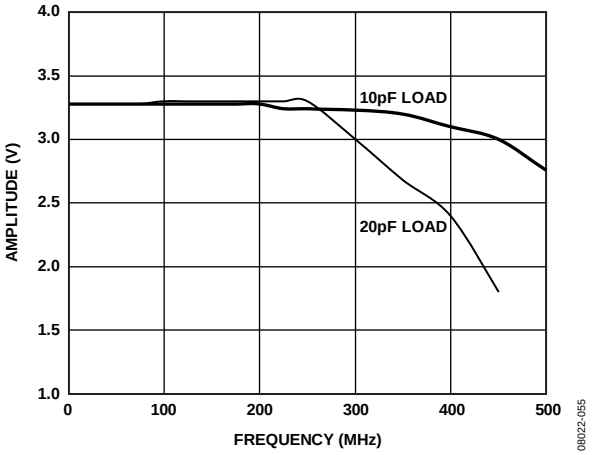


Figure 15. Amplitude vs. Toggle Rate, 3.3 V CMOS (Strong Mode)

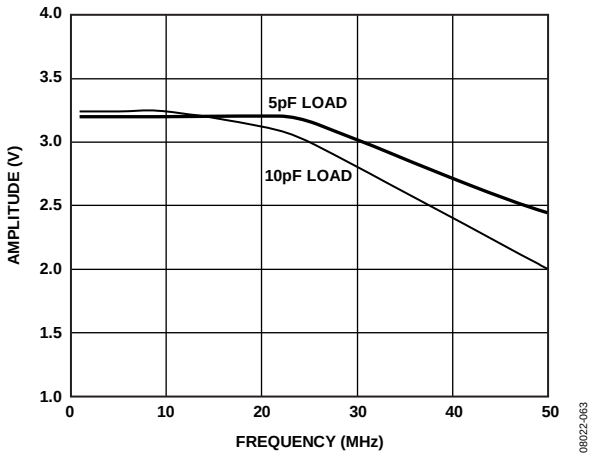


Figure 18. Amplitude vs. Toggle Rate, 3.3 V CMOS (Weak Mode)

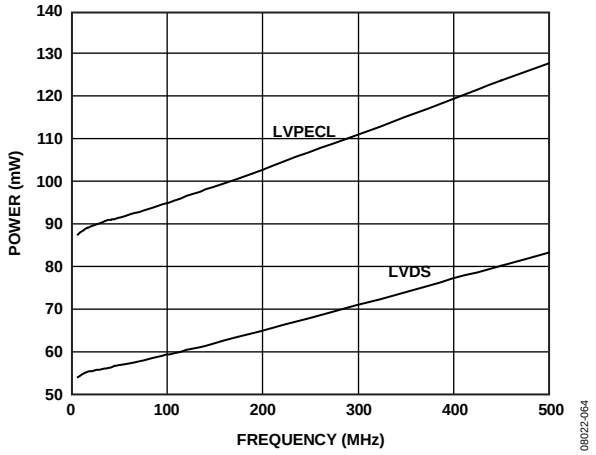


Figure 19. Power Consumption vs. Frequency, LVPECL and LVDS (Single Channel)

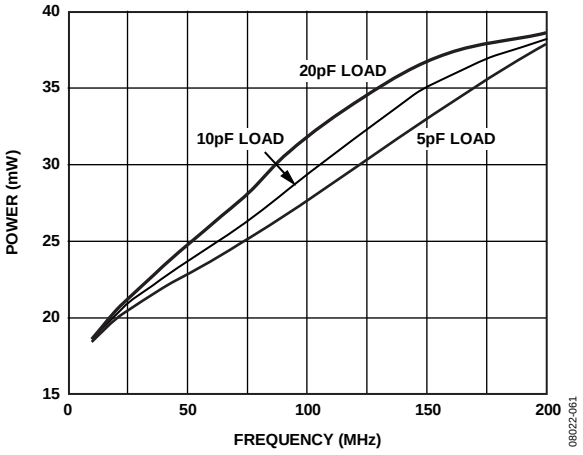


Figure 22. Power Consumption vs. Frequency, 1.8 V CMOS

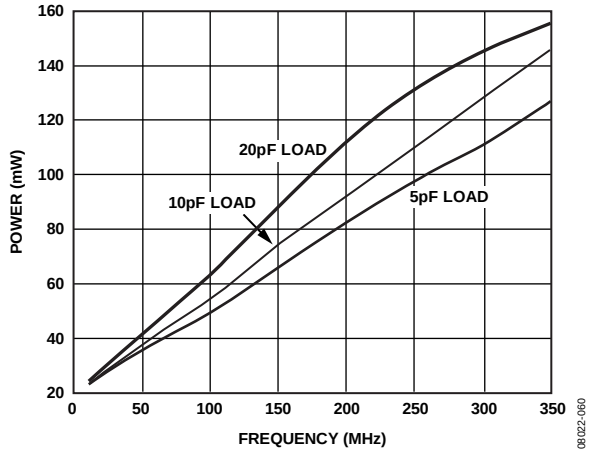


Figure 20. Power Consumption vs. Frequency, 3.3 V CMOS (Strong Mode)

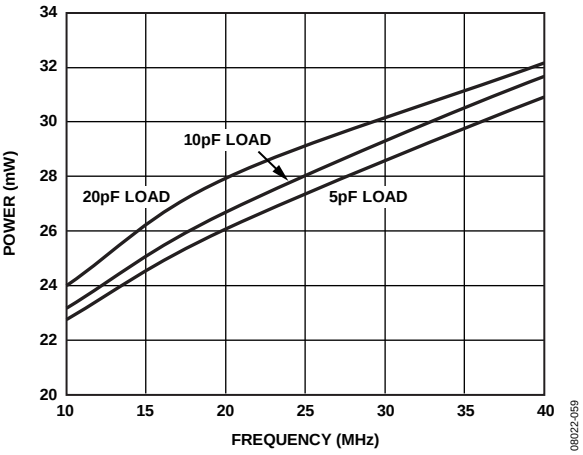


Figure 23. Power Consumption vs. Frequency, 3.3 V CMOS (Weak Mode)

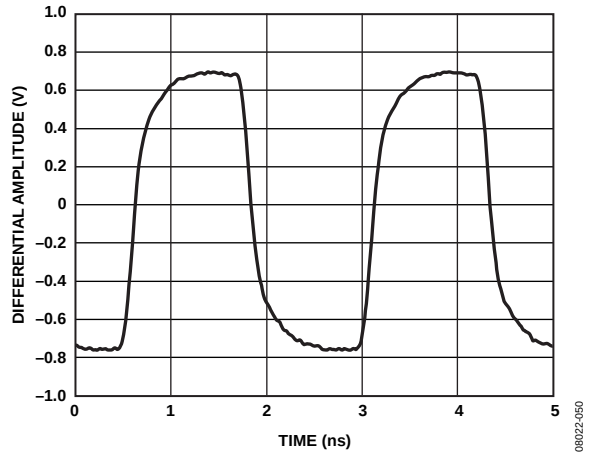


Figure 21. Output Waveform, LVPECL (400 MHz)

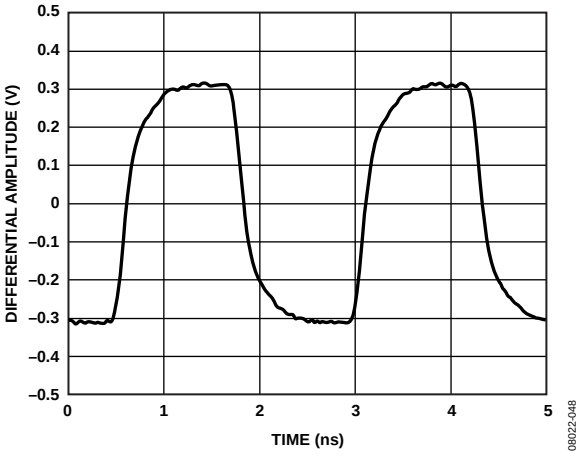


Figure 24. Output Waveform, LVDS (400 MHz)

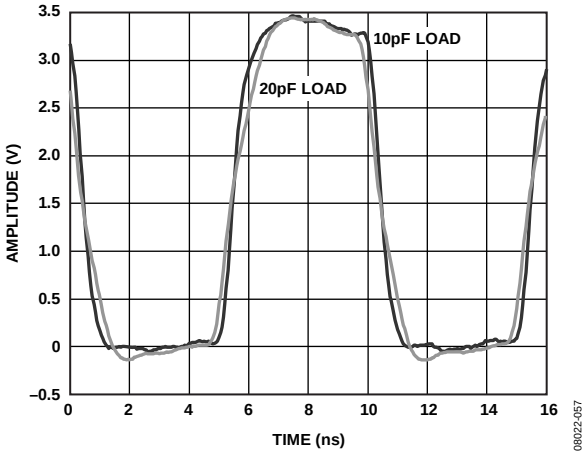


Figure 25. Output Waveform, 3.3 V CMOS (100 MHz, Strong Mode)

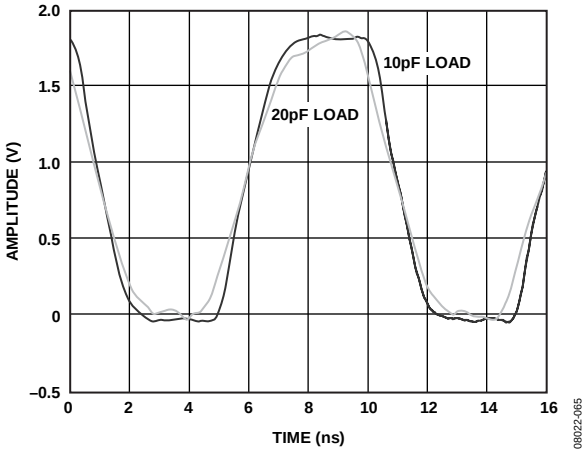


Figure 26. Output Waveform, 1.8 V CMOS (100 MHz)

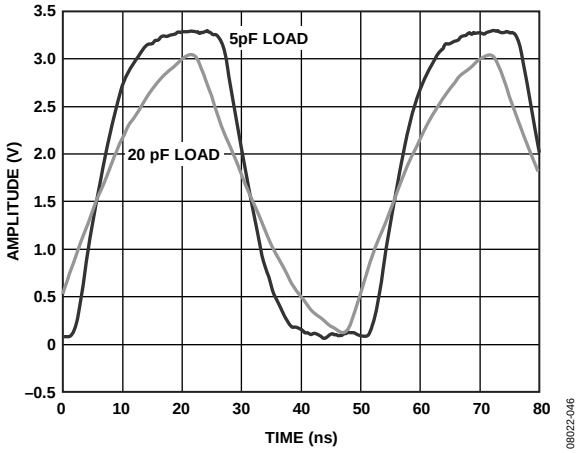


Figure 27. Output Waveform, 3.3 V CMOS (20 MHz, Weak Mode)

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

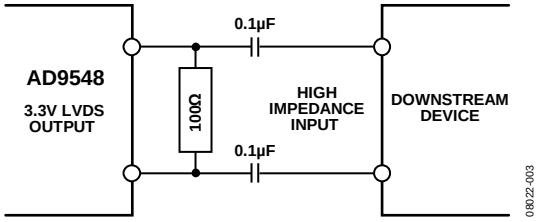


Figure 28. AC-Coupled LVDS or LVPECL Output Driver

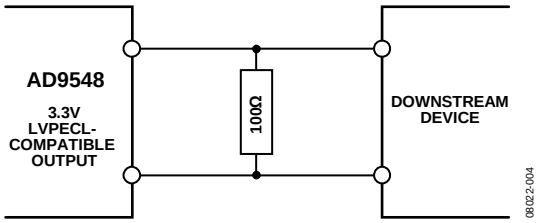


Figure 29. DC-Coupled LVDS or LVPECL Output Driver

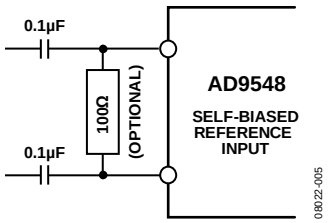


Figure 30. Reference Input

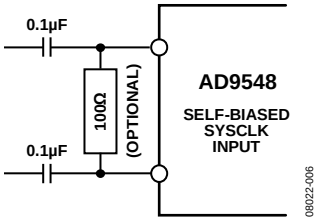


Figure 31. SYSCLKx Input

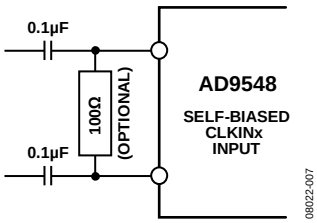


Figure 32. CLKINx Input

GETTING STARTED

POWER-ON RESET

The AD9548 monitors the voltage on the power supplies at power-up. When DVDD3 is greater than 2.35 V ± 0.1 V and DVDD (Pin 1, Pin 6, Pin 12, Pin 77, Pin 83, and Pin 88) is greater than 1.4 V ± 0.05 V, the device generates a 75 ns reset pulse. The power-up reset pulse is internal and independent of the RESET pin. This internal power-up reset sequence eliminates the need for the user to provide external power supply sequencing. Within 45 ns after the leading edge of the internal reset pulse, the M0 to M7 multifunction pins behave as high impedance digital inputs and remain so until programmed otherwise.

INITIAL PIN PROGRAMMING

During a device reset (either via the power-up reset pulse or the RESET pin), the multifunction pins (M0 to M7) behave as high impedance inputs, but upon removal of the reset condition, level-sensitive latches capture the logic pattern present on the multifunction pins. The AD9548 requires that the user supply the desired logic state to the M0 to M7 pins by means of pull-up and/or pull-down resistors (nominally 10 kΩ to 30 kΩ).

The initial state of the M0 to M7 pins following a reset is referred to as FncInit, Bits[7:0]. Bits[7:0] of FncInit map directly to the logic states of M7:0, respectively. The three LSBs of FncInit (FncInit, Bits[2:0]) determine whether the serial port interface behaves according to the SPI or I^2C protocol. Specifically, FncInit, Bits[2:0] = 000 selects the SPI interface, while any other value selects the I^2C port with the three LSBs of the I^2C bus address set to the value of FncInit, Bits[2:0].

The five MSBs of FncInit (FncInit, Bits[7:3]) determine the operation of the EEPROM loader. On the falling edge of RESET, if FncInit, Bits[7:3] = 00000, then the EEPROM contents are not transferred to the control registers and the device registers assume their default values. However, if FncInit, Bits[7:3] ≠ 00000, then the EEPROM controller transfers the contents of the EEPROM to the control registers with condition = FncInit, Bits[7:3] (see the EEPROM section).

DEVICE REGISTER PROGRAMMING

The initial state of the M0 to M7 pins establishes the serial I/O port protocol (SPI or I^2C). Using the appropriate serial port protocol, and assuming that an EEPROM download is not used, program the device according to the recommended sequence described in the Program the System Clock Functionality section through the Generate the Output Clock section.

Program the System Clock Functionality

The system clock parameters reside in the 0100 register address space. They include the following:

- System clock PLL controls
- System clock period
- System clock stability timer

It is essential to program the system clock period because many of the AD9548 subsystems rely on this value. It is highly recommended to program the system clock stability timer, as well. This is especially important when using the system clock PLL but also applies if using an external system clock source, especially if the external source is not expected to be completely stable when power is applied to the AD9548.

Initialize the System Clock

After the system clock functionality is programmed, issue an I/O update using Register 0005, Bit 0 to invoke the system clock settings.

Calibrate the System Clock (Only if Using SYSCLK PLL)

Set the calibrate system clock bit in the sync/cal register (Address 0A02, Bit 0) and issue an I/O update. Then clear the calibrate system clock bit and issue another I/O update. This action allows time for the calibration to proceed while programming the remaining device registers.

Program the Multifunction Pins (Optional)

This step is required only if the user intends to use any of the multifunction pins for status or control. The multifunction pin parameters resides in the 0200 to 0207 register address space. The default configuration of the multifunction pins is as an undesignated high impedance input pin.

Program the IRQ Functionality (Optional)

This step is required only if the user intends to use the IRQ feature. IRQ control resides in the 0200 to 0207 register address space. It includes the following:

- IRQ pin mode control
- IRQ mask

The IRQ mask default values prevent interrupts from being generated. The IRQ pin mode default is open-drain NMOS.

Program the Watchdog Timer (Optional)

This step is required only if the user intends to use it. Watchdog timer control resides in the 0200 register address space. The watchdog timer is disabled by default.

Program the DAC Full-Scale Current (Optional)

This step is required only if the user intends to use a full-scale current setting other than the default value. DAC full-scale current control resides in the 0200 register address space.

Program the Digital Phase-Locked Loop (DPLL)

The DPLL parameters reside in the 0300 register address space. They include the following:

- Free-run frequency (DDS frequency tuning word)
- DDS phase offset
- DPLL pull-in range limits
- DPLL closed-loop phase offset
- Phase slew control (for hitless reference switching)

- Tuning word history control (for holdover operation)

Program the Clock Distribution Outputs

The clock distribution parameters reside in the 0400 register address space. They include the following:

- Output power-down control
- Output enable (disabled by default)
- Output synchronization
- Output mode control
- Output divider functionality

Program the Reference Inputs

The reference input parameters reside in the 0500 register address space. They include the following:

- Reference power-down
- Reference logic family
- Reference profile assignment control
- Phase build-out control

Program the Reference Profiles

The reference profile parameters reside in the 0600 to 0700 register address space. They include the following:

- Reference priority
- Reference period
- Reference period tolerance
- Reference validation timer
- Reference redetect timer
- Digital loop-filter coefficients
- Reference prescaler (R-divider)
- Feedback dividers (S, U, and V)
- Phase and frequency lock detector controls

Generate the Reference Acquisition

After the registers are programmed, issue an I/O update using Register 0005, Bit 0 to invoke all of the register settings programmed up to this point.

If the settings are programmed for manual profile assignment, the DPLL locks to the first available reference that has the highest priority. If the settings are programmed for automatic profile assignment, then write to the reference profile detect register (Address 0A0D) to select the state machines that require starting. Next, issue an I/O update (Address 0005, Bit 0) to start the selected state machines. Upon completion of the reference detection sequence, the DPLL locks to the first available reference with the highest priority.

Generate the Output Clock

If the registers are programmed for automatic clock distribution synchronization via DPLL phase or frequency lock, the synthesized output signal appears at the clock distribution outputs (assuming the output is enabled and that the DDS output signal has been routed to the CLKIN input pins). Otherwise, set and then clear the sync distribution bit (Address 0A02, Bit 1) or use a multifunction pin input (if programmed accordingly) to generate a clock distribution sync pulse, which causes the synthesized output signal to appear at the clock distribution outputs.

THEORY OF OPERATION

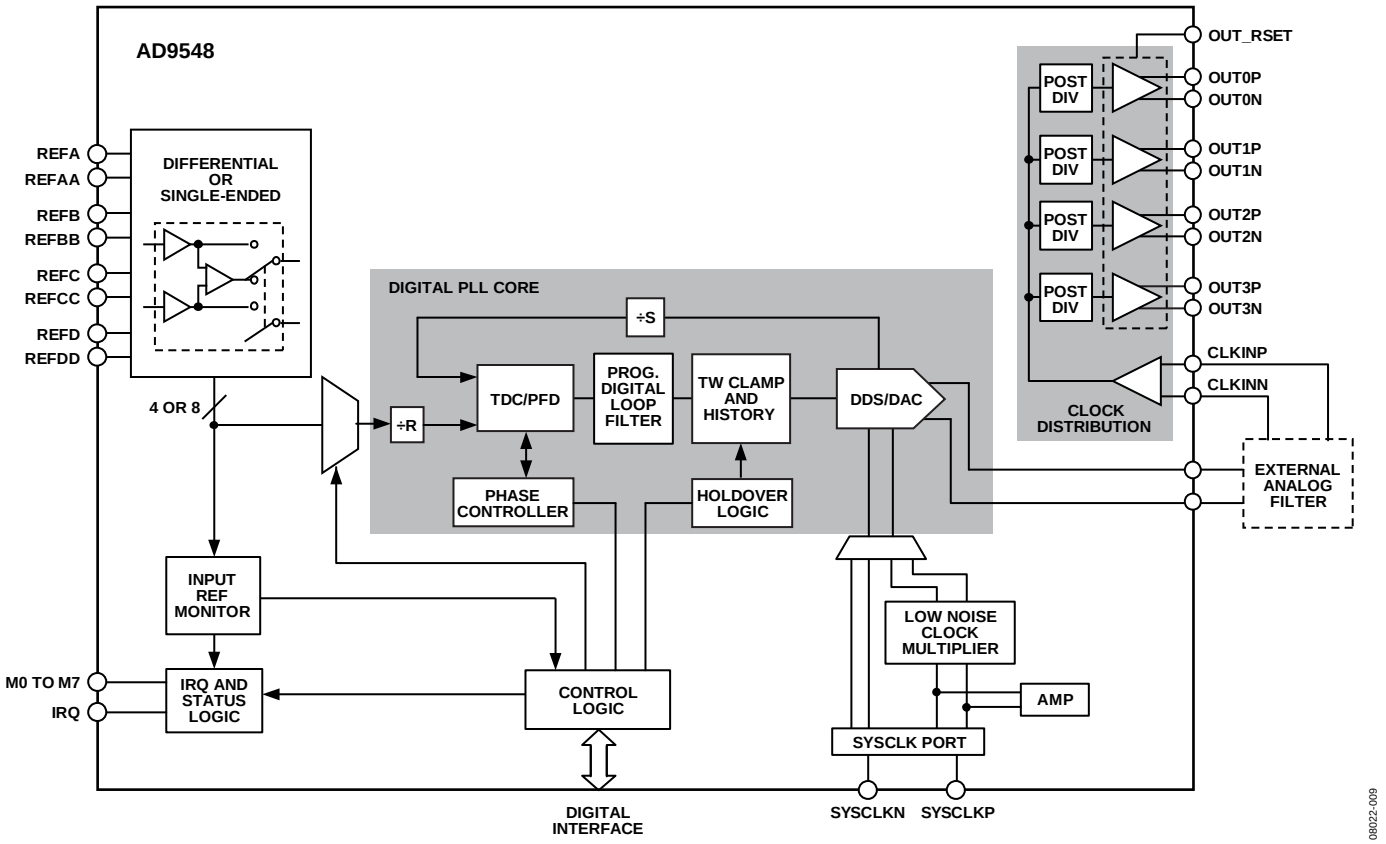


Figure 33. Detailed Block Diagram

OVERVIEW

The AD9548 provides clocking outputs directly related in phase and frequency to the selected (active) reference but with jitter characteristics primarily governed by the system clock. The AD9548 supports up to eight reference inputs and a wide range of reference frequencies. The core of this product is a digital phase-locked loop (DPLL). The DPLL has a programmable digital loop filter that greatly reduces jitter transferred from the active reference to the output. The AD9548 supports both manual and automatic holdover. While in holdover, the AD9548 continues to provide an output as long as the DAC sample clock is present. The holdover output frequency is a time average of the output frequency history just prior to the transition to the holdover condition.

The device offers manual and automatic reference switchover capability if the active reference is degraded or fails completely. A direct digital synthesizer (DDS) and integrated DAC constitute a digitally controlled oscillator (DCO). The DCO output is a sinusoidal signal (450 MHz maximum) at a frequency determined by the active reference frequency and the programmed values of the reference prescaler (R) and feedback divider (S). Although not explicitly shown in Figure 33, the S-divider has both an integer and fractional component, which is similar to a fractional-N synthesizer.

The SYSCLKx input provides the sample clock for the DAC, which is either a directly applied high frequency source or a low frequency source coupled with the integrated PLL-based frequency multiplier. The low frequency option also allows for the use of a crystal resonator connected directly across the SYSCLKx inputs.

The DAC output routes directly off-chip, where an external filter removes the sampling artifacts before returning the signal on-chip at the CLKINx inputs. Once on-chip, an integrated comparator converts the filtered sinusoidal signal to a clock signal (square wave) with very fast rise and fall times.

The clock distribution section provides four output drivers. Each driver is programmable either as a single differential LVPECL/LVDS output or as a dual single-ended CMOS output. Furthermore, each of the four outputs has a dedicated 30-bit programmable postdivider. The clock distribution section operates at up to 725 MHz. This enables use of a band-pass reconstruction filter (for example, a SAW filter) to extract a Nyquist image from the DAC output spectrum, thereby allowing output frequencies that exceed the typical 450 MHz limit at the DAC output.

REFERENCE CLOCK INPUTS

Four pairs of pins provide access to the reference clock receivers. Each pair is configurable either as a single differential receiver or as two independent single-ended receivers. To accommodate input signals with slow rising and falling edges, both the differential and single-ended input receivers employ hysteresis. Hysteresis also ensures that a disconnected or floating input does not cause the receiver to oscillate spontaneously.

When configured for differential operation, the input receivers accommodate either ac- or dc-coupled input signals. The receiver is internally dc biased in order to handle ac-coupled operation.

When configured for single-ended operation, the input receivers exhibit a pull-down load of 45 kΩ (typical). Three user-programmable threshold voltage ranges are available for each single-ended receiver.

REFERENCE MONITORS

The reference monitors depend on a known and accurate system clock period. Therefore, the functioning of the reference monitors is not reliable until the system clock is stable. To avoid an incorrect valid indication, the reference monitors indicate fault status until the system clock stability timer expires (see the System Clock Stability Timer section).

Reference Period Monitor

Each reference input has a dedicated monitor that repeatedly measures the reference period. The AD9548 uses the reference period measurements to determine the validity of the reference based on a set of user provided parameters in the profile register area of the register map (see the Profile Registers (Register 0600 to Register 07FF) section). The AD9548 also uses the reference period monitor to assign a particular reference to a profile when the user programs the device for automatic profile assignment.

The monitor works by comparing the measured period of a particular reference input with the parameters stored in the profile register assigned to that same reference input. The parameters include the reference period, an inner tolerance, and an outer tolerance. A 50-bit number defines the reference period in units of femtoseconds. The 50-bit range allows for a reference period entry of up to 1.125 sec. However, an actual reference signal with a period in excess of 1 sec is beyond the recommended operating range of the device. A 20-bit number defines the inner and outer tolerances. The value stored in the register is the reciprocal of the tolerance specification. For example, a tolerance specification of 50 ppm yields a register value of 1/(50 ppm) = 1/0.000050 = 20,000 (0x04E20).

The use of two tolerance values provides hysteresis for the monitor decision logic. The inner tolerance applies to a previously faulted reference and specifies the largest period tolerance that a previously faulted reference can exhibit before it qualifies as nonfaulted. The outer tolerance applies to an already nonfaulted reference. It specifies the largest period tolerance that a nonfaulted reference can exhibit before being faulted.

To produce decision hysteresis, the inner tolerance must be less than the outer tolerance. That is, a faulted reference must meet tighter requirements to become nonfaulted than a nonfaulted reference must meet to become faulted.

Reference Validation Timer

Each reference input has a dedicated validation timer. The validation timer establishes the amount of time that a previously faulted reference must remain fault free before the AD9548 declares it nonfaulted. The timeout period of the validation timer is programmable via a 16-bit register (see the validation register contained within each of the eight profile registers in the register map, Address 0600 to Address 07FF). The 16-bit number stored in the validation register represents units of milliseconds, which yields a maximum timeout period of 65,535 ms.

Note that a validation period of 0 must be programmed to disable the validation timer. With the validation timer disabled, the user must validate a reference manually via the force validation timeout register (Address 0A0E).

Reference Redetect Timer

Each reference input has a dedicated redetect timer. The redetect timer is useful only with the device programmed for automatic profile selection. The redetect timer establishes the amount of time that a reference must remain faulted before the AD9548 attempts to reassign it to a new profile. The timeout period of the redetect timer is programmable via a 16-bit register (see the redetect timeout register contained within each of the eight profile registers in the register map, Address 0600 to Address 07FF). The 16-bit number stored in the redetect timeout register represents units of milliseconds, which yields a maximum timeout period of 65,535 ms.

Note that a timeout period of 0 must be programmed to disable the redetect timer.

Reference Validation Override Control

Register 0A0E to Register 0A10 provide the user with the ability to override the reference validation logic enabling a certain level of troubleshooting capability. Each of the eight input references has a dedicated block of validation logic as shown in Figure 34. The state of the valid signal at the output is what defines a particular reference as valid (1) or not (0), which includes the validation period (if activated) as prescribed by the validation timer. The override controls are the three control bits on the left side of the diagram.

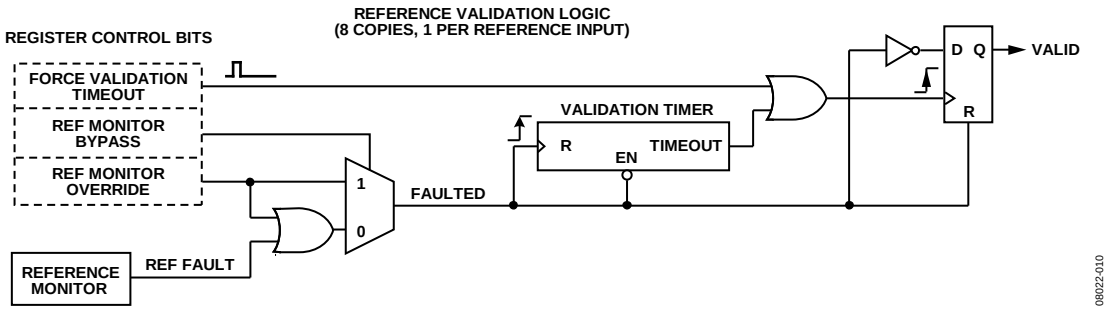


Figure 34. Reference Validation Override

The main feature to note is that any time faulted = 1, the output latch is reset, which forces valid = 0 (indicating an invalid reference) regardless of the state of any other signal. Under the default condition (that is, all three control bits are 0), the reference monitor is the primary source of the validation process. This is because, under the default condition, the ref fault signal from the reference monitor is identically equal to the faulted signal.

The function of the faulted signal is fourfold.

- Any time faulted = 1, then valid = 0, regardless of the state of any other control signal. Therefore, faulted = 1 indicates an invalid reference.
- Any time the faulted signal transitions from 0 to 1 (that is, from nonfaulted to faulted), the validation timer is momentarily reset, which means that, once it is enabled, it must exhaust its full counting sequence before it expires.
- When faulted = 0 (that is, the reference is not faulted), the validation timer is allowed to perform its timing sequence. When faulted = 1 (that is, the reference is faulted), the validation timer is reset and halted.
- The faulted signal passes through an inverter, converting it to a nonfaulted signal, which appears at the input of the valid latch. This allows the valid latch to capture the state of the nonfaulted signal when the validation timer expires.

The ref monitor bypass control bit enables bypassing of the ref fault signal generated by the reference monitor. When ref monitor bypass = 1, the state of the faulted signal is dictated by the ref monitor override control bit. This is useful when the user relies on an external reference monitor rather than the internal monitor resident in the device. The user programs the ref monitor override bit based on the status of the external monitor. On the other hand, when ref monitor bypass = 0, the ref monitor override control bit allows the user to manually test the operation of both the valid latch and the validation timer. In this case, the user relies on the signal generated by the internal reference monitor (ref fault) but uses the ref monitor override bit to emulate a faulted reference. That is, when ref monitor override = 1, then faulted = 1, but when ref monitor override = 0, then faulted = ref fault.

In addition, the user has the ability to emulate a timeout of the validation timer via the appropriate force validation timeout control bit in Register 0A0E. Writing a Logic 1 to any of these autoclearing bits triggers the valid latch, which is identically equivalent to a timeout of the validation timer.

REFERENCE PROFILES

The AD9548 has eight independent profile registers. A profile register contains 50 bytes that establish a particular set of device parameters. Each of the eight input references can be assigned to any one of the eight profiles (that is, more than one reference can be assigned to the same profile). The profiles allow the user to prescribe the specific device functionality that should take effect when one of the input references (assigned to the profile) becomes the active reference. Each profile register has the same format and stores the following device parameters:

- Reference priority
- Reference period value (in femtoseconds)
- Inner tolerance value (1/tolerance)
- Outer tolerance value (1/tolerance)
- Validation timer value (milliseconds)
- Redetect timer value (milliseconds)
- Digital loop filter coefficients
- Reference prescaler setting (R-divider)
- Feedback divider settings (S, U, and V)
- DPLL phase lock detector threshold level
- DPLL phase lock detector fill rate
- DPLL phase lock detector drain rate
- DPLL frequency lock detector threshold level
- DPLL frequency lock detector fill rate
- DPLL frequency lock detector drain rate

Reference-to-Profile Assignment Control

The user can manually assign a reference to a profile or let the device make the assignment automatically. The manual reference profile selection register (Address 0503 to Address 0506) is where the user programs whether a reference-to-profile assignment is manual or automatic. The manual reference profile selection register is a 4-byte register partitioned into eight half bytes (or nibbles). The eight nibbles form a one-to-one correspondence with the eight reference inputs: one nibble for REF A, the next for REF AA, and so on. For a reference configured as a differential input, however, the device ignores the nibble associated with the two-letter input. For example, if

the B reference is differential, then only the REFB nibble matters (the device ignores the REFBB nibble).

The MSB of each nibble is the manual profile bit, whereas the three LSBs of each nibble identify one of the eight profiles (0 to 7). A Logic 1 for the manual profile bit assigns the associated reference to the profile identified by the three LSBs of the nibble. A Logic 0 for the manual profile bit configures the associated reference for automatic reference-to-profile assignment (the three LSBs are ignored in this case). Note that references configured for automatic reference-to-profile assignment require activation (see the Reference-to-Profile Assignment State Machine section).

Reference-to-Profile Assignment State Machine

The functional flexibility of the AD9548 resides in the way that it assigns a particular input reference to one of the eight reference profiles. The reference-to-profile assignment state machine effectively builds a reference-to-profile table that maps the index of each input reference to a profile (see Table 22).

Each entry in the profile column consists of a profile number (0 to 7) or a null value. A null value appears when a reference-to-profile assignment does not exist for a particular reference input (following a reset, for example). The information in Table 22 appears in the register map (Register 0D0C to Register 0D13) so that the user has access to the reference-to-profile assignments on a real-time basis. Register 0D0C contains the information for REF A, Register 0D0D contains the information for REF AA, and so on to Register 0D13 for REF DD. Bit 7 of each register is the null indicator for that particular reference. If Bit 7 = 0, then the profile assignment for that particular reference is null. If Bit 7 = 1, then that particular reference is assigned to the profile (0 to 7) identified by Bits[6:4]. Note that Bits[6:4] are meaningless unless Bit 7 = 1.

Table 22. Reference-to-Profile Table

Reference Input	Reference Index	Profile
A	0	Profile number (or null value)
AA	1	Profile number (or null value)
B	2	Profile number (or null value)
BB	3	Profile number (or null value)
C	4	Profile number (or null value)
CC	5	Profile number (or null value)
D	6	Profile number (or null value)
DD	7	Profile number (or null value)

Following a reset, the reference-to-profile assignment state machine is inactive to avoid improperly assigning a reference to a profile before the system clock stabilizes. The reason is that the state machine relies on accurate information from the reference monitors, which, in turn, rely on a stable system clock. Because the reference-to-profile assignment state machine is inactive at power-up, the user must initiate it manually by writing to the reference profile detect register (Address 0A0D). The state machine activates immediately, unless the system clock is not stabilized, in which case, activation occurs upon expiration of the system clock stability timer. Note that initialization of the state machine is on a per-reference basis. That is, each reference input is associated with an independent initialization control bit.

Once initialized for processing a reference, the state machine continuously monitors that reference until the occurrence of a device reset. This is true even when the user programs a reference for manual profile selection, in which case, the state machine associated with that particular reference operates with its activity masked. The masked background activity allows for seamless operation if the user subsequently reprograms the reference for automatic profile selection.

Reference-to-Profile Assignment

When a reference is programmed for manual profile assignment (see Register 0503 to Register 0506), the reference-to-profile assignment state machine simply puts the programmed manual profile number into the profile column of the reference-to-profile table (see Table 22) in the row associated with the appropriate reference. However, when the user programs a reference for automatic profile assignment, the state machine must figure out which profile to assign to the reference.

As long as a null entry appears in the reference-to-profile table for a particular input reference, the validation logic for that reference enters a period estimation mode. Note that a null entry is the default state following a reset, but it also occurs when a reference redetect timer expires. The period estimation mode enables the validation logic to make a blind estimate of the period of the input reference with a tolerance of 0.1%. The validation logic remains in the period estimation mode until it successfully estimates the reference period.

Upon a successful reference period measurement by the validation logic, the state machine compares the measured period to the nominal reference period programmed into each of the eight profiles. The state machine assigns the reference to the profile with the closest match to the measured period. If more than one profile exactly matches the reference period, then the state machine chooses the profile with the lowest numeric index. For example, if the reference period in both Profile 3 and Profile 5 matches the measured period, then Profile 3 is given the assignment.

To safeguard against making a poor reference-to-profile assignment, the state machine ensures that the measured reference period is within 6.25% of the nominal reference period that appears in the closest match profile. Otherwise, the state machine does not make a profile assignment and leaves the null entry in the reference-to-profile table.

As long as there are input references programmed for automatic profile assignment, and for which the profile assignment is null, the state machine continues to cycle through those references searching for a profile match. Furthermore, unless an input

reference is assigned to a profile, it is considered invalid and excluded as a candidate for a reference switchover.

REFERENCE SWITCHOVER

An attractive feature of the AD9548 is its versatile reference switchover capability. The flexibility of the reference switchover functionality resides in a sophisticated prioritization algorithm coupled with register-based controls. This scheme provides the user with maximum control over the state machine that handles reference switchover.

The main reference switchover control resides in the loop mode register (Address 0A01). The user selection mode bits (Register 0A01, Bits[4:3]) allow the user to select one of the reference switchover state machine's four operating modes, as follows:

- Automatic mode (Address A01, Bits[4:3] = 00)
- Fallback mode (Address 0A01, Bits[4:3] = 01)
- Holdover mode (Address 0A01, Bits[4:3] = 10)
- Manual mode (Address 0A01, Bits[4:3] = 11)

In automatic mode, a fully automatic priority-based algorithm selects which reference is the active reference. When programmed for automatic mode, the device ignores the user selection reference bits (Register 0A01, Bits[2:0]). However, when programmed for any of the other three modes, the device makes use of the user reference bits. These bits specify a particular input reference (000 = REF A, 001 = REF AA ..., 111 = REF DD).

In fallback mode, the user reference is the active reference whenever it is valid. Otherwise, the device switches to a new reference using the automatic, priority-based algorithm.

In holdover mode, the user reference is the active reference whenever it is valid. Otherwise, the device switches to holdover mode.

In manual mode, the user reference is the active reference whether it is valid or not. Note that, when using this mode, the user must program the reference-to-profile assignment (see register 0503 to Register 0506) as manual for the particular reference declared as the user reference. The reason is that if the user reference fails and its redetect timer expires, then its profile assignment (shown in Table 22) becomes null. This means that the active reference (user reference) does not have an assigned profile, which places the AD9548 into an undefined state.

The user also has the option to force the device directly into holdover or free-run operation via the user holdover and user free-run bits (Register 0A01, Bit 6 and Bit 5, respectively]). In free-run mode, the free running frequency tuning word register (Address 0300 to Address 0305) defines the DDS output frequency. In holdover mode, the DDS output frequency depends on the holdover control settings (see the Holdover section).

Automatic Priority-Based Reference Switchover

The AD9548 has a two-tiered, automatic, priority-based algorithm that is in effect for both automatic and fallback reference switchover. The algorithm relies on the fact that each reference profile contains both a selection priority and a promoted priority. The selection and promoted priority values range from 0 (highest priority) to 7 (lowest priority). The selection priority determines the order in which references are chosen as the active reference. The promoted priority is a separate priority value given to a reference only after it becomes the active reference.

An automatic reference switchover occurs on failure of the active reference or when a previously failed reference becomes valid and its selection priority is higher than the promoted priority of the currently active reference (assuming that the automatic or fallback reference switchover is in effect). When performing an automatic reference switchover, the AD9548 chooses a reference based on the priority settings within the profiles. That is, the device switches to the reference with the highest selection priority (lowest numeric priority value). It does so by using the reference-to-profile table (see Table 22) to determine the reference associated with the profile exhibiting the highest priority.

If multiple references share the same profile, then the device chooses the reference having the lowest index value. For example, if the A, B, and CC references (Index 0, Index 2, and Index 5, respectively) share the same profile, then a switchover to Reference A occurs because Reference A has the lowest index value. Note, however, that only valid references are included in switchover of the selection process. The switchover control logic ignores any reference with a status indication of invalid.

The promoted priority parameter allows the user to assign a higher priority to a reference after it becomes the active reference. For example, suppose four references have a selection priority of 3 and a promoted priority of 1, and the remaining references have a selection priority or 2 and a promoted priority of 2. Now, assume that one of the Priority 3 references becomes active because all of the Priority 2 references have failed. Sometime later, however, a Priority 2 reference becomes valid. The switchover logic normally attempts to automatically switch over to the Priority 2 reference because it has higher priority than the presently active Priority 3 reference. However, because the Priority 3 reference is active, its promoted priority of 1 is in effect. This is a higher priority than the newly validated reference's priority of 2, so the switchover does not occur. This mechanism enables the user to give references preferential treatment while they are selected as the active reference. An example of promoted vs. nonpromoted priority switching appears in state diagram form in Figure 35. Figure 36 shows a block diagram of the interrelationship between the reference inputs, monitors, validation logic, profile selection, and priority selection functionality.

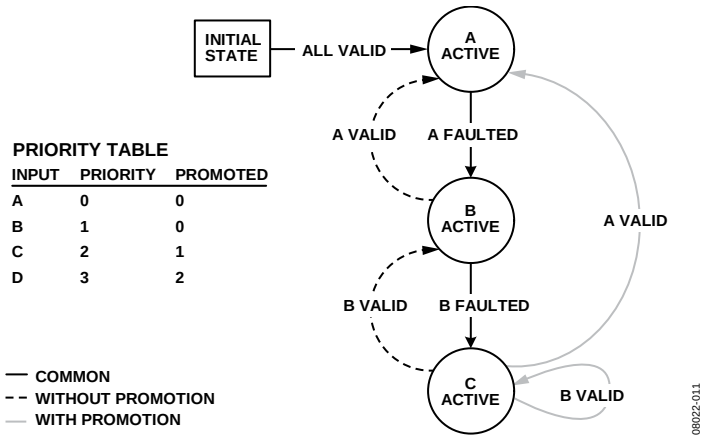


Figure 35. Example of Priority Promotion

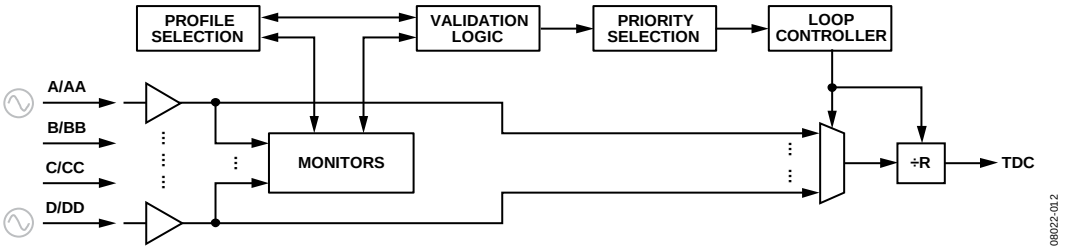


Figure 36. Reference Clock Block Diagram

Phase Build-Out Reference Switching

Phase build-out reference switching is the term given to a reference switchover that completely masks any phase difference between the previous reference and the new reference. That is, there is virtually no phase change detectable at the output when a phase build-out switchover occurs.

The AD9548 handles phase build-out switching based on whether the new reference is a phase master. A phase master is any reference with a selection priority value that is less than the phase master threshold priority value (that is, higher priority). The phase master threshold priority value resides in the phase build-out switching register (Address 0507), whereas the selection priority resides in the profile registers (Address 0600 to Address 07FF). By default, the phase master threshold priority is 0; therefore, no references can be phase masters until the user changes the phase master threshold priority.

Whenever the AD9548 switches from one reference to another, it compares the selection priority value stored in the profile assigned to the new reference with the phase master threshold priority. The AD9548 performs a phase build-out switchover only if the new reference is not a phase master.

Hitless Reference Switching (Phase Slew Control)

Hitless reference switching is the term given to a reference switchover that limits the rate of change of the phase of the output clock while the PLL is in the process of acquiring phase lock. This prevents the output frequency offset from becoming excessive.

The all-digital nature of the DPLL core (see the Digital PLL (DPLL) Core section) gives the user numerical control of the rate at which phase changes occur at the DPLL output. When enabled, a phase slew controller monitors the phase difference between the feedback and reference inputs to the DPLL. The phase slew controller has the ability to place a user-specified limit on the rate of change of phase, thus providing a mechanism for hitless reference switching.

The user sets a limit on the rate of change of phase by storing the appropriate value in the 16-bit phase slew rate limit register (Address 0316 to Address 0317). The 16-bit word (representing ns/sec) puts an upper bound on the rate of change of the phase at the output of the DPLL during a reference switchover. A phase slew rate value of 0 (default) disables the phase slew controller.

The accuracy of the phase slew controller depends on both the phase slew limit value and the system clock frequency. Generally, an increase in the phase slew rate limit value or a decrease in the system clock frequency tends to reduce the error. As such, the accuracy is best for the largest phase slew limit value and the lowest system clock frequency. For example, assuming the use of a 1 GHz system clock, a phase slew limit value of 315 ns/sec (or more) ensures an error of less than 10%, whereas a phase slew rate limit value above ~3100 ns/sec ensures an error of less than 1%. On the other hand, assuming the use of a 500 MHz system clock, the same phase slew rate limit values ensure an error of less than 5% or 0.5%, respectively.

DIGITAL PLL (DPLL) CORE

DPLL Overview

A diagram of the digital PLL core of the AD9584 appears in Figure 37. The phase/frequency detector, feedback path, lock detectors, phase offset, and phase slew rate limiting that comprise this second generation DPLL are all digital implementations.

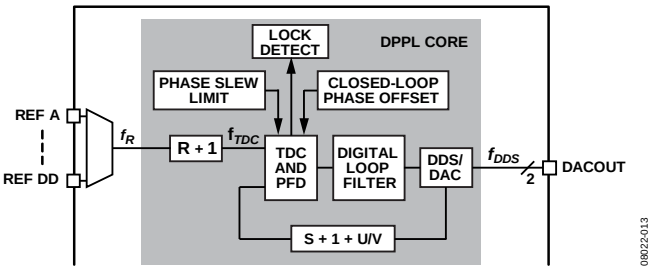


Figure 37. Digital PLL Core

The start of the DPLL signal chain is the reference signal, f_R, which is the frequency of the reference input. A reference prescaler reduces the frequency of this signal by an integer factor, R + 1, where R is the 30-bit value stored in the appropriate profile register and 0 ≤ R ≤ 1,073,741,823. Therefore, the frequency at the output of the R-divider (or the input to TDC) is

$$f_{TDC} = \frac{f_R}{R+1}$$

A time-to-digital converter (TDC) samples the output of the R-divider. The TDC/PFD produces a time series of digital words and delivers them to the digital loop filter. The digital loop filter offers the following advantages:

- Determination of the filter response by numeric coefficients rather than by discrete component values
- The absence of analog components (R/L/C), which eliminates tolerance variations due to aging
- The absence of thermal noise associated with analog components
- The absence of control node leakage current associated with analog components (a source of reference feed-through spurs in the output spectrum of a traditional analog PLL)

The digital loop filter produces a time series of digital words at its output and delivers them to the frequency tuning input of a DDS, with the DDS replacing the function of the VCO in an analog PLL. The digital words from the loop filter tend to steer the DDS frequency toward frequency and phase lock with the input signal (f_{TDC}). The DDS provides an analog output signal via an integrated DAC, effectively mimicking the operation of an analog VCO.

The DPLL includes a feedback divider that causes the DDS to operate at an integer-plus-fractional multiple (S + 1 + U/V) of f_{TDC}. S is the 30-bit value stored in the profile register and has a range of 7 ≤ S ≤ 1,073,741,823. U and V are the 10-bit numerator and denominator values of the optional fractional divide component and are also stored in the profile register. Together they establish the nominal DDS frequency (f_{DDS}), given by

$$f_{DDS} = \frac{f_R}{R+1}\left(S+1+\frac{U}{V}\right)$$

Normally, fractional-N designs exhibit distinctive phase noise and spurious artifacts resulting from the modulation of the integer divider based on the fractional value. Such is not the case for the AD9548 because it uses a purely digital means to determine phase errors. Because the phase errors incurred by modulating the feedback divider are deterministic, it is possible to compensate for them digitally. The result is a fractional-N PLL with no discernable modulation artifacts.

TDC/PFD

The TDC is a highly integrated functional block that incorporates both analog and digital circuitry. There are two pins associated with the TDC that the user must connect to external components. Figure 38 shows the recommended component values and their connections.

For best performance, place components as close as possible to the device pins. Components with low effective series resistance (ESR) and low parasitic inductance yield the best results.

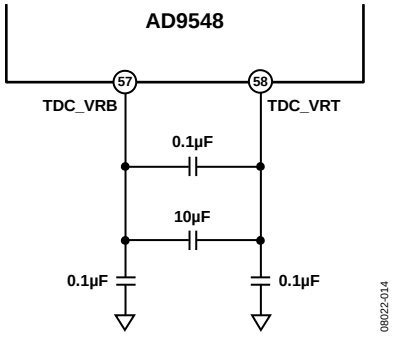


Figure 38. TDC Pin Connections

The phase-frequency detector (PFD) is an all-digital block. It compares the digital output from the TDC (which relates to the active reference edge) with the digital word from the feedback block (which relates to the rollover edge of the DDS accumulator after division by the feedback divider). It uses a digital code pump and digital integrator (rather than a conventional charge pump and capacitor) to generate the error signal that steers the DDS frequency toward phase lock.

Closed-Loop Phase Offset

The all-digital nature of the TDC/PFD provides for numerical control of the phase offset between the reference and feedback edges. This allows the user to adjust the relative timing of the distribution output edges relative to the reference input edges by programming the 40-bit fixed phase lock offset register

(Address 030F to Address 0313). The 40-bit word is a signed (twos complement) number that represents units of picoseconds.

In addition, the user can adjust the closed-loop phase offset (positive or negative) in incremental fashion. To do so, program the desired step size in the 16-bit incremental phase lock offset step size register (Address 0314 to Address 0315). This is an unsigned number that represents units of picoseconds. The programmed step size is added to the current closed-loop phase offset each time the user writes a Logic 1 to the increment phase offset bit (Register 0A0C, Bit 0). Conversely, the programmed step size is subtracted from the current closed-loop phase offset each time the user writes a Logic 1 to the decrement phase offset bit (Register 0A0C, Bit 1). The serial I/O port control logic clears both of these bits automatically. The user can remove the incrementally accumulated phase by writing a Logic 1 to the reset incremental phase offset bit (Register 0A0C, Bit 2), which is also cleared automatically. Alternatively, rather than using the serial I/O port, the multifunction pins can be set up to perform the increment, decrement, and clear functions.

Note that the incremental phase offset is completely independent of the offset programmed into the fixed phase lock offset register. However, if the phase slew limiter is active (see the Hitless Reference Switching (Phase Slew Control) section), then any instantaneous change in closed-loop phase offset (fixed or incremental) will be subject to possible slew limitation by the action of the phase slew limiter.

Programmable Digital Loop Filter

The AD9548 loop filter is a third order digital IIR filter that is analogous to the third order analog loop shown in Figure 39.

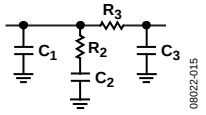


Figure 39. Third Order Analog Loop Filter

The filter requires four coefficients as shown in Figure 40. The AD9548 evaluation board software automatically generates the required loop filter coefficient values based on the user's design criteria. The Calculating Digital Filter Coefficients section contains the design equations for calculating the loop filter coefficients manually.

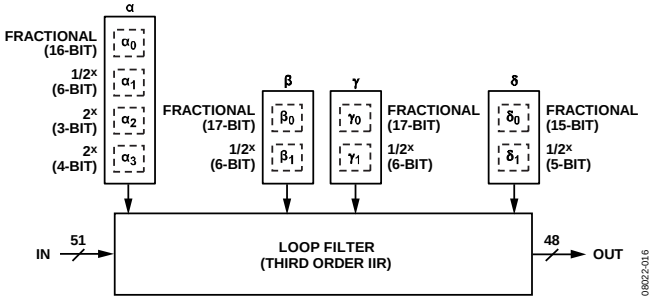


Figure 40. Third Order Digital IIR Loop Filter

Each coefficient has a fractional component representing a value from 0 up to, but not including, unity. Each coefficient also has an exponential component representing a power of 2 with a negative exponent. That is, the user enters a positive number (x) that the hardware interprets as a negative exponent of two (2^{-x}). Thus, the β, γ, and δ coefficients always represent values less than unity. The α coefficient, however, has two additional exponential components, but the hardware interprets these as a positive exponent of 2 (that is, 2^{x}). This allows the α coefficient to be a value greater than unity. The positive exponent appears as two separate terms in order to provide sufficient dynamic range.

DPLL Phase Lock Detector

The DPLL contains an all-digital phase lock detector. The user controls the threshold sensitivity and hysteresis of the phase detector via the profile registers.

The phase lock detector behaves in a manner analogous to water in a tub (see Figure 41). The total capacity of the tub is 4096 units with −2048 denoting empty, 0 denoting the 50% point, and +2048 denoting full. The tub also has a safeguard to prevent overflow. Furthermore, the tub has a low water mark at −1024 and a high water mark at +1024. To change the water level, the user adds water with a fill bucket or removes water with a drain bucket. The user specifies the size of the fill and drain buckets via the 8-bit fill rate and drain rate values in the profile registers.

The water level in the tub is what the lock detector uses to determine the lock and unlock conditions. Whenever the water level is below the low water mark (−1024), the detector indicates an unlock condition. Conversely, whenever the water level is above the high water mark (+1024), the detector indicates a lock condition. While the water level is between the marks, the detector simply holds its last condition. This concept appears graphically in Figure 41, with an overlay of an example of the instantaneous water level (vertical) vs. time (horizontal) and the resulting lock/unlock states.

During any given PFD phase error sample, the detector either adds water with the fill bucket or removes water with the drain bucket (one or the other but not both). The decision of whether to add or remove water depends on the threshold level specified by the user. The phase lock threshold value is a 16-bit number stored in the profile registers and is expressed in picoseconds. Thus, the phase lock threshold extends from 0 ns to ±65.535 ns and represents the magnitude of the phase error at the output of the PFD.

The phase lock detector compares each phase error sample at the output of the PFD to the programmed phase threshold value. If the absolute value of the phase error sample is less than or equal to the programmed phase threshold value, then the detector control logic dumps one fill bucket into the tub. Otherwise, it removes one drain bucket from the tub. Notice that it is not the polarity of the phase error sample, but its magnitude relative to the phase threshold value, that determines whether to fill or drain. If more filling is taking place than

draining, the water level in the tub eventually rises above the high water mark (+1024), which causes the phase lock detector to indicate lock. If more draining is taking place than filling, then the water level in the tub eventually falls below the low water mark (−1024), which causes the phase lock detector to indicate unlock. The ability to specify the threshold level, fill rate, and drain rate enables the user to tailor the operation of the phase lock detector to the statistics of the timing jitter associated with the input reference signal.

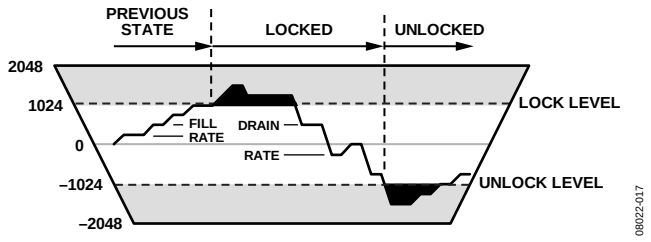


Figure 41. Lock Detector Diagram

Note that whenever the AD9548 enters the free-run or holdover mode, the DPLL phase lock detector indicates unlocked. In addition, whenever the AD9548 performs a reference switch-over, the state of the lock detector prior to the switch is preserved during the transition period.

DPLL Frequency Lock Detector

The operation of the frequency lock detector is identical to that of the phase lock detector. The only difference is that the fill or drain decision is based on the period deviation between the reference and feedback signals of the DPLL instead of the phase error at the output of the PFD.

The frequency lock detector uses a 24-bit frequency threshold register specified in units of picoseconds. Thus, the frequency threshold value extends from 0 µs to ±16.777215 µs. It represents the magnitude of the difference in period between the reference and feedback signals at the input to the DPLL. For example, if the reference signal is 1.25 MHz and the feedback signal is 1.38 MHz, then the period difference is approximately 75.36 ns ($|1/1{,}250{,}000 - 1/1{,}380{,}000| \approx 75.36$ ns).

DIRECT DIGITAL SYNTHESIZER

DDS Overview

One of the primary building blocks of the digital PLL is a direct digital synthesizer (DDS). The DDS behaves like a sinusoidal signal generator. The frequency of the sinusoid generated by the DDS is determined by a frequency tuning word (FTW), which is a digital (that is, numeric) value. Unlike an analog sinusoidal generator, a DDS uses digital building blocks and operates as a sampled system. Thus, it requires a sampling clock (f_S) that serves as the fundamental timing source of the DDS. The accumulator behaves as a modulo-2^{48} counter with a programmable step size (FTW). A block diagram of the DDS appears in Figure 42.

The input to the DDS is the 48-bit FTW. The FTW serves as a step size value. On each cycle of f_S, the accumulator adds the value of the FTW to the running total at its output. For example, given FTW = 5, the accumulator counts by fives, incrementing on each f_S cycle. Over time, the accumulator reaches the upper end of its capacity (2^{48} in this case), at which point, it rolls over but retains the excess. The average rate at which the accumulator rolls over establishes the frequency of the output sinusoid. The average rollover rate of the accumulator establishes the output frequency (f_{DDS}) of the DDS and is given by

$$f_{DDS} = \left(\frac{FTW}{2^{48}}\right) f_S$$

Solving this equation for FTW yields

$$FTW = \text{round}\left[2^{48}\left(\frac{f_{DDS}}{f_S}\right)\right]$$

For example, given that f_S = 1 GHz and f_{DDS} = 155.52 MHz, then FTW = 437,749,988,378,041 (0x27D028A1DFB9).

Note that the minimum DAC output frequency is 62.5 MHz; therefore, normal operation requires an FTW that yields an output frequency in excess of this lower bound.

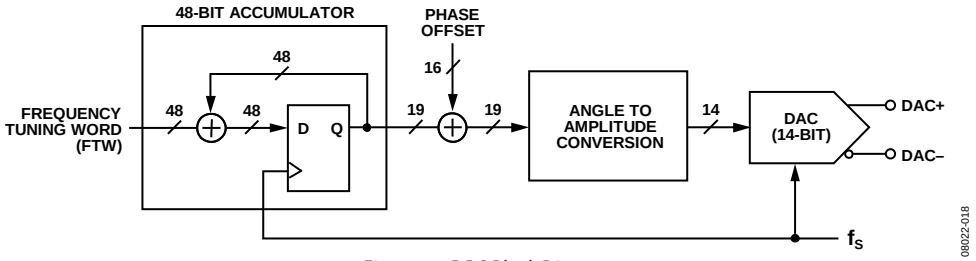


Figure 42. DDS Block Diagram

DDS Phase Offset

The relative phase of the sinusoid generated by the DDS is numerically controlled by adding a phase offset word to the output of the DDS accumulator. This is accomplished via the open loop phase offset register (Address 030D to Address 030E), which is a programmable 16-bit value (Δphase). The resulting phase offset, ΔΦ (in radians), is given by

$$\Delta\Phi = 2\pi\left(\frac{\Delta phase}{2^{16}}\right)$$

Phase offset and relative time offset are directly related. The time offset is $(\Delta phase/2^{16})/f_{DDS}$ (in seconds), where f_{DDS} is the output frequency of the DDS (in hertz).

DAC Output

The output of the digital core of the DDS is a time series of numbers representing a sinusoidal waveform. The DAC translates the numeric values to an analog signal. The DAC output signal appears at two pins that constitute a balanced current source architecture (see Figure 43).

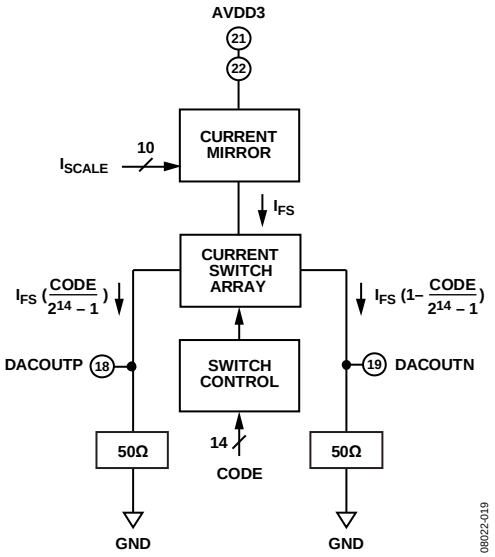


Figure 43. DAC Output Pins

The value of I_{FS} is programmable via the 10-bit DAC full-scale current word in the DAC current register (Address 0213 to Address 0214). The value of the 10-bit word (I_{SCALE}) sets I_{FS} according to the following formula:

$$I_{FS} = 120\ \mu A \times \left(72 + \left(\frac{3}{16}\right) I_{SCALE}\right)$$

TUNING WORD PROCESSING

The frequency tuning words that dictate the output frequency of the DDS come from one of three sources (see Figure 44).

- The free running frequency tuning word register
- The output of the digital loop filter
- The output of the tuning word history processor

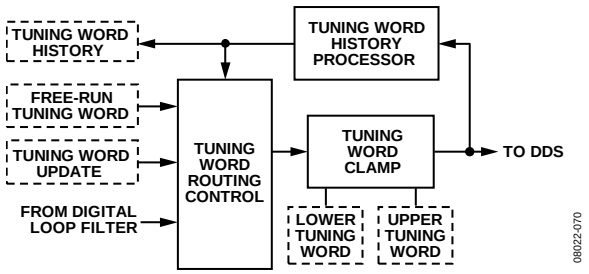


Figure 44. Tuning Word Processing

When the DPLL is in free-run mode, the DDS tuning word is the value stored in the free running frequency tuning word register (Address 0300 to Address 0305). When the DPLL is operating normally (closed loop), the DDS tuning word comes from the output of the digital loop filter, which changes dynamically in order to maintain phase lock with the input reference signal (assuming that the device has not performed an automatic switch to holdover mode). When the DPLL is in holdover mode, the DDS tuning word depends on a historical record of past tuning words during the time that the DPLL operated in closed-loop mode.

However, regardless of the operating mode, the DDS output frequency is ultimately subject to the boundary conditions imposed by the frequency clamp logic, as explained in the Frequency Clamp section.

Frequency Clamp

The user controls the frequency clamp boundaries via the pull-in range limits registers (Address 0307 to Address 030C). These registers allow the user to fix the DDS output frequency between an upper and lower bound with a granularity of 24 bits. Note that these upper and lower bounds apply regardless of the frequency tuning word that appears at the input to the DDS. The register value relates to the absolute upper or lower frequency bound (f_{CLAMP}) as

$$f_{CLAMP} = f_S \times (N/2^{24})$$

Where N is the value stored in the upper- or lower-limit register,and f_S is the system sample rate.

Even though the frequency clamp limits put a bound on the DDS output frequency, the DPLL is still free to steer the DDS frequency within the clamp limits. The default register values set the clamp range from 0 Hz (dc) to f_S, effectively eliminating the frequency clamp functionality until the user alters the register values.

Frequency Tuning Word History

The AD9548 has the ability to track the history of the tuning word samples generated by the DPLL digital loop filter output. It does so by periodically computing the average tuning word value over a user-specified interval. The user programs the interval via the 24-bit history accumulation timer register (Address 0318 to Address 031A). This 24-bit value represents a time interval (T_{AVG}) in milliseconds that extends from 1 ms to a maximum of 4:39:37.215 (hr:min:sec).

Note that history accumulation timer = 0 should not be programmed because it may cause improper device operation.

The control logic performs a calculation of the average tuning word during the T_{AVG} interval and stores the result in the holdover history register (Address 0D14 to Address 0D19). Computation of the average for each T_{AVG} interval is independent of the previous interval (that is, the average is a memoryless average as opposed to a true moving average). In addition, at the end of each T_{AVG} interval, the device generates an internal strobe pulse. The strobe pulse sets the history updated bit in the IRQ monitor register (assuming the bit is enabled via the IRQ mask register). Furthermore, the strobe pulse is available as an output signal via the multifunction pins (see the Multifunction Pins (M0 to M7) section).

History accumulation begins whenever the device switches to a new reference. By default, the device clears any previous history when it switches to a new reference. Furthermore, the user can clear the tuning word history under software control via Register 0A03, Bit 2, or under hardware control via the multifunction pins (see the Multifunction Pins (M0 to M7) section). However, the user has the option of programming the device to retain (rather than clear) the old history by setting the persistent history bit (Register 031B, Bit 3).

Whenever the tuning word history is nonexistent (that is, after a power-up, reset, or switchover to a new reference with the persistent history bit cleared), the device waits for the history accumulation timer (T_{AVG}) to expire before storing the first history value in the holdover history register.

In cases where T_{AVG} is quite large (4½ hours, for example), a problem arises in that the first averaged result does not become available until the full T_{AVG} interval passes. Thus, it is possible that as much as 4½ hours can elapse before the first averaged result is available. If the device has to switch to holdover mode during this time, a tuning word history is not available.

To alleviate this problem, the user has access to the incremental average bits in the history mode register (Register 031B, Bits[2:0]). If the history has been cleared, then this 3-bit value, K ($0 \le K \le 7$), specifies the number of intermediate averages to take during the first, and only the first, T_{AVG} interval. When K = 0, no intermediate averages are calculated; therefore, the first average occurs after interval T_{AVG} (the default operating mode). However, if K = 4, for example, four intermediate averages are taken during the first T_{AVG} interval.

These average computations occur at $T_{AVG}/16$, $T_{AVG}/8$, $T_{AVG}/4$, $T_{AVG}/2$, and T_{AVG} (notice that the denominator exhibits a sequence of powers of 2 beginning with $T_{AVG}/2^K$). The calculation of intermediate averages occurs only during the first T_{AVG} interval. All subsequent average computations occur at evenly spaced intervals of T_{AVG}.

LOOP CONTROL STATE MACHINE

The loop control state machine is responsible for monitoring, initiating, and sequencing changes to the DPLL loop. Generally, it automatically controls the transition between input references and the entry and exit of holdover mode. In controlling loop state changes, the state machine also arbitrates the application of new loop filter coefficients, divider settings, and phase detector offsets based on the profile settings. The user can manually force the device into holdover or free-run mode via the loop mode register (Address 0A01), as well as force the selection of a specific input reference.

Switchover

Switchover occurs when the loop controller switches directly from one input reference to another. Functionally, the AD9548 handles a reference switchover by briefly entering holdover mode and then immediately recovering. During the switchover event, however, the AD9548 preserves the status of the lock detectors to avoid phantom unlock indications.

Holdover

The holdover state of the DPLL is an open-loop operating mode. That is, the device no longer operates as a closed-loop system. Instead, the output frequency remains constant and is dependent on the device programming and availability of tuning word history.

If a tuning word history exists (see the Frequency Tuning Word History section), then the holdover frequency is the average frequency just prior to entering the holdover state. If there is no tuning word history, then the holdover frequency depends on the state of the single sample fallback bit in the history mode register (Register 031B, Bit 4). If the single sample fallback bit is Logic 0, then the holdover frequency is the frequency defined in the free running frequency tuning word register (Address 0300 to Address 0305). If the single sample fallback bit is Logic 1, then the holdover frequency is the last instantaneous frequency output by the DDS just prior to the device entering holdover mode (note that this is not the average frequency prior to holdover).

The initial holdover frequency accuracy depends on the loop bandwidth of the DPLL and the time elapsed to compute a tuning word history. The longer the historical average, the more accurate the initial holdover frequency (assuming a drift-free system clock). Furthermore, the stability of the system clock establishes the stability and long-term accuracy of the holdover output frequency. Another consideration is the 48-bit frequency tuning resolution of the DDS and its relationship to fractional frequency error, $\Delta f_O/f_O$, as follows:

$$\frac{\Delta f_O}{f_O} = \frac{f_S}{2^{49} f_O}$$

where, f_S is the sample rate of the output DAC, and f_O is the DDS output frequency.

The worst-case scenario is maximum f_S (1 GHz) and minimum f_O (62.5 MHz), which yields $\Delta f_O/f_O = 2.8 \times 10^{-14}$, less than one part in 10 trillion.

Recovery from Holdover

When in holdover and a valid reference becomes available, the device exits holdover operation. The loop state machine restores the DPLL to closed-loop operation, locks to the selected reference, and sequences the recovery of all the loop parameters based on the profile settings for the active reference.

Note that, if the user holdover bit (Register 0A01, Bit 6) is set, the device does not automatically exit holdover when a valid reference is available. However, automatic recovery can occur after clearing the user holdover bit.

SYSTEM CLOCK INPUTS

Functional Description

The system clock circuit provides a low jitter, stable, high frequency clock for use by the rest of the chip. The user has the option of directly driving the SYSCLKx inputs with a high frequency clock source at the desired system clock rate. Alternatively, the SYSCLKx input can be configured to operate in conjunction with the internal SYSCLK PLL. The SYSCLK PLL can synthesize the system clock by means of a crystal resonator connected across the SYSCLKx input pins or by means of direct application of a low frequency clock source.

The SYSCLKx inputs are internally biased to a dc level of ~1 V. Take care to ensure that any external connections do not disturb the dc bias because this may significantly degrade performance. Generally, the recommendation is that the SYSCLKx inputs be ac-coupled to the signal source (except when using a crystal resonator).

System Clock Period

Many of the user-programmable parameters of the AD9548 have absolute time units. To make this possible, the AD9548 requires a priori knowledge of the period of the system clock. To accommodate this requirement, the user programs the 21-bit nominal system clock period in the nominal SYSCLK period register (Address 0106 to Address 0108). The contents of this register reflect the actual period of the system clock in femtoseconds. The user must properly program this register to ensure proper operation of the device because many of its subsystems rely on this value.

System Clock Details

A block diagram of the system clock appears in Figure 45. The signal at the SYSCLKx input pins becomes the internally buffered DAC sampling clock (f_S) via one of three paths.

- High frequency direct (HF)
- Low frequency synthesized (LF)
- Crystal resonator synthesized (XTAL)

Note that both the LF and XTAL paths require the use of the SYSCLK PLL (see the SYSCLK PLL Multiplier section).

The main purpose of the HF path is to allow the direct use of a high frequency (500 MHz to 1 GHz) external clock source for clocking the AD9548. This path is optimized for high frequency and low noise floor. Note that the HF input also provides a path to SYSCLK PLL (see the SYSCLK PLL Multiplier section), which includes an input divider (M) programmable for divide-by -1, -2, -4, or -8. The purpose of the divider is to limit the frequency at the input to the PLL to less than 150 MHz (the maximum PFD rate).

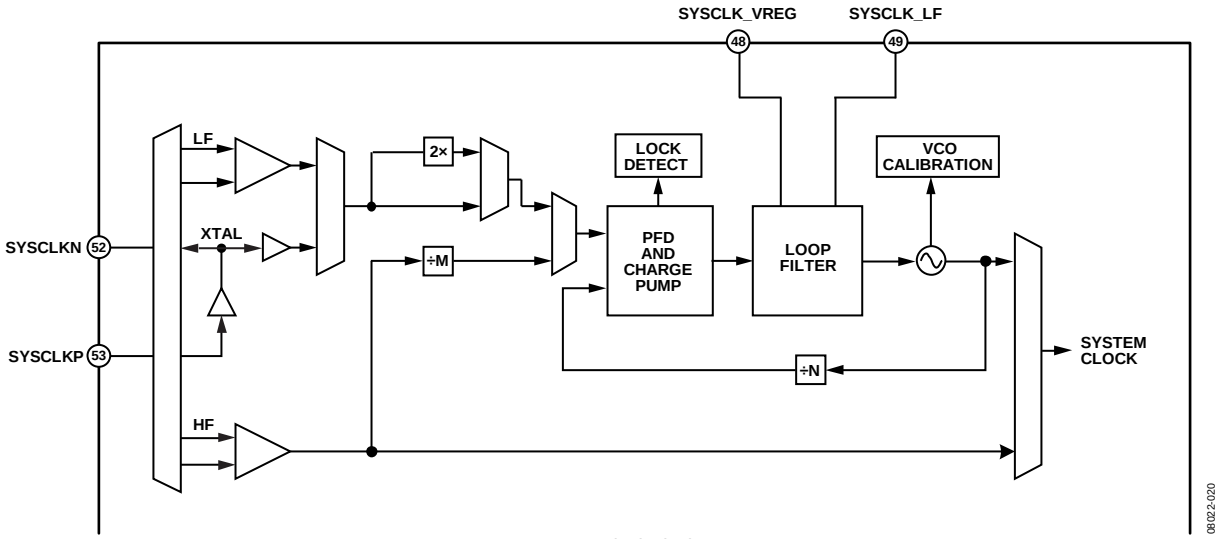


Figure 45. System Clock Block Diagram

The LF path permits the user to provide an LVPECL, LVDS, CMOS, or sinusoidal low frequency clock for multiplication by the integrated SYSCLK PLL. The LF path handles input frequencies from 3.5 MHz up to 100 MHz. However, when using a sinusoidal input signal, it is best to use a frequency in excess of 20 MHz. Otherwise, the resulting low slew rate can lead to substandard noise performance. Note that the LF path includes an optional 2× frequency multiplier to double the rate at the input to the SYSCLK PLL and potentially reduce the PLL in-band noise. However, to avoid exceeding the maximum PFD rate of 150 MHz, using the 2× frequency multiplier is valid only for input frequencies below 125 MHz.

The XTAL path enables the connection of a crystal resonator (typically 10 MHz to 50 MHz) across the SYSCLKx input pins. An internal amplifier provides the negative resistance required to induce oscillation. The internal amplifier expects a 3.2 mm × 2.5 mm AT cut, fundamental mode crystal with a maximum motional resistance of 100 Ω. The following crystals, listed in alphabetical order, may meet these criteria. Note that, whereas these crystals may meet the preceding criteria according to their data sheets, Analog Devices, Inc., does not guarantee their operation with the AD9548 nor does Analog Devices endorse one crystal manufacturer/supplier over another.

- AVX/Kyocera CX3225SB
- ECS ECX-32
- Epson/Toyocom TSX-3225
- Fox FX3225BS
- NDK NX3225SA
- Siward SX-3225

SYSCLK PLL MULTIPLIER

The SYSCLK PLL multiplier is an integer-N design and relies on an integrated LC tank and VCO. It provides a means to convert a low frequency clock input to the desired system clock frequency, f_S (900 MHz to 1 GHz). The SYSCLK PLL multiplier accepts input signals between 3.5 MHz and 500 MHz, but frequencies in excess of 150 MHz require the M-divider to ensure compliance with the maximum PFD rate (150 MHz). The PLL contains a feedback divider (N) that is programmable for divide values between 6 and 255. The nominal VCO gain is 70 MHz/V.

Lock Detector

The SYSCLK PLL has a built-in lock detector. Register 0100, Bit 2 determines whether the lock detector is active. When active (default), the user controls the sensitivity of the lock detector via the lock detect divider bits (Register 0100, Bits[1:0]).

Note that 0 must be written to the system clock stability timer (Register 0106 to Register 0108) whenever the lock detector is disabled (Register 0100, Bit 2 = 1).

The SYSCLK PLL phase detector operates at the PFD rate, which is f_{VCO}/N. Each PFD sample indicates whether the reference and feedback signals are phase aligned (within a certain threshold range).

While the PLL is in the process of acquiring a lock condition, the PFD samples typically consist of an arbitrary sequence of in-phase and out-of-phase indications. As the PLL approaches complete phase lock, the number of consecutive in-phase PFD samples grows larger. Thus, one way of indicating a locked condition is to count the number of consecutive in-phase PFD samples and if it exceeds a certain value, then declare the PLL locked.

This is exactly the role of the lock detect divider bits. When the lock detector is enabled (Register 0100, Bit 2 = 0), the lock detect divider bits determine the number of consecutive in-phase decisions required (128, 256, 512, or 1024) before the lock detector declares a locked condition. The default setting is 128.

Charge Pump

The charge pump operates in either automatic or manual mode based on the charge pump mode bit (Register 0100, Bit 6).

When Register 0100, Bit 6 = 0, the AD9548 automatically selects the appropriate charge pump current based on the N-divider value. Note that the user cannot control the charge pump current bits (Register 0100, Bits[5:3]) in automatic mode. When Register 0100, Bit 6 = 1, the user determines the charge pump current via the charge pump current bits (Register 0100, Bits[5:3]). The charge pump current varies from 125 µA to 1 mA in 125 µA steps. The default setting is 500 µA.

SYSCLK PLL Loop Filter

The AD9548 has an internal second order loop filter that establishes the loop dynamics for input signals between 12.5 MHz and 100 MHz. By default, the device uses the internal loop filter. However, an external loop filter option is available by setting the external loop filter enable bit (Register 0100, Bit 7). This bypasses the internal loop filter and allows the device to use an externally connected second order loop filter, as shown in Figure 46.

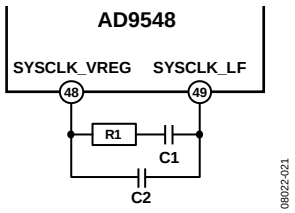


Figure 46. External Loop Filter Schematic

To determine the external loop filter components, the user decides on the desired open loop bandwidth (f_{OL}) and phase margin (ϕ). These parameters allow calculation of the loop filter components, as follows:

$$R1 = \frac{\pi N f_{OL}}{I_{CP} K_{VCO}}\left(1 + \frac{1}{\sin(\varphi)}\right)$$

$$C1 = \frac{I_{CP} K_{VCO} \tan(\varphi)}{2N(\pi f_{OL})^2}$$

$$C2 = \frac{I_{CP} K_{VCO}}{N(2\pi f_{OL})^2}\left(\frac{1 - \sin(\varphi)}{\cos(\varphi)}\right)$$

where $K_{VCO} = 7 \times 10^7$ V/ns (typical), I_{CP} is the programmed charge pump current (amperes), N is the programmed feedback divider value, f_{OL} is the desired open-loop bandwidth (in hertz), and Φ is the desired phase margin (in radians).

For example, assuming that N = 40, I_{CP} = 0.5 mA, f_{OL} = 400 kHz, and Φ = 50°, then the loop filter calculations yield R1 = 3.31 kΩ, C1 = 330 pF, and C2 = 50.4 pF.

System Clock Stability Timer

The system clock stability timer (Register 0106 to Register 0108) is a 20-bit value programmed in milliseconds. If the programmed timer value is 0, then the timer immediately indicates that it has timed out. If the programmed timer value is a nonzero value and the SYSCLK PLL is enabled, then the timer starts timing when the SYSCLK PLL lock detector indicates lock and times out after the prescribed period. However, when the user disables the SYSCLK PLL, then the timer ignores the SYSCLK PLL lock detector and starts timing as soon as the SYSCLK PLL is disabled. The user can monitor the status of the stability timer via Register 0D01, Bit 4, via the multifunction pins or via the IRQ pin.

Note that the system clock stability timer must be programmed before the SYSCLK PLL is either activated or disabled.

SYSCLK PLL Calibration

When using the SYSCLK PLL, it is necessary to calibrate the LC VCO to ensure that the PLL can remain locked to the system clock input signal. Assuming the presence of either an external SYSCLK input signal or a crystal resonator, the calibration process executes after the user sets and then clears the calibrate system clock bit in the cal/sync register (Register 0A02, Bit 0). During the calibration process, the device calibrates the VCO amplitude and frequency. The status of the system clock calibration process is user accessible via the system clock register (Register 0D01, Bit 1). It is also available via the IRQ monitor register (Register 0D02, Bit 1) provided the status bit is enabled via the IRQ mask register.

When the calibration sequence is complete, the SYSCLK PLL eventually attains a lock condition, at which point the system clock stability timer begins its countdown sequence. Expiration of the timer indicates that the SYSCLK PLL is stable, which is reflected in the system clock register (Register 0D01, Bit 4).

Note that the monitors/detectors associated with the input references (REFA/AA – REFD/DD) are internally disabled until the SYSCLK PLL indicates that it is stable.

CLOCK DISTRIBUTION

The clock distribution block of the AD9548 provides an integrated solution for generating multiple clock outputs based on frequency dividing the DPLL output. The distribution output consists of four channels (OUT0 to OUT3). Each of the four output channels has a dedicated divider and output driver, as appears in Figure 47.

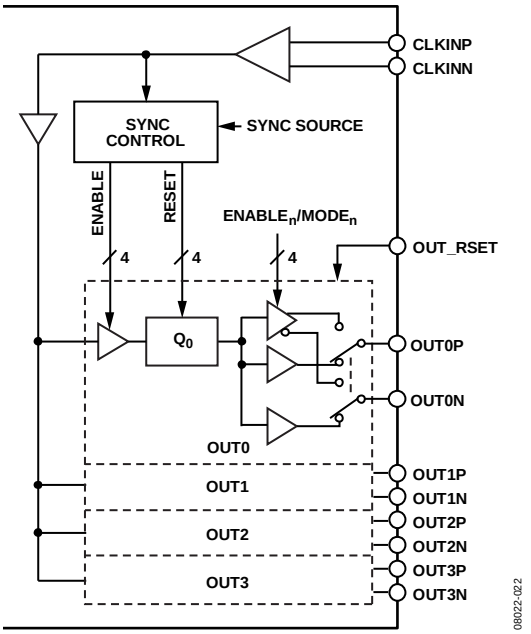


Figure 47. Clock Distribution

Clock Input (CLKINx)

The clock input handles input signals from a variety of logic families (assuming proper terminations and sufficient voltage swing). It also handles sine wave input signals such as those delivered by the DAC reconstruction filter. Its default operating frequency range is 62.5 MHz to 500 MHz.

Super-Nyquist Operation

Typically, the maximum usable frequency at the DAC output is about 45% of the system clock frequency. However, because it is a sampled DAC, its output spectrum contains Nyquist images. Of particular interest are the images appearing in the first Nyquist zone (50% to 100% of the system clock frequency). Super-Nyquist operation takes advantage of these higher frequencies, but this implies that the CLKINx input operates in excess of 500 MHz, which is outside of its default operating limits.

The CLKINx receiver actually consists of two separate receivers: the default receiver and an optional high frequency receiver,

which handles input signals up to 800 MHz. To select the high frequency receiver, write a Logic 1 to Register 0400, Bit 4.

Super-Nyquist operation requires a band-pass filter at the DAC output instead of the usual low-pass reconstruction filter. Super-Nyquist operation is viable as long as the image frequency does not exceed the 800 MHz input range of the receiver. Furthermore, to provide acceptable jitter performance, which is a consideration for image signals with low amplitude, the signal at the CLKINx input must meet the minimum slew rate requirements.

Clock Dividers

The output clock distribution dividers are referred to as Q0 to Q3, corresponding to the OUT0 to OUT3 output channels, respectively. Each divider is programmable with 30 bits of division depth. The actual divider ratio is one more than the programmed register value; therefore, a register value of 3, for example, results in a divide ratio of 4. Thus, each divider offers a range of divide ratios from 1 to 2^{30} (1 to 1,073,741,824).

With an even divide ratio, the output signal always exhibits a 50% duty cycle. When the clock divider is bypassed (a divide ratio of 1), the output duty cycle is the same as the input duty cycle. Odd output divide ratios (excluding 1) exhibit automatic duty cycle correction given by

$$Output\ \ Duty\ Cycle = \frac{N + 2X - 1}{2N}$$

where N (which must be an odd number) is the divide ratio and X is the normalized fraction of the high portion of the input period (that is, $0 < X < 1$).

For example, if N = 5 and the input duty cycle is 20% (X = 0.2), then the output duty cycle is 44%. Note that, when the user programs an output as noninverting, then the device adjusts the falling edge timing to accomplish the duty cycle correction. Conversely, the device adjusts the rising edge timing for an inverted output.

Output Power-Down

Each of the output channels offers independent control of power-down functionality via the distribution settings register (Address 0400). Each output channel has a dedicated power-down bit for powering down the output driver. However, if all four outputs are powered down, the entire distribution output enters a deep sleep mode.

Even though each channel has a channel power-down control signal, it may sometimes be desirable to power down an output driver while maintaining the divider's synchronization with the other channel dividers. This is accomplished by either of the following methods:

- In CMOS mode, use the divider output enable control bit to stall an output. This provides power savings while maintaining dc drive at the output.
- In LVDS/LVPECL mode, place the output in tristate mode (this works in CMOS mode as well).

Output Enable

Each of the output channels offers independent control of enable/disable functionality via the distribution enable register (Address 0401). The distribution outputs use synchronization logic to control enable/disable activity to avoid the production of runt pulses and ensure that outputs with the same divide ratios become active/inactive in unison.

Output Mode

The user has independent control of the operating mode of each of the four output channels via the distribution channel modes register (Address 0404 to Address 0407). The operating mode control includes

- Logic family and pin functionality
- Output drive strength
- Output polarity

The three least significant bits of each of the four distribution channel mode registers comprise the mode bits. The mode value selects the desired logic family and pin functionality of an output channel, as given in Table 23.

Table 23. Output Channel Logic Family and Pin Functionality

Mode Bits [2:0]	Logic Family and Pin Functionality
000	CMOS (both pins)
001	CMOS (positive pin); tristate (negative pin)
010	Tristate (positive pin); CMOS (negative pin)
011	Tristate (both pins)
100	LVDS
101	LVPECL
110	Unused
111	Unused

Regardless of the selected logic family, each is capable of dc operation. However, the upper frequency is limited by the load conditions, drive strength, and impedance matching inherent in each logic family. Practical limitations set the maximum CMOS frequency to approximately 250 MHz, whereas LVPECL and LVDS are capable of 725 MHz.

In addition to the three mode bits, each of the four distribution channel mode registers includes the following control bits:

- Polarity invert
- CMOS phase invert
- Drive strength

The polarity invert bit enables the user to choose between normal polarity and inverted polarity. Normal polarity is the default state. Inverted polarity reverses the representation of Logic 0 and Logic 1 regardless of the logic family.

The CMOS phase invert bit applies only when the mode bits select the CMOS logic family. In CMOS mode, both output pins

of the channel have a dedicated CMOS driver. By default, both drivers deliver identical signals. However, setting the CMOS phase invert bit causes the signal on an OUTxN pin to be the opposite of the signal appearing on the OUTxP pin.

The drive strength bit allows the user to control whether the output uses weak (0) or strong (1) drive capability (applies to CMOS and LVDS but not LVPECL). For the CMOS family, the strong setting implies normal CMOS drive capability, whereas the weak setting implies low capacitive loading and allows for reduced EMI. For the LVDS family, the weak setting provides 3.5 mA drive current for standard LVDS operation, whereas the strong setting provides 7 mA for double terminated or double voltage LVDS operation. Note that 3.5 mA and 7 mA are the nominal drive current values when using the internal current setting resistor.

Output Current Control with an External Resistor

By default, the output drivers have an internal current setting resistor (3.12 kΩ nominal) that establishes the nominal drive current for the LVDS and LVPECL operating modes. Instead of using the internal resistor, the user can set the external distribution resistor bit (Register 0400, Bit 5) and connect an external resistor to the OUT_RSET pin. Note that this feature supports an external resistor value of 3.12 kΩ only, allowing for tighter control of the output current than is possible by using the internal current setting resistor. However, if the user elects to use a nonstandard external resistance, the following equations provide the output drive current as a function of the external resistance (R):

$$I_{LVDS0} = \frac{10.8325}{R}$$

$$I_{LVDS1} = \frac{21.665}{R}$$

$$I_{LVPECL} = \frac{24.76}{R}$$

The numeric subscript associated with the LVDS output current corresponds to the logic state of the drive strength bit in the distribution channel modes register (Address 0404 to Address 0407). For R = 3.12 kΩ, the equations yield I_{LVDS0} = 3.5 mA, I_{LVDS1} = 7.0 mA, and I_{LVPECL} = 8.0 mA. Note that the device maintains a constant 1.238 V (nominal) across the external resistor.

Clock Distribution Synchronization

A block diagram of the distribution synchronization functionality appears in Figure 48. The synchronization sequence begins with the primary synchronization signal, which ultimately results in delivery of a synchronization strobe to the clock distribution logic.

As indicated, the primary synchronization signal originates from four possible sources.

- Direct sync source via the sync distribution bit (Register 0A02, Bit 1)
- Automatic sync source based on frequency or phase lock detection as controlled via the automatic synchronization register (Address 0403)
- Multifunction pin sync source via one of the multifunction pins (M0 to M7)
- EEPROM sync source via the EEPROM

All four sources of the primary synchronization signal are logic OR'd, so any one of them can synchronize the clock distribution output at any time. When using the multifunction pins, the synchronization event is the falling edge of the selected signal. When using the sync distribution bit, the user sets and then clears the bit. The synchronization event is the clearing operation; that is, the Logic 1 to Logic 0 transition of the bit.

The primary synchronization signal can synchronize the distribution output directly or it can enable a secondary synchronization signal. This functionality depends on the two sync source bits in the distribution synchronization register (Register 0402, Bits[5:4]).

When sync source = 00 (direct), the falling edge of the primary synchronization signal synchronizes the distribution output directly.

When sync source = 01, the rising edge of the primary synchronization signal triggers the circuitry that detects a rising edge of the active input reference. The detection of the rising edge is what synchronizes the distribution output.

When sync source = 10, the rising edge of the primary synchronization signal triggers the circuitry that detects a rollover of the DDS accumulator (after processing by the DPLL feedback divider). This corresponds to the zero crossing of the output of the phase-to-amplitude converter in the DDS (less the open-loop phase offset stored in Register 030D to Register 030E). The detection of the DPLL feedback edge is what synchronizes the distribution output.

Active Reference Synchronization (Zero Delay)

Active reference synchronization is the term applied to the case when sync source = 01 (Register 0402, Bits[5:4]). Referring to Figure 48, this means that the active reference sync path is active because Bit 4 = 1, enabling the lower AND gate and disabling the upper AND gate. The edge detector in the active reference sync block monitors the rising edges of the active reference (the mux selects the active reference automatically). The edge detector is armed via the primary synchronization signal, which is one of the four inputs to the OR gate (typically the direct sync source). As soon as the edge detector is armed, its output goes high, which stalls the output dividers in the clock distribution block. Furthermore, once armed, a rising edge from the active reference forces the output of the edge detector low. This restarts the output dividers, thereby synchronizing the clock distribution block.

The term zero delay applies because it provides a means to edge align the output signal with the active input reference signal. Typically, zero-delay architectures use the output signal in the feedback loop of a PLL to track input/output edge alignment. Active reference synchronization, however, operates open loop. That is, synchronization of the output via the distribution synchronization logic occurs on a single edge of the active reference.

The fact that an active reference edge triggers the falling edge of the synchronization pulse means that the falling edge is asynchronous to the signal that clocks the distribution output dividers (CLKINx). Therefore, the output clock distribution logic reclocks the internal synchronization pulse to synchronize it with the CLKINx signal. This means that the output dividers restart after a deterministic delay associated with the reclocking circuitry. This deterministic delay has two components. The first deterministic delay component is four or five periods of the CLKINx signal. The one period uncertainty is due to the unknown position of the asynchronous reference clock edge relative to the CLKINx signal. The second deterministic delay component is one output period of the distribution divider.

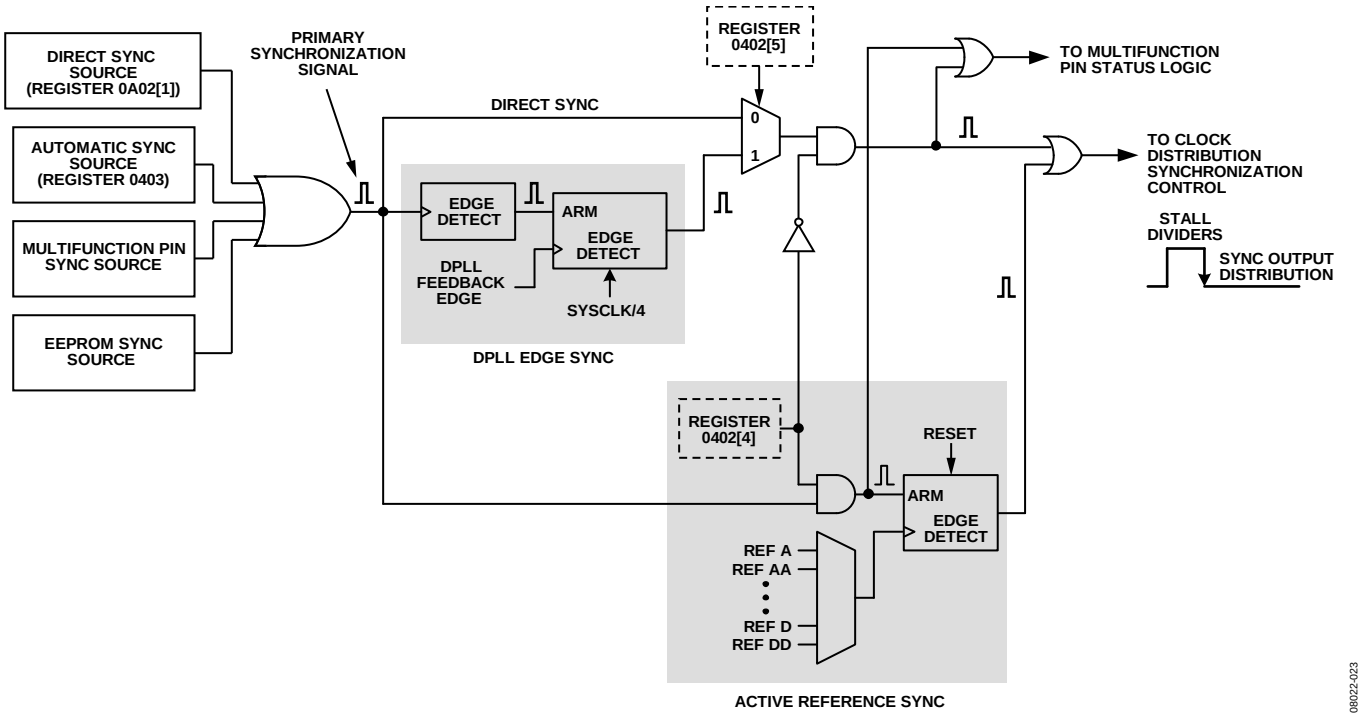


Figure 48. Output Synchronization Block Diagram

The deterministic delay, expressed as $t_{LATENCY}$ in the following equation is a function of the frequency division factor (Q_n) of the channel divider associated with the zero-delay channel.

$$t_{LATENCY} = (Q_n + 4) \times t_{CLK_IN}$$

or

$$t_{LATENCY} = (Q_n + 5) \times t_{CLK_IN}$$

In addition to deterministic delay, there is random delay (t_{PROP}) associated with the propagation of the reference signal through the input reference receiver, as well as the propagation of the clock signal through the clock distribution logic. The total delay is

$$t_{DELAY} = t_{LATENCY} + t_{PROP}$$

The user can compensate for t_{DELAY} by using the phase offset controls of the device to move the edge timing of the distribution output signal relative to the input reference edge. One method is to use the open-loop phase offset registers (Address 030D to Address 030E) for timing adjustment. However, be sure to use sufficiently small phase increments to make the adjustment. Too large a phase step can result in the clock distribution logic missing a CLKINx edge, thus ruining the edge alignment process. The appropriate phase increment depends on the transient response of any external circuitry connected between the DACOUTx and CLKINx pins.

The other method is to use the closed-loop phase offset registers (Address 030F to Address 0315) for timing adjustment. However, be sure to use a sufficiently small phase vs. time profile. Changing the phase too quickly can cause the DPLL to lose lock, thus ruining the edge alignment process. Note that the AD9548 phase slew limit register (Address 0316 to Address 0317) can be used to limit the rate of change of phase automatically, thereby mitigating the potential loss-of-lock problem.

To guarantee synchronization of the output dividers, it is important to make any edge timing adjustments after the synchronization event. Furthermore, when making timing adjustments, the distribution outputs can be disabled and then enabled after the adjustment is complete. This prevents the device from generating output clock signals during the timing adjustment process.

Note that the form of zero-delay synchronization described here does not track propagation time variations within the distribution clock input path or the reference input path (on or off chip) over temperature, supply, and so on. It is strictly a one-time synchronization event.

Synchronization Mask

Each output channel has dedicated synchronization mask bits (Register 0402, Bits[3:0]). When the mask bit associated with a particular channel is set, then that channel does not respond to the synchronization signal. This allows the device to operate with the masked channels active and the unmasked channels stalled while they wait for a synchronization pulse.

STATUS AND CONTROL

MULTIFUNCTION PINS (M0 TO M7)

The AD9548 has eight digital CMOS I/O pins (M0 to M7) that are configurable for a variety of uses. The function of these pins is programmable via the register map. Each pin can control or monitor an assortment of internal functions based on the contents of Register 0200 to Register 0207. To monitor an internal function with a multifunction pin, write a Logic 1 to the most significant bit of the register associated with the desired multifunction pin. The value of the seven least significant bits of the register defines the control function, as shown in Table 24.

Table 24. Multifunction Pin Output Functions, Register 0200 to Register 0207 (Bit 7 = 1)

Bits[6:0] Value	Output Function	Source Proxy
0	Static Logic 0	
1	Static Logic 1	
2	System clock divided by 32	
3	Watchdog timer output	
4	EEPROM upload in progress	Register 0D00, Bit 0
5	EEPROM download in progress	Register 0D00, Bit 1
6	EEPROM fault detected	Register 0D00, Bit 2
7	SYSCLK PLL lock detected	Register 0D01, Bit 0
8	SYSCLK PLL calibration in progress	Register 0D01, Bit 1
9	Unused	
10	Unused	
11	SYSCLK PLL stable	Register 0D01, Bit 4
12 to 15	Unused	
16	DPLL free running	Register 0D0A, Bit 0
17	DPLL active	Register 0D0A, Bit 1
18	DPLL in holdover	Register 0D0A, Bit 2
19	DPLL in reference switchover	Register 0D0A, Bit 3
20	Active reference: phase master	Register 0D0A, Bit 6
21	DPLL phase locked	Register 0D0A, Bit 4
22	DPLL frequency locked	Register 0D0A, Bit 5
23	DPLL phase slew limited	Register 0D0A, Bit 7
24	DPLL frequency clamped	Register 0D0B, Bit 7
25	Tuning word history available	Register 0D0B, Bit 6
26	Tuning word history updated	Register 0D05, Bit 4
27 to 31	Unused	
32	Reference A fault	Register 0D0C, Bit 2
33	Reference AA fault	Register 0D0D, Bit 2
34	Reference B fault	Register 0D0E, Bit 2
35	Reference BB fault	Register 0D0F, Bit 2
36	Reference C fault	Register 0D10, Bit 2
37	Reference CC fault	Register 0D11, Bit 2
38	Reference D fault	Register 0D12, Bit 2
39	Reference DD fault	Register 0D13, Bit 2
40 to 47	Unused	
48	Reference A valid	Register 0D0C, Bit 3
49	Reference AA valid	Register 0D0D, Bit 3
50	Reference B valid	Register 0D0E, Bit 3
51	Reference BB valid	Register 0D0F, Bit 3
52	Reference C valid	Register 0D10, Bit 3
53	Reference CC valid	Register 0D11, Bit 3
54	Reference D valid	Register 0D12, Bit 3
55	Reference DD valid	Register 0D13, Bit 3
56 to 63	Unused	
64	Reference A active eference	Register 0D0B, Bits[2:0]
65	Reference AA active reference	Register 0D0B, Bits[2:0]
66	Reference B active reference	Register 0D0B, Bits[2:0]
67	Reference BB active reference	Register 0D0B, Bits[2:0]
68	Reference C active reference	Register 0D0B, Bits[2:0]
69	Reference CC active reference	Register 0D0B, Bits[2:0]
70	Reference D active reference	Register 0D0B, Bits[2:0]
71	Reference DD active reference	Register 0D0B, Bits[2:0]
72 to 79	Unused	
80	Clock distribution sync pulse	Register 0D03, Bit 3
81 to 127	Unused	

To control an internal function with a multifunction pin, write a Logic 0 to the most significant bit of the register associated with the desired multifunction pin. The monitored function depends on the value of the seven least significant bits of the register, as shown in Table 25.

Table 25. Multifunction Pin Input Functions, Register 0200 to Register 0207 (Bit 7 = 0)

Bits[6:0] Value	Output Function	Destination Proxy
0	Unused (default)	
1	I/O update	Register 0005, Bit 0
2	Full power-down	Register 0A00, Bit 0
3	Watchdog reset	Register 0A03, Bit 0
4	IRQ reset	Register 0A03, Bit 1

Bits[6:0] Value	Output Function	Destination Proxy
5	Tuning word history reset	Register 0A03, Bit 2
6 to 15	Unused	
16	Holdover	Register 0A01, Bit 6
17	Free run	Register 0A01, Bit 5
18	Reset incremental phase offset	Register 0A0C, Bit 2
19	Increment incremental phase offset	Register 0A0C, Bit 0
20	Decrement incremental phase offset	Register 0A0C, Bit 1
21 to 31	Unused	
32	Override Reference Monitor A	Register 0A0F, Bit 0
33	Override Reference Monitor AA	Register 0A0F, Bit 1
34	Override Reference Monitor B	Register 0A0F, Bit 2
35	Override Reference Monitor BB	Register 0A0F, Bit 3
36	Override Reference Monitor C	Register 0A0F, Bit 4
37	Override Reference Monitor CC	Register 0A0F, Bit 5
38	Override Reference Monitor D	Register 0A0F, Bit 6
39	Override Reference Monitor DD	Register 0A0F, Bit 7
40 to 47	Unused	
48	Force validation Timeout A	Register 0A0E, Bit 0
49	Force validation Timeout AA	Register 0A0E, Bit 1
50	Force validation Timeout B	Register 0A0E, Bit 2
51	Force validation Timeout BB	Register 0A0E, Bit 3
52	Force validation Timeout C	Register 0A0E, Bit 4
53	Force validation Timeout CC	Register 0A0E, Bit 5
54	Force validation Timeout D	Register 0A0E, Bit 6
55	Force validation Timeout DD	Register 0A0E, Bit 7
56 to 63	Unused	
64	Enable OUT0	Register 0401, Bit 0
65	Enable OUT1	Register 0401, Bit 1
66	Enable OUT2	Register 0401, Bit 2
67	Enable OUT3	Register 0401, Bit 3
68	Enable OUT0, OUT1, OUT2, OUT3	Register 0401, Bits[3:0]
69	Sync clock distribution outputs	Register 0A02, Bit 1
70 to 127	Unused	

If more than one multifunction pin operates on the same control signal, then internal priority logic ensures that only one multifunction pin serves as the signal source. The selected pin is the one with the lowest numeric suffix. For example, if both M3 and M7 operate on the same control signal, then M3 is used as the signal source and the redundant pins are ignored.

At power-up, the multifunction pins can be used to force the device into certain configurations as defined in the initial pin programming section. This functionality, however, is valid only during power-up or following a reset, after which the pins can be reconfigured via the serial programming port or via the EEPROM.

IRQ PIN

The AD9548 has a dedicated interrupt request (IRQ) pin. The IRQ pin output mode register (Register 0208, Bits[1:0]) controls how the IRQ pin asserts an interrupt based on the value of the two bits, as follows:

00—The IRQ pin is high impedance when deasserted and active low when asserted and requires an external pull-up resistor (this is the default operating mode).

01—The IRQ pin is high impedance when deasserted and active high when asserted and requires an external pull-down resistor.

10—The IRQ pin is Logic 0 when deasserted and Logic 1 when asserted.

11—The IRQ pin is Logic 1 when deasserted and Logic 0 when asserted.

The AD9548 asserts the IRQ pin whenever any of the bits in the IRQ monitor register (Address 0D02 to Address 0D09) are Logic 1. Each bit in this register is associated with an internal function capable of producing an interrupt. Furthermore, each bit of the IRQ monitor register is the result of a logical AND of the associated internal interrupt signal and the corresponding bit in the IRQ mask register (Address 0209 to Address 0210). That is, the bits in the IRQ mask register have a one-to-one correspondence with the bits in the IRQ monitor register. Whenever an internal function produces an interrupt signal and the associated IRQ mask bit is set, then the corresponding bit in the IRQ monitor register is set. The user should be aware that clearing a bit in the IRQ mask register removes only the mask associated with the internal interrupt signal. It does not clear the corresponding bit in the IRQ monitor register.

The IRQ pin is the result of a logical OR of all the IRQ monitor register bits. Thus, the AD9548 asserts the IRQ pin so long as any of the IRQ monitor register bits are Logic 1. Note that it is possible to have multiple bits set in the IRQ monitor register. Therefore, when the AD9548 asserts the IRQ pin, it may indicate an interrupt from several different internal functions. The IRQ monitor register provides the user with a means to interrogate the AD9548 to determine which internal function(s) produced the interrupt.

Typically, when the AD9548 asserts the IRQ pin, the user interrogates the IRQ monitor register to identify the source of the interrupt request. After servicing an indicated interrupt, the user should clear the associated IRQ monitor register bit via the IRQ clearing register (Address 0A04 to Address 0A0B). The bits in the IRQ clearing register have a one-to-one correspondence with the bits in the IRQ monitor register. Note that the IRQ clearing register is autoclearing. The IRQ pin remains asserted until the user clears all of the bits in the IRQ monitor register that indicate an interrupt.

It is also possible to collectively clear all of the IRQ monitor register bits by setting the reset all IRQs bit in the reset function register (Register 0A03, Bit 1). Note that this is an autoclearing bit. Setting this bit results in deassertion of the IRQ pin. Alternatively, the user can program any of the multifunction pins to clear all IRQs. This allows the user to clear all IRQs by means of a hardware pin rather than by a serial I/O port operation.

WATCHDOG TIMER

The watchdog timer is a general-purpose programmable timer. To set the timeout period, the user writes to the 16-bit watchdog timer register (Address 0211 to Address 0212). A value of 0 in this register disables the timer. A nonzero value sets the timeout period in milliseconds, giving the watchdog timer a range of 1 ms to 65.535 sec. The relative accuracy of the timer is approximately 0.1% with an uncertainty of 0.5 ms.

If enabled, the timer runs continuously and generates a timeout event whenever the timeout period expires. The user has access to the watchdog timer status via the IRQ mechanism and the multifunction pins (M0 to M7). In the case of the multifunction pins, the timeout event of the watchdog timer is a pulse that lasts 32 system clock periods.

There are two ways to reset the watchdog timer (thereby preventing it from causing a timeout event). The first is by writing a Logic 1 to the autoclearing reset watchdog bit in the reset function register (Register 0A03, Bit 0). Alternatively, the user can program any of the multifunction pins to reset the watchdog timer. This allows the user to reset the timer by means of a hardware pin rather than by a serial I/O port operation.

EEPROM

EEPROM Overview

The AD9548 contains an integrated 2048-byte, electrically erasable, programmable read-only memory (EEPROM). The AD9548 can be configured to perform a download at power-up via the multifunction pins (M3 to M7), but uploads and downloads can also be done on demand via the EEPROM control register (Address 0E00 to Address 0E03).

The EEPROM provides the ability to upload and download configuration settings to and from the register map. Figure 49 shows a functional diagram of the EEPROM.

Register 0E10 to Register 0E3F represent a 48-byte scratch pad that enables the user to store a sequence of instructions for transferring data to the EEPROM from the device settings portion of the register map. Note that the default values for these registers provide a sample sequence for saving/retrieving all of the AD9548 EEPROM-accessible registers. Figure 49 shows the connectivity between the EEPROM and the controller that manages data transfer between the EEPROM and the register map.

The controller oversees the process of transferring EEPROM data to and from the register map. There are two modes of operation handled by the controller: saving data to the EEPROM (upload mode) or retrieving data from the EEPROM (download mode). In either case, the controller relies on a specific instruction set.

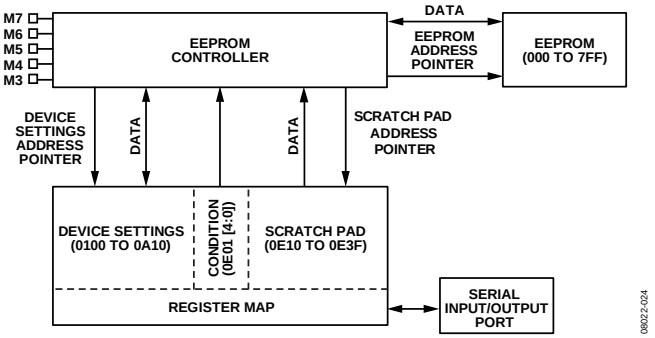


Figure 49. EEPROM Functional Diagram

Table 26. EEPROM Controller Instruction Set

Instruction Value (Hex)	Instruction Type	Bytes Required	Description
00 to 7F	Data	3	A data instruction tells the controller to transfer data to or from the device settings part of the register map. A data instruction requires two additional bytes that together indicate a starting address in the register map. Encoded in the data instruction is the number of bytes to transfer, which is one more than the instruction value.
80	I/O update	1	When the controller encounters this instruction while downloading from the EEPROM, it issues a soft I/O update (see Register 0005 in Table 41).
A0	Calibrate	1	When the controller encounters this instruction while downloading from the EEPROM, it initiates a system clock calibration sequence (see Register 0A02 in Table 120).
A1	Distribution sync	1	When the controller encounters this instruction while downloading from the EEPROM, it issues a sync pulse to the output distribution synchronization (see Register 0A02 in Table 120).
B0 to CF	Condition	1	B1 to CF are condition instructions and correspond to Condition 1 through Condition 31, respectively. B0 is the null condition instruction. See the EEPROM Conditional Processing section for details.
FE	Pause	1	When the controller encounters this instruction in the scratch pad while uploading to the EEPROM, it resets the scratch pad address pointer and holds the EEPROM address pointer at its last value. This allows storage of more than one instruction sequence in the EEPROM. Note that the controller does not copy this instruction to the EEPROM during upload.
FF	End	1	When the controller encounters this instruction in the scratch pad while uploading to the EEPROM, it resets both the scratch pad address pointer and the EEPROM address pointer and then enters an idle state. When the controller encounters this instruction while downloading from the EEPROM, it resets the EEPROM address pointer and then enters an idle state.

EEPROM Instructions

Table 26 lists the EEPROM controller instruction set. The controller recognizes all instruction types whether it is in upload or download mode, except for the pause instruction, which it only recognizes in upload mode.

The I/O update, calibrate, distribution sync, and end instructions are mostly self-explanatory. The others, however, warrant further detail, as described in the following paragraphs.

Data instructions are those that have a value from 00 to 7F. A data instruction tells the controller to transfer data between the EEPROM and the register map. The controller needs the following two parameters to carry out the data transfer:

- The number of bytes to transfer
- The register map target address

The controller decodes the number of bytes to transfer directly from the data instruction itself by adding one to the value of the instruction. For example, the data instruction, 1A, has a decimal value of 26; therefore, the controller knows to transfer 27 bytes (one more than the value of the instruction). Whenever the controller encounters a data instruction, it knows to read the next two bytes in the scratch pad because these contain the register map target address.

Note that, in the EEPROM scratch pad, the two registers that comprise the address portion of a data instruction have the MSB of the address in the D7 position of the lower register address. The bit weight increases left to right, from the lower register address to the higher register address. Furthermore, the starting address always indicates the lowest numbered register map address in the range of bytes to transfer. That is, the controller always starts at the register map target address and counts upward regardless of whether the serial I/O port is operating in I^2C, SPI LSB-first, or SPI MSB-first mode.

As part of the data transfer process during an EEPROM upload, the controller calculates a 1-byte checksum and stores it as the final byte of the data transfer. As part of the data transfer process during an EEPROM download, however, the controller again calculates a 1-byte checksum value but compares the newly calculated checksum with the one that was stored during the upload process. If an upload/download checksum pair does not match, the controller sets the EEPROM fault status bit. If the upload/download checksums match for all data instructions encountered during a download sequence, the controller sets the EEPROM complete status bit.

Condition instructions are those that have a value from B0 to CF. Condition instructions B1 to CF represent Condition 1 to Condition 31, respectively. The B0 condition instruction is

special because it represents the null condition (see the EEPROM Conditional Processing section).

A pause instruction, like an end instruction, is stored at the end of a sequence of instructions in the scratch pad. When the controller encounters a pause instruction during an upload sequence, it keeps the EEPROM address pointer at its last value. This way the user can store a new instruction sequence in the scratch pad and upload the new sequence to the EEPROM. The new sequence is stored in the EEPROM address locations immediately following the previously saved sequence. This process is repeatable until an upload sequence contains an end instruction. The pause instruction is also useful when used in conjunction with condition processing. It allows the EEPROM to contain multiple occurrences of the same register(s), with each occurrence linked to a set of conditions (see the EEPROM Conditional Processing section).

EEPROM Upload

To upload data to the EEPROM, the user must first ensure that the write enable bit (Register 0E00, Bit 0) is set. Then, on setting the autoclearing save to EEPROM bit (Register 0E02, Bit 0), the controller initiates the EEPROM data storage process.

Uploading EEPROM data requires that the user first write an instruction sequence into the scratch pad registers. During the upload process, the controller reads the scratch pad data byte by byte, starting at Register 0E10 and incrementing the scratch pad address pointer as it goes until it reaches a pause or End instruction.

As the controller reads the scratch pad data, it transfers the data from the scratch pad to the EEPROM (byte by byte) and increments the EEPROM address pointer accordingly, unless it encounters a data instruction. A data instruction tells the controller to transfer data from the device settings portion of the register map to the EEPROM. The number of bytes to transfer is encoded within the data instruction, and the starting address for the transfer appears in the next two bytes in the scratch pad.

When the controller encounters a data instruction, it stores the instruction in the EEPROM, increments the EEPROM address pointer, decodes the number of bytes to be transferred, and increments the scratch pad address pointer. Then it retrieves the next two bytes from the scratch pad (the target address) and increments the scratch pad address pointer by 2. Next, the controller transfers the specified number of bytes from the register map (beginning at the target address) to the EEPROM.

When it completes the data transfer, the controller stores an extra byte in the EEPROM to serve as a checksum for the transferred block of data. To account for the checksum byte, the controller increments the EEPROM address pointer by one more than the number of bytes transferred. Note that, when the controller transfers data associated with an active register, it actually transfers the buffered contents of the register (see the Buffered/Active Registers section for details on the difference between buffered and active registers). This allows for the transfer of nonzero autoclearing register contents.

Note that conditional processing (see the EEPROM Conditional Processing section) does not occur during an upload sequence.

EEPROM Download

An EEPROM download results in data transfer from the EEPROM to the device register map. To download data, the user sets the autoclearing load from EEPROM bit (Register 0E03, Bit 1). This commands the controller to initiate the EEPROM download process. During download, the controller reads the EEPROM data byte by byte, incrementing the EEPROM address pointer as it goes, until it reaches an end instruction. As the controller reads the EEPROM data, it executes the stored instructions, which includes transferring stored data to the device settings portion of the register map whenever it encounters a data instruction.

Note that conditional processing (see the EEPROM Conditional Processing section) is only applicable when downloading.

Automatic EEPROM Download

Following a power-up, an assertion of the RESET pin, or a soft reset (Register 0000, Bit 5 = 1), if FncInit[7:3] ≠ 0 (see the Initial Pin Programming section), then the instruction sequence stored in the EEPROM executes automatically with condition = FncInit[7:3]. In this way, a previously stored set of register values downloads automatically on power-up or with a hard or soft reset. See the EEPROM Conditional Processing section for details regarding conditional processing and the way it modifies the download process.

EEPROM Conditional Processing

The condition instructions allow conditional execution of EEPROM instructions during a download sequence. During an upload sequence, however, they are stored as is and have no effect on the upload process.

Note that, during EEPROM downloads, the condition instructions themselves and the end instruction always execute unconditionally.

Conditional processing makes use of two elements: the condition (from Condition 1 to Condition 31) and the condition tag board. The relationships among the condition, the condition tag board, and the EEPROM controller appear schematically in Figure 50.

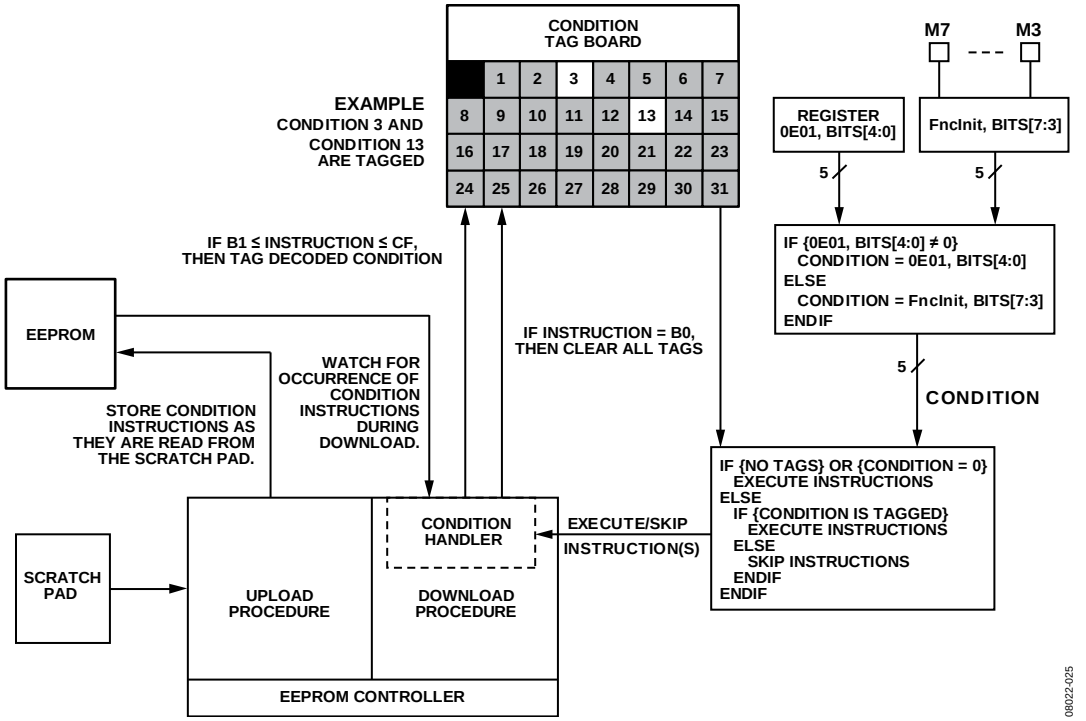


Figure 50. EEPROM Conditional Processing

The condition is a 5-bit value with 32 possibilities. Condition = 0 is the null condition. When the null condition is in effect, the EEPROM controller executes all instructions unconditionally. The remaining 31 possibilities, condition = 1 through condition = 31, modify the EEPROM controller's handling of a download sequence. The condition originates from one of two sources (see Figure 50), as follows:

- FncInit, Bits[7:3], which is the state of the M3 to M7 multifunction pins at power-up (see the Initial Pin Programming section)
- Register 0E01, Bits[4:0]

If Register 0E01, Bits[4:0] ≠ 0, then the condition is the value stored in Register 0E01, Bits[4:0]; otherwise, the condition is FncInit, Bits[7:3]. Note that a nonzero condition present in Register 0E01, Bits[4:0] takes precedence over FncInit, Bits[7:3].

The condition tag board is a table maintained by the EEPROM controller. When the controller encounters a condition instruction, it decodes the B1 through CF instructions as condition = 1 through condition = 31, respectively, and tags that particular condition in the condition tag board. However, the B0 condition instruction decodes as the null condition, for which the controller clears the condition tag board, and subsequent download instructions execute unconditionally (until the controller encounters a new condition instruction).

During download, the EEPROM controller executes or skips instructions depending on the value of condition and the contents of the condition tag board. Note, however, that condition instructions and the end instruction always execute unconditionally during download. If condition = 0, then all instructions during download execute unconditionally. If condition ≠ 0 and there are any tagged conditions in the condition tag board, then the controller executes instructions only if the condition is tagged. If the condition is not tagged, then the controller skips instructions until it encounters a condition instruction that decodes as a tagged condition. Note that the condition tag board allows for multiple conditions to be tagged at any given moment. This conditional processing mechanism enables the user to have one download instruction sequence with many possible outcomes depending on the value of the condition and the order in which the controller encounters condition instructions.

Table 27 lists a sample EEPROM download instruction sequence. It illustrates the use of condition instructions and how they alter the download sequence. The table begins with the assumption that no conditions are in effect. That is, the most recently executed condition instruction is B0 or no conditional instructions have been processed.

Table 27. EEPROM Conditional Processing Example

Instruction	Action
0x08 0x01 0x00	Transfer the system clock register contents regardless of the current condition.
0xB1	Tag Condition 1
0x19 0x04 0x00	Transfer the clock distribution register contents only if condition = 1
0xB2	Tag Condition 2
0xB3	Tag Condition 3
0x07 0x05 0x00	Transfer the reference input register contents only if condition = 1, 2, or 3
0x0A	Calibrate the system clock only if condition = 1, 2, or 3
0xB0	Clear the condition tag board
0x80	Execute an I/O update regardless of the value of the condition
0x0A	Calibrate the system clock regardless of the value of the condition

Storing Multiple Device Setups in EEPROM

Conditional processing makes it possible to create a number of different device setups, store them in EEPROM, and download a specific setup on demand. To do so, first program the device control registers for a specific setup. Then, store an upload sequence in the EEPROM scratch pad with the following general form:

1. Condition instruction (B1 to CF) to identify the setup with a specific condition (1 to 31)
2. Data instructions (to save the register contents) along with any required calibrate and/or I/O update instructions
3. Pause instruction (FE)

With the upload sequence written to the scratch pad, perform an EEPROM upload (Register 0E02, Bit 0).

Reprogram the device control registers for the next desired setup. Then store a new upload sequence in the EEPROM scratch pad with the following general form:

1. Condition instruction (B0)
2. The next desired condition instruction (B1 to CF, but different than the one used during the previous upload to identify a new setup)
3. Data instructions (to save the register contents) along with any required calibrate and/or I/O update instructions
4. Pause instruction (FE)

With the upload sequence written to the scratch pad, perform an EEPROM upload (Register 0E02, Bit 0).

Repeat the process of programming the device control registers for a new setup, storing a new upload sequence in the EEPROM scratch pad (Step 1 through Step 4), and executing an EEPROM upload (Register 0E02, Bit 0) until all of the desired setups have been uploaded to the EEPROM.

Note that, on the final upload sequence stored in the scratch pad, the pause instruction (FE) must be replaced with an end instruction (FF).

To download a specific setup on demand, first store the condition associated with the desired setup in Register 0E01, Bits[4:0]. Then perform an EEPROM download (Register 0E03, Bit 1). Alternatively, to download a specific setup at power-up, apply the required logic levels necessary to encode the desired condition on the M3 to M7 multifunction pins. Then power up the device; an automatic EEPROM download occurs. The condition (as established by the M3 to M7 multifunction pins) guides the download sequence and results in a specific setup.

Keep in mind that the number of setups that can be stored in the EEPROM is limited. The EEPROM can hold a total of 2048 bytes. Each nondata instruction requires one byte of storage. Each data instruction, however, requires N + 4 bytes of storage, where N is the number of transferred register bytes and the other four bytes include the data instruction itself (one byte), the target address (two bytes), and the checksum calculated by the EEPROM controller during the upload sequence (one byte).

SERIAL CONTROL PORT

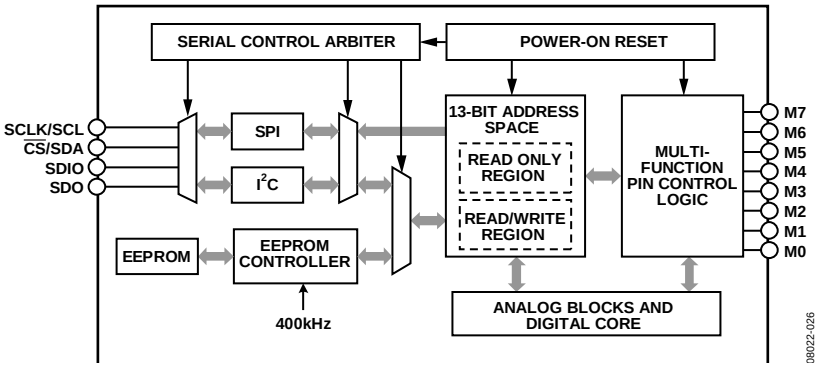


Figure 51. Serial Port Functional Diagram

The AD9548 serial control port is a flexible, synchronous serial communications port that provides a convenient interface to many industry-standard microcontrollers and microprocessors. The AD9548 serial control port is compatible with most synchronous transfer formats, including Philips I²C, Motorola SPI, and Intel SSR protocols. The serial control port allows read/write access to the AD9548 register map.

In SPI mode, single or multiple byte transfers are supported. The SPI port configuration is programmable via Register 0000. This register is integrated into the SPI control logic rather than in the register map and is distinct from the I²C Register 0000. It is also inaccessible to the EEPROM controller.

A functional diagram of the serial control port, including its relationship to the EEPROM, appears in Figure 51.

Although the AD9548 supports both the SPI and I²C serial port protocols, only one is active following power-up (as determined by the multifunction pins, M0 to M2, during the startup sequence). That is, the only way to change the serial port protocol is to reset the device (or cycle the device power supply). Both protocols use a common set of control pins as shown in Figure 52.

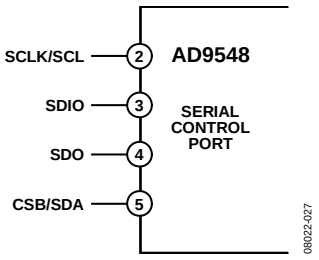


Figure 52. Serial Control Port

SPI/I²C PORT SELECTION

Because the AD9548 supports both SPI and I²C protocols, the active serial port protocol depends on the logic state of the three multifunction pins, M0 to M2, at startup. If all three pins are set to Logic 0 at startup, then the SPI protocol is active. Otherwise, the I²C protocol is active with seven different I²C slave address settings based on the startup logic pattern on the M0 to M2 pins (see Table 28). Note that the four MSBs of the slave address are hardware coded as 1011.

Table 28. Serial Port Mode Selection

M2	M1	M0	Serial Port Mode
0	0	0	SPI
0	0	1	I²C (address = 1001001)
0	1	0	I²C (address = 1001010)
0	1	1	I²C (address = 1001011)
1	0	0	I²C (address = 1001100)
1	0	1	I²C (address = 1001101)
1	1	0	I²C (address = 1001110)
1	1	1	I²C (address = 1001111)

SPI SERIAL PORT OPERATION

Pin Descriptions

The SCLK (serial clock) pin serves as the serial shift clock. This pin is an input. SCLK synchronizes serial control port read and write operations. The rising edge SCLK registers write data bits, and the falling edge registers read data bits. The SCLK pin supports a maximum clock rate of 40 MHz.

The SDIO (serial data input/output) pin is a dual-purpose pin and acts as either an input only (unidirectional mode) or as both an input and an output (bidirectional mode). The AD9548 default SPI mode is bidirectional.

The SDO (serial data output) pin is useful only in unidirectional I/O mode. It serves as the data output pin for read operations.

The $\overline{CS}$ (chip select) pin is an active low control that gates read and write operations. This pin is internally connected to a 30 kΩ pull-up resistor. When $\overline{CS}$ is high, the SDO and SDIO pins go into a high impedance state.

SPI Mode Operation

The SPI port supports both 3-wire (bidirectional) and 4-wire (unidirectional) hardware configurations and both MSB-first and LSB-first data formats. Both the hardware configuration

and data format features are programmable. By default, the AD9548 uses the bidirectional MSB-first mode. The reason that bidirectional is the default mode is so that the user can still write to the device, if it is wired for unidirectional operation, to switch to unidirectional mode.

Assertion (active low) of the $\overline{CS}$ pin initiates a write or read operation to the AD9548 SPI port. For data transfers of three bytes or fewer (excluding the instruction word), the device supports the $\overline{CS}$ stalled high mode (see Table 29). In this mode, the $\overline{CS}$ pin can be temporarily deasserted on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can be deasserted only on byte boundaries, however. This applies to both the instruction and data portions of the transfer.

During stall high periods, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort a transfer midstream, then the state machine must be reset by either completing the transfer or by asserting the $\overline{CS}$ pin for at least one complete SCLK cycle (but less than eight SCLK cycles). Deasserting the $\overline{CS}$ pin on a nonbyte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (see Table 29), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented. $\overline{CS}$ must be deasserted at the end of the last byte transferred, thereby ending the stream mode.

Table 29. Byte Transfer Count

W1	W0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

Communication Cycle—Instruction Plus Data

The SPI protocol consists of a two-part communication cycle. The first part is a 16-bit instruction word that is coincident with the first 16 SCLK rising edges and a payload. The instruction word provides the AD9548 serial control port with information regarding the payload. The instruction word includes the R/$\overline{W}$ bit that indicates the direction of the payload transfer (that is, a read or write operation). The instruction word also indicates the number of bytes in the payload and the starting register address of the first payload byte.

Write

If the instruction word indicates a write operation, the payload is written into the serial control port buffer of the AD9548. Data bits are registered on the rising edge of SCLK. The length of the transfer (1, 2, or 3 bytes or streaming mode) depends on the W0 and W1 bits (see Table 29) in the instruction byte. When not streaming, $\overline{CS}$ can be deasserted after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is asserted. Deasserting the $\overline{CS}$ pin on a nonbyte boundary resets the serial control port. Reserved or blank registers are not skipped over automatically during a write sequence. Therefore, the user must know what bit pattern to write to the reserved registers to preserve proper operation of the part. Generally, it does not matter what data is written to blank registers, but it is customary to write 0s.

Most of the serial port registers are buffered (see the Buffered/Active Registers section for details on the difference between buffered and active registers). Therefore, data written into buffered registers does not take effect immediately. An additional operation is needed to transfer buffered serial control port contents to the registers that actually control the device. This is accomplished with an I/O update operation, which is performed in one of two ways. One is by writing a Logic 1 to Register 0005, Bit 0 (this bit is self-clearing). The other is to use an external signal via an appropriately programmed multifunction pin. The user can change as many register bits as desired before executing an I/O update. The I/O update operation transfers the buffer register contents to their active register counterparts.

Read

The AD9548 supports the long instruction mode only. If the instruction word indicates a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word. N is the number of data bytes read and depends on the W0 and W1 bits of the instruction word. The readback data is valid on the falling edge of SCLK. Blank registers are not skipped over during readback.

A readback operation takes data from either the serial control port buffer registers or the active registers, as determined by Register 0004, Bit 0.

SPI Instruction Word (16 Bits)

The MSB of the 16-bit instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits, W1 and W0, indicate the number of bytes in the transfer (see Table 29). The final 13 bits are the register address (A12 to A0), which indicates the starting register address of the read/write operation (see Table 31).

SPI MSB-/LSB-First Transfers

The AD9548 instruction word and payload can be MSB first or LSB first. The default for the AD9548 is MSB first. The LSB-first mode can be set by writing a 1 to Register 0000, Bit 6. Immediately after the LSB-first bit is set, subsequent serial control port operations are LSB first.

When MSB-first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant payload byte. Subsequent data bytes must follow in order from high address to low address. In MSB-first mode, the serial control port internal

address generator decrements for each data byte of the multibyte transfer cycle.

When Register 0000, Bit 6 = 1 (LSB first), the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant payload byte followed by multiple data bytes. The serial control port internal byte address generator increments for each byte of the multibyte transfer cycle.

For multibyte MSB-first (default) I/O operations, the serial control port register address decrements from the specified starting address toward Address 0000. For multibyte LSB-first I/O operations, the serial control port register address increments from the starting address toward Address 1FFF.

Unused addresses are not skipped during multibyte I/O operations; therefore, the user should write the default value to a reserved register and 0s to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 30. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
LSB First	Increment	0x0000 ... 0x1FFF
MSB First	Decrement	0x1FFF ... 0x0000

Table 31. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

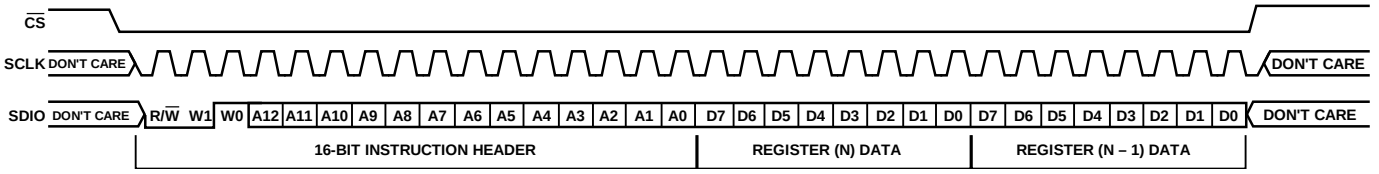


Figure 53. Serial Control Port Write—MSB First, 16-Bit Instruction, Two Bytes of Data

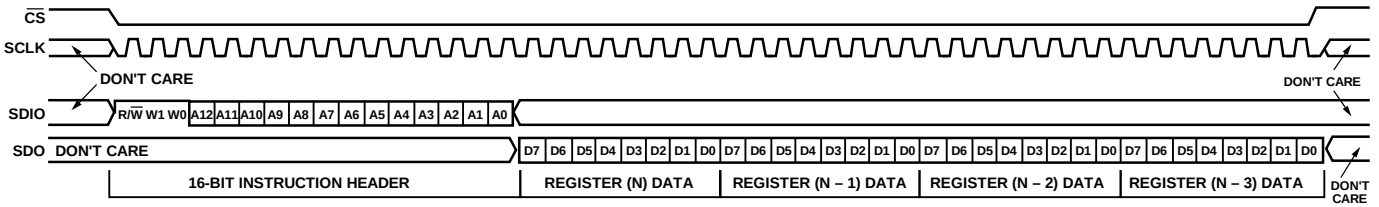


Figure 54. Serial Control Port Read—MSB First, 16-Bit Instruction, Four Bytes of Data

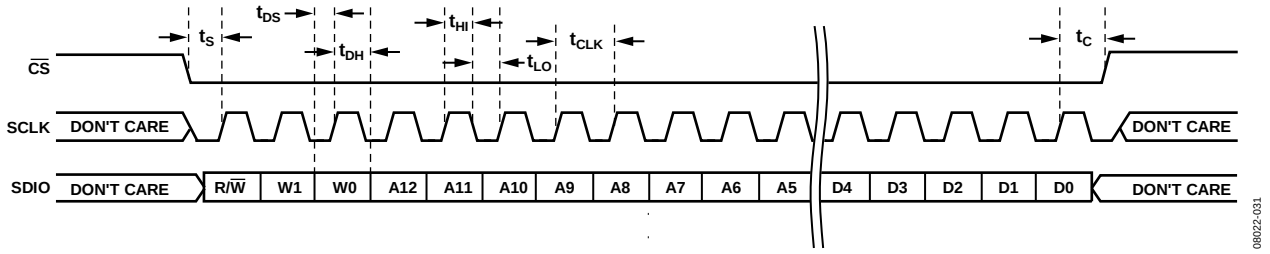


Figure 55. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

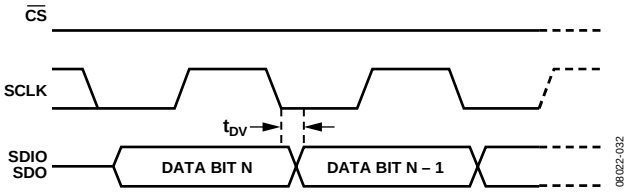


Figure 56. Timing Diagram for Serial Control Port Register Read

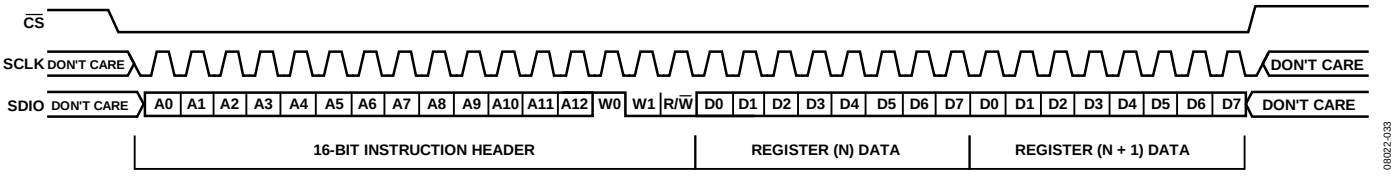


Figure 57. Serial Control Port Write—LSB First, 16-Bit Instruction, Two Bytes of Data

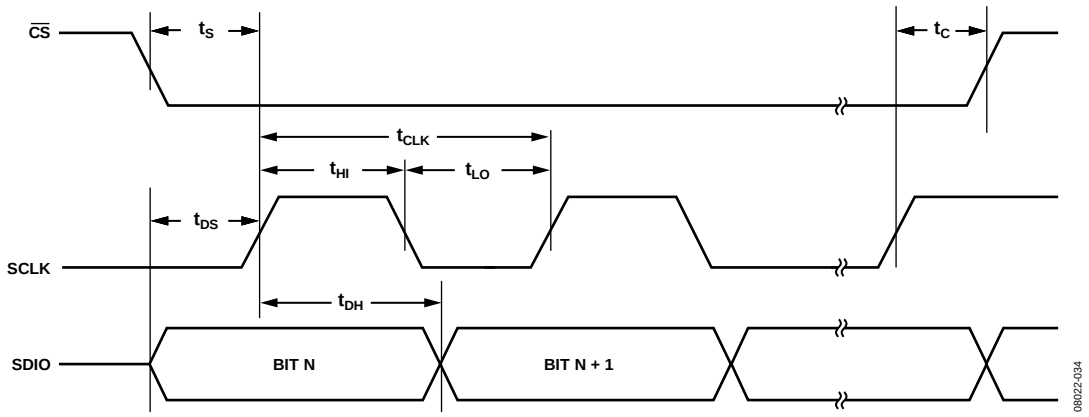


Figure 58. Serial Control Port Timing—Write

Table 32. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and the rising edge of SCLK
t_{DH}	Hold time between data and the rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of the communication cycle)
t_C	Setup time between the SCLK rising edge and $\overline{CS}$ rising edge (end of the communication cycle)
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state
t_{DV}	SCLK to valid SDIO and SDO (see Figure 56)

I²C SERIAL PORT OPERATION

The I²C interface has the advantage of requiring only two control pins and is a de facto standard throughout the I²C industry. However, its disadvantage is programming speed, which is 400 kbps maximum. The AD9548 I²C port design is based on the I²C fast mode standard from Philips, so it supports both the 100 kHz standard mode and 400 kHz fast mode. Fast mode imposes a glitch tolerance requirement on the control signals. That is, the input receivers ignore pulses of less than 50 ns duration.

The AD9548 I²C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I²C bus system, the AD9548 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by the AD9548. The AD9548 uses direct 16-bit memory addressing instead of traditional 8-bit memory addressing.

The AD9548 allows up to seven unique slave devices to occupy the I²C bus. These are accessed via a 7-bit slave address transmitted as part of an I²C packet. Only the device with a matching slave address responds to subsequent I²C commands. The device slave address is 1001xxx (the three right bits are determined by the M0 to M2 pins). The four MSBs (1001) are hard-wired, while the three LSBs (xxx, determined by the M0 to M2 pins) are programmable via the power-up state of the multifunction pins (see the Initial Pin Programming section).

I²C Bus Characteristics

A summary of the various I²C protocols appears in Table 33.

Table 33. I²C Bus Abbreviation Definitions

Abbreviation	Definition
S	Start
Sr	Repeated start
P	Stop
A	Acknowledge
$\overline{A}$	Nonacknowledge
$\overline{W}$	Write
R	Read

The transfer of data is shown in Figure 59. One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.

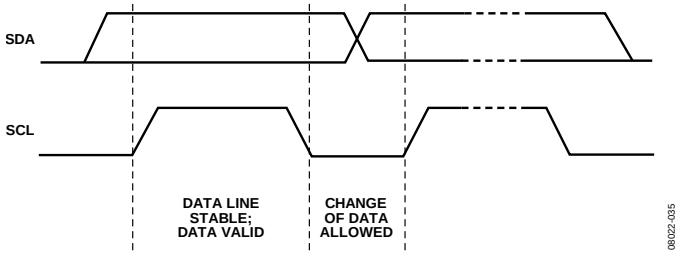


Figure 59. Valid Bit Transfer

Start/stop functionality is shown in Figure 60. The start condition is characterized by a high-to-low transition on the SDA line while SCL is high. The start condition is always generated by the master to initialize a data transfer. The stop condition is characterized by a low-to-high transition on the SDA line while SCL is high. The stop condition is always generated by the master to terminate a data transfer. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit; bytes are sent MSB first.

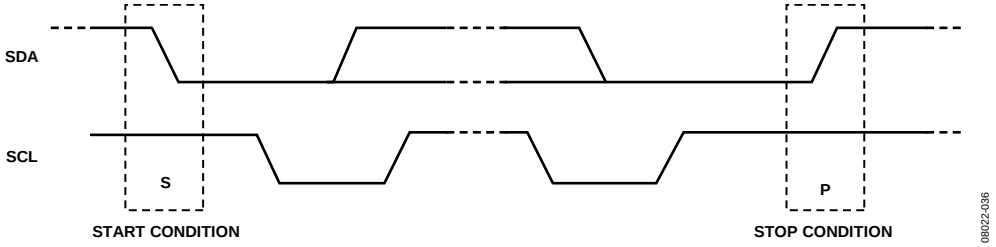


Figure 60. Start and Stop Conditions

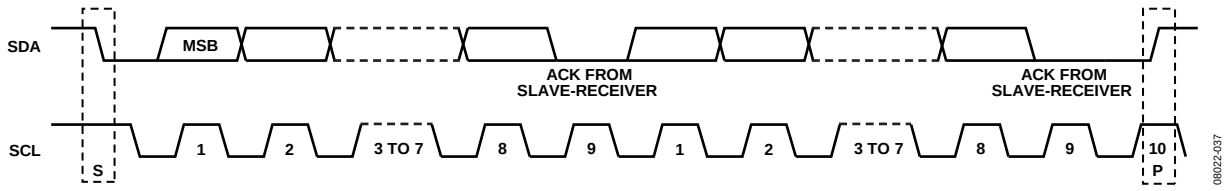


Figure 61. Acknowledge Bit

The acknowledge bit (A) is the ninth bit attached to any 8-bit data byte. An acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has been received. It is done by pulling the SDA line low during the ninth clock pulse after each 8-bit data byte.

The nonacknowledge bit ($\overline{A}$) is the ninth bit attached to any 8-bit data byte. A nonacknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has not been received. It is done by leaving the SDA line high during the ninth clock pulse after each 8-bit data byte.

Data Transfer Process

The master initiates data transfer by asserting a start condition. This indicates that a data stream follows. All I²C slave devices connected to the serial bus respond to the start condition.

The master then sends an 8-bit address byte over the SDA line, consisting of a 7-bit slave address (MSB first) plus an R/$\overline{W}$ bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write, 1 = read).

The peripheral whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master (transmitter) writes to the slave device (receiver). If the R/$\overline{W}$ bit is 1, the master (receiver) reads from the slave device (transmitter).

The format for these commands is described in the Data Transfer Format section

Data is then sent over the serial bus in the format of nine clock pulses, one data byte (eight bits) from either master (write mode) or slave (read mode) followed by an acknowledge bit from the receiving device. The number of bytes that can be transmitted per transfer is unrestricted. In write mode, the first two data bytes immediately after the slave address byte are the internal memory (control registers) address bytes, with the high address byte first. This addressing scheme gives a memory address of up to $2^{16} - 1 =$ 65,535. The data bytes after these two memory address bytes are register data written to or read from the control registers. In read mode, the data bytes after the slave address byte are register data written to or read from the control registers.

When all data bytes are read or written, stop conditions are established. In write mode, the master (transmitter) asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the slave device (receiver). In read mode, the master device (receiver) receives the last data byte from the slave device (transmitter) but does not pull SDA low during the ninth clock pulse. This is known as a nonacknowledge bit. By receiving the nonacknowledge bit, the slave device knows the data transfer is finished and enters idle mode. The master then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition.

A start condition can be used in place of a stop condition. Furthermore, a start or stop condition can occur at any time, and partially transferred bytes are discarded.

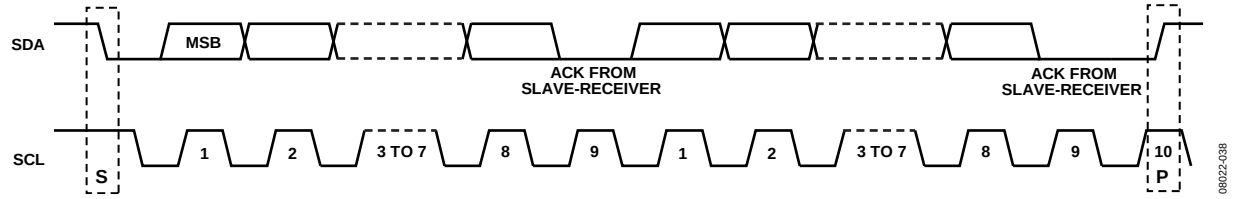


Figure 62. Data Transfer Process (Master Write Mode, 2-Byte Transfer)

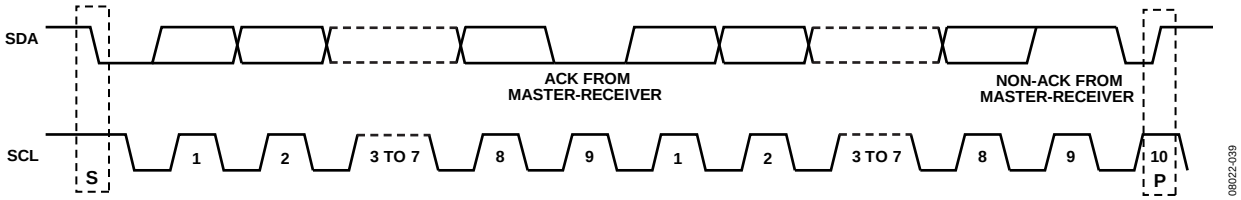


Figure 63. Data Transfer Process (Master Read Mode, 2-Byte Transfer)

Data Transfer Format

Write byte format—the write byte protocol is used to write a register address to the RAM starting from the specified RAM address.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	A	P

Send byte format—the send byte protocol is used to set up the register address for subsequent reads.

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	P

Receive byte format—the receive byte protocol is used to read the data byte(s) from RAM starting from the current address.

S	Slave address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

Read byte format—the combined format of the send byte and the receive byte.

S	Slave Address	$\overline{W}$	A	RAM Address High Byte	A	RAM Address Low Byte	A	Sr	Slave Address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

I²C Serial Port Timing

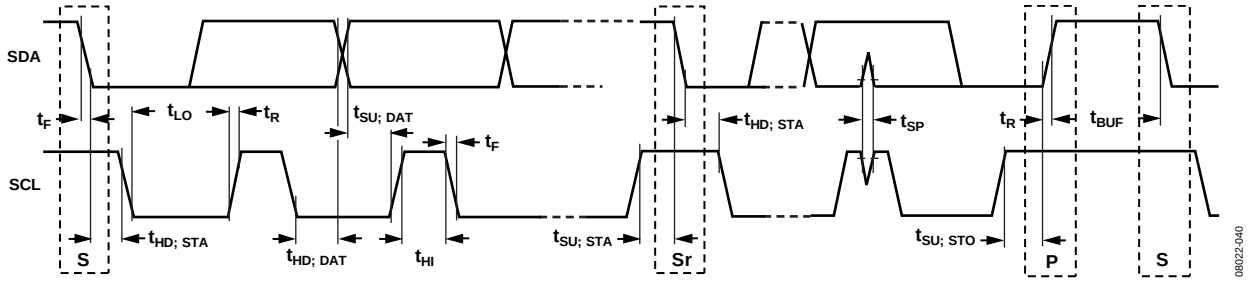


Figure 64. I²C Serial Port Timing

Table 34. I²C Timing Definitions

Parameter	Description
f_{SCL}	Serial clock
t_{BUF}	Bus free time between stop and start conditions
$t_{HD;\ STA}$	Repeated hold time start condition
$t_{SU;\ STA}$	Repeated start condition setup time
$t_{SU;\ STO}$	Stop condition setup time
$t_{HD;\ DAT}$	Data hold time
$t_{SU;\ DAT}$	Date setup time
t_{LO}	SCL clock low period
t_{HI}	SCL clock high period
t_R	Minimum/maximum receive SCL and SDA rise time
t_F	Minimum/maximum receive SCL and SDA fall time
t_{SP}	Pulse width of voltage spikes that must be suppressed by the input filter

I/O PROGRAMMING REGISTERS

The register map spans an address range from 0x0000 through 0x0E3F (0 to 3647, decimal). Each address provides access to 1 byte (eight bits) of data. Each individual register is identified by its four-digit hexadecimal address (for example, Register 0A10). In some cases, a group of addresses collectively define a register (for example, the IRQ mask register consists of Register 0209, Register 020A, Register 020B, Register 020C, Register 020D, Register 020E, Register 020F, and Register 0210).

In general, when a group of registers defines a control parameter, the LSB of the value resides in the D0 position of the register with the lowest address. The bit weight increases right to left, from the lowest register address to the highest register address. For example, the default value of the incremental phase lock offset step size register (Address 0314 to Address 0315) is the 16-bit hexadecimal number, 0x03E8 (not 0xE803).

Note that the EEPROM storage sequence registers (Address 0E10 to Address 0E3F) are an exception to the above convention (see the EEPROM Instructions section).

BUFFERED/ACTIVE REGISTERS

There are two broad categories of registers in the AD9548, buffered and active (see Figure 65). Buffered registers are those that can be written to directly from the serial port. They do not need an I/O update to apply their contents to the internal device functions. In contrast, active registers require an I/O update to transfer data between the buffer registers and the internal device functions. In operation, the user programs as many buffer registers as desired and then issues an I/O update. The I/O update occurs by writing to Register 0005, Bit 0 = 1 (or by the external application of the necessary logic level to one of the multifunction pins previously programmed as an I/O update input). The contents of buffer registers connected directly to the internal device functions affect those functions immediately. The contents of buffer registers that connect to active registers do not affect the internal device functions until the I/O update event occurs.

An S or C in the Opt column of the register map identifies a register as an active register (otherwise, it is a buffer register). An S entry means that the I/O update signal to the active register is synchronized with the serial port clock or with an input signal driving one of the multifunction pins. On the other hand, a C entry means that the I/O update signal to the active register is synchronized with a clock signal derived from the internal system clock ($f_S/32$), as shown in Figure 65.

When reading back a register that has both buffered and active contents, the user can use Register 0004, Bit 0 to select whether to read back the buffer or active contents. Readback of the active contents occurs when Register 0004, Bit 0 = 0, whereas readback of the buffer contents occurs when Register 0004, Bit 0 = 1. Note that a read-only active register requires an I/O update before reading its contents.

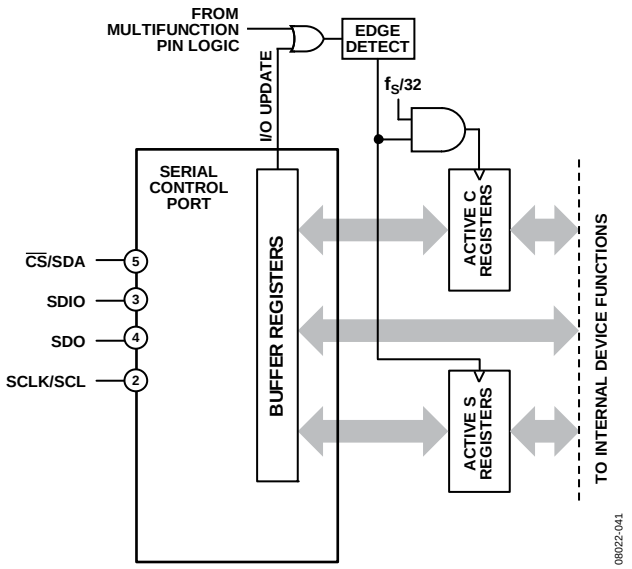


Figure 65. Buffered and Active Registers

AUTOCLEAR REGISTERS

An A in the Opt column of the register map identifies an autoclear register. Typically, the active value for an autoclear register takes effect following an I/O update. The bit is cleared by the internal device logic upon completion of the prescribed action.

REGISTER ACCESS RESTRICTIONS

Read and write access to the register map may be restricted depending on the register in question, the source and direction of access, and the current state of the device. Each register can be classified into one or more access types. When more than one type applies, the most restrictive condition that applies at the moment is used.

Whenever access is denied to a register, all attempts to read the register return a 0 byte, and all attempts to write to the register are ignored. Access to nonexistent registers is handled in the same way as for a denied register.

Regular Access

Registers with regular access do not fall into any other category. Both read and write access to registers of this type can be from either the serial ports or EEPROM controller. However, only one of these sources can have access to a register at any given time (access is mutually exclusive). Whenever the EEPROM controller is active, either in load or store mode, it has exclusive access to these registers.

Read-Only Access

An R in the Opt column of the register map identifies read-only registers. Access is available at all times, including when the EEPROM controller is active.

Exclusion from EEPROM Access

An E in the Opt column of the register map identifies a register with contents that are inaccessible to the EEPROM. That is, the contents of this type of register cannot be transferred directly to the EEPROM or vice versa. Note that read-only registers (R) are inaccessible to the EEPROM, as well.

REGISTER MAP

Table 35.

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
			Serial port control and part identification								
0000	E	SPI control	Unidirec-tional	LSB first/ Inc Addr	Soft reset	Long instruction	Unused				10
0000	Dup	I2C control	Unused		Soft reset	Unused					00
0001	E	Reserved	Unused								
0002	R	Reserved	Silicon revision number								01
0003	R		Device ID								48
0004	E	Readback	Unused							Read buffer register	00
0005	A, E	I/O update	Unused							I/O update	00
			System clock								
0100	S		External loop filter enable	Charge pump mode (auto/ man)	Charge pump current [2:0]			Lock detect timer disable	Lock detect divider [1:0]		18
0101	S		N-divider [7:0]								28
0102	S		Unused	M-divider reset	M-divider [1:0]		2× frequency multiplier enable	PLL enable	SYSCLK reference select [1:0]		45
0103	C	Nom SYSCLK period	Nominal system clock period (femtoseconds) [15:0] [1 ns @ 1 ppm accuracy]								40
0104	C										42
0105	C		Unused			Nominal system clock period [20:16]					0F
0106	C	System clock stability	System clock stability period (milliseconds) [15:0]								01
0107	C										00
0108	C		Unused				System clock stability period (milliseconds) [19:16]				00
			General configuration								
0200	S	M0	M0 in/out	M0 function [6:0]							00
0201	S	M1	M1 in/out	M1 function [6:0]							00
0202	S	M2	M2 in/out	M2 function [6:0]							00
0203	S	M3	M3 in/out	M3 function [6:0]							00
0204	S	M4	M4 in/out	M4 function [6:0]							00
0205	S	M5	M5 in/out	M5 function [6:0]							00
0206	S	M6	M6 in/out	M6 function [6:0]							00
0207	S	M7	M7 in/out	M7 function [6:0]							00
0208	C	IRQ pin output mode	Unused						IRQ pin output mode [1:0]		00
0209	C	IRQ mask	Unused		SYSCLK unlocked	SYSCLK locked	Unused	Unused	SYSCLK Cal complete	SYSCLK Cal started	00
020A	C		Unused				Distribution sync	Watchdog timer	EEPROM fault	EEPROM complete	00
020B	C		Switching	Closed	Freerun	Holdover	Freq unlocked	Freq locked	Phase unlocked	Phase locked	00
020C	C		Unused			History updated	Frequency unclamped	Frequency clamped	Phase slew unlimited	Phase slew limited	00
020D	C		Ref AA new profile	Ref AA validated	Ref AA fault cleared	Ref AA fault	Ref A new profile	Ref A validated	Ref A fault cleared	Ref A fault	00
020E	C		Ref BB new profile	Ref BB validated	Ref BB fault cleared	Ref BB fault	Ref B new profile	Ref B validated	Ref B fault cleared	Ref B fault	00
020F	C		Ref CC new profile	Ref CC validated	Ref CC fault cleared	Ref CC fault	Ref C new profile	Ref C validated	Ref C fault cleared	Ref C fault	00

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
0210	C		Ref DD new profile	Ref DD validated	Ref DD fault cleared	Ref DD fault	Ref D new profile	Ref D validated	Ref D fault cleared	Ref D fault	00
0211	C	Watchdog timer	Watchdog timer (ms) [15:0] [up to 65.5 sec]								00
0212	C										00
0213	S	DAC current	DAC full-scale current [7:0]								FF
0214	S		DAC shutdown	Unused					DAC full-scale current [9:8]		01
			DPLL								
0300	C	Free running frequency tuning word	Free running frequency tuning word [47:0]								00
0301	C										00
0302	C										00
0303	C										00
0304	C										00
0305	C										00
0306	A, C	Update TW	Unused							Update TW	00
0307	C	Pull-in range limits	Pull-in range lower limit [23:0]								00
0308	C										00
0309	C										00
030A	C		Pull-in range upper limit [23:0]								FF
030B	C										FF
030C	C										FF
030D	C	Open loop phase offset	DDS phase offset word [15:0]								00
030E	C										00
030F	C	Closed loop phase offset	Fixed phase lock offset [39:0] (picoseconds; signed)								00
0310	C										00
0311	C										00
0312	C										00
0313	C										00
0314	C		Incremental phase lock offset step size [15:0] (picoseconds)								E8
0315	C										03
0316	C	Phase slew limit	Phase slew rate limit [15:0] (ns/sec)								00
0317	C										00
0318	C	History accumulation timer	History accumulation timer [23:0] (milliseconds)								30
0319	C										75
031A	C										00
031B	C	History mode	Unused			Single sample fallback	Persistent history	Incremental average [2:0]			00
			Clock distribution output								
0400	S	Distribution settings	Unused		External distribution resistor	Receiver mode	OUT3 power-down	OUT2 power-down	OUT1 power-down	OUT0 power-down	00
0401	S	Distribution enable	Unused				OUT3 enable	OUT2 enable	OUT1 enable	OUT0 enable	00
0402	S	Distribution synchronization	Unused		Sync source [1:0]		OUT3 sync mask	OUT2 sync mask	OUT1 sync mask	OUT0 sync mask	00
0403	C	Automatic synchronization	Unused						Automatic sync mode [1:0]		00
0404	S	Distribution channel modes	Unused		OUT0 CMOS phase invert	OUT0 polarity invert	OUT0 drive strength	OUT0 mode			03
0405	S		Unused		OUT1 CMOS phase invert	OUT1 polarity invert	OUT1 drive strength	OUT1 mode			03

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
0406	S		Unused		OUT2 CMOS phase invert	OUT2 polarity invert	OUT2 drive strength	OUT2 mode			03
0407	S		Unused		OUT3 CMOS phase invert	OUT3 polarity invert	OUT3 drive strength	OUT3 mode			03
0408	S	Distribution channel dividers	Q0 [23:0]								00
0409	S										00
040A	S										00
040B	S		Unused		Q0 [29:24]						00
040C	S		Q1 [23:0]								00
040D	S										00
040E	S										00
040F	S		Unused		Q1 [29:24]						00
0410	S		Q2 [23:0]								00
0411	S										00
0412	S										00
0413	S		Unused		Q2 [29:24]						00
0414	S		Q3 [23:0]								00
0415	S										00
0416	S										00
0417	S		Unused		Q3 [29:24]						00
			Reference inputs								
0500	S	Reference power-down	Ref DD power-down	Ref D power-down	Ref CC power-down	Ref C power-down	Ref BB power-down	Ref B power-down	Ref AA power-down	Ref A power-down	00
0501	S	Reference logic family	Ref BB logic family [1:0]		Ref B logic family [1:0]		Ref AA logic family [1:0]		Ref A logic family [1:0]		00
0502	S		Ref DD logic family [1:0]		Ref D logic family [1:0]		Ref CC Logic Family [1:0]		Ref C Logic Family [1:0]		00
0503	C	Manual reference profile selection	Enable Ref AA manual profile	Ref AA manual profile [2:0]			Enable Ref A manual profile	Ref A manual profile [2:0]			00
0504	C		Enable Ref BB Manual Profile	Ref BB manual profile [2:0]			Enable Ref B manual profile	Ref B manual profile [2:0]			00
0505	C		Enable Ref CC Manual Profile	Ref CC manual profile [2:0]			Enable Ref C manual profile	Ref C manual profile [2:0]			00
0506	C		Enable Ref DD Manual Profile	Ref DD manual profile [2:0]			Enable Ref D manual profile	Ref D manual profile [2:0]			00
0507	C	Phase build-out switching	Unused					Phase master threshold priority [2:0]			00
			Profile 0								
0600		Priorities	Unused		Promoted priority [2:0]			Selection priority [2:0]			00
0601		Reference period	Nominal period (femtoseconds) [47:0] (up to 1.125 sec)								00
0602											00
0603											00
0604											00
0605											00
0606											00
0607			Unused						Nominal period [49:48]		00
0608		Tolerance	Inner tolerance (1/tolerance) [15:0] (removes fault status; 10% down to 1 ppm)								00
0609											00
060A			Unused				Inner tolerance [19:16]				00
060B			Outer tolerance (1/tolerance) [15:0] (indicates fault status; 10% down to 1 ppm)								00
060C											00
060D			Unused				Outer tolerance [19:16]				00
060E		Validation	Validation timer (milliseconds) [15:0] (up to 65.5 sec)								00

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
060F											00
0610		Redetect timeout	Redetect timer (milliseconds) [15:0] [up to 65.5 seconds]								00
0611											00
0612		Digital loop filter coefficients	Alpha-0 linear [15:0]								00
0613											00
0614			Alpha-2 exponent [1:0]		Alpha-1 exponent [5:0]						00
0615			Beta-0 linear [6:0]							Alpha-2 exponent [2]	00
0616			Beta-0 linear [14:7]								00
0617			Unused	Beta-1 exponent [4:0]					Beta-0 linear [16:15]		00
0618			Gamma-0 linear [15:0]								00
0619											00
061A			Unused		Gamma-1 exponent [4:0]					Gamma-0 linear [16]	00
061B			Delta-0 linear [7:0]								00
061C			Delta-1 exponent [0]	Delta-0 linear [14:8]							00
061D			Alpha-3 exponent [3:0]				Delta-1 exponent [4:1]				00
061E		Frequency multiplication	R [23:0]								00
061F											00
0620											00
0621			Unused		R [29:24]						00
0622			S [23:0]								00
0623											00
0624											00
0625			Unused		S [29:24]						00
0626			V [7:0]								00
0627			U [3:0]				Unused		V [9:8]		00
0628			Unused		U [9:4]						00
0629		Lock detectors	Phase lock threshold (picoseconds) [15:0]								00
062A											00
062B			Phase lock fill rate [7:0]								00
062C			Phase lock drain rate [7:0]								00
062D			Frequency lock threshold (picoseconds) [23:0]								00
062E											00
062F											00
0630			Frequency lock fill rate [7:0]								00
0631			Frequency lock drain rate [7:0]								00
			Profile 1								
0632		Priorities	Unused		Promoted priority [2:0]			Selection priority [2:0]			00
0633		Reference period	Nominal period (femtoseconds) [47:0] (up to 1.125 sec)								00
0634											00
0635											00
0636											00
0637											00
0638											00
0639			Unused						Nominal period [49:48]		00
063A		Tolerance	Inner tolerance (1/tolerance) [15:0] (removes fault status; 10% down to 1 ppm)								00
063B											00
063C			Unused				Inner tolerance [19:16]				00
06CD			Outer tolerance (1/tolerance) [15:0] (indicates fault status; 10% down to 1 ppm)								00
063E											00
063F			Unused				Outer tolerance [19:16]				00
0640		Validation	Validation timer (milliseconds) [15:0] (up to 65.5 sec)								00
0641											00

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
0642		Redetect timeout	Redetect timer (milliseconds) [15:0] (up to 65.5 sec)								00
0643											00
0644		Digital loop filter coefficients	Alpha-0 linear [15:0]								00
0645											00
0646			Alpha-2 exponent [1:0]		Alpha-1 exponent [5:0]						00
0647			Beta-0 linear [6:0]							Alpha-2 exponent [2]	00
0648			Beta-0 linear [14:7]								00
0649			Unused	Beta-1 exponent [4:0]					Beta-0 linear [16:15]		00
064A			Gamma-0 linear [15:0]								00
064B											00
064C			Unused		Gamma-1 exponent [4:0]					Gamma-0 linear [16]	00
064D			Delta-0 linear [7:0]								00
064E			Delta-1 exponent [0]	Delta-0 linear [14:8]							00
064F			Alpha-3 exponent [3:0]				Delta-1 exponent [4:1]				00
0650		Frequency multiplication	R [23:0]								00
0651											00
0652											00
0653			Unused		R [29:24]						00
0654			S [23:0]								00
0655											00
0656											00
0657			Unused		S [29:24]						00
0658			V [7:0]								00
0659			U [3:0]				Unused		V [9:8]		00
065A			Unused		U [9:4]						00
065B		Lock detectors	Phase lock threshold (picoseconds) [15:0]								00
065C											00
065D			Phase lock fill rate [7:0]								00
065E			Phase lock drain rate [7:0]								00
065F			Frequency lock threshold (picoseconds) [23:0]								00
0660											00
0661											00
0662			Frequency lock fill rate [7:0]								00
0663			Frequency lock drain rate [7:0]								00
0664 to 067F			Unused								
			Profile 2								
0680		Priorities	Unused		Promoted priority [2:0]			Selection priority [2:0]			00
0681		Reference period	Nominal period (femtoseconds) [47:0] (up to 1.125 sec)								00
0682											00
0683											00
0684											00
0685											00
0686											00
0687			Unused						Nominal period [49:48]		00
0688		Tolerance	Inner tolerance (1/tolerance) [15:0] (removes fault status; 10% down to 1 ppm)								00
0689											00
068A			Unused				Inner tolerance [19:16]				00
068B			Outer tolerance (1/tolerance) [15:0] (indicates fault status; 10% down to 1 ppm)								00
068C											00
068D			Unused				Outer tolerance [19:16]				00
068E		Validation	Validation timer (milliseconds) [15:0] (up to 65.5 sec)								00
068F											00

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
0690		Redetect timeout	Redetect timer (milliseconds) [15:0] (up to 65.5 seconds)								00
0691											00
0692		Digital loop filter coefficients	Alpha-0 linear [15:0]								00
0693											00
0694			Alpha-2 exponent [1:0]		Alpha-1 exponent [5:0]						00
0695			Beta-0 linear [6:0]							Alpha-2 exponent [2]	00
0696			Beta-0 linear [14:7]								00
0697			Unused	Beta-1 exponent [4:0]					Beta-0 linear [16:15]		00
0698			Gamma-0 linear [15:0]								00
0699											00
069A			Unused		Gamma-1 exponent [4:0]					Gamma-0 linear [16]	00
069B			Delta-0 linear [7:0]								00
069C			Delta-1 exponent [0]	Delta-0 linear [14:8]							00
069D			Alpha-3 exponent [3:0]				Delta-1 exponent [4:1]				00
069E		Frequency multiplication	R [23:0]								00
069F											00
06A0											00
06A1			Unused		R [29:24]						00
06A2			S [23:0]								00
06A3											00
06A4											00
06A5			Unused		S [29:24]						00
06A6			V [7:0]								00
06A7			U [3:0]				Unused		V [9:8]		00
06A8			Unused		U [9:4]						00
06A9		Lock detectors	Phase lock threshold (picoseconds) [15:0]								00
06AA											00
06AB			Phase lock fill rate [7:0]								00
06AC			Phase lock drain rate [7:0]								00
06AD			Frequency lock threshold (picoseconds) [23:0]								00
06AE											00
06AF											00
06B0			Frequency lock fill rate [7:0]								00
06B1			Frequency lock drain rate [7:0]								00
			Profile 3								
06B2		Priorities	Unused		Promoted priority [2:0]			Selection priority [2:0]			00
06B3		Reference period	Nominal period (femtoseconds) [47:0] (up to 1.125 sec)								00
06B4											00
06B5											00
06B6											00
06B7											00
06B8											00
06B9			Unused						Nominal period [49:48]		00
06BA		Tolerance	Inner tolerance (1/tolerance) [15:0] (removes fault status; 10% down to 1 ppm)								00
06BB											00
06BC			Unused				Inner tolerance [19:16]				00
06BD			Outer tolerance (1/tolerance) [15:0] (indicates fault status; 10% down to 1 ppm)								00
06BE											00
06BF			Unused				Outer tolerance [19:16]				00

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
06C0		Validation	Validation timer (milliseconds) [15:0] (up to 65.5 sec)								00
06C1											00
06C2		Redetect timeout	Redetect timer (milliseconds) [15:0] (up to 65.5 sec)								00
06C3											00
06C4		Digital loop filter coefficients	Alpha-0 linear [15:0]								00
06C5											00
06C6			Alpha-2 exponent [1:0]		Alpha-1 exponent [5:0]						00
06C7			Beta-0 linear [6:0]							Alpha-2 exponent [2]	00
06C8			Beta-0 linear [14:7]								00
06C9			Unused	Beta-1 exponent [4:0]					Beta-0 linear [16:15]	00	
06CA			Gamma-0 linear [15:0]								00
06CB											00
06CC			Unused		Gamma-1 exponent [4:0]					Gamma-0 linear [16]	00
06CD			Delta-0 linear [7:0]								00
06CE			Delta-1 exponent [0]	Delta-0 linear [14:8]							00
06CF			Alpha-3 exponent [3:0]				Delta-1 exponent [4:1]				00
06D0		Frequency multiplication	R [23:0]								00
06D1											00
06D2											00
06D3			Unused		R [29:24]						00
06D4			S [23:0]								00
06D5											00
06D6											00
06D7			Unused		S [29:24]						00
06D8			V [7:0]								00
06D9			U [3:0]				Unused		V [9:8]		00
06DA			Unused		U [9:4]						00
06DB		Lock detectors	Phase lock threshold (picoseconds) [15:0]								00
06DC											00
06DD			Phase lock fill rate [7:0]								00
06DE			Phase lock drain rate [7:0]								00
06DF			Frequency lock threshold (picoseconds) [23:0]								00
06E0											00
06E1											00
06E2			Frequency lock fill rate [7:0]								00
06E3			Frequency lock drain rate [7:0]								00
06E4-06FF			Unused								
			Profile 4 through Profile 7								
0700-07FF		Profile 4 through Profile 7	The functionality of the Profile 4 through Profile 7 address locations (Address 0700 to Address 07FF) is identical to that of the Profile 0 through Profile 3 address locations (Address 0600 to Address 06FF).								
			Operational controls								
0A00	S	General power-down	Reset Sans regmap	Unused	SYSCLK power-down	Reference power-down	TDC power-down	DAC power-down	Dist power-down	Full power-down	00
0A01	C	Loop mode	Unused	User holdover	User freerun	User selection mode [1:0]		User reference selection [2:0]			00
0A02	S	Cal/sync	Unused						Sync distribution	Calibrate system clock	00

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
0A03	A, C	ResetFunc	Unused	Clear LF	Clear CCI	Clear phase accumulator	Reset auto sync	Reset TW history	Reset all IRQs	Reset watchdog	00
0A04	A, C	IRQ clearing	Unused		SYSCLK unlocked	SYSCLK locked	Unused	Unused	SYSCLK Cal complete	SYSCLK Cal started	00
0A05	A, C		Unused				Distribution sync	Watchdog timer	EEPROM fault	EEPROM complete	00
0A06	A, C		Switching	Closed	Freerun	Holdover	Freq unlocked	Freq locked	Phase unlocked	Phase locked	00
0A07	A, C		Unused			History updated	Freq unclamped	Freq clamped	Phase slew unlimited	Phase slew limited	00
0A08	A, C		Ref AA new profile	Ref AA validated	Ref AA fault cleared	Ref AA fault	Ref A new profile	Ref A validated	Ref A fault cleared	Ref A fault	00
0A09	A, C		Ref BB new profile	Ref BB validated	Ref BB fault cleared	Ref BB fault	Ref B new profile	Ref B validated	Ref B fault cleared	Ref B fault	00
0A0A	A, C		Ref CC new profile	Ref CC validated	Ref CC fault cleared	Ref CC fault	Ref C new profile	Ref C validated	Ref C fault cleared	Ref C fault	00
0A0B	A, C		Ref DD new profile	Ref DD validated	Ref DD fault cleared	Ref DD fault	Ref D new profile	Ref D validated	Ref D fault cleared	Ref D fault	00
0A0C	A, C	Incremental phase offset	Unused					Reset phase offset	Decrement phase offset	Increment phase offset	00
0A0D	A, C	Reference profile detect	Detect DD	Detect D	Detect CC	Detect C	Detect BB	Detect B	Detect AA	Detect A	00
0A0E	A, C	Force validation timeout	Force Timeout DD	Force Timeout D	Force Timeout CC	Force Timeout C	Force Timeout BB	Force Timeout B	Force Timeout AA	Force Timeout A	00
0A0F	C	Reference monitor override	Ref Mon Override DD	Ref Mon Override D	Ref Mon Override CC	Ref Mon Override C	Ref Mon Override BB	Ref Mon Override B	Ref Mon Override AA	Ref Mon Override A	00
0A10	C	Reference monitor bypass	Ref Mon Bypass DD	Ref Mon Bypass D	Ref Mon Bypass CC	Ref Mon Bypass C	Ref Mon Bypass BB	Ref Mon Bypass B	Ref Mon Bypass AA	Ref Mon Bypass A	00
			Status (read only; accessible during EEPROM transactions)								
0D00	R	EEPROM	Unused					Fault detected	Load in progress	Save in progress	
0D01	R	System clock	Unused			Stable	Unused	Unused	Cal in progress	Lock detected	
0D02	R	IRQ monitor	Unused		SYSCLK unlocked	SYSCLK locked	Unused	Unused	SYSCLK Cal complete	SYSCLK Cal started	
0D03	R		Unused				Distribution sync	Watchdog timer	EEPROM fault	EEPROM complete	
0D04	R		Switching	Closed	Freerun	Holdover	Freq unlocked	Freq locked	Phase unlocked	Phase locked	
0D05	R		Unused			History updated	Freq unclamped	Freq clamped	Phase slew unlimited	Phase slew limited	
0D06	R		Ref AA new profile	Ref AA validated	Ref AA fault cleared	Ref AA fault	Ref A new profile	Ref A validated	Ref A fault cleared	Ref A fault	
0D07	R		Ref BB new profile	Ref BB validated	Ref BB fault cleared	Ref BB fault	Ref B new profile	Ref B validated	Ref B fault cleared	Ref B fault	
0D08	R		Ref CC new profile	Ref CC validated	Ref CC fault cleared	Ref CC fault	Ref C new profile	Ref C validated	Ref C fault cleared	Ref C fault	
0D09	R		Ref DD new profile	Ref DD validated	Ref DD fault cleared	Ref DD fault	Ref D new profile	Ref D validated	Ref D fault cleared	Ref D fault	
0D0A	R, C	DPLL status	Offset slew limiting	Phase build-out	Freq lock	Phase lock	Loop switching	Holdover	Active	Free running	
0D0B	R, C		Frequency	History	Active reference priority [3:0]			Active reference [3:0]			

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
			clamped	available							
0D0C	R, C	Ref A	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D0D	R, C	Ref AA	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D0E	R, C	Ref B	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D0F	R, C	Ref BB	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D10	R, C	Ref C	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D11	R, C	Ref CC	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D12	R. C	Ref D	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D13	R, C	Ref DD	Profile selected	Selected profile [2:0]			Valid	Fault	Fast	Slow	
0D14	R, C	Holdover history	Tuning word readback [47:0]								
0D15	R, C										
0D16	R, C										
0D17	R, C										
0D18	R, C										
0D19	R, C										
			Nonvolatile memory (EEPROM) control								
0E00		Write protect	Unused						Half rate mode	Write enable	00
0E01	E	Condition	Unused			Condition value [4:0]					00
0E02	A, E	Save	Unused							Save to EEPROM	00
0E03	A, E	Load	Unused						Load from EEPROM	Unused	00
			EEPROM storage sequence								
0E10	E	System clock	Data: 9 bytes								08
0E11	E		Address: 0x0100								01
0E12	E										00
0E13	E	I/O update	Action: IO_Update								80
0E14	E	SYSCLK calibrate	Action: calibrate system clock								A0
0E15	E	General	Data: 21 bytes								14
0E16	E		Address: 0x0200								02
0E17	E										00
0E18	E	DPLL	Data: 28 bytes								1B
0E19	E		Address: 0x0300								03
0E1A	E										00
0E1B	E	Clock distribution	Data: 26 bytes								19
0E1C	E		Address: 0x0400								04
0E1D	E										00
0E1E	E	I/O update	Action: IO_Update								80
0E1F	E	Reference inputs	Data: 8 bytes								07
0E20	E		Address: 0x0500								05
0E21	E										00
0E22	E	Profile 0 and Profile 1	Data: 100 bytes								63
0E23	E		Address: 0x0600								06
0E24	E										00

Addr	Opt	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def
0E25	E	Profile 2 and Profile 3	Data: 100 bytes								63
0E26	E		Address: 0x0680								06
0E27	E										80
0E28	E	Profile 4 and Profile 5	Data: 100 bytes								63
0E29	E		Address: 0x0700								07
0E2A	E										00
0E2B	E	Profile 6 and Profile 7	Data: 100 bytes								63
0E2C	E		Address: 0x0780								07
0E2D	E										80
0E2E	E	I/O update	Action: IO_Update								80
0E2F	E	Operational controls	Data: 17 bytes								10
0E30	E		Address: 0x0A00								0A
0E31	E										00
0E32	E	I/O update	Action: IO_Update								80
0E33	E	End of data	Action: end of data								FF
0E34 to 0E3F	E		Continuation of scratch pad area								

REGISTER MAP BIT DESCRIPTIONS

SERIAL PORT CONFIGURATION (REGISTER 0000 TO REGISTER 0005)

Table 36. Serial Configuration

Address	Bits	Bit Name	Description
0000	[7]	Unidirectional	Select SPI port SDO pin operating mode. 0 (default) = 3-wire. 1 = 4-wire (SDO pin enabled).
	[6]	LSB first	Bit order for SPI port. 0 (default) = most significant bit and byte first. 1 = least significant bit and byte first.
	[5]	Soft reset	Device reset (invokes an EEPROM download if M[7:3] ≠ 0). 0 (default) = normal operation. 1 = reset.
	[4]	Long instruction	16-bit mode (the only mode supported by the device). This bit is read only and reads back as Logic 1.
	[0]	Unused	

Table 37. Reserved Register

Address	Bits	Bit Name	Description
0001	[7:0]	Unused	

Table 38. Silicon Revision Level (Read-Only)

Address	Bits	Bit Name	Description
0002	[7:0]	Reserved	Default = 0x01 = 0b00000001

Table 39. Device ID (Read Only)

Address	Bits	Bit Name	Description
0003	[7:0]	Reserved	Default = 0x48 = 0b01001000

Table 40. Register Readback Control

Address	Bits	Bit Name	Description
0004	[7:1]	Unused	
	0	Read buffer register	For buffered registers, serial port readback reads from actual (active) registers instead of from the buffer. 0 (default) = reads values currently applied to the internal logic of the device. 1 = reads buffered values that take effect on the next assertion of the I/O update.

Table 41. Soft I/O Update

Address	Bits	Bit Name	Description
0005	[7:1]	Unused	
	0	I/O update	Writing a 1 to this bit transfers the data in the serial I/O buffer registers to the internal control registers of the device. This is an autoclearing bit.

SYSTEM CLOCK (REGISTER 0100 TO REGISTER 0108)

Table 42. Charge Pump and Lock Detect Control

Address	Bits	Bit Name	Description
0100	[7]	External loop filter enable	Enables use of an external SYSCLK PLL loop filter 0 (default) = internal loop filter 1 = external loop filter
	[6]	Charge pump mode	Charge pump current control 0 (default) = automatic 1 = manual
	[5:3]	Charge pump current	Selects charge pump current when Bit 6 = 1 000 = 125 µA 001 = 250 µA 010 = 375 µA 011 (default) = 500 µA 100 = 625 µA 101 = 750 µA 110 = 875 µA 111 = 1000 µA
	[2]	Lock detect timer disable	Enable the SYSCLK PLL lock detect timer 0 (default) = enable 1 = disable
	[1:0]	Lock detect timer	Select lock detect timer depth 00 (default) = 128 01 = 256 10 = 512 11 = 1024

Table 43. N Divider

Address	Bits	Bit Name	Description
0101	[7:0]	N-divider	System clock PLL feedback divider value: 6 ≤ N ≤ 255 (default = 0x28 = 40)

Table 44. SYSCLK Input Options

Address	Bits	Bit Name	Description
0102	[7]	Unused	
	[6]	M-divider reset	Reset the M-divider 0 = normal operation 1 (default) = reset When not using the M-divider, program this bit to Logic 1.
	[5:4]	M-divider	System clock input divider 00 (default) = 1 01 = 2 10 = 4 11 = 8
	[3]	2× frequency multiplier enable	Enable the 2× frequency multiplier 0 (default) = disable 1 = enable
	[2]	PLL enable	Enable the SYSCLK PLL 0 = disable 1 (default) = enable
	[1:0]	System clock source	Input mode select for SYSCLKx pins 00 = crystal resonator 01 (default) = low frequency clock source 10 = high frequency (direct) clock source 11 = input receiver power-down

Table 45. Nominal System Clock (SYSCLK) Period[1]

Address	Bits	Bit Name	Description
0103	[7:0]	System clock period (expressed in femtoseconds)	System clock period, Bits[7:0]
0104	[7:0]		System clock period, Bits[15:8]
0105	[7:5]	Unused	
	[4:0]	System clock period	System clock period, Bits[20:16]

[1] Units are femtoseconds. The default value is 0x0F424 = 1,000,000 (1 ns) and implies a system clock frequency of 1 GHz.

Table 46. System Clock Stability Period[1]

Address	Bits	Bit Name	Description
0106	[7:0]	System clock stability period	System clock stability period, Bits[7:0] (default = 0x01)
0107	[7:0]		System clock stability period, Bits[15:8] (default = 0x00)
0108	[7:4]	Unused	
	[3:0]	System clock stability period	System clock stability period, Bits[19:16] (default = 0x0) (default period = 0x00001, or 1 ms)

[1] Units are milliseconds. The default value is 0x000001 = 1 (1 ms).

GENERAL CONFIGURATION (REGISTER 0200 TO REGISTER 0214)

Register 0200 to Register 0207—Multifunction Pin Control (M0 to M7)

Table 47. Multifunction Pin (M0 to M7) Control[1]

Address	Bits	Bit Name	Description
0200	[7]	M0 in/out	In/out control for the M0 pin 0 (default) = input (control pin) 1 = output (status pin)
	[6:0]	M0 function	See Table 24 and Table 25 (default = 0xb0000000)
0201	[7]	M1 in/out	In/out control for the M1 pin (same as M0)
	[6:0]	M1 function	See Table 24 and Table 25 (default = 0xb0000000)
0202	[7]	M2 in/out	In/out control for the M2 pin (same as M0)
	[6:0]	M2 function	See Table 24 and Table 25 (default = 0xb0000000)
0203	[7]	M3 in/out	In/out control for the M3 pin (same as M0)
	[6:0]	M3 function	See Table 24 and Table 25 (default = 0xb0000000)
0204	[7]	M4 in/out	In/out control for the M4 pin (same as M0)
	[6:0]	M4 function	See Table 24 and Table 25 (default = 0xb0000000)
0205	[7]	M5 in/out	In/out control for the M5 pin (same as M0)
	[6:0]	M5 function	See Table 24 and Table 25 (default = 0xb0000000)
0206	[7]	M6 in/out	In/out control for the M6 pin (same as M0)
	[6:0]	M6 function	See Table 24 and Table 25 (default = 0xb0000000)
0207	[7]	M7 in/out	In/out control for the M7 pin (same as M0)
	[6:0]	M7 function	See Table 24 and Table 25 (default = 0xb0000000)

[1] The default setting for all the multifunction pins is as an unused control input pin.

Table 48. IRQ Pin Output Mode

Address	Bits	Bit Name	Description
0208	[7:2]	Unused	
	[1:0]	IRQ pin output mode	Select the output mode of the IRQ pin 00 (default) = NMOS, open drain (requires an external pull-up resistor) 01 = PMOS, open drain (requires an external pull-down resistor) 10 = CMOS, active high 11 = CMOS, active low

Register 0209 to Register 0210—IRQ Mask

The IRQ mask register bits form a one-to-one correspondence with the bits of the IRQ monitor register (Address 0D02 to Address 0D09). When set to Logic 1, the IRQ mask bits enable the corresponding IRQ monitor bits to indicate an IRQ event. The default for all IRQ mask bits is Logic 0, which prevents the IRQ monitor from detecting any internal interrupts.

Table 49. IRQ Mask for SYSCLK

Address	Bits	Bit Name	Description
0209	[7:6]	Unused	
	[5]	SYSCLK unlocked	Enables IRQ for indicating a SYSCLK PLL state transition from locked to unlocked
	[4]	SYSCLK locked	Enables IRQ for indicating a SYSCLK PLL state transition from unlocked to locked
	[3:2]	Unused	
	[1]	SYSCLK Cal complete	Enables IRQ for indicating that SYSCLK calibration has completed
	[0]	SYSCLK Cal started	Enables IRQ for indicating that SYSCLK calibration has begun

Table 50. IRQ Mask for Distribution Sync, Watchdog Timer, and EEPROM

Address	Bits	Bit Name	Description
020A	[7:4]	Unused	
	[3]	Distribution sync	Enables IRQ for indicating a distribution sync event
	[2]	Watchdog timer	Enables IRQ for indicating expiration of the watchdog timer
	[1]	EEPROM fault	Enables IRQ for indicating a fault during an EEPROM load or save operation
	[0]	EEPROM complete	Enables IRQ for indicating successful completion of an EEPROM load or save operation

Table 51. IRQ Mask for the Digital PLL

Address	Bits	Bit Name	Description
020B	[7]	Switching	Enables IRQ for indicating that the DPLL is switching to a new reference
	[6]	Closed	Enables IRQ for indicating that the DPLL has entered closed-loop operation
	[5]	Freerun	Enables IRQ for indicating that the DPLL has entered free-run mode
	[4]	Holdover	Enables IRQ for indicating that the DPLL has entered holdover mode
	[3]	Freq unlocked	Enables IRQ for indicating that the DPLL lost frequency lock
	[2]	Freq locked	Enables IRQ for indicating that the DPLL has acquired frequency lock
	[1]	Phase unlocked	Enables IRQ for indicating that the DPLL lost phase lock
	[0]	Phase locked	Enables IRQ for indicating that the DPLL has acquired phase lock

Table 52. IRQ Mask for History Update, Frequency Limit, and Phase Slew Limit

Address	Bits	Bit Name	Description
020C	[7:5]	Unused	
	[4]	History updated	Enables IRQ for indicating the occurrence of a tuning word history update
	[3]	Frequency unclamped	Enables IRQ for indicating a state transition frequency limiter from clamped to unclamped
	[2]	Frequency clamped	Enables IRQ for indicating a state transition of the frequency limiter from unclamped to clamped
	[1]	Phase slew unlimited	Enables IRQ for indicating a state transition of the phase slew limiter from slew limiting to not slew limiting
	[0]	Phase slew limited	Enables IRQ for indicating a state transition of the phase slew limiter from not slew limiting to slew limiting

Table 53. IRQ Mask for Reference Inputs

Address	Bits	Bit Name	Description
020D	[7]	Ref AA new profile	Enables IRQ for indicating that Ref AA has switched to a new profile
	[6]	Ref AA validated	Enables IRQ for indicating that Ref AA has been validated
	[5]	Ref AA fault cleared	Enables IRQ for indicating that Ref AA has been cleared of a previous fault
	[4]	Ref AA fault	Enables IRQ for indicating that Ref AA has been faulted
	[3]	Ref A new profile	Enables IRQ for indicating that Ref A has switched to a new profile
	[2]	Ref A validated	Enables IRQ for indicating that Ref A has been validated
	[1]	Ref A fault cleared	Enables IRQ for indicating that Ref A has been cleared of a previous fault
	[0]	Ref A fault	Enables IRQ for indicating that Ref A has been faulted
020E	[7]	Ref BB new profile	Enables IRQ for indicating that Ref BB has switched to a new profile
	[6]	Ref BB validated	Enables IRQ for indicating that Ref BB has been validated
	[5]	Ref BB fault cleared	Enables IRQ for indicating that Ref BB has been cleared of a previous fault
	[4]	Ref BB fault	Enables IRQ for indicating that Ref BB has been faulted
	[3]	Ref B new profile	Enables IRQ for indicating that Ref B has switched to a new profile
	[2]	Ref B validated	Enables IRQ for indicating that Ref B has been validated
	[1]	Ref B fault cleared	Enables IRQ for indicating that Ref B has been cleared of a previous fault
	[0]	Ref B fault	Enables IRQ for indicating that Ref B has been faulted
020F	[7]	Ref CC new profile	Enables IRQ for indicating that Ref CC has switched to a new profile
	[6]	Ref CC validated	Enables IRQ for indicating that Ref CC has been validated
	[5]	Ref CC fault cleared	Enables IRQ for indicating that Ref CC has been cleared of a previous fault
	[4]	Ref CC fault	Enables IRQ for indicating that Ref CC has been faulted
	[3]	Ref C new profile	Enables IRQ for indicating that Ref C has switched to a new profile
	[2]	Ref C validated	Enables IRQ for indicating that Ref C has been validated
	[1]	Ref C fault cleared	Enables IRQ for indicating that Ref C has been cleared of a previous fault
	[0]	Ref C fault	Enables IRQ for indicating that Ref C has been faulted
0210	[7]	Ref DD new profile	Enables IRQ for indicating that Ref DD has switched to a new profile
	[6]	Ref DD validated	Enables IRQ for indicating that Ref DD has been validated
	[5]	Ref DD fault cleared	Enables IRQ for indicating that Ref DD has been cleared of a previous fault
	[4]	Ref DD fault	Enables IRQ for indicating that Ref DD has been faulted
	[3]	Ref D new profile	Enables IRQ for indicating that Ref D has switched to a new profile
	[2]	Ref D validated	Enables IRQ for indicating that Ref D has been validated
	[1]	Ref D fault cleared	Enables IRQ for indicating that Ref D has been cleared of a previous fault
	[0]	Ref D fault	Enables IRQ for indicating that Ref D has been faulted

Table 54. Watchdog Timer[1]

Address	Bits	Bit Name	Description
0211	[7:0]	Watchdog timer	Watchdog timer, Bits[7:0] (default = 0x00)
0212	[7:0]		Watchdog timer, Bits[15:8] (default = 0x00)

[1] The watchdog timer is expressed in milliseconds. The default value is 0 (disabled).

Table 55. Auxiliary DAC[1]

Address	Bits	Bit Name	Description
0213	[7:0]	Full-scale current	Full scale current, Bits[7:0] (default = 0xFF)
0214	[7]	DAC shutdown	Shut down the DAC current sources. 0 (default) = normal operation 1 = shut down
	[6:2]	Unused	
	[1:0]	Full-scale current	Full-scale current, Bits[9:8] (default = 0b01) (default current = 0x1FF, or 20.1 mA)

[1] The default DAC full-scale current value is 0x01FF = 511, which equates to 20.1375 mA.

DPLL CONFIGURATION (REGISTER 0300 TO REGISTER 031B)

Table 56. Free Running Frequency Tuning Word[1]

Address	Bits	Bit Name	Description
0300	[7:0]	Frequency (expressed as a 48-bit frequency tuning word)	Free running frequency tuning word, Bits[7:0]
0301	[7:0]		Free running frequency tuning word, Bits[15:8]
0302	[7:0]		Free running frequency tuning word, Bits[23:9]
0303	[7:0]		Free running frequency tuning word, Bits[31:24]
0304	[7:0]		Free running frequency tuning word, Bits[39:32]
0305	[7:0]		Free running frequency tuning word, Bits[47:40]

[1] The default free running tuning word is 0x000000 = 0, which equates to 0 Hz.

Table 57. Update TW

Address	Bits	Bit Name	Description
0306	[7:1]	Unused	
	[0]	Update TW	A Logic 1 written to this bit transfers the free running frequency tuning word (Register 0300 to Register 0305) to the register imbedded in the tuning word processing logic. Note that it is not necessary to write the update TW bit when the device is in free-run mode. This is an autoclearing bit.

Table 58. Pull-In Range Lower Limit[1]

Address	Bits	Bit Name	Description
0307	[7:0]	Pull-in range lower limit (expressed as a 24-bit frequency tuning word)	Lower limit pull-in range, Bits[7:0]
0308	[7:0]		Lower limit pull-in range, Bits[15:8]
0309	[7:0]		Lower limit pull-in range, Bits[23:9]
030A	[7:0]	Pull-in range upper limit (expressed as a 24-bit frequency tuning word)	Upper limit pull-in range, Bits[7:0]
030B	[7:0]		Upper limit pull-in range, Bits[15:8]
030C	[7:0]		Upper limit pull-in range, Bits[23:9]

[1] The default pull-in range lower limit is 0 and the upper range limit is 0xFFFFFF, which effectively spans the full output frequency range of the DDS.

Table 59. DDS Phase Offset[1]

Address	Bits	Bit Name	Description
030D	[7:0]	Open-loop phase offset (expressed in $\pi/2^{15}$ radians)	DDS phase offset, Bits[7:0]
030E	[7:0]		DDS phase offset, Bits[15:8]

[1] The default DDS phase offset is 0.

Table 60. Fixed Closed-Loop Phase Lock Offset[1]

Address	Bits	Bit Name	Description
030F	[7:0]	Fixed phase lock offset (expressed in pico-seconds)	Fixed phase lock offset, Bits[7:0]
0310	[7:0]		Fixed phase lock offset, Bits[15:8]
0311	[7:0]		Fixed phase lock offset, Bits[23:16]
0312	[7:0]		Fixed phase lock offset, Bits[31:24]
0313	[7:0]		Fixed phase lock offset, Bits[39:32]

[1] The default fixed closed loop phase lock offset is 0.

Table 61. Incremental Closed-Loop Phase Lock Offset Step Size[1]

Address	Bits	Bit Name	Description
0314	[7:0]	Incremental phase lock offset step size (expressed in pico-seconds per step)	Incremental phase lock offset step size, Bits[7:0]
0315	[7:0]		Incremental phase lock offset step size, Bits[15:8]

[1] The default incremental closed-loop phase lock offset step size value is 0x03E8 = 1000 (1 ns).

Table 62. Phase Slew Rate Limit[1]

Address	Bits	Bit Name	Description
0316	[7:0]	Phase slew limit (expressed in nano-seconds per second)	Phase slew rate limit, Bits[7:0]
0317	[7:0]		Phase slew rate limit, Bits[15:8]

[1] The default phase slew rate limit is 0 (or disabled).

Table 63. History Accumulation Timer[1]

Address	Bits	Bit Name	Description
0318	[7:0]	History accumulation timer (expressed in milliseconds)	History accumulation timer, Bits[7:0]
0319	[7:0]		History accumulation timer, Bits[15:8]
031A	[7:0]		History accumulation timer, Bits[23:16]

[1] Do not program a timer value of 0. The history accumulation timer default value is 0x007530 = 30,000 (30 sec).

Table 64. History Mode

Address	Bits	Bit Name	Description
031B	[7:5]	Unused	
	[4]	Single-sample fallback	Controls the holdover history. If tuning word history is not available for the reference that was active just prior to holdover, then 0 (default) = use the free running frequency tuning word register value. 1 = use the last tuning word from the DPLL.
	[3]	Persistent history	Controls the holdover history initialization. When switching to a new reference 0 (default) = clear the tuning word history. 1 = retain the previous tuning word history.
	[2:0]	Incremental average	History mode value from 0 to 7 (default = 0).

CLOCK DISTRIBUTION OUTPUT CONFIGURATION (REGISTER 0400 TO REGISTER 0419)

Table 65. Distribution Settings[1]

Address	Bits	Bit Name	Description
0400	[7:6]	Unused	
	[5]	External distribution resistor	Output current control for the clock distribution outputs 0 (default) = internal current setting resistor 1 = external current setting resistor
	[4]	Receiver mode	Clock distribution receiver mode 0 (default) = normal operation 1 = high frequency mode (super-Nyquist)
	[3]	OUT3 power-down	Power-down clock distribution output OUT3 0 (default) = normal operation 1 = power-down
	[2]	OUT2 power-down	Power-down clock distribution output OUT2 0 (default) = normal operation 1 = power-down
	[1]	OUT1 power-down	Power-down clock distribution output OUT1 0 (default) = normal operation 1 = power-down
	[0]	OUT0 power-down	Power-down clock distribution output OUT0 0 (default) = normal operation 1 = power-down

[1] When Bits[3:0] = 1111, the clock distribution output enters a deep sleep mode.

Table 66. Distribution Enable

Address	Bits	Bit Name	Description
0401	[7:4]	Unused	
	[3]	OUT3 enable	Enable the OUT3 driver. 0 (default) = disable. 1 = enable.
	[2]	OUT2 enable	Enable the OUT2 driver. 0 (default) = disable. 1 = enable.
	[1]	OUT1 enable	Enable the OUT1 driver. 0 (default) = disable. 1 = enable.
	[0]	OUT0 enable	Enable the OUT0 driver. 0 (default) = disable. 1 = enable.

Table 67. Distribution Synchronization

Address	Bits	Bit Name	Description
0402	[7:6]	Unused	
	[5:4]	Sync source	Select the sync source for the clock distribution output channels. 00 (default) = direct. 01 = active reference. 10 = DPLL feedback edge. 11 = reserved.
	[3]	OUT3 sync mask	Mask the synchronous reset to the OUT3 divider. 0 (default) = unmasked 1 = masked.
	[2]	OUT2 sync mask	Mask the synchronous reset to the OUT2 divider. 0 (default) = unmasked. 1 = masked.
	[1]	OUT1 sync mask	Mask the synchronous reset to the OUT1 divider. 0 (default) = unmasked. 1 = masked.
	[0]	OUT0 sync mask	Mask the synchronous reset to the OUT0 divider. 0 (default) = unmasked. 1 = masked.

Table 68. Automatic Synchronization

Address	Bits	Bit Name	Description
0403	[7:2]	Unused	
	[1:0]	Automatic sync mode	Autosync mode 00 (default) = disabled 01 = sync on DPLL frequency lock 10 = sync on DPLL phase lock 11 = reserved

Table 69. Distribution Channel Modes

Address	Bits	Bit Name	Description
0404	[7:6]	Unused	
	[5]	OUT0 CMOS phase invert	When the output mode is CMOS, the bit inverts the relative phase between the two CMOS output pins. Otherwise, this bit is nonfunctional. 0 (default) = not inverted. 1 = inverted.
	[4]	OUT0 polarity invert	Invert the polarity of OUT0. 0 (default) = not inverted. 1 = inverted.
	[3]	OUT0 drive strength	OUT0 output drive capability control. 0 (default) = CMOS: low drive strength; LVDS: 3.5 mA nominal. 1 = CMOS: normal drive strength; LVDS: 7 mA nominal.
	[2:0]	OUT0 mode	OUT0 operating mode select. 000 = CMOS (both pins) 001 = CMOS (positive pin), tristate (negative pin). 010 = tristate (positive pin), CMOS (negative pin). 011 (default) = tristate (both pins). 100 = LVDS. 101 = LVPECL. 110 = reserved. 111 = reserved.

Address	Bits	Bit Name	Description
0405	[7:6]	Unused	
	[5]	OUT1 CMOS phase invert	When the output mode is CMOS, the bit inverts the relative phase between the two CMOS output pins. Otherwise, this bit is nonfunctional. 0 (default) = not inverted. 1 = inverted.
	[4]	OUT1 polarity invert	Invert the polarity of OUT1. 0 (default) = not inverted. 1 = inverted.
	[3]	OUT1 drive strength	OUT1 output drive capability control. 0 (default) = CMOS: low drive strength; LVDS: 3.5 mA nominal. 1 = CMOS: normal drive strength; LVDS: 7 mA nominal.
	[2:0]	OUT1 mode	OUT1 operating mode select. 000 = CMOS (both pins). 001 = CMOS (positive pin), tristate (negative pin). 010 = tristate (positive pin), CMOS (negative pin). 011 (default) = tristate (both pins). 100 = LVDS. 101 = LVPECL. 110 = reserved. 111 = reserved.
0406	[7:6]	Unused	
	[5]	OUT2 CMOS phase invert	When the output mode is CMOS, the bit inverts the relative phase between the two CMOS output pins. Otherwise, this bit is nonfunctional. 0 (default) = not inverted. 1 = inverted.
	[4]	OUT2 polarity invert	Invert the polarity of OUT2. 0 (default) = not inverted. 1 = inverted.
	[3]	OUT2 drive strength	OUT2 output drive capability control. 0 (default) = CMOS: low drive strength; LVDS: 3.5 mA nominal. 1 = CMOS: normal drive strength; LVDS: 7 mA nominal.
	[2:0]	OUT2 mode	OUT2 operating mode select. 000 = CMOS (both pins). 001 = CMOS (positive pin), tristate (negative pin). 010 = tristate (positive pin), CMOS (negative pin). 011 (default) = tristate (both pins). 100 = LVDS. 101 = LVPECL. 110 = reserved. 111 = reserved.

Address	Bits	Bit Name	Description
0407	[7:6]	Unused	
	[5]	OUT3 CMOS phase invert	When the output mode is CMOS, the bit inverts the relative phase between the two CMOS output pins. Otherwise, this bit is nonfunctional. 0 (default) = not inverted. 1 = inverted.
	[4]	OUT3 polarity invert	Invert the polarity of OUT3. 0 (default) = not inverted. 1 = inverted.
	[3]	OUT3 drive strength	OUT3 output drive capability control. 0 (default) = CMOS: low drive strength; LVDS: 3.5 mA nominal. 1 = CMOS: normal drive strength; LVDS: 7 mA nominal.
	[2:0]	OUT3 mode	OUT3 operating mode select. 000 = CMOS (both pins). 001 = CMOS (positive pin), tristate (negative pin). 010 = tristate (positive pin), CMOS (negative pin). 011 (default) = tristate (both pins). 100 = LVDS. 101 = LVPECL. 110 = reserved. 111 = reserved.

Register 0408 to Register 0417—Distribution Channel Dividers

Table 70. Q0 Divider[1]

Address	Bits	Bit Name	Description
0408	[7:0]	Q0	Q0 divider, Bits[7:0]
0409	[7:0]		Q0 divider, Bits[15:8]
040A	[7:0]		Q0 divider, Bits[23:16]
040B	[7:6]	Unused	
	[5:0]	Q0	Q0 divider, Bits[29:24]

[1] The default value is 0 (or divide by 1).

Table 71. Q1 Divider[1]

Address	Bits	Bit Name	Description
040C	[7:0]	Q1	Q1 divider, Bits[7:0]
040D	[7:0]		Q1 divider, Bits[15:8]
040E	[7:0]		Q1 divider, Bits[23:16]
040F	[7:6]	Unused	
	[5:0]	Q1	Q1 divider, Bits[29:24]

[1] The default value is 0 (or divide by 1).

Table 72. Q2 Divider[1]

Address	Bits	Bit Name	Description
0410	[7:0]	Q2	Q2 divider, Bits[7:0]
0411	[7:0]		Q2 divider, Bits[15:8]
0412	[7:0]		Q2 divider, Bits[23:16]
0413	[7:6]	Unused	
	[5:0]	Q2	Q2 divider, Bits[29:24]

[1] The default value is 0 (or divide by 1).

Table 73. Q3 Divider[1]

Address	Bits	Bit Name	Description
0414	[7:0]	Q3	Q3 divider, Bits[7:0]
0415	[7:0]		Q3 divider, Bits[15:8]
0416	[7:0]		Q3 divider, Bits[23:16]
0417	[7:6]	Unused	
	[5:0]	Q3	Q3 divider, Bits[29:24]

[1] The default value is 0 (or divide by 1).

REFERENCE INPUT CONFIGURATION (REGISTER 0500 TO REGISTER 0507)

Table 74. Reference Power-Down

When all bits are set, the reference receiver section enters a deep sleep mode.

Address	Bits	Bit Name	Description
0500	[7]	Ref DD power-down	REF DD input receiver power-down 0 (default) = normal operation 1 = power-down
	[6]	Ref D power-down	REF D input receiver power-down 0 (default) = normal operation 1 = power-down
	[5]	Ref CC power-down	REF CC input receiver power-down 0 (default) = normal operation 1 = power-down
	[4]	Ref C power-down	REF C input receiver power-down 0 (default) = normal operation 1 = power-down
	[3]	Ref BB power-down	REF BB input receiver power-down 0 (default) = normal operation 1 = power-down
	[2]	Ref B power-down	REF B input receiver power-down 0 (default) = normal operation 1 = power-down
	[1]	Ref AA power-down	REF AA input receiver power-down 0 (default) = normal operation 1 = power-down
	[0]	Ref A power-down	REF A input receiver power-down 0 (default) = normal operation 1 = power-down

Table 75. Reference Logic Family

Address	Bits	Bit Name	Description
0501	[7:6]	Ref BB logic family	Select the logic family for the REF BB input receiver (ignored if Bits[5:4] = 00) 00 (default) = disabled 01 = 1.2 V to 1.5 V CMOS 10 = 1.8 V to 2.5 V CMOS 11 = 3.0 V to 3.3 V CMOS
	[5:4]	Ref B logic family	Select logic family for REF B input receiver. 00 (default) = differential (REFB/BB is positive/negative input) 01 = 1.2 V to 1.5 V CMOS 10 = 1.8 V to 2.5 V CMOS 11 = 3.0 V to 3.3 V CMOS
	[3:2]	Ref AA logic family	The same as Register 0501, Bits[7:6] but for REF AA
	[1:0]	Ref A logic family	The same as Register 0501, Bits[5:4] but for REF A
0502	[7:6]	Ref DD logic family	The same as Register 0501, Bits[7:6] but for REF DD
	[5:4]	Ref D logic family	The same as Register 0501, Bits[5:4] but for REF D
	[3:2]	Ref CC logic family	The same as Register 0501, Bits[7:6] but for REF CC
	[1:0]	Ref C logic family	The same as Register 0501, Bits[5:4] but for REF C

Table 76. Manual Reference Profile Selection

Address	Bits	Bit Name	Description
0503	[7]	Enable Ref AA manual profile	Select manual or automatic reference profile assignment for REF AA 0 (default) = automatic 1 = manual
	[6:4]	Ref AA manual profile	Manual profile assignment 000 (default) = Profile 0 001 = Profile 1 010 = Profile 2 011 = Profile 3 100 = Profile 4 101 = Profile 5 110 = Profile 6 111 = Profile 7
	[3]	Enable Ref A manual profile	Same as Register 0503, Bit 7 but for REF A
	[2:0]	Ref A manual profile	Same as Register 0503, Bits[6:4] but for REF A
0504	[7]	Enable Ref BB manual profile	Same as Register 0503, Bit 7 but for REF B
	[6:4]	Ref BB manual profile	Same as Register 0503, Bits[6:4] but for REF BB
	[3]	Enable Ref B manual profile	Same as Register 0503, Bit 7 but for REF B
	[2:0]	Ref B manual profile	Same as Register 0503, Bits[6:4] but for REF B
0505	[7]	Enable Ref CC manual profile	Same as Register 0503, Bit 7 but for REF CC
	[6:4]	Ref CC manual profile	Same as Register 0503, Bits[6:4] but for REF CC
	[3]	Enable Ref C manual profile	Same as Register 050, Bit 7 but for REF C
	[2:0]	Ref C manual profile	Same as Register 0503, Bits[6:4] but for REF C
0506	[7]	Enable Ref DD M manual profile	Same as Register 0503, Bit 7 but for REF DD
	[6:4]	Ref DD manual profile	Same as Register 0503, Bits[6:4] but for REF DD
	[3]	Enable Ref D manual profile	Same as Register 0503, Bit 7 but for REF D
	[2:0]	Ref D manual profile	Same as Register 0503, Bits[6:4] but for REF D

Table 77. Phase Build-Out Switching

Address	Bits	Bit Name	Description
0507	[7:3]	Unused	
	[2:0]	Phase master threshold priority	Threshold priority level (a value of 0 to 7, with 0 (default) being the highest priority level). References with a selection priority value lower than this value are treated as phase masters (see the Profile Registers (Register 0600 to Register 07FF) section for the selection priority value).

PROFILE REGISTERS (REGISTER 0600 TO REGISTER 07FF)

Note that the default value of every bit is 0 for Profile 0 to Profile 7.

Register 0600 to Register 0631—Profile 0

Table 78. Priorities—Profile 0

Address	Bits	Bit Name	Description
0600	[7:6]	Unused	
	[5:3]	Promoted priority	User-assigned priority level (0 to 7) of the reference associated with Profile 0 while that reference is the active reference. The numeric value of the promoted priority must be less than or equal to the numeric value of the selection priority.
	[2:0]	Selection priority	User-assigned priority level (0 to 7) of the reference associated with Profile 0, which ranks that reference relative to the others.

Table 79. Reference Period—Profile 0

Address	Bits	Bit Name	Description
0601	[7:0]	Reference period (in femtoseconds)	Nominal reference period, Bits[7:0]
0602	[7:0]		Nominal reference period, Bits[15:8]
0603	[7:0]		Nominal reference period, Bits[23:16]
0604	[7:0]		Nominal reference period, Bits[31:24]
0605	[7:0]		Nominal reference period, Bits[39:32]
0606	[7:0]		Nominal reference period, Bits[47:40]
0607	[7:2]	Unused	
	[1:0]	Reference period	Nominal reference period, Bits[49:48]

Table 80. Tolerance—Profile 0

Address	Bits	Bit Name	Description
0608	[7:0]	Inner tolerance	Inner tolerance, Bits[7:0]
0609	[7:0]		Inner tolerance, Bits[15:8]
060A	[7:4]	Unused	
	[3:0]	Inner tolerance	Inner tolerance, Bits[19:16]
060B	[7:0]	Outer tolerance	Outer tolerance, Bits[7:0]
060C	[7:0]		Outer tolerance, Bits[5:8]
060D	[7:4]	Unused	
	[3:0]	Outer tolerance	Outer tolerance, Bits[19:16]

Table 81. Validation Timer—Profile 0

Address	Bits	Bit Name	Description
060E	[7:0]	Validation timer (in milliseconds)	Validation timer, Bits[7:0]
060F	[7:0]		Validation timer, Bits[15:8]

Table 82. Redetect Timer—Profile 0

Address	Bits	Bit Name	Description
0610	[7:0]	Redetect timer (in milliseconds)	Redetect timer, Bits[7:0]
0611	[7:0]		Redetect timer, Bits[15:8]

Table 83. Digital Loop Filter Coefficients—Profile 0[1]

Address	Bits	Bit Name	Description
0612	[7:0]	Alpha-0 linear	Alpha-0 coefficient linear, Bits[7:0]
0613	[7:0]		Alpha-0 coefficient linear, Bits[15:8]
0614	[7:6]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bits[1:0]
	[5:0]	Alpha-1 exponent	Alpha-1 coefficient exponent, Bits[5:0]
0615	[7:1]	Beta-0 linear	Beta-0 coefficient linear, Bits[6:0]
	[0]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bit 2
0616	[7:0]	Beta-0 linear	Beta-0 coefficient linear, Bits[14:7]
0617	[7]	Unused	
	[6:2]	Beta-1 exponent	Beta-1 coefficient exponent, Bits[4:0]
	[1:0]	Beta-0 linear	Beta-0 coefficient linear, Bits[16:15]
0618	[7:0]	Gamma-0 linear	Gamma-0 coefficient linear, Bits[7:0]
0619	[7:0]		Gamma -0 coefficient linear, Bits[15:8]
061A	[7:6]	Unused	
	[5:1]	Gamma-1 exponent	Gamma-1 coefficient exponent, Bits[4:0]
	[0]	Gamma-0 linear	Gamma-0 coefficient linear, Bit 16
061B	[7:0]	Delta-0 linear	Delta-0 coefficient linear, Bits[7:0]
061C	[7]	Delta-1 exponent	Delta-1 coefficient exponent, Bit 0
	[6:0]	Delta-0 linear	Delta-0 coefficient linear, Bits[14:8]
061D	[7:4]	Alpha-3 exponent	Alpha-3 coefficient exponent, Bits[3:0]
	[3:0]	Delta-1 exponent	Delta-1 coefficient exponent, Bits[4:1]

[1] The digital loop filter coefficients (α, β, γ, and δ) have the general form: $x(2^y)$, where x is the linear component and y is the exponential component of the coefficient. The value of the linear component (x) constitutes a fraction, where $0 \le x < 1$. The exponential component (y) is an integer. See the Calculating Digital Filter Coefficients section for details.

Table 84. R-Divider—Profile 0[1]

Address	Bits	Bit Name	Description
061E	[7:0]	R	R, Bits[7:0]
061F	[7:0]		R, Bits[15:8]
0620	[7:0]		R, Bits[23:16]
0621	[7:6]	Unused	
	[5:0]	R	R, Bits[29:24]

[1] The value stored in the R-divider register yields an actual divide ratio of one more than the programmed value.

Table 85. S-Divider—Profile 0[1]

Address	Bits	Bit Name	Description
0622	[7:0]	S	S, Bits[7:0]
0623	[7:0]		S, Bits[15:8]
0624	[7:0]		S, Bits[23:16]
0625	[7:6]	Unused	
	[5:0]	S	S, Bits[29:24]

[1] The value stored in the S-divider register yields an actual divide ratio of one more than the programmed value. Furthermore, the value of S must be at least 7.

Table 86. Fractional Feedback Divider—Profile 0

Address	Bits	Bit Name	Description
0626	[7:0]	V	V, Bits[7:0]
0627	[7:4]	U	U, Bits[3:0]
	[3:2]	Unused	
	[1:0]	V	V, Bits[9:8]
0628	[7:6]	Unused	
	[5:0]	U	U, Bits[9:4]

Table 87. Lock Detectors—Profile 0

Address	Bits	Bit Name	Description
0629	[7:0]	Phase lock threshold (in picoseconds)	Phase lock threshold, Bits[7:0]
062A	[7:0]		Phase lock threshold, Bits[15:8]
062B	[7:0]	Phase lock fill rate	Phase lock fill rate, Bits[7:0]
062C	[7:0]	Phase lock drain rate	Phase lock drain rate, Bits[7:0]
062D	[7:0]	Frequency lock threshold (in picoseconds)	Frequency lock threshold, Bits[7:0]
062E	[7:0]		Frequency lock threshold, Bits[15:8]
062F	[7:0]		Frequency lock threshold, Bits[23:16]
0630	[7:0]	Frequency lock fill rate	Frequency lock fill rate, Bits[7:0]
0631	[7:0]	Frequency lock drain rate	Frequency lock drain rate, Bits[7:0]

Register 0632 to Register 067F—Profile 1

Table 88. Priorities—Profile 1

Address	Bits	Bit Name	Description
0632	[7:6]	unused	
	[5:3]	Promoted priority	User-assigned priority level (0 to 7) of the reference associated with Profile 1 while that reference is the active reference. The numeric value of the promoted priority must be less than or equal to the numeric value of the selection priority.
	[2:0]	Selection priority	User-assigned priority level (0 to 7) of the reference associated with Profile 1, which ranks that reference relative to the others.

Table 89. Reference Period—Profile 1

Address	Bits	Bit Name	Description
0633	[7:0]	Reference period (in femtoseconds)	Nominal reference period, Bits[7:0]
0634	[7:0]		Nominal reference period, Bits[15:8]
0635	[7:0]		Nominal reference period, Bits[23:16]
0636	[7:0]		Nominal reference period, Bits[31:24]
0637	[7:0]		Nominal reference period, Bits[39:32]
0638	[7:0]		Nominal reference period, Bits[47:40]
0639	[7:2]	Unused	
	[1:0]	Reference period	Nominal reference period, Bits[49:48]

Table 90. Tolerance—Profile 1

Address	Bits	Bit Name	Description
063A	[7:0]	Inner tolerance	Inner tolerance, Bits[7:0]
063B	[7:0]		Inner tolerance, Bits[15:8]
063C	[7:4]	Unused	
	[3:0]	Inner tolerance	Inner tolerance, Bits[19:16]
063D	[7:0]	Outer tolerance	Outer tolerance, Bits[7:0]
063E	[7:0]		Outer tolerance, Bits[15:8]
063F	[7:4]	Unused	
	[3:0]	Outer tolerance	Outer tolerance, Bits[19:16]

Table 91. Validation Timer—Profile 1

Address	Bits	Bit Name	Description
0640	[7:0]	Validation timer (in milliseconds)	Validation timer, Bits[7:0]
0641	[7:0]		Validation timer, Bits[15:8]

Table 92. Redetect Timer—Profile 1

Address	Bits	Bit Name	Description
0642	[7:0]	Redetect timer (in milliseconds)	Redetect timer, Bits[7:0]
0643	[7:0]		Redetect timer, Bits[15:8]

Table 93. Digital Loop Filter Coefficients—Profile 1[1]

Address	Bits	Bit Name	Description
0644	[7:0]	Alpha-0 linear	Alpha-0 coefficient linear, Bits[7:0]
0645	[7:0]		Alpha-0 coefficient linear, Bits[15:8]
0646	[7:6]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bits[1:0]
	[5:0]	Alpha-1 exponent	Alpha-1 coefficient exponent, Bits[5:0]
0647	[7:1]	Beta -0 linear	Beta-0 coefficient linear, Bits[6:0]
	[0]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bit 2
0648	[7:0]	Beta-0 linear	Beta-0 coefficient linear, Bits[14:7]
0649	[7]	Unused	
	[6:2]	Beta-1 exponent	Beta-1 coefficient exponent, Bits[4:0]
	[1:0]	Beta-0 linear	Beta-0 coefficient linear, Bits[16:15]
064A	[7:0]	Gamma-0 linear	Gamma-0 coefficient linear, Bits[7:0]
064B	[7:0]		Gamma-0 coefficient linear, Bits[15:8]
064C	[7:6]	Unused	
	[5:1]	Gamma-1 exponent	Gamma-1 coefficient exponent, Bits[4:0]
	[0]	Gamma-0 linear	Gamma-0 coefficient linear, Bit 16
064D	[7:0]	Delta-0 linear	Delta-0 coefficient linear, Bits[7:0]
064E	[7]	Delta-1 exponent	Delta-1 coefficient exponent, Bit 0
	[6:0]	Delta-0 linear	Delta-0 coefficient linear, Bits[14:8]
064F	[7:4]	Alpha-3 exponent	Alpha-3 coefficient exponent, Bits[3:0]
	[3:0]	Delta-1 exponent	Delta-1 coefficient exponent, Bits[4:1]

[1] The digital loop filter coefficients (α, β, γ, and δ) have the general form: $x(2^y)$, where x is the linear component and y is the exponential component of the coefficient. The value of the linear component (x) constitutes a fraction, where $0 \leq x < 1$. The exponential component (y) is an integer. See the Calculating Digital Filter Coefficients section for details.

Table 94. R-Divider—Profile 1[1]

Address	Bits	Bit Name	Description
0650	[7:0]	R	R, Bits[7:0]
0651	[7:0]		R, Bits[15:8]
0652	[7:0]		R, Bits[23:16]
0653	[7:6]	Unused	
	[5:0]	R	R, Bits[29:24]

[1] The value stored in the R-divider register yields an actual divide ratio of one more than the programmed value.

Table 95. S-Divider—Profile 1[1]

Address	Bits	Bit Name	Description
0654	[7:0]	S	S, Bits[7:0]
0655	[7:0]		S, Bits[15:8]
0656	[7:0]		S, Bits[23:16]
0657	[7:6]	Unused	
	[5:0]	S	S, Bits[29:24]

[1] The value stored in the S-divider register yields an actual divide ratio of one more than the programmed value. Furthermore, the value of S must be at least 7.

Table 96. Fractional Feedback Divider—Profile 1

Address	Bits	Bit Name	Description
0658	[7:0]	V	V, Bits[7:0]
0659	[7:4]	U	U, Bits[3:0]
	[3:2]	Unused	
	[1:0]	V	V, Bits[9:8]
065A	[7:6]	Unused	
	[5:0]	U	U, Bits[9:4]

Table 97. Lock Detectors—Profile 1

Address	Bits	Bit Name	Description
065B	[7:0]	Phase lock threshold (in picoseconds)	Phase lock threshold, Bits[7:0]
065C	[7:0]		Phase lock threshold, Bits[15:8]
065D	[7:0]	Phase lock fill rate	Phase lock fill rate, Bits[7:0]
065E	[7:0]	Phase lock drain rate	Phase lock drain rate, Bits[7:0]
065F	[7:0]	Frequency lock threshold (in picoseconds)	Frequency lock threshold, Bits[7:0]
0660	[7:0]		Frequency lock threshold, Bits[15:8]
0661	[7:0]		Frequency lock threshold, Bits[23:16]
0662	[7:0]	Frequency lock fill rate	Frequency lock fill rate, Bits[7:0]
0663	[7:0]	Frequency lock drain rate	Frequency lock drain rate, Bits[7:0]
0664 to 067F	[7:0]	Unused	

Register 0680 to Register 06B1—Profile 2

Table 98. Priorities—Profile 2

Address	Bits	Bit Name	Description
0680	[7:6]	Unused	
	[5:3]	Promoted priority	User-assigned priority level (0 to 7) of the reference associated with Profile 2 while that reference is the active reference. The numeric value of the promoted priority must be less than or equal to the numeric value of the selection priority.
	[2:0]	Selection priority	User-assigned priority level (0 to 7) of the reference associated with Profile 2, which ranks that reference relative to the others.

Table 99. Reference Period—Profile 2

Address	Bits	Bit Name	Description
0681	[7:0]	Reference period (in femtoseconds)	Nominal reference period, Bits[7:0]
0682	[7:0]		Nominal reference period, Bits[15:8]
0683	[7:0]		Nominal reference period, Bits[23:16]
0684	[7:0]		Nominal reference period, Bits[31:24]
0685	[7:0]		Nominal reference period, Bits[39:32]
0686	[7:0]		Nominal reference period, Bits[47:40]
0687	[7:2]	Unused	
	[1:0]	Reference period	Nominal reference period, Bits[49:48]

Table 100. Tolerance—Profile 2

Address	Bits	Bit Name	Description
0688	[7:0]	Inner tolerance	Inner tolerance, Bits[7:0]
0689	[7:0]		Inner tolerance, Bits[15:8]
068A	[7:4]	Unused	
	[3:0]	Inner tolerance	Inner tolerance, Bits[19:16]
068B	[7:0]	Outer tolerance	Outer tolerance, Bits[7:0]
068C	[7:0]		Outer tolerance, Bits[15:8]
068D	[7:4]	Unused	
	[3:0]	Outer tolerance	Outer tolerance, Bits[19:16]

Table 101. Validation Timer—Profile 2

Address	Bits	Bit Name	Description
068E	[7:0]	Validation timer (in milliseconds)	Validation timer, Bits[7:0]
068F	[7:0]		Validation timer, Bits[15:8]

Table 102. Redetect Timer—Profile 2

Address	Bits	Bit Name	Description
0690	[7:0]	Redetect timer (in milliseconds)	Redetect timer, Bits[7:0]
0691	[7:0]		Redetect timer, Bits[15:8]

Table 103. Digital Loop Filter Coefficients—Profile 2[1]

Address	Bits	Bit Name	Description
0692	[7:0]	Alpha-0 linear	Alpha-0 coefficient linear, Bits[7:0]
0693	[7:0]		Alpha-0 coefficient linear, Bits[15:8]
0694	[7:6]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bits[1:0]
	[5:0]	Alpha-1 exponent	Alpha-1 coefficient exponent, Bits[5:0]
0695	[7:1]	Beta-0 linear	Beta-0 coefficient linear, Bits[6:0]
	[0]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bit 2
0696	[7:0]	Beta 0-linear	Beta-0 coefficient linear, Bits[14:7]
0697	[7]	Unused	
	[6:2]	Beta-1 exponent	Beta-1 coefficient exponent, Bits[4:0]
	[1:0]	Beta-0 linear	Beta-0 coefficient linear, Bits[16:15]
0698	[7:0]	Gamma-0 linear	Gamma-0 coefficient linear, Bits[7:0]
0699	[7:0]		Gamma-0 coefficient linear, Bits[15:8]
069A	[7:6]	Unused	
	[5:1]	Gamma-1 exponent	Gamma-1 coefficient exponent, Bits[4:0]
	[0]	Gamma-0 linear	Gamma-0 coefficient linear, Bit 6
069B	[7:0]	Delta -0 linear	Delta-0 coefficient linear, Bits[7:0]

Address	Bits	Bit Name	Description
069C	[7]	Delta-1 exponent	Delta-1 coefficient exponent, Bit 0
	[6:0]	Delta-0 linear	Delta-0 coefficient linear, Bits[14:8]
069D	[7:4]	Alpha-3 exponent	Alpha-3 coefficient exponent, Bits[3:0]
	[3:0]	Delta-1 exponent	Delta-1 coefficient exponent, Bits[4:1]

[1] The digital loop filter coefficients (α, β, γ, and δ) have the general form: $x(2^y)$, where x is the linear component and y is the exponential component of the coefficient. The value of the linear component (x) constitutes a fraction, where $0 \leq x < 1$. The exponential component (y) is an integer. See the Calculating Digital Filter Coefficients section for details.

Table 104. R-Divider—Profile 2[1]

Address	Bits	Bit Name	Description
069E	[7:0]	R	R, Bits[7:0]
069F	[7:0]		R, Bits[15:8]
06A0	[7:0]		R, Bits[23:16]
06A1	[7:6]	Unused	
	[5:0]	R	R, Bits[29:24]

[1] The value stored in the R-divider register yields an actual divide ratio of one more than the programmed value.

Table 105. S-Divider—Profile 2[1]

Address	Bits	Bit Name	Description
06A2	[7:0]	S	S, Bits[7:0]
06A3	[7:0]		S, Bits[15:8]
06A4	[7:0]		S, Bits[23:16]
06A5	[7:6]	Unused	
	[5:0]	S	S, Bits[29:24]

[1] The value stored in the S-divider register yields an actual divide ratio of one more than the programmed value. Furthermore, the value of S must be at least 7.

Table 106. Fractional Feedback Divider—Profile 2

Address	Bits	Bit Name	Description
06A6	[7:0]	V	V, Bits[7:0]
06A7	[7:4]	U	U, Bits[3:0]
	[3:2]	Unused	
	[1:0]	V	V, Bits[9:8]
06A8	[7:6]	Unused	
	[5:0]	U	U, Bits[9:4]

Table 107. Lock Detectors—Profile 2

Address	Bits	Bit Name	Description
06A9	[7:0]	Phase lock threshold (in picoseconds)	Phase lock threshold, Bits[7:0]
06AA	[7:0]		Phase lock threshold, Bits[15:8]
06AB	[7:0]	Phase lock fill rate	Phase lock fill rate, Bits[7:0]
06AC	[7:0]	Phase lock drain rate	Phase lock drain rate, Bits[7:0]
06AD	[7:0]	Frequency lock threshold (in picoseconds)	Frequency lock threshold, Bits[7:0]
06AE	[7:0]		Frequency lock threshold, Bits[15:8]
06AF	[7:0]		Frequency lock threshold, Bits[23:16]
06B0	[7:0]	Frequency lock fill rate	Frequency lock fill rate, Bits[7:0]
06B1	[7:0]	Frequency lock drain rate	Frequency lock drain rate, Bits[7:0]

Register 06B2 to Register 07FF—Profile 3

Table 108. Priorities—Profile 3

Address	Bits	Bit Name	Description
06B2	[7:6]	Unused	
	[5:3]	Promoted priority	User-assigned priority level (0 to 7) of the reference associated with Profile 3 while that reference is the active reference. The numeric value of the promoted priority must be less than or equal to the numeric value of the selection priority.
	[2:0]	Selection priority	User-assigned priority level (0 to 7) of the reference associated with Profile 3, which ranks that reference relative to the others.

Table 109. Reference Period—Profile 3

Address	Bits	Bit Name	Description
06B3	[7:0]	Reference period (in femtoseconds)	Nominal reference period, Bits[7:0]
06B4	[7:0]		Nominal reference period, Bits[15:8]
06B5	[7:0]		Nominal reference period, Bits[23:16]
06B6	[7:0]		Nominal reference period, Bits[31:24]
06B7	[7:0]		Nominal reference period, Bits[39:32]
06B8	[7:0]		Nominal reference period, Bits[47:40]
06B9	[7:2]	Unused	
	[1:0]	Reference period	Nominal reference period, Bits[49:48]

Table 110. Tolerance—Profile 3

Address	Bits	Bit Name	Description
06BA	[7:0]	Inner tolerance	Inner tolerance, Bits[7:0]
06BB	[7:0]		Inner tolerance, Bits[15:8]
06BC	[7:4]	Unused	
	[3:0]	Inner tolerance	Inner tolerance, Bits[19:16]
06BD	[7:0]	Outer tolerance	Outer tolerance, Bits[7:0]
06BE	[7:0]		Outer tolerance, Bits[15:8]
06BF	[7:4]	Unused	
	[3:0]	Outer tolerance	Outer tolerance, Bits[19:16]

Table 111. Validation Timer—Profile 3

Address	Bits	Bit Name	Description
06C0	[7:0]	Validation timer (in milliseconds)	Validation timer, Bits[7:0]
06C1	[7:0]		Validation timer, Bits[15:8]

Table 112. Redetect Timer—Profile 3

Address	Bits	Bit Name	Description
06C2	[7:0]	Redetect timer (in milliseconds)	Redetect timer, Bits[7:0]
06C3	[7:0]		Redetect timer, Bits[15:8]

Table 113. Digital Loop Filter Coefficients—Profile 3[1]

Address	Bits	Bit Name	Description
06C4	[7:0]	Alpha-0 linear	Alpha-0 coefficient linear, Bits[7:0]
06C5	[7:0]		Alpha-0 coefficient linear, Bits[15:8]
06C6	[7:6]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bits[1:0]
	[5:0]	Alpha-1 exponent	Alpha-1 coefficient exponent, Bits[5:0]
06C7	[7:1]	Beta-0 linear	Beta-0 coefficient linear, Bits[6:0]
	[0]	Alpha-2 exponent	Alpha-2 coefficient exponent, Bit 2
06C8	[7:0]	Beta-0 linear	Beta-0 coefficient linear, Bits[14:7]
06C9	[7]	Unused	
	[6:2]	Beta-1 exponent	Beta-1 coefficient exponent, Bits[4:0]
	[1:0]	Beta-0 linear	Beta-0 coefficient linear, Bits[16:15]

Address	Bits	Bit Name	Description
06CA	[7:0]	Gamma-0 linear	Gamma-0 coefficient linear, Bits[7:0]
06CB	[7:0]		Gamma-0 coefficient linear, Bits[15:8]
06CC	[7:6]	Unused	
	[5:1]	Gamma-1 exponent	Gamma-1 coefficient exponent, Bits[4:0]
	[0]	Gamma-0 linear	Gamma-0 coefficient linear, Bit 16
06CD	[7:0]	Delta-0 linear	Delta-0 coefficient linear, Bits[7:0]
06CE	[7]	Delta-1 exponent	Delta-1 coefficient exponent, Bit 0
	[6:0]	Delta-0 linear	Delta-0 coefficient linear, Bits[14:8]
06CF	[7:4]	Alpha-3 exponent	Alpha-3 coefficient exponent, Bits[3:0]
	[3:0]	Delta-1 exponent	Delta-1 coefficient exponent, Bits[4:1]

[1] The digital loop filter coefficients (α, β, γ, and δ) have the general form: $x(2^y)$, where x is the linear component and y is the exponential component of the coefficient. The value of the linear component (x) constitutes a fraction, where $0 \le x < 1$. The exponential component (y) is an integer. See the Calculating Digital Filter Coefficients section for details.

Table 114. R Divider—Profile 3[1]

Address	Bits	Bit Name	Description
06D0	[7:0]	R	R, Bits[7:0]
06D1	[7:0]		R, Bits[15:8]
06D2	[7:0]		R, Bits[23:16]
06D3	[7:6]	Unused	
	[5:0]	R	R, Bits[29:24]

[1] The value stored in the R-divider register yields an actual divide ratio of one more than the programmed value.

Table 115. S Divider—Profile 3[1]

Address	Bits	Bit Name	Description
06D4	[7:0]	S	S, Bits[7:0]
06D5	[7:0]		S, Bits[15:8]
06D6	[7:0]		S, Bits[23:16]
06D7	[7:6]	Unused	
	[5:0]	S	S, Bits[29:24]

[1] The value stored in the S-divider register yields an actual divide ratio of one more than the programmed value. Furthermore, the value of S must be at least 7.

Table 116. Fractional Feedback Divider—Profile 3

Address	Bits	Bit Name	Description
06D8	[7:0]	V	V, Bits[7:0]
06D9	[7:4]	U	U, Bits[3:0]
	[3:2]	Unused	
	[1:0]	V	V, Bits[9:8]
06DA	[7:6]	Unused	
	[5:0]	U	U, Bits[9:4]

Table 117. Lock Detectors—Profile 3

Address	Bits	Bit Name	Description
06DB	[7:0]	Phase lock threshold (in picoseconds)	Phase lock threshold, Bits[7:0]
06DC	[7:0]		Phase lock threshold, Bits[15:8]
06DD	[7:0]	Phase lock fill rate	Phase lock fill rate, Bits[7:0]
06DE	[7:0]	Phase lock drain rate	Phase lock drain rate, Bits[7:0]
06DF	[7:0]	Frequency lock threshold (in picoseconds)	Frequency lock threshold, Bits[7:0]
06E0	[7:0]		Frequency lock threshold, Bits[15:8]
06E1	[7:0]		Frequency lock threshold, Bits[23:16]
06E2	[7:0]	Frequency lock fill rate	Frequency lock fill rate, Bits[7:0]
06E3	[7:0]	Frequency lock drain rate	Frequency lock drain rate, Bits[7:0]
06E4 to 06FF	[7:0]	Unused	

Register 0700 to Register 07FF—Profile 4 to Profile 7

Profile 4 (Register 0700 to Register 0731) is identical to Profile 0 (Register 0600 to Register0631).

Profile 5 (Register 0732 to Register 077F) is identical to Profile 1 (Register 0632 to Register 067F).

Profile 6 (Register 0780 to Register 07B1) is identical to Profile 2 (Register 0680 to Register 06B1).

Profile 7 (Register 07B2 to Register 07FF) is identical to Profile 3 (Register 06B2 to Register 06FF).

OPERATIONAL CONTROLS (REGISTER 0A00 TO REGISTER 0A10)

Table 118. General Power-Down

Address	Bits	Bit Name	Description
0A00	[7]	Reset sans reg map	Reset internal hardware but retain programmed register values. 0 (default) = normal operation. 1 = reset.
	[6]	Unused	
	[5]	SYSCLK power-down	Place SYSCLK input and PLL in deep sleep mode. 0 (default) = normal operation. 1 = power-down.
	[4]	Reference power-down	Place reference clock inputs in deep sleep mode. 0 (default) = normal operation. 1 = power-down.
	[3]	TDC power-down	Place the time-to-digital converter in deep sleep mode. 0 (default) = normal operation. 1 = power-down.
	[2]	DAC power-down	Place the DAC in deep sleep mode. 0 (default) = normal operation. 1 = power-down.
	[1]	Dist power-down	Place the clock distribution outputs in deep sleep mode. 0 (default) = normal operation. 1 = power-down.
	[0]	Full power-down	Place the entire device in deep sleep mode. 0 (default) = normal operation. 1 = power-down.

Table 119. Loop Mode

Address	Bits	Bit Name	Description
0A01	[7]	Unused	
	[6]	User holdover	Force the device into holdover mode. 0 (default) = normal operation. 1 = force device into holdover mode. The device behaves as though all input references are faulted.
	[5]	User freerun	Force the device into free-run mode. 0 (default) = normal operation. 1 = force device into free-run mode. The free running frequency tuning word register specifies the DDS output frequency. Note that, when the user freerun bit is set, it overrides the user holdover bit.
	[4:3]	User selection mode	Select the operating mode of the reference switching state machine. 00 (default) = automatic mode. The fully automatic priority-based algorithm selects the active reference (Bits[2:0] are ignored). 01 = fallback mode. The active reference is the user reference (Bits[2:0]) as long as it is valid. Otherwise, use the fully automatic priority-based algorithm to select the active reference. 10 = holdover mode. The active reference is the user reference (Bits[2:0]) as long as it is valid. Otherwise, enter holdover mode. 11 = manual mode. The active reference is always the user reference (Bits[2:0]). When using manual mode, be sure that the reference declared as the user reference (Bits[2:0]) is programmed for manual reference-to-profile assignment in the appropriate manual reference profile selection register (Address 0503 to Address 0506).
	[2:0]	User reference selection	Input reference when user selection mode = 01, 10, or 11. 000 (default) = Input Reference A 001 = Input Reference AA 010 = Input Reference B 011 = Input Reference BB 100 = Input Reference C 101 = Input Reference CC 110 = Input Reference D 111 = Input Reference DD

Table 120. Cal/Sync

Address	Bits	Bit Name	Description
0A02	[7:2]	unused	
	[1]	Sync distribution	Setting this bit (default = 0) initiates synchronization of the clock distribution output. While this bit = 1, the clock distribution output stalls. Synchronization occurs on the 1 to 0 transition of this bit.
	[0]	Calibrate system clock	Setting this bit (default = 0) initiates an internal calibration of the SYSCLK PLL (assuming it is enabled). The calibration routine automatically selects the proper VCO frequency band and signal amplitude. The internal system clock stalls during the calibration procedure, disabling the device until the calibration is complete (a few milliseconds).

Register 0A03—ResetFunc

Table 121. Reset Functions[1]

Address	Bits	Bit Name	Description
0A03	[7]	Unused	
	[6]	Clear LF	Setting this bit (default = 0) clears the digital loop filter (intended as a debug tool).
	[5]	Clear CCI	Setting this bit (default = 0) clears the CCI filter (intended as a debug tool).
	[4]	Clear phase accumulator	Setting this bit (default = 0) clears DDS phase accumulator (not a recommended action).
	[3]	Reset auto sync	Setting this bit (default = 0) resets the automatic synchronization logic (see Register 0403).
	[2]	Reset TW history	Setting this bit (default = 0) resets the tuning word history logic (part of holdover functionality).
	[1]	Reset all IRQs	Setting this bit (default = 0) clears the entire IRQ monitor register (Register 0D02 to Register 0D09). It is the equivalent of setting all the bits of the IRQ clearing register (Register 0A04 to Register 0A0B).
	[0]	Reset watchdog	Setting this bit (default = 0) resets the watchdog timer (see Register 0211 to Register 0212). If the timer had timed out, it simply starts a new timing cycle. If the timer has not yet timed out, it restarts at time zero without causing a timeout event. Continuously resetting the watchdog timer at intervals less than its timeout period prevents the watchdog timer from generating a timeout event.

[1] All bits in this register are autoclearing.

Register 0A04 to Register 0A0B—IRQ Clearing

The IRQ clearing registers are identical in format to the IRQ monitor registers (Address 0D02 to Address 0D09). When set to Logic 1, an IRQ clearing bit resets the corresponding IRQ monitor bit, thereby canceling the interrupt request for the indicated event. The IRQ clearing register is an autoclearing register.

Table 122. IRQ Clearing for SYSCLK

Address	Bits	Bit Name	Description
0A04	[7:6]	Unused	
	[5]	SYSCLK unlocked	Clears SYSCLK unlocked IRQ
	[4]	SYSCLK locked	Clears SYSCLK locked IRQ
	[3:2]	Unused	
	[1]	SYSCLK Cal complete	Clears SYSCLK calibration complete IRQ
	[0]	SYSCLK Cal started	Clears SYSCLK calibration started IRQ

Table 123. IRQ Clearing for Distribution Sync, Watchdog Timer, and EEPROM

Address	Bits	Bit Name	Description
0A05	[7:4]	Unused	
	[3]	Distribution sync	Clears distribution sync IRQ
	[2]	Watchdog timer	Clears watchdog timer IRQ
	[1]	EEPROM fault	Clears EEPROM fault IRQ
	[0]	EEPROM complete	Clears EEPROM complete IRQ

Table 124. IRQ Clearing for the Digital PLL

Address	Bits	Bit Name	Description
0A06	[7]	Switching	Clears switching IRQ
	[6]	Closed	Clears closed IRQ
	[5]	Freerun	Clears freerun IRQ
	[4]	Holdover	Clears holdover IRQ
	[3]	Freq unlocked	Clears frequency unlocked IRQ
	[2]	Freq locked	Clears frequency locked IRQ
	[1]	Phase unlocked	Clears phase unlocked IRQ
	[0]	Phase locked	Clears phase locked IRQ

Table 125. IRQ Clearing for History Update, Frequency Limit, and Phase Slew Limit

Address	Bits	Bit Name	Description
0A07	[7:5]	Unused	
	[4]	History updated	Clears history updated IRQ
	[3]	Frequency unclamped	Clears frequency unclamped IRQ
	[2]	Frequency clamped	Clears frequency clamped IRQ
	[1]	Phase slew unlimited	Clears phase slew unlimited IRQ
	[0]	Phase slew limited	Clears phase slew limited IRQ

Table 126. IRQ Clearing for Reference Inputs

Address	Bits	Bit Name	Description
0A08	[7]	Ref AA new profile	Clears Ref AA new profile IRQ
	[6]	Ref AA validated	Clears Ref AA validated IRQ
	[5]	Ref AA fault cleared	Clears Ref AA fault cleared IRQ
	[4]	Ref AA fault	Clears Ref AA fault IRQ
	[3]	Ref A new profile	Clears Ref A new profile IRQ
	[2]	Ref A validated	Clears Ref A validated IRQ
	[1]	Ref A fault cleared	Clears Ref A fault cleared IRQ
	[0]	Ref A fault	Clears Ref A fault IRQ
0A09	[7]	Ref BB new profile	Clears Ref BB new profile IRQ
	[6]	Ref BB validated	Clears Ref BB validated IRQ
	[5]	Ref BB fault cleared	Clears Ref BB fault cleared IRQ
	[4]	Ref BB fault	Clears Ref BB fault IRQ
	[3]	Ref B new profile	Clears Ref B new profile IRQ
	[2]	Ref B validated	Clears Ref B validated IRQ
	[1]	Ref B fault cleared	Clears Ref B fault cleared IRQ
	[0]	Ref B fault	Clears Ref B fault IRQ
0A0A	[7]	Ref CC new profile	Clears Ref CC new profile IRQ
	[6]	Ref CC validated	Clears Ref CC validated IRQ
	[5]	Ref CC fault cleared	Clears Ref CC fault cleared IRQ
	[4]	Ref CC fault	Clears Ref CC fault IRQ
	[3]	Ref C new profile	Clears Ref C new profile IRQ
	[2]	Ref C validated	Clears Ref C validated IRQ
	[1]	Ref C fault cleared	Clears Ref C fault cleared IRQ
	[0]	Ref C fault	Clears Ref C fault IRQ
0A0B	[7]	Ref DD new profile	Clears Ref DD new profile IRQ
	[6]	Ref DD validated	Clears Ref DD validated IRQ
	[5]	Ref DD fault cleared	Clears Ref DD fault cleared IRQ
	[4]	Ref DD fault	Clears Ref DD fault IRQ
	[3]	Ref D new profile	Clears Ref D new profile IRQ
	[2]	Ref D validated	Clears Ref D validated IRQ
	[1]	Ref D fault cleared	Clears Ref D fault cleared IRQ
	[0]	Ref D fault	Clears Ref D fault IRQ

Table 127. Incremental Phase Offset Control

Address	Bits	Bit Name	Description
0A0C	[7:3]	Unused	
	[2]	Reset phase offset	Resets the incremental phase offset to 0. This is an autoclearing bit.
	[1]	Decr phase offset	Decrements the incremental phase offset by the amount specified in the incremental phase lock offset step size register (Register 0314 to Register 0315). This is an autoclearing bit.
	[0]	Incr phase offset	Increments the incremental phase offset by the amount specified in the incremental phase lock offset step size register (Register 0314 to Register 0315). This is an autoclearing bit.

Table 128. Reference Profile Selection State Machine Startup[1]

Address	Bits	Bit Name	Description
0A0D	[7]	Detect DD	Setting this bit starts the profile selection state machine for Input Reference DD.
	[6]	Detect D	Setting this bit starts the profile selection state machine for Input Reference D.
	[5]	Detect CC	Setting this bit starts the profile selection state machine for Input Reference CC.
	[4]	Detect C	Setting this bit starts the profile selection state machine for Input Reference C.
	[3]	Detect BB	Setting this bit starts the profile selection state machine for Input Reference BB.
	[2]	Detect B	Setting this bit starts the profile selection state machine for Input Reference B.
	[1]	Detect AA	Setting this bit starts the profile selection state machine for Input Reference AA.
	[0]	Detect A	Setting this bit starts the profile selection state machine for Input Reference A.

[1] All bits in this register are autoclearing.

Table 129. Reference Validation Override Controls[1]

Address	Bits	Bit Name	Description
0A0E	[7]	Force Timeout DD	Setting this bit emulates a timeout of the validation timer for Reference DD. This is an autoclearing bit.
	[6]	Force Timeout D	Setting this bit emulates a timeout of the validation timer for Reference D. This is an autoclearing bit.
	[5]	Force Timeout CC	Setting this bit emulates a timeout of the validation timer for Reference CC. This is an autoclearing bit.
	[4]	Force Timeout C	Setting this bit emulates a timeout of the validation timer for Reference C. This is an autoclearing bit.
	[3]	Force Timeout BB	Setting this bit emulates a timeout of the validation timer for Reference BB. This is an autoclearing bit.
	[2]	Force Timeout B	Setting this bit emulates a timeout of the validation timer for Reference B. This is an autoclearing bit.
	[1]	Force Timeout AA	Setting this bit emulates a timeout of the validation timer for Reference AA. This is an autoclearing bit.
	[0]	Force Timeout A	Setting this bit emulates a timeout of the validation timer for Reference A. This is an autoclearing bit.

Address	Bits	Bit Name	Description
0A0F	[7]	Ref Mon Override DD	Overrides the reference monitor REF fault signal for Reference DD (default = 0, not overridden).
	[6]	Ref Mon Override D	Overrides the reference monitor REF fault signal for Reference D (default = 0, not overridden).
	[5]	Ref Mon Override CC	Overrides the reference monitor REF fault signal for Reference CC (default = 0, not overridden).
	[4]	Ref Mon Override C	Overrides the reference monitor REF fault signal for Reference C (default = 0, not overridden).
	[3]	Ref Mon Override BB	Overrides the reference monitor REF fault signal for Reference BB (default = 0, not overridden).
	[2]	Ref Mon Override B	Overrides the reference monitor REF fault signal for Reference B (default = 0, not overridden).
	[1]	Ref Mon Override AA	Overrides the reference monitor REF fault signal for Reference AA (default = 0, not overridden).
	[0]	Ref Mon Override A	Overrides the reference monitor REF fault signal for Reference A (default = 0, not overridden).
0A10	[7]	Ref Mon Bypass DD	Bypasses the reference monitor for Reference DD (default = 0, not bypassed).
	[6]	Ref Mon Bypass D	Bypasses the reference monitor for Reference D (default = 0, not bypassed).
	[5]	Ref Mon Bypass CC	Bypasses the reference monitor for Reference CC (default = 0, not bypassed).
	[4]	Ref Mon Bypass C	Bypasses the reference monitor for Reference C (default = 0, not bypassed).
	[3]	Ref Mon Bypass BB	Bypasses the reference monitor for Reference BB (default = 0, not bypassed).
	[2]	Ref Mon Bypass B	Bypasses the reference monitor for Reference B (default = 0, not bypassed).
	[1]	Ref Mon Bypass AA	Bypasses the reference monitor for Reference AA (default = 0, not bypassed).
	[0]	Ref Mon Bypass A	Bypasses the reference monitor for Reference A (default = 0, not bypassed).

[1] See Figure 34 for details.

STATUS READBACK (REGISTER 0D00 TO REGISTER 0D19)

All bits in Register 0D00 to Register 0D19 are read only.

Table 130. EEPROM Status

Address	Bits	Bit Name	Description
0D00	[7:3]	Unused	
	[2]	Fault detected	An error occurred while saving data to or loading data from the EEPROM.
	[1]	Load in progress	The control logic sets this bit while data is being read from the EEPROM.
	[0]	Save in progress	The control logic sets this bit while data is being written to the EEPROM.

Table 131. SYSCLK Status

Address	Bits	Bit Name	Description
0D01	[7:5]	Unused	
	[4]	Stable	The control logic sets this bit when the device considers the system clock to be stable (see the System Clock Stability Timer section).
	[3:2]	Unused	
	[1]	Cal in progress	The control logic holds this bit set while the system clock calibration is in progress.
	[0]	Lock detected	Indicates the status of the system clock PLL. 0 = unlocked. 1 = locked (or the PLL is disabled).

Register 0D02 to Register 0D09—IRQ Monitor

If not masked via the IRQ mask register (Address 0209 to Address 0210), then the appropriate IRQ monitor bit is set to a Logic 1 when the indicated event occurs. These bits can only be cleared via the IRQ clearing register (Address 0A04 to Address 0A0B), the reset all IRQs bit (Register 0A03, Bit 1), or a device reset.

Table 132. IRQ Monitor for SYSCLK

Address	Bits	Bit Name	Description
0D02	[7:6]	Unused	
	[5]	SYSCLK unlocked	Indicates a SYSCLK PLL state transition from locked to unlocked
	[4]	SYSCLK locked	Indicates a SYSCLK PLL state transition from unlocked to locked
	[3:2]	Unused	
	[1]	SYSCLK Cal complete	Indicates that SYSCLK calibration has completed
	[0]	SYSCLK Cal started	Indicates that SYSCLK calibration has begun

Table 133. IRQ Monitor for Distribution Sync, Watchdog Timer, and EEPROM

Address	Bits	Bit Name	Description
0D03	[7:4]	Unused	
	[3]	Distribution sync	Indicates a distribution sync event
	[2]	Watchdog timer	Indicates expiration of the watchdog timer
	[1]	EEPROM fault	Indicates a fault during an EEPROM load or save operation
	[0]	EEPROM complete	Indicates successful completion of an EEPROM load or save operation

Table 134. IRQ Monitor for the Digital PLL

Address	Bits	Bit Name	Description
0D04	[7]	Switching	Indicates that the DPLL is switching to a new reference
	[6]	Closed	Indicates that the DPLL has entered closed-loop operation
	[5]	Freerun	Indicates that the DPLL has entered free-run mode
	[4]	Holdover	Indicates that the DPLL has entered holdover mode
	[3]	Freq unlocked	Indicates that the DPLL lost frequency lock
	[2]	Freq locked	Indicates that the DPLL has acquired frequency lock
	[1]	Phase unlocked	Indicates that the DPLL lost phase lock
	[0]	Phase locked	Indicates that the DPLL has acquired phase lock

Table 135. IRQ Monitor for History Update, Frequency Limit, and Phase Slew Limit

Address	Bits	Bit Name	Description
0D05	[7:5]	Unused	
	[4]	History updated	Indicates the occurrence of a tuning word history update
	[3]	Freq unclamped	Indicates a frequency limiter state transition from clamped to unclamped
	[2]	Freq clamped	Indicates a frequency limiter state transition from unclamped to clamped
	[1]	Phase slew unlimited	Indicates a phase slew limiter state transition from slew limiting to not slew limiting
	[0]	Phase slew limited	Indicates a phase slew limiter state transition from not slew limiting to slew limiting

Table 136. IRQ Monitor for Reference Inputs

Address	Bits	Bit Name	Description
0D06	[7]	Ref AA new profile	Indicates that Ref AA has switched to a new profile
	[6]	Ref AA validated	Indicates that Ref AA has been validated
	[5]	Ref AA fault cleared	Indicates that Ref AA has been cleared of a previous fault
	[4]	Ref AA fault	Indicates that Ref AA has been faulted
	[3]	Ref A new profile	Indicates that Ref A has switched to a new profile
	[2]	Ref A validated	Indicates that Ref A has been validated
	[1]	Ref A fault cleared	Indicates that Ref A has been cleared of a previous fault
	[0]	Ref A fault	Indicates that Ref A has been faulted

Address	Bits	Bit Name	Description
0D07	[7]	Ref BB new profile	Indicates that Ref BB has switched to a new profile
	[6]	Ref BB validated	Indicates that Ref BB has been validated
	[5]	Ref BB fault cleared	Indicates that Ref BB has been cleared of a previous fault
	[4]	Ref BB fault	Indicates that Ref BB has been faulted
	[3]	Ref B new profile	Indicates that Ref B has switched to a new profile
	[2]	Ref B validated	Indicates that Ref B has been validated
	[1]	Ref B fault cleared	Indicates that Ref B has been cleared of a previous fault
	[0]	Ref B fault	Indicates that Ref B has been faulted
0D08	[7]	Ref CC new profile	Indicates that Ref CC has switched to a new profile
	[6]	Ref CC validated	Indicates that Ref CC has been validated
	[5]	Ref CC fault cleared	Indicates that Ref CC has been cleared of a previous fault
	[4]	Ref CC fault	Indicates that Ref CC has been faulted
	[3]	Ref C new profile	Indicates that Ref C has switched to a new profile
	[2]	Ref C validated	Indicates that Ref C has been validated
	[1]	Ref C fault cleared	Indicates that Ref C has been cleared of a previous fault
	[0]	Ref C fault	Indicates that Ref C has been faulted
0D09	[7]	Ref DD new profile	Indicates that Ref DD has switched to a new profile
	[6]	Ref DD validated	Indicates that Ref DD has been validated
	[5]	Ref DD fault cleared	Indicates that Ref DD has been cleared of a previous fault
	[4]	Ref DD fault	Indicates that Ref DD has been faulted
	[3]	Ref D new profile	Indicates that Ref D has switched to a new profile
	[2]	Ref D validated	Indicates that Ref D has been validated
	[1]	Ref D fault cleared	Indicates that Ref D has been cleared of a previous fault
	[0]	Ref D fault	Indicates that Ref D has been faulted

Table 137. DPLL Status

Address	Bits	Bit Name	Description
0D0A	[7]	Offset slew limiting	The current closed-loop phase offset is rate limited.
	[6]	Phase build-out	A phase build-out transition was made to the currently active reference.
	[5]	Freq lock	The DPLL has achieved frequency lock.
	[4]	Phase lock	The DPLL has achieved phase lock.
	[3]	Loop switching	The DPLL is in the process of a reference switchover.
	[2]	Holdover	The DPLL is in holdover mode.
	[1]	Active	The DPLL is active (that is, operating in a closed-loop condition)
	[0]	Free running	The DPLL is free running (that is, operating in an open-loop condition)
0D0B	[7]	Frequency clamped	The upper or lower frequency tuning word clamp is in effect.
	[6]	History available	There is sufficient tuning word history available for holdover operation.
	[5:3]	Active reference priority	Priority value of the currently active reference. 000 = highest priority. 111 = lowest priority.
	[2:0]	Active reference	Index of the currently active reference. 000 = Reference A. 001 = Reference AA. 010 = Reference B. 011 = Reference BB. 100 = Reference C. 101 = Reference CC. 110 = Reference D. 111 = Reference DD.

Table 138. Input Reference Status

Address	Bits	Bit Name	Description
0D0C	[7]	Profile selected	The control logic sets this bit when it assigns Ref A to one of the eight profiles.
	[6:4]	Selected profile	The index (0 to 7) of the profile assigned to Ref A. Note that these bits are meaningless unless Bit 7 = 1.
	[3]	Valid	Ref A is valid for use (it is unfaulted and its validation timer has expired).
	[2]	Fault	Ref A is not valid for use.
	[1]	Fast	If Bit 7 = 1, then this bit indicates that the frequency of Ref A is higher than allowed by its profile settings. If Bit 7 = 0, then this bit indicates that the frequency of Ref A is above the maximum input reference frequency supported by the device.
	[0]	Slow	If Bit 7 = 1, then this bit indicates that the frequency of Ref A is lower than allowed by its profile settings. If Bit 7 = 0, then this bit indicates that the frequency of Ref A is below the minimum input reference frequency supported by the device.
0D0D	[7:0]		Same as 0D0C but for REF AA instead of REF A.
0D0E	[7:0]		Same as 0D0C but for REF B instead of REF A.
0D0F	[7:0]		Same as 0D0C but for REF BB instead of REF A.
0D10	[7:0]		Same as 0D0C but for REF C instead of REF A.
0D11	[7:0]		Same as 0D0C but for REF CC instead of REF A.
0D12	[7:0]		Same as 0D0C but for REF D instead of REF A.
0D13	[7:0]		Same as 0D0C but for REF DD instead of REF A.

Table 139. Holdover History[1]

Address	Bits	Bit Name	Description
0D14	[7:0]	Holdover history	Tuning word readback, Bits[7:0]
0D15	[7:0]		Tuning word readback, Bits[15:8]
0D16	[7:0]		Tuning word readack, Bits[23:9]
0D17	[7:0]		Tuning word readback, Bits[31:24]
0D18	[7:0]		Tuning word readback, Bits[39:32]
0D19	[7:0]		Tuning word readback, Bits[47:40]

[1] These registers contain the current 48-bit DDS frequency tuning word generated by the tuning word history logic.

NONVOLATILE MEMORY (EEPROM) CONTROL (REGISTER 0E00 TO REGISTER 0E03)

Table 140. EEPROM Control

Address	Bits	Bit Name	Description
0E00	[7:2]	Unused	
	[1]	Half rate mode	EEPROM serial communication rate. 0 (default) = 400 kHz (normal). 1 = 200 kHz.
	[0]	Write enable	EEPROM write enable/protect. 0 (default) = EEPROM write protected. 1 = EEPROM write enabled.
0E01	[7:5]	Unused	
	[4:0]	Condition value	When set to a nonzero value (default = 0), these bits establish the condition for EEPROM downloads.
0E02	[7:1]	Unused	
	0	Save to EEPROM	Upload data to the EEPROM based on the EEPROM storage sequence. This is an autoclearing bit.
0E03	[7:2]	Unused	
	[1]	Load from EEPROM	Download data from the EEPROM. This is an autoclearing bit.
	[0]	Unused	

EEPROM STORAGE SEQUENCE (REGISTER 0E10 TO REGISTER 0E3F)

The default settings of Register 0E10 to Register 0E33 embody a sample scratch pad instruction sequence. The following is a description of the register defaults under the assumption that the controller has been instructed to carry out an EEPROM storage sequence.

Table 141. EEPROM Storage Sequence for System Clock Settings

Address	Bits	Bit Name	Description
0E10	[7:0]	System clock	The default value of this register is 0x08, which the controller interprets as a data instruction. Its decimal value is 8, which tells the controller to transfer nine bytes of data (8 + 1) beginning at the address specified by the next two bytes. The controller stores 0x08 in the EEPROM and increments the EEPROM address pointer.
0E11	[7:0]	System clock	The default value of these two registers is 0x0100. Note that Register 0E11 and Register 0E12 are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0100). The controller stores 0x0100 in the EEPROM and increments the EEPROM pointer by 2. It then transfers nine bytes from the register map (beginning at Address 0x0100) to the EEPROM and increments the EEPROM address pointer by 10 (nine data bytes and one checksum byte). The nine bytes transferred correspond to the system clock parameters in the register map.
0E12	[7:0]		
0E13	[7:0]	I/O update	The default value of this register is 0x80, which the controller interprets as an I/O update instruction. The controller stores 0x80 in the EEPROM and increments the EEPROM address pointer.

Table 142. EEPROM Storage Sequence for System Clock Calibration

Address	Bits	Bit Name	Description
0E14	[7:0]	SYSCLK calibrate	The default value of this register is 0xA0, which the controller interprets as a calibrate instruction. The controller stores 0xA0 in the EEPROM and increments the EEPROM address pointer.

Table 143. EEPROM Storage Sequence for General Configuration Settings

Address	Bits	Bit Name	Description
0E15	[7:0]	General	The default value of this register is 0x14, which the controller interprets as a data instruction. Its decimal value is 20, which tells the controller to transfer 21 bytes of data (20 + 1) beginning at the address specified by the next two bytes. The controller stores 0x14 in the EEPROM and increments the EEPROM address pointer.
0E16	[7:0]	General	The default value of these two registers is 0x0200. Note that Register 0E16 and Register 0E17 are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0200). The controller stores 0x0200 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 21 bytes from the register map (beginning at Address 0x0200) to the EEPROM and increments the EEPROM address pointer by 22 (21 data bytes and one checksum byte). The 21 bytes transferred correspond to the general configuration parameters in the register map.
0E17	[7:0]		

Table 144. EEPROM Storage Sequence for DPLL Settings

Address	Bits	Bit Name	Description
0E18	[7:0]	DPLL	The default value of this register is 0x1B, which the controller interprets as a data instruction. Its decimal value is 27, which tells the controller to transfer 28 bytes of data (27 + 1) beginning at the address specified by the next two bytes. The controller stores 0x1B in the EEPROM and increments the EEPROM address pointer.
0E19	[7:0]	DPLL	The default value of these two registers is 0x0300. Note that Register 0E19 and Register 0E1A are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0300). The controller stores 0x0300 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 28 bytes from the register map (beginning at Address 0x0300) to the EEPROM and increments the EEPROM address pointer by 29 (28 data bytes and one checksum byte). The 28 bytes transferred correspond to the DPLL parameters in the register map.
0E1A	[7:0]		

Table 145. EEPROM Storage Sequence for Clock Distribution Settings

Address	Bits	Bit Name	Description
0E1B	[7:0]	Clock distribution	The default value of this register is 0x19, which the controller interprets as a data instruction. Its decimal value is 25, which tells the controller to transfer 26 bytes of data (25 + 1) beginning at the address specified by the next two bytes. The controller stores 0x19 in the EEPROM and increments the EEPROM address pointer.
0E1C	[7:0]	Clock distribution	The default value of these two registers is 0x0400. Note that Register 0E1C and Register 0E1D are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0400). The controller stores 0x0400 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 26 bytes from the register map (beginning at Address 0x0400) to the EEPROM and increments the EEPROM address pointer by 27 (26 data bytes and one checksum byte). The 26 bytes transferred correspond to the clock distribution parameters in the register map.
0E1D	[7:0]		
0E1E	[7:0]	I/O update	The default value of this register is 0x80, which the controller interprets as an I/O update instruction. The controller stores 0x80 in the EEPROM and increments the EEPROM address pointer.

Table 146. EEPROM Storage Sequence for Reference Input Settings

Address	Bits	Bit Name	Description
0E1F	[7:0]	Reference inputs	The default value of this register is 0x07, which the controller interprets as a data instruction. Its decimal value is 7, which tells the controller to transfer eight bytes of data (7 + 1) beginning at the address specified by the next two bytes. The controller stores 0x07 in the EEPROM and increments the EEPROM address pointer.
0E20	[7:0]	Reference inputs	The default value of these two registers is 0x0500. Note that Register 0E20 and Register 0E21 are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0500). The controller stores 0x0500 in the EEPROM and increments the EEPROM pointer by 2. It then transfers eight bytes from the register map (beginning at Address 0x0500) to the EEPROM and increments the EEPROM address pointer by nine (eight data bytes and one checksum byte). The eight bytes transferred correspond to the reference inputs parameters in the register map.
0E21	[7:0]		

Table 147. EEPROM Storage Sequence for Profile 0 and Profile 1 Settings

Address	Bits	Bit Name	Description
0E22	[7:0]	Profile 0 and Profile 1	The default value of this register is 0x63, which the controller interprets as a data instruction. Its decimal value is 99, which this tells the controller to transfer 100 bytes of data (99 + 1) beginning at the address specified by the next two bytes. The controller stores 0x63 in the EEPROM and increments the EEPROM address pointer.
0E23	[7:0]	Profile 0 and Profile 1	The default value of these two registers is 0x0600. Note that Register 0E23 and Register 0E24 are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0600). The controller stores 0x0600 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 100 bytes from the register map (beginning at Address 0x0600) to the EEPROM and increments the EEPROM address pointer by 101 (100 data bytes and one checksum byte). The 99 bytes transferred correspond to the Profile 0 and Profile 1 parameters in the register map.
0E24	[7:0]		

Table 148. EEPROM Storage Sequence for Profile 2 and Profile 3 Settings

Address	Bits	Bit Name	Description
0E25	[7:0]	Profile 2 and Profile 3	The default value of this register is 0x63, which the controller interprets as a data instruction. Its decimal value is 99, which tells the controller to transfer 100 bytes of data (99 + 1) beginning at the address specified by the next two bytes. The controller stores 0x63 in the EEPROM and increments the EEPROM address pointer.
0E26	[7:0]	Profile 2 and Profile 3	The default value of these two registers is 0x0680. Note that Register 0E26 and Register 0E27 are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0680). The controller stores 0x0680 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 100 bytes from the register map (beginning at Address 0x0680) to the EEPROM and increments the EEPROM address pointer by 101 (100 data bytes and one checksum byte). The 99 bytes transferred correspond to the Profile 2 and Profile 3 parameters in the register map.
0E27	[7:0]		

Table 149. EEPROM Storage Sequence for Profile 4 and Profile 5 Settings

Address	Bits	Bit Name	Description
0E28	[7:0]	Profile 4 and Profile 5	The default value of this register is 0x63, which the controller interprets as a data instruction. Its decimal value is 99, which this tells the controller to transfer 100 bytes of data (99 + 1) beginning at the address specified by the next two bytes. The controller stores 0x63 in the EEPROM and increments the EEPROM address pointer.
0E29	[7:0]	Profile 4 and Profile 5	The default value of these two registers is 0x0700. Note that Register 0E29 and Register 0E2A are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0700). The controller stores 0x0700 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 100 bytes from the register map (beginning at Address 0x0700) to the EEPROM and increments the EEPROM address pointer by 101 (100 data bytes and one checksum byte). The 99 bytes transferred correspond to the Profile 4 and Profile 5 parameters in the register map.
0E2A	[7:0]		

Table 150. EEPROM Storage Sequence for Profile 6 and Profile 7 Settings

Address	Bits	Bit Name	Description
0E2B	[7:0]	Profile 6 and Profile 7	The default value of this register is 0x63, which the controller interprets as a data instruction. Its decimal value is 99, which this tells the controller to transfer 100 bytes of data (99 + 1) beginning at the address specified by the next two bytes. The controller stores 0x63 in the EEPROM and increments the EEPROM address pointer.
0E2C	[7:0]	Profile 6 and Profile 7	The default value of these two registers is 0x0780. Note that Register 0E2C and Register 0E2C are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0780). The controller stores 0x0780 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 100 bytes from the register map (beginning at Address 0x0780) to the EEPROM and increments the EEPROM address pointer by 101 (100 data bytes and one checksum byte). The 99 bytes transferred correspond to the Profile 6 and Profile 7 parameters in the register map.
0E2D	[7:0]		
0E2E	[7:0]	I/O update	The default value of this register is 0x80, which the controller interprets as an I/O update instruction. The controller stores 0x80 in the EEPROM and increments the EEPROM address pointer.

Table 151. EEPROM Storage Sequence for Operational Control Settings

Address	Bits	Bit Name	Description
0E2F	[7:0]	Operational controls	The default value of this register is 0x10, which the controller interprets as a data instruction. Its decimal value is 16, which this tells the controller to transfer 17 bytes of data (16 + 1) beginning at the address specified by the next two bytes. The controller stores 0x10 in the EEPROM and increments the EEPROM address pointer.
0E30	[7:0]	Operational controls	The default value of these two registers is 0x0A00. Note that Register 0E30 and Register 0E31 are the most significant and least significant bytes of the target address, respectively. Because the previous register contains a data instruction, these two registers define a starting address (in this case, 0x0A00). The controller stores 0x0A00 in the EEPROM and increments the EEPROM pointer by 2. It then transfers 17 bytes from the register map (beginning at Address 0x0A00) to the EEPROM and increments the EEPROM address pointer by 18 (17 data bytes and one checksum byte). The 17 bytes transferred correspond to the operational controls parameters in the register map.
0E31	[7:0]		
0E32	[7:0]	I/O update	The default value of this register is 0x80, which the controller interprets as an I/O update instruction. The controller stores 0x80 in the EEPROM and increments the EEPROM address pointer.

Table 152. EEPROM Storage Sequence for End of Data

Address	Bits	Bit Name	Description
0E33	[7:0]	End of data	The default value of this register is 0xFF, which the controller interprets as an end instruction. The controller stores this instruction in the EEPROM, resets the EEPROM address pointer, and enters an idle state. Note that, if this were a pause rather than an end instruction, the controller actions would be the same except that the controller would not reset the EEPROM address pointer.

POWER SUPPLY PARTITIONS

The AD9548 features multiple power supplies, and their power consumption varies with the AD9548 configuration. This section provides information about which power supplies can be grouped together and how the power consumption of each block varies with frequency.

The numbers quoted here are for comparison only. Please refer to the Specifications section for exact numbers. With each group, bypass capacitors of 1 µF in parallel with 10 µF should be used.

Upon applying power to the device, internal circuitry monitors the 1.8 V digital core supply and the 3.3 V digital I/O supply. When these supplies cross the desired threshold level, the device generates an internal 10 µs reset pulse. This pulse does not appear on the RESET pin.

3.3 V SUPPLIES

The 3.3 V supply domain consists of two main partitions, digital (DVDD3) and analog (AVDD3). Take care to keep these two supply domains separate.

Furthermore, the AVDD3 consists of two subdomains: the clock distribution output domain (Pin 31, Pin 37, Pin 38, and Pin 44) and the rest of the AVDD3 supply connections. Generally, these supply domains can be joined together. However, if an application requires 1.8 V CMOS driver operation in the clock distribution output block, then provide one 1.8 V supply domain to power the clock distribution output block. Each output driver has a dedicated supply pin, as shown in Table 153.

Table 153. Output Driver Supply Pins

Output Driver	Supply Pin
OUT0	31
OUT1	37
OUT2	38
OUT3	44

1.8 V SUPPLIES

The 1.8 V supply domain consists of two main partitions, digital (DVDD) and analog (AVDD). These two supply domains must be kept separate.

THERMAL PERFORMANCE

Table 154. Thermal Parameters for the AD9548 88-Lead LFCSP Package

Symbol	Thermal Characteristic Using a JEDEC51-7 Plus JEDEC51-5 2S2P Test Board[1]	Value[2]	Unit
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/s airflow per JEDEC JESD51-2 (still air)	18	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/s airflow per JEDEC JESD51-6 (moving air)	16	°C/W
θ_{JMA}	Junction-to-ambient thermal resistance, 2.5 m/s airflow per JEDEC JESD51-6 (moving air)	14	°C/W
θ_{JB}	Junction-to-board thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-8 (moving air)	9	°C/W
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-Std 883, Method 1012.1	1.0	°C/W
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.1	°C/W

[1] The exposed pad on the bottom of the package must be soldered to ground to achieve the specified thermal performance.
[2] Results are from simulations. The PCB is a JEDEC multilayer type. Thermal performance for actual applications requires careful inspection of the conditions in the application to determine if they are similar to those assumed in these calculations.

The AD9548 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used. Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the customer at the top center of the package.
Ψ_{JT} is the value as indicated in Table 154.
PD is the power dissipation (see the Power Dissipation section).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations.

CALCULATING DIGITAL FILTER COEFFICIENTS

The digital loop filter coefficients (α, β, γ, and δ (see Figure 40)) relate to the time constants (T_1, T_2, and T_3) associated with the equivalent analog circuit for a third order loop filter (Figure 66).

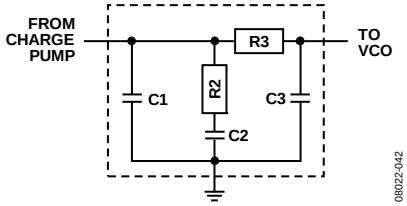


Figure 66. Third Order Analog Loop Filter

The design process begins by deciding on two design parameters related to the second order loop filter shown in Figure 67: the desired open-loop bandwidth (f_P) and phase margin (θ).

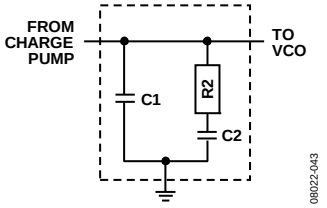


Figure 67. Second Order Analog Loop Filter

An analysis of the second order loop filter leads to its primary time constant, T_1. It can be shown that T_1 is expressible in terms of f_P and θ as

$$T_1 = \frac{1-\sin(\theta)}{\omega_P \cos(\theta)}$$

where $\omega_P = 2\pi f_P$.

An analysis of the third order loop filter leads to the definition of another time constant, T_3. It can be shown that T_3 is expressible in terms of the desired amount of additional attenuation introduced by R_3 and C_3 at some specified frequency offset (f_{OFFSET}) from the PLL output frequency.

$$T_3 = \frac{\sqrt{10^{\frac{ATTEN}{10}} - 1}}{\omega_{OFFSET}}$$

where $\omega_{OFFSET} = 2\pi f_{OFFSET}$.

Note that ATTEN is the desired excess attenuation in decibels.

Furthermore, ATTEN and ω_{OFFSET} should be chosen so that

$$T_3 \le \frac{1}{5 f_P}$$

With an expression for T_1 and T_3, it is possible to define an adjusted open-loop bandwidth (f_C) that is slightly less than f_P. It can be shown that ω_C (f_C expressed as a radian frequency) is expressible in terms of T_1, T_3, and θ (phase margin) as

$$\omega_C = \frac{(T_1 + T_3)\tan(\theta)}{T_1 T_3 + (T_1 + T_3)^2}\left[\sqrt{1 + \frac{T_1 T_3 + (T_1 + T_3)^2}{[(T_1 + T_3)\tan(\theta)]^2}} - 1\right]$$

It can also be shown that the adjusted open-loop bandwidth leads to T_2 (the secondary time constant of the second order loop filter) expressed as

$$T_2 = \frac{1}{\omega_C{}^2 (T_1 + T_3)}$$

Calculation of the digital loop filter coefficients requires a scaling constant, K (related to the system clock frequency, f_S), and the PLL feedback divide ratio, D.

$$K = \frac{30{,}517{,}578{,}125}{2^{33}} f_S$$

$$D = S + \frac{U}{V} + 1$$

where S, U, and V are the integer and fractional feedback divider values that reside in the profile registers. Keep in mind that the desired integer feedback divide ratio is one more than the stored value of S (hence, the +1 term in the equation for D in this equation). This leads to the digital filter coefficients given by

$$\alpha = \frac{\omega_C{}^2 T_2 D}{T_1 K}\sqrt{\frac{\left(1 + (\omega_C T_1)^2\right)\left(1 + (\omega_C T_3)^2\right)}{1 + (\omega_C T_2)^2}}$$

$$\beta = \frac{-32}{f_S}\left(\frac{1}{T_1} + \frac{1}{T_2}\right)$$

$$\gamma = \frac{-32}{f_S T_1}$$

$$\delta = \frac{32}{f_S T_3}$$

Calculation of the coefficient register values requires the application of some special functions described as follows:

The if() function

y = if(*test_statement*, *true_value*, *false_value*)

where *test_statement* is a conditional expression (for example, x < 3), *true_value* is what y equals if the conditional expression is true, and *false_value* is what y equals if the conditional expression is false.

The round() function

y = round(*x*)

If x is an integer, then y = x. Otherwise, y is the nearest integer to x. For example, round(2.1) = 2, round(2.5) = 3, and round(−3.1) = −3.

The ceil() function

$y = \text{ceil}(x)$

If x is an integer, then y = x. Otherwise, y is the next integer to the right on the number line. For example, ceil(2.8) = 3, whereas ceil(−2.8) = −2.

The min() function

$y = \min(x_0, x_1, \ldots x_n)$

where x_0 through x_n is a list of real numbers, and the value of y is the number in the list that is the farthest to the left on the number line.

The max() function

$y = \max(x_0, x_1, \ldots x_n)$

where x_0 through x_n is a list of real numbers, and the value of y is the number in the list that is the farthest to the right on the number line.

The $\log_2()$ function

$$\log_2(x) = \frac{\ln(x)}{\ln(2)}$$

where ln() is the natural log function and x is a positive, nonzero number.

Assume that the coefficient calculations for α, β, γ, and δ yield the following results:

$\alpha = 0.012735446$

$\beta = -6.98672 \times 10^{-5}$

$\gamma = -7.50373 \times 10^{-5}$

$\delta = 0.002015399$

These values are floating point numbers that must be quantized according to the bit widths of the linear and exponential components of the coefficients as they appear in the register map. Note that the calculations that follow indicate a positive value for the register entries of β and γ. The reason is that β and γ, which are supposed to be negative values, are stored in the AD9548 registers as positive values. The AD9548 converts the stored values to negative numbers within its signal processing core. A detailed description of the register value computations for α, β, γ, and δ is contained in the Calculation of the α Register Values section to the Calculation of the δ Register Values section.

CALCULATION OF THE α REGISTER VALUES

The quantized α coefficient consists of four components, α_0, α_1, α_2, and α_3 according to

$$\alpha \approx \alpha_{quantized} = \alpha_0 \times 2^{16-\alpha_1+\alpha_2+\alpha_3}$$

where α_0, α_1, α_2, and α_3 are the register values. α_2 provides front-end gain and α_3 provides back-end gain, and α_1 shifts the binary decimal point of α_0 to the left to accommodate small values of α. Calculation of α_1 is a two-step process, as follows:

$$w = \text{if}(\alpha < 1, -\text{ceil}(\log_2(\alpha)), 0)$$

$$\alpha_1 = \text{if}(\alpha < 1, \min[63, \max(0, w)], 0)$$

If gain is necessary (that is, α > 1), then it is beneficial to apply most or all of it to the front-end gain (α_2) implying that the calculation of α_2 is to be done before α_3. Calculation of α_2 is a three-step process that leads directly to the calculation of α_3.

$$x = \text{if}(\alpha > 1, \text{ceil}(\log_2(\alpha)), 0)$$

$$y = \text{if}(\alpha > 1, \min[22, \max(0, x)], 0)$$

$$\alpha_2 = \text{if}(y \geq 8, 7, y)$$

$$\alpha_3 = \text{if}(y \geq 8, y - 7, 0)$$

Calculation of α_0 is a two-step process, as follows:

$$z = \text{round}(\alpha \times 2^{16+\alpha_1-\alpha_2-\alpha_3})$$

$$\alpha_0 = \min[65{,}535, \max(1, z)]$$

Using the example value of α = 0.012735446 yields

$w = 6$, so $\alpha_1 = 6$

$x = 0$ and $y = 0$, so $\alpha_2 = 0$ and $\alpha_3 = 0$

$z = 53{,}416.332099584$, so $\alpha_0 = 53{,}416$

This leads to the following quantized value, which is very close to the desired value of 0.012735446:

$$\alpha_{quantized} = 53416 \times 2^{-22} \approx 0.01273566821$$

CALCULATION OF THE β REGISTER VALUES

The quantized β coefficient consists of two components, β_0 and β_1 according to

$$-\beta \approx \beta_{quantized} = \beta_0 \times 2^{-(17+\beta_1)}$$

where β_0 and β_1 are the register values. Calculation of β_1 is a two-step process that leads to the calculation of β_0, which is also a two-step process.

$$x = -\text{ceil}(\log_2(|\beta|))$$

$$\beta_1 = \min[31, \max(0, x)]$$

$$y = \text{round}(|\beta| \times 2^{17+\beta_1})$$

$$\beta_0 = \min[131{,}071, \max(1, y)]$$

Using the example value of $-\beta = 6.98672 \times 10^{-5}$ yields

$x = 13$, so $\beta_1 = 13$

$y = 75{,}019.3347657728$, so $\beta_0 = 75{,}019$

This leads to the following quantized value, which is very close to the desired value of 6.98672×10^{-5}:

$$\beta_{quantized} = 75{,}019 \times 2^{-30} \approx 6.986688823 \times 10^{-5}$$

CALCULATION OF THE γ REGISTER VALUES

The quantized γ coefficient consists of two components, γ_0 and γ_1 according to

$$-\gamma \approx \gamma_{quantized} = \gamma_0 \times 2^{-(17+\gamma_1)}$$

where γ_0 and γ_1 are the register values. Calculation of γ_1 is a two-step process that leads to the calculation of γ_0, which is also a two-step process.

$$x = -\text{ceil}(\log_2(|\gamma|))$$

$$\gamma_1 = \min[31, \max(0, x)]$$

$$y = \text{round}(|\gamma| \times 2^{17+\gamma_1})$$

$$\gamma_0 = \min[131{,}071, \max(1, y)]$$

Using the example value of $-\gamma = 7.50373 \times 10^{-5}$ yields

$x = 13$, so $\gamma_1 = 13$

$y = 80{,}570.6873700352$, so $\gamma_1 = 80{,}571$

This leads to the following quantized value, which is very close to the desired value of 7.50373×10^{-5}:

$$\gamma_{quantized} = 80571 \times 2^{-30} \approx 7.503759116 \times 10^{-5}$$

CALCULATION OF THE δ REGISTER VALUES

The quantized δ coefficient consists of two components, δ_0 and δ_1, according to

$$\delta \approx \delta_{quantized} = \delta_0 \times 2^{-(15+\delta_1)}$$

where δ_0 and δ_1 are the register values.

Calculation of δ_1 is a two-step process that leads to the calculation of δ_0, which is also a two-step process.

$$x = -\text{ceil}(\log_2(\delta))$$

$$\delta_1 = \min[31, \max(0, x)]$$

$$y = \text{round}(\delta \times 2^{15+\delta_1})$$

$$\delta_0 = \min[32{,}767, \max(1, y)]$$

Given the example value of $\delta = 0.002015399$, the preceding formulas yield

$x = 8$, $\delta_1 = 8$

$y = 16{,}906.392174592$, $\delta_0 = 16{,}906$

This leads to the following quantized value, which is very close to the desired value of 0.002015399:

$$\delta_{quantized} = 16906 \times 2^{-23} \approx 0.002015352249$$

OUTLINE DIMENSIONS

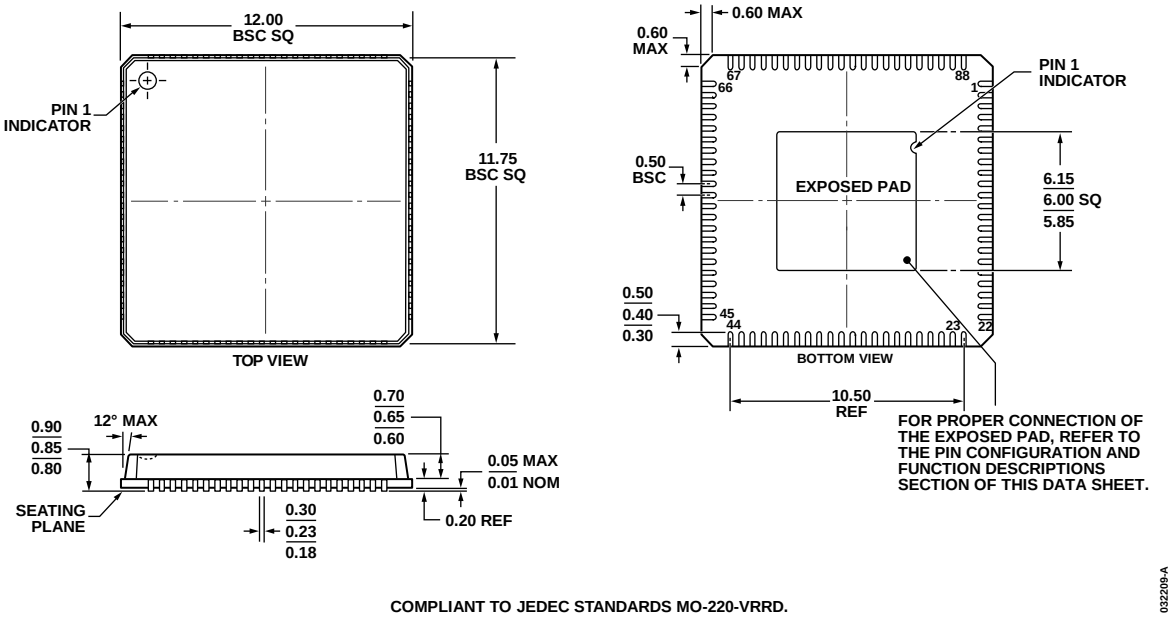


Figure 68. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
12 mm × 12 mm Body, Very Thin Quad
(CP-88-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9548BCPZ[1]	−40°C to +85°C	88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-88-2
AD9548BCPZ-REEL7[1]	−40°C to +85°C	88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-88-2
AD9548/PCBZ[1]	−40°C to +85°C	Evaluation Board	CP-88-2

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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