RISCore32300™ Family System Controller Chip

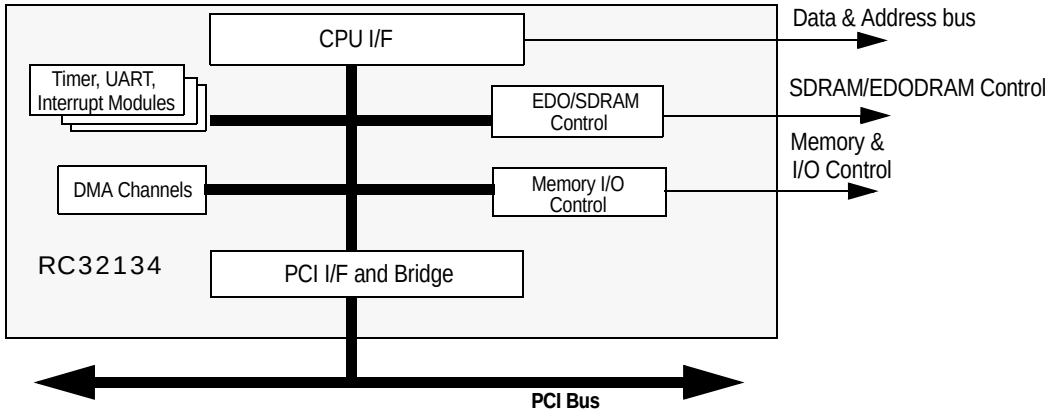
IDT79RC32134

RISController

Features

- **RC32300-family System Controller**
  - *Direct connection between RC32364 and RC32134*
  - *Up to 75 MHz operation*
  - *Drives latched address bus to memory and peripherals*
  - *Direct control of optional external data buffers*
  - *Programmable system watch-dog timers*
  - *Big or Little endian support*
- **Interrupt Control**
  - *Provides services for internal and external sources*
  - *Allows status of each interrupt to be read and masked*
- **Three general purpose 32-bit timer/counters**
- **Programmable IO (PIO)**
  - *Input/Output/Interrupt source*
  - *Individually programmable*
- **SDRAM/EDODRAM Controller (32-bit memory only)**
  - *4 banks, non-interleaved, 256 MB total*
  - *Automatic refresh generation*
- **UART Interface**
  - *Two 16550 Compatible UARTs*
  - *Baud rate support up to 1.5M*
- **8/16/32-bit boot PROM support**
- **Boundary Scan JTAG Interface (IEEE Std. 1149.1 compatible)**
- **Memory & Peripheral Controller**
  - *6 banks, up to 8MB per bank*
  - *8/16/ or 32-bit interface per bank*
  - *Supports Flash ROM, SRAM, dual-port memory, and peripheral devices*
  - *Intel or Motorola style IO supports external wait-state generation*
- **4 DMA Channels**
  - *4 general purpose DMA, each with Endianness swappers and byte lane data alignment*
  - *Any channel can be used for PCI*
  - *Supports memory-to-memory, memory-to-I/O,memory-to-PCI, PCI-to-PCI, I/O-to-I/O transfers, and I/O support of scatter/gather*
  - *Supports chaining via linked lists of records*
  - *Supports unaligned transfers*
  - *Supports burst transfers*
  - *Programmable burst size*
- **PCI Bridge**
  - *32-bit PCI, up to 33 MHz*
  - *Revision 2.1 compliant*
  - *Target and master*
  - *Host or satellite*
  - *Three slot PCI arbiter, on-chip*
  - *Serial EEPROM support, for loading configuration registers*
- **3.3V core operation**
- **3.3V I/O operation with 5V tolerant I/O**
- **208 pin PQFP package**

Block Diagram



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Description

The IDT79RC32134 is a high performance system controller chip that supports IDT's RISCore32300 CPU family. The RC32134 offers a direct connection to IDT's RC32364 32-bit embedded microprocessor. The RC32134 provides the system logic for boot memory, main memory, I/O, and PCI. It also includes on-chip peripherals such as DMA channels, reset circuitry, interrupts, timers, and UARTs. Together, the RC32364 CPU and the RC32134 system controller form a complete CPU subsystem for embedded designs.

Figure 1 illustrates the typical system implementation, based on the RC32364 CPU and the RC32134 system controller. The RC32134 interfaces directly to the RC32364 and provides all of the necessary control and address signals to drive the external memory and I/O. Note that, depending on the loading of the CPU data bus, external data buffers could be used to reduce the loading and isolate different memory regions. As illustrated in the system block diagram, the memory and I/O data path is external to the RC32134.

Device Overview

The RC32134 interfaces directly to the RC32364's system bus. The RC32134 latches the address from the RC32364 internally and decodes it to detect which memory, I/O, or on-chip peripheral is being accessed, per the internal address map of the RC32134. The RC32134 generates all necessary control signals and address buses to the external memory and I/O. For main memory, I/O, on-chip peripherals, registers, and PCI, the RC32134 divides the physical address space into 14 different regions.

The data path for the local memory and peripherals (with the exception of PCI) is external to the RC32134. The data path from the PCI bus and from the internal peripherals and registers is internal to the RC32134.

Memory Controller. The Memory Controller on the RC32134 provides all of the address buses and control signals for interfacing the RC32364 CPU to standard SRAM, PROM, FLASH, and I/O and includes the boot PROM interface. The memory controller provides six individual chip selects and supports 8,16, and 32-bit wide memory and I/Os. Two chip selects have highly configurable memory address ranges, allowing selection of various memory types and widths to be supported. The RC32134 provides controls for optional external data transceivers for systems that require fast signalling with large loads.

SDRAM Controller. The SDRAM controller optimization provides higher throughput while using available DRAM technology. The SDRAM control register directly manages four banks of 32-bit physical non-interleaved memory. Each bank is 32-bits wide and supports a maximum of 64 MB per bank. Total memory support is 256 MB. The SDRAM controller has a built in refresh generator.

EDO DRAM Controller. The RC32134 EDO DRAM Controller supports up to 4 banks of non-interleaved 32-bit wide EDO DRAMs. Most of the EDO DRAM pins are shared with the SDRAM controller, and as such, the two operations can not be simultaneously enabled. Selection between SDRAM or EDO DRAM is made at boot-time through system software operations. The EDO supports 256 MB total of EDO DRAM. The EDO controller has a built in refresh generator.

PCI Interface. To transfer data between main memory and the PCI bus, the RC32134 incorporates a PCI interface. At reset time the PCI interface can be configured as either a host or satellite interface. The PCI interface supports 32-bit PCI at up to 33MHz and is PCI Specification, Revision 2.1 compliant.

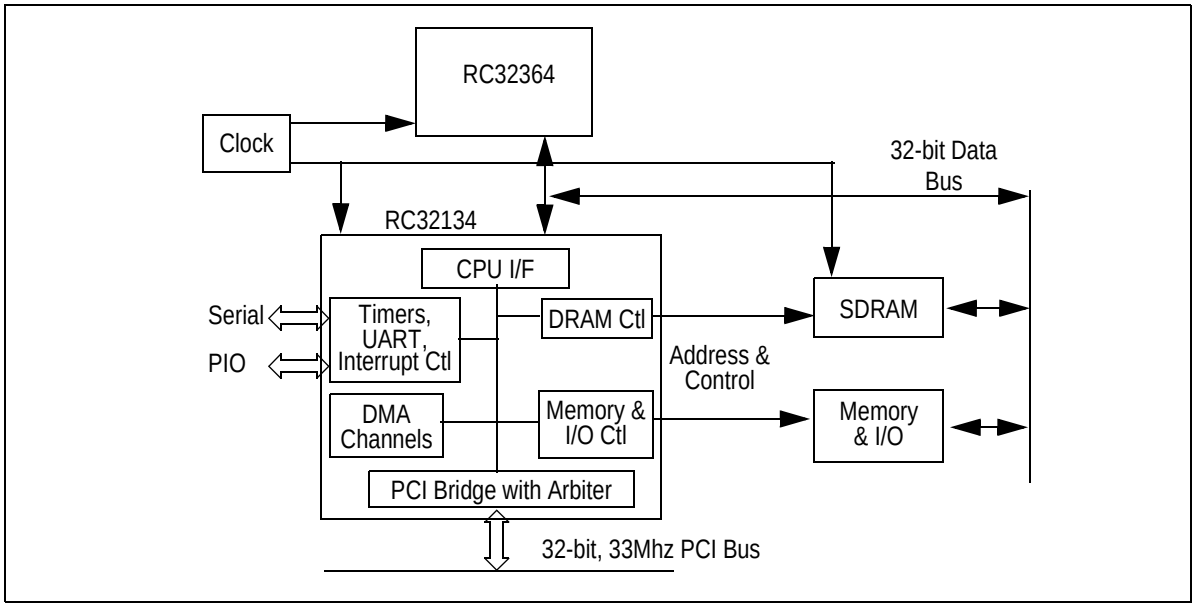


Figure 1 System Block Diagram

As a PCI master, the RC32134 can generate memory, I/O, or configuration cycles for direct local-to-PCI bus accesses. The PCI interface incorporates a 3-slot PCI bus arbiter, which includes fixed and round robin arbitration modes.

As a PCI target, the RC32134 allows access to its internal registers and to the RISCore32300 local bus through the PCI I/O read and write, or Memory read and write commands. The RC32134 PCI interface supports swapping little endian data to big endian, when the CPU subsystem is configured as a big endian system. For more information on the PDCI interface, please refer to the PCI Specification, Revision 2.1.

DMA Controller. Four general purpose DMA channels move data between source and destination ports. Source and destination ports can be system memory, PCI or I/O devices. Any of the four channels can be used for PCI initiator reads or writes. All four channels support a descriptor structure, to allow efficient data scatter/gather. The DMA controller supports swapping of data between big and little endian memory and I/O subsystems by memory region. It also supports quad-word burst transfers. All external 16 and 8-bit memory I/Os are treated as memory-mapped, word-aligned devices.

Expansion Interrupt Controller. The Expansion Interrupt Controller provides the interrupt logic for software to analyze the various RC32134 generated system interrupts and adds to the control already provided through the CP0 registers of the RC32364. Each system interrupt is registered and the pending status provided through this feature. The pending status can then be used to automatically generate a hardware interrupt to the CPU via individual mask bits. The pending interrupt status can also be optionally set or cleared by a direct software write.

PIO. Programmable I/O (PIO) pins are provided on the RC32134 so that any unused peripheral pins can be programmed for use as general purpose discrete I/O pins. These PIO pins can be software programmed as bidirectional lines, allowing pin values to be software programmed in output mode and software readable while in the input mode. The PIO pins can also be used as a source of interrupts to the CPU. Maximum Interfacing flexibility is thus provided without requiring extensive modifications to the board.

UART. The RC32134 incorporates two 16550 (an enhanced version of the 16450) compatible UARTs. To relieve the CPU of software overhead, the 16550 UART can be put into FIFO mode, allowing execution of either 16450 or 16550 compatible software. Two sets of 16-byte FIFOs are enabled during the 16550 mode: one set in the receive data path and one set in the transmit data path. A baud rate generator is included that divides the system clock by 1 to 64K and provides a 16X clock for driving the transmitter and receiver logic.

Timers/Counters. Three on-chip 32-bit general purpose Timers are provided on the RC32134. Each timer consists of both a count and a compare register. The count register resets to zero and then counts upward until it equals the compare register. When the count and compare registers are equal, the TC_n output is asserted and the count is then reset to zero.

JTAG. Board-level manufacturing debugging is facilitated through implementation of a fully compliant IEEE std. 1149.1 JTAG Boundary Scan interface.

Thermal Considerations

The RC32134 is guaranteed in a case temperature range of 0°C to +90°C, for commercial temperature devices; - 40°C to +90°C for industrial temperature devices. The speed (power) of the device and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification. The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device. Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 1

	∅CA					
Airflow (ft/min)	0	200	400	600	800	1000
208 PQFP	18	14	11	9	8	7

Table 1 Thermal Resistance (∅CA) at Various Airflows

Revision History:

July 21, 1999:

Changed the following: Thermal Resistance values; Table 2, Pin Descriptions; Logic diagram - RC32134; Clock parameter temperature from 85 to 90 degrees; AC timing characteristics - RC32134; DC electrical characteristics; Power consumption - RC32134; Absolute maximum ratings diagram; Pin-out 208-PQFP table; RC32134 alternate signal functions.

September 2, 1999: Corrected package drawing from 144-pin to 208-pin.

November 1, 1999: Removed Maximum column from Power Consumption table.

November 9, 1999: Moved pin 208 (sdram_245_oe_n) from Low drive to High drive in DC Electrical Characteristics Table.

April 28, 2000: Added Mode Configuration Interface Reset Sequence figure on page 14.

January 6, 2000:

- *Re*ordered Alternate Signals for the PIO Interface in Table 2 and changed pci_eeprom_mdi to pci_eeprom_mdo.
- Switched alternate pin signals for pci_eeprom_mdo and pci_eeprom_mdi in PCI Interface section of Table 2.
- Switched alternate pin signals for uart_rx and uart_tx in UART Interface section of Table 2.
- In RC32134 Alternate Signal Functions table, changed pin designations under Alt #1 column for pins 22 - 29.
- Changed 64145 references to 32134 in the Note section of the AC Timing Characteristics table.
- Updated the User Manual Timing Diagram Reference column in the AC Timing Characteristics table.

March 20, 2000: Changed PCI speed to 33 MHz.

June 20, 2000: Values were revised for three local memory/peripheral bus signals in the AC Timing Characteristics table.

July 12, 2000: Revised Tsu and Thld symbol numbers in UART section of AC Timing Characteristics table and revised reference to timing diagram.

April 9, 2001: In the Local Memory/Peripheral bus section of the AC Timing Characteristics table, deleted cpu_coldreset_n associated with Tsu4.

Pin Description Table

The following table lists the pins provided on the RC32134. Note that several pins are multiplexed and have been assigned alternate functions. These pins are designated and defined accordingly throughout this table. Also note that those pin names followed by _n are active-low signals.

Pin Name	Type	Alternate Signal(s)	Description
Local Memory and Peripheral Pins			
cpu_ad[31:0]	I/O	Not applicable	**CPU Address/Data Bus** This is the RC32134's primary multiplexed and bidirectional address and data bus. The RC32134 latches this bus internally and uses it to generate the necessary address lines to the external memory and peripherals. If the transaction is a write, the CPU then drives data on cpu_ad(31:0). During CPU generated transactions, the CPU drives Address(31:4) into the cpu_ad bus, during its address phase. During DMA generated transactions (or RC32134 internal register reads), the address phase is unused and the chip drives data during a write.
cpu_addr[3:2]	I	Not applicable	**CPU LSB Address Bus** During CPU generated transactions, the CPU drives Address(3:2) onto the cpu_addr bus. The RC32134 does not internally use the cpu_addr bus during the data phase. However, 8- or 16-bit memory or I/O systems must attach these two pins instead of mem_addr(3:2).
cpu_ale	I	Not applicable	**CPU Address Latch Enable** During CPU generated transactions, this signal indicates that the cpu_ad (31:0) is driving a valid address and can be latched internally by the RC32134.
cpu_cip_n	I	Not applicable	**CPU Cycle In Progress** During CPU generated transactions, this active-low signal indicates that a bus transaction is active. An external pullup resistor is required.
cpu_wr_n	I	Not applicable	**CPU Write Status** During CPU generated transactions, this active-low signal indicates whether or not a write is occurring. If a write is not occurring, then the implication is that a read is in progress.
cpu_be_n[3:0]	I	Not applicable	**CPU Byte Enable Bus** During CPU generated transactions, these active-low signals indicate which byte lanes are in use. **Note:** The table below indicates which cpu_be_n signal corresponds to which byte lane, whether or not the system is in big or little endian mode cpu_be_n[0] → Data Bits 7:0 cpu_be_n[1] → 15:8 cpu_be_n[2] → 23:16 cpu_be_n[3] → 31:24
cpu_ack_n	O	Not applicable	**CPU Acknowledge** During CPU generated transactions, this active-low signal is generated by the RC32134 to indicate that the present data have been accepted.
cpu_last_n	I	Not applicable	**CPU Last Data** During CPU generated transactions, this active-low signal indicates during the data phase that the present data is the last data.
cpu_buserr_n	O	Not applicable	**CPU Bus Error** During both CPU and DMA generated transactions, this active-low signal indicates that a bus error has occurred. This signal can also be optionally attached to an interrupt line.

Table 2 RC32134 Pin Descriptions (Page 1 of 8)

Pin Name	Type	Alternate Signal(s)	Description
cpu_masterclk	I	sdram_clk	**CPU Master System Clock** Provides the basic system clock. This clock must be the same clock that is provided to the RC32364 and also, if used, to SDRAM.
cpu_coldreset_n	I	Not applicable	**CPU Cold Reset** This active-low signal is asserted to the RC32364 CPU and RC32134 after V_{CC} becomes valid on the initial power-up. The Reset initialization vectors, for both the RC32364 and the RC32134, are latched by cold reset.
cpu_reset_n	O	Not applicable	**CPU Warm Reset** This active-low signal is a secondary reset signal asserted to the CPU at least 256 clocks after cold reset, allowing, for instance, stabilization of RC32364's PLL.
cpu_busreq_n	O	Not applicable	**CPU Bus Request** This active-low signal requests the CPU bus from the RC32364, for instance, by RC32134 to perform a DMA operation.
cpu_busgnt_n	I	Not applicable	**CPU Bus Grant** This active-low signal is a CPU bus grant from the RC32364, indicating that the local CPU bus has been released to the RC32134.
cpu_int_n	O	interrupt_n	**CPU Interrupt** This active-low signal is an interrupt indication to the CPU from RC32134's Interrupt Controller. Note: This pin is typically hooked up to the CPU's interrupt 3.
cpu_dt_r_n	O	mem_245_dt_r_n, sdram_245_dt_r_n, edodram_245_dt_r_n	**CPU Direction Transmit/Receive** This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during DMA read operations. This signal is tri-stated during CPU accesses (when the CPU owns the bus) and driven during DMA generated accesses. **Note:** An external pull-up resistor is required.
PCI Interface			
pci_ad[31:0]	I/O	Not applicable	**PCI Multiplexed Address/Data Bus** This address is driven by the Bus Master during initial frame_n assertion. The Data is then driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads.
pci_cbe_n[3:0]	I/O	Not applicable	**PCI Multiplexed Command/Byte Enable Bus** The Command bus (active high) is driven by the Bus Master during the initial frame_n assertion. The Byte Enable bus (active low) is driven by the Bus Master during the data phase(s). **Note:** The table below indicates which cpu_be_n signal corresponds to which byte lane, whether or not the system is in big or little endian mode.
pci_par	I/O	Not applicable	**PCI Parity** This signal indicates even parity of the pci_ad[31:0] bus and is driven by the Bus Master during Address and Write Data phases. During the Read data phase, this signal is driven by the Bus Slave.
pci_frame_n	I/O	Not applicable	**PCI Frame Negated** This active-low signal is driven by the Bus Master and indicates the duration of a PCI transfer. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last data.

	Data Bits
pci_be[0]	7:0
pci_be[1]	15:8
pci_be[2]	23:16
pci_be[3]	31:24

Table 2 RC32134 Pin Descriptions (Page 2 of 8)

Pin Name	Type	Alternate Signal(s)	Description
pci_trdy_n	I/O	Not applicable	**PCI Target Ready Negated** This active-low signal is driven by the Bus Slave and indicates that the current data can complete (the bus slave can accept/drive data).
pci_irdy_n	I/O	Not applicable	**PCI Initiator Ready Negated** Driven by the Bus Master, this active-low signal indicates that the current data can complete (PCI initiator is ready to accept/drive data).
pci_stop_n	I/O	Not applicable	**PCI Stop Negated** Driven by the Bus Slave this active-low signal terminates the current bus transaction.
pci_idsel	I	pci_req_n[2]	**PCI Initialization Device Select** **Host mode**: pci_req_n[2] is an input indicating a request from an external device. **Satellite mode:** used as pci_idsel pin which selects this device during a configuration read or write.
pci_perr_n	I/O	Not applicable	**PCI Parity Error Negated** Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs.
pci_serr_n	I/O	Not applicable	**System Error** Driven by any agent, this active-low signal indicates an address parity error, data parity during a Special Cycle command, or any other system error. An external 2.7K (5V) ohm or 8.2K (3.3V) ohm pull-up resistor is required, per the PCI revision 2.1 specifications.
pci_clk	I	Not applicable	**PCI Clock** Clock for PCI bus transactions that uses the rising edge for all timing references. Note that the PCI clock does not need to be synchronized to the cpu_masterclk.
pci_rst_n	I	Not applicable	**PCI Reset Negated** **In Host mode,** this active-low signal resets all PCI related logic. In **Satellite mode,** with boot from PCI mode, this signal resets all PCI related logic and also asserts the warm reset, cpu_rst_n, to the RC32134. and the RC32364.
pci_devsel_n	I/O	Not applicable	**PCI Device Select Negated** This active-low signal is driven by the target to indicate that the target has decoded the present address as a target address.
pci_req_n[2]	I	pci_idsel	**PCI Bus Request #2 Negated** This is an active-low signal that in **Host mode** is an input indicating a request from an external device. In **Satellite mode** pci_req_n[2] is used as the pci_idsel pin, which selects this device during a configuration read or write.
pci_req_n[1]	I	Not applicable	**PCI Bus Request #1 Negated** In **Host mode,** pci_req_n[1] is an input indicating a request from an external device. In **Satellite mode** pci_req_n[1] is unused.
pci_req_n[0]	I/O	Not applicable	**PCI Bus Request #0 Negated** In **Host mode,** this active-low signal is an input indicating a request from an external device. In **Satellite mode,** pci_req_n[0] is an output indicating a request from this device.
pci_gnt_n[2]	O	pci_inta_n	**PCI Bus Grant #2 Negated** In **Host mode,** this active-low signal is an output indicating a grant to an external device. In **Satellite mode,** pci_gnt_n[2] is used as the pci_inta_n output pin. An external 5k ohm pull-up resistor is required, per the PCI revision 2.1 specifications. **Note**: In host mode, int_n[1] on the RC32364 can be used for a pci_inta_n input and pci_int[d:c:b]_n uses int_n[5:4:2] on the RC32364 Bus Interface.
pci_gnt_n[1]	O	pci_eeprom_cs	**PCI Bus Grant #1 Negated** In **Host mode,** this active-low signal is an output indicating grants to external devices. In **Satellite mode,** pci_gnt_n[1] is used as the pci_eeprom_cs output pin for Serial Chip Select, for loading PCI Configuration Registers in the RC32134 Reset Initialization Vector PCI boot mode.

Table 2 RC32134 Pin Descriptions (Page 3 of 8)

Pin Name	Type	Alternate Signal(s)	Description
pci_gnt_n[0]	I/O	Not applicable	**PCI Bus Grant #0 Negated** In **Host mode,** this active-low signal is an output indicating a grant to an external device. In **Satellite mode,** pci_gnt_n[0] is an input indicating a grant to this device.
pci_inta_n	I/O	pci_gnt_n[2]	**PCI Interrupt #A Negated** In **Host mode,**pci_gnt_n[2] is an output indicating a grant to an external device. In **Satellite mode,** pci_gnt_n[2] is used as the pci_inta_n output pin. An external pull-up is required, per the PCI revision 2.1 specifications. Note: In host mode, int_n[1] on the RC32364 can be used for a pci_inta_n input and pci_int[d:c:b]_n uses int_n[5:4:2] on the RC32364 Bus Interface.
pci_lock_n	I	Not applicable	**PCI Lock Negated** This active-low signal is driven by the Bus Master and indicates that an exclusive operation is occurring.
pci_eeprom_mdo	I/O	pio[11]	**PCI EEPROM Master Data Out** In **Serial mode,** this signal is an output pin from RC32134 that connects as an Input to a Serial Chip for the Serial data input stream. In **PCI satellite mode,** it is an output pin from RC32134 that connects as an Input to a Serial Chip for the Serial data input stream for loading PCI Configuration Registers in the RC32134 Reset Initialization Vector PCI boot mode. This pin is also multiplexed as a PIO pin.
pci_eeprom_mdi	I/O	pio[8]	**PCI EEPROM Master Data In** The **Serial mode** provides an input pin to RC32134 from the Output of a Serial Chip for the Serial data output stream. The **PCI satellite mode** provides an input pin to RC32134 from the Output of a Serial Chip for the Serial data output stream, for PCI Configuration Registers in the RC32134 Reset Initialization Vector PCI boot mode. This pin is also multiplexed as a PIO pin.
pci_eeprom_cs	I/O	pci_gnt_n[1]	**PCI EEPROM Chip Select** **Host mode:** pci_gnt_n[1] is an output indicating grants to external devices. **Satellite mode:** Used as pci_eeprom_cs output pin for SPI Chip Select for loading PCI Configuration Registers in the RC32134 Reset Initialization Vector PCI boot mode.
pci_eeprom_sk	I/O	pio[10]	**PCI EEPROM Serial Clock** **Serial mode:** Output pin for Serial Clock. **PCI satellite mode:** Output pin for Serial Clock for loading PCI Configuration Registers in the RC32134 Reset Initialization Vector PCI boot mode. This pin is also multiplexed as a PIO pin.
Memory/I/O Controller			
mem_addr[22:2]	I/O	edodram_addr[15:2] sdram_addr[15:13] sdram_addr[11:2]	**Memory Address Bus** These signals provide the Memory or DRAM address, during a Memory or DRAM bus transactiion. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. For 32-bit system, use mem_addr[3:2] for the least significant address bits [3:2]. For 8 or 16-bit wide ports, to provide the least significant address bits [3:0], use cpu_addr[3:2] and cpu_be_n[1:0]. mem_addr subsets mem_addr[22:20] | I/O | reset_boot_mode[1:0], reset_pci_host_mode mem_addr[15:2] | I/O | sdram_addr[15:13], sdram_addr[11:2], edodram_addr[15:2]
mem_cs_n[5:0]	O	Not applicable	**Memory Chip Select Negated** This active-low signal indicates that a Memory or I/O Bank is actively selected.

Table 2 RC32134 Pin Descriptions (Page 4 of 8)

Pin Name	Type	Alternate Signal(s)	Description
mem_oe_n	O	Not applicable	**Memory Output Enable Negated** This active-low signal indicates that either a Memory or I/O Bank can output its data lines onto the cpu_ad bus.
mem_we_n[3:0]	O	Not applicable	**Memory Write Enable Negated Bus** These active-low signals indicate which bytes are to be written during a memory or I/O transaction.
mem_wait_n	I	edo_dram_wait_n	**Memory Wait Negated** In **MEM, IOI, IOM modes** this active-low signal allows external wait-states to be injected during the last cycle before data is sampled. In **DPM (dual-port) mode**, this signal allows dual-port busy signal to restart memory transaction.
mem_245_oe_n	O	Not applicable	**Memory FCT245 Output Enable Negated** This active-low signal controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank.
mem_245_dt_r_n	O	cpu_dt_r_n	**Memory FCT245 Direction Xmit/Rcv Negated** Uses the cpu_dt_r_n pin.
EDODRAM Controller			
edodram_addr[15:2]	O	mem_addr[15:2]	**Edodram_addr/sdram_addr mode** These are output signals that provide a DRAM address during a DRAM transaction. The DRAM address multiplexes between Row and Column Addresses. During each word data, the column address increments either in linear or sub-block ordering, depending on the type of transaction. Allows an external memory debug emulator to inject wait-states. For more detail, see the user's manual.
edodram_ras_n[3:0]	O	sdram_cs_n[3:0]	**DRAM Row Address Strobe Negated Bus** **SDRAM mode:** Provides chip select to each SDRAM bank. **EDODRAM mode:** Used as edodram_ras_n[3:0] pins to provide a RAS signal for each EDODRAM bank.
edodram_cas_n[3:0]	O	sdram_bemask_n[3:0]	**DRAM Column Address Strobe Negated Bus** In the **EDODRAM mode** these signals are used as edodram_cas_n[3:0] to provide a CAS signal for each byte lane. In the **SDRAM mode,** these signals provide byte enables for each byte lane of all DRAM banks.
edodram_oe_n	O	sdram_ras_n, sdram_245_oe_n	**DRAM EDO Output Enable Negated** **In the EDODRAM mode**, this active-low signal provides an output enable signal for reads for particular OE types of EDODRAM. This signal also controls the output enable to an optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank. This signal also controls the output enable to each EDO DRAM chip. Alternatively, because the EDODRAM controller always uses Early Writes and CAS controlled non-interleaved Reads, the OE_n pin, on each EDO DRAM chip, can simply be tied to ground. **The SDRAM RAS** mode is a control signal to all SDRAM banks. In **SDRAM mode**, this signal controls the output enable to an optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank.
edodram_we_n	O	sdram_we_n	**DRAM EDO Write Enable Negated** In **EDODRAM** mode, this active-low signal is used as the edodram_we_n pin to provide a write enable signal for EDODRAM. Write enable is valid at all times and high during refresh. In **SDRAM mode,** this signal provides the SDRAM WE control signal to all SDRAM banks.
edodram_wait_n	I	mem_wait_n	**DRAM Wait Negated** In the **EDO DRAM mode**, this active-low signal allows external wait-states to be injected at any time during the EDO DRAM cycle. In the **MEM, IOI, IOM modes**, this active-low signal allows external wait-states to be injected during the last cycle before data is sampled. The DPM (dual-port) mode allows the dual-port busy signal to restart memory transactions.

Table 2 RC32134 Pin Descriptions (Page 5 of 8)

Pin Name	Type	Alternate Signal(s)	Description
edodram_245_oe_n	O	sdram_245_oe_n	**DRAM FCT245 Output Enable Negated** **In the SDRAM mode this active-low signal** controls the output enable to an optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank. In the **EDODRAM mode** this signal controls the output enable to an optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank. This signal also controls the output enable to each EDO DRAM chip. Alternatively, because the EDODRAM controller always uses Early Writes and CAS controlled non-interleaved Reads, the OE_n pin, on each EDO DRAM chip, can simply be tied to ground.
edodram_245_dt_r_n	O	cpu_dt_r_n	**DRAM/Mem FCT245 Direct Xmit/Rcv Negated** This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during DMA read operations. This signal is tri-stated during CPU accesses (when the CPU owns the bus) and drives during DMA generated accesses.

SDRAM Controller Interface

sdram_addr[15:13] sdram_addr[11:2]	O	mem_addr[15:13] mem_addr[11:2]	**SDRAM Address Bus** These signals are outputs providing a DRAM address during a DRAM transaction. The DRAM address multiplexes between Row and Column Addresses. During each word data, the column address increments either in linear or sub-block ordering, depending on the type of transaction.
sdram_addr_12	O	PIO[9]	**SDRAM Address line 12** This SDRAM address is dedicated to the SDRAM and multiplexes between the row address; and during the precharge command, the "all bank" indicator.
sdram_ras_n	O	edodram_oe_n	**SDRAM RAS Negated** **SDRAM mode:** Provides SDRAM RAS control signal to all SDRAM banks. **EDODRAM mode:** Provides an output enable signal for reads for particular OE types of EDODRAM.
sdram_cas_n	O	Not applicable	**SDRAM CAS Negated** This active-low signal provides an SDRAM CAS control signal to all SDRAM banks.
sdram_we_n	O	edodram_we_n	**SDRAM WE Negated** **SDRAM mode:** Provides SDRAM WE control signal to all SDRAM banks. **EDODRAM mode:** Used as edodram_we_n pin to provide a write enable signal for EDODRAM. Write enable is valid at all times and high during refresh.
sdram_clk	I	cpu_masterclk	**SDRAM Clock** This signal provides the basic system clock and must be the same clock that is provided to the RC32364 and also, if used, to SDRAM.
sdram_cke	O	Not applicable	**SDRAM Clock Enable** In the **SDRAM mode** this signal provides the clock enable to all SDRAM banks.
sdram_cs_n[3:0]	O	edodram_ras_n[3:0]	**SDRAM Chip Select Negated Bus** In **SDRAM mode,** these active-low signals provide chip select to each SDRAM bank. In **EDODRAM mode** they are used as the edodram_ras_n[3:0] pins and provide a RAS signal for each EDODRAM bank.
sdram_bemask_n[3:0]	O	edodram_cas_n[3:0]	**SDRAM Byte Enable Mask Negated Bus** The **SDRAM mode** provides byte enables for each byte lane of all DRAM banks. To provide a CAS signal for each byte lane, the **EDODRAM mode** is used as edodram_cas_n[3:0].
sdram_245_oe_n	O	edodram_245_oe_n, edodram_oe_n	**SDRAM FCT245 Output Enable Negated** In **SDRAM mode,** this active-low signal controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank. In **EDODRAM mode** this signal controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to any DRAM bank. Also controls output enable to each EDO DRAM chip. Alternatively, because the EDODRAM controller always uses Early Writes and CAS controlled non-interleaved Reads, the OE_n pin on each EDO DRAM chip can simply be tied to ground.

Table 2 RC32134 Pin Descriptions (Page 6 of 8)

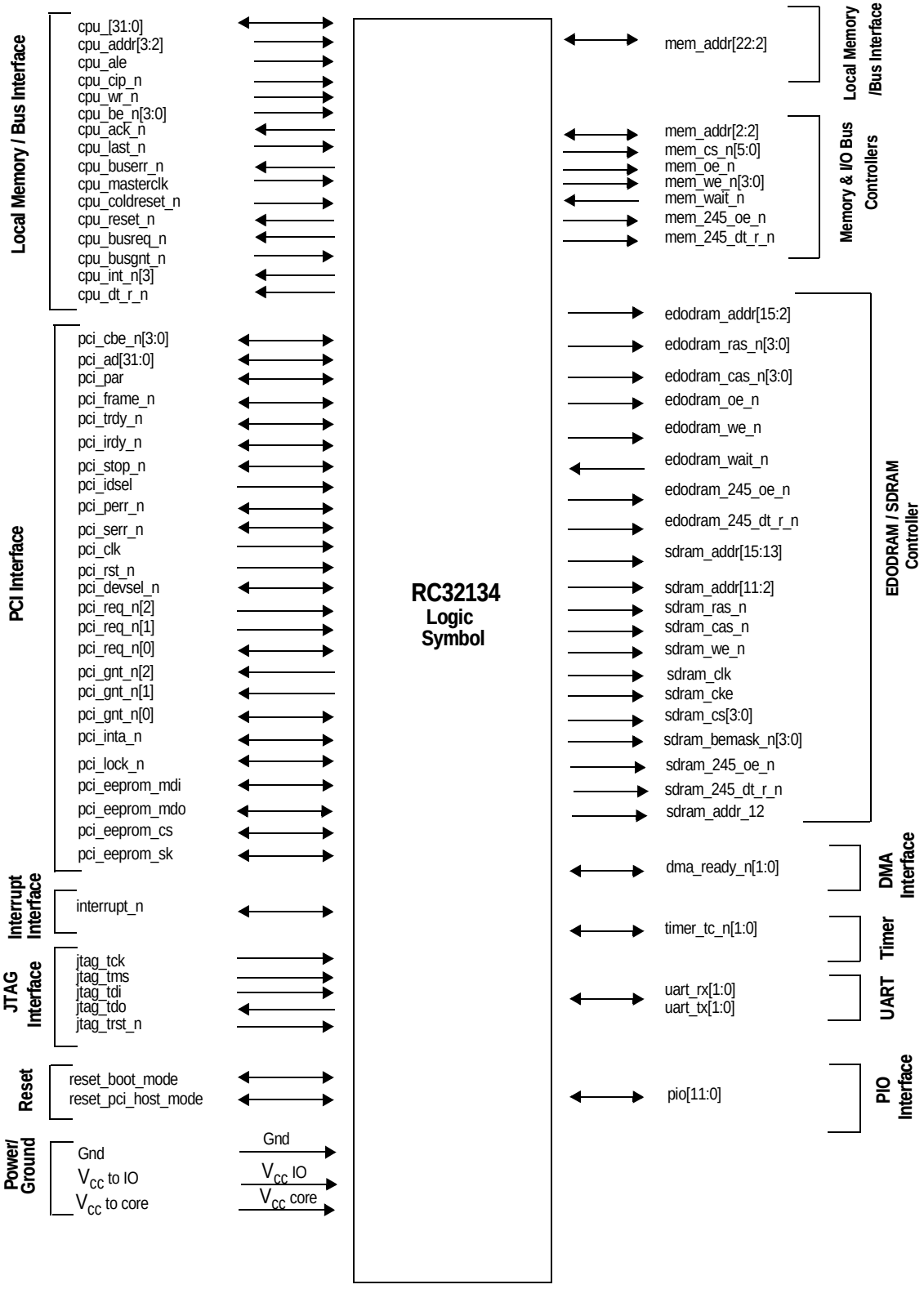
Pin Name	Type	Alternate Signal(s)	Description
sdram_245_dt_r_n	O	cpu_dt_r_n	**SDRAM FCT245 Direction Transmit/Receive** This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank and is asserted during DMA read operations. This signal is tri-stated during CPU accesses (when the CPU owns the bus) and drives during DMA generated accesses.
DMA Interface			
dma_ready_n[1:0]	I/O	dma_done_n[1:0] pio[1:0]	**DMA Ready Negated Bus** Input pin for general purpose DMA channels[1:0] that can initiate the next datum in the current DMA descriptor frame. dma_ready_n[1:0] pins are not synchronized internally by the RC32134 and thus must meet the specified setup and hold time with respect to the input clock.
dma_done_n[1:0]	I/O	dma_ready_n[1:0]	**DMA Done** Input pin for general purpose DMA channels[1:0] that can terminate the current DMA descriptor frame.
Interrupt Controller			
interrupt_n	I/O	cpu_int_n	**Interrupt Negated** Uses cpu_int_n. This active-low signal is an interrupt indication to the CPU from RC32134's Interrupt Controller.
PIO Interface			
pio[11:0]	I/O	pci_eeprom_mdo pci_eeprom_sk sdram_addr_12 pci_eeprom_mdi uart _rx[0], uart_tx[0] uart_rx[1], uart_tx[1] timer_tc_n[0], timer_tc_n[1] dma_ready_n[0] dma_ready_n[1]	**Programmable Input/Output** General purpose pins that can each be configured as a general purpose input or general purpose output. The pci_eeprom_mdo, pci_eeprom_sk, and sdram_addr12 default to outputs. The rest default to inputs.
Timer/Counter			
timer_tc_n[1:0]	O	timer_gate_n[1:0], pio[3:2]	**Timer Terminal Count Overflow Negated** Output indicating that the timer has reached its count compare value and has overflowed back to 0.
timer_gate_n[1:0]	I	timer_tc_n[1:0], pio[3:2]	**Timer Gate Negated** Input indicating that the timer may count one tick on the next clock edge.
UART Interface			
uart_rx[1:0]	I/O	pio[7] pio[5]	**UART Receive Data Bus** UART mode: Each UART channel receives data on their respective input pin.
uart_tx[1:0]	I/O	pio[6] pio[4]	**UART Transmit Data Bus** UART mode: Each UART channel sends data on their respective output pin. Note that these pins default to inputs at reset time and must be programmed via the PIO interface before being used as UART outputs.

Table 2 RC32134 Pin Descriptions (Page 7 of 8)

<table>
<tr><th>Pin Name</th><th>Type</th><th>Alternate Signal(s)</th><th>Description</th></tr>
<tr><td colspan="4">Reset</td></tr>
<tr><td>reset_boot_mode[1:0]</td><td>I/O</td><td>mem_addr[22:21]</td><td>Reset Initialization Vector
Used as Reset Initialization. Vector input pins that are latched by coldreset_n de-asserting.
<table><tr><th>Value</th><th>Description</th></tr><tr><td>11</td><td>Non-boot mode. Idle at reset. This RC32134 does not supply boot code control.</td></tr><tr><td>10</td><td>Reserved.</td></tr><tr><td>01</td><td>PCI-boot mode. (pci_host_mode must be in satellite mode). RC32134 will reset either from a cold reset or from a PCI reset. Boot code is provided via PCI.</td></tr><tr><td>00</td><td>Standard-boot mode. Boot from this RC32134's memory controller (typical system).</td></tr></table></td></tr>
<tr><td>reset_pci_host_mode</td><td>I/O</td><td>mem_addr[20]</td><td>Reset PCI Host Mode
Used as Reset Initialization. Vector input pins that are latched by coldreset_n de-asserting. Programming for this signal is as indicated below:
<table><tr><th>Value</th><th>Description</th></tr><tr><td>1</td><td>PCI is in satellite mode.</td></tr><tr><td>0</td><td>PCI is in host mode (typical system).</td></tr></table></td></tr>
<tr><td colspan="4">JTAG</td></tr>
<tr><td>jtag_tck</td><td>I</td><td>Not applicable</td><td>JTAG Test Clock
Provides clock for boundary scan test cells. Note: Must be either dynamically driven or an external pull-up or pull-down resistor is required, if JTAG is not being used.</td></tr>
<tr><td>jtag_tms</td><td>I</td><td>Not applicable</td><td>JTAG Test Mode
This signal provides command/mode input for boundary scan test cells. An external pull-up resistor is required.</td></tr>
<tr><td>jtag_tdi</td><td>I</td><td>Not applicable</td><td>JTAG Test Data Input
Provides data input for boundary scan test cells. An external pull-up resistor is required.</td></tr>
<tr><td>jtag_tdo</td><td>O</td><td>Not applicable</td><td>JTAG Test Data Out
Provides data output for boundary scan test cells.</td></tr>
<tr><td>jtag_trst_n</td><td>I</td><td>Not applicable</td><td>JTAG Test Reset Negated
This active-low signal provides reset to boundary scan test cells. Note: An external pull-up resistor is required. This pin must be driven low to reset the JTAG tap controller, or held low if JTAG is not being used.</td></tr>
</table>

Table 2 RC32134 Pin Descriptions (Page 8 of 8)

Logic Diagram — RC32134



Note: The alternate signals are listed in “RC32134 Alternate Signal Functions” on page 22

Clock Parameters — RC32134

(Tc = 0°C to +90°C Commercial, Tc = -40°C to +90°C Industrial, V_{cc} Core = +3.3V±5%)

Parameter	Symbol	Test Conditions	RC32134 75MHz		Units
			Min	Max	
cpu_masterclock HIGH	t_{MCHIGH}	Transition ≤ 3ns	6	—	ns
cpu_masterclock LOW	t_{MCLOW}	Transition ≤ 3ns	6	—	ns
cpu_masterclock period	t_{MCP}		13.33	—	ns
cpu_masterclock Rise& Fall Time	t_{MCRise}, t_{MCFall}		—	3	ns
pci_clk Period	t_{PCP}		30	—	ns
pci_clk Rise& Fall Time	t_{PCRise}, t_{PCFall}	PCI 2.1	—	3	ns
jtag_tck Rise& Fall Time	t_{JCRise}, t_{JCFall}		—	5	ns
jtag clock period	jtag_clk		100	—	ns

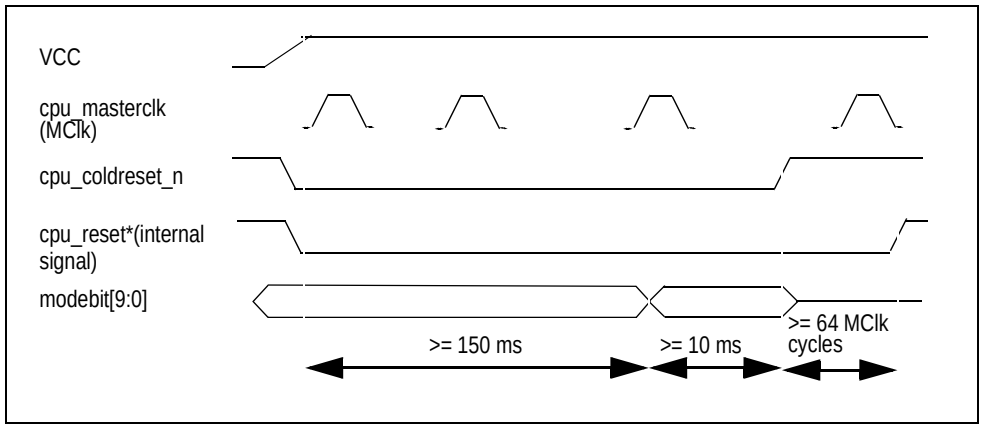


Figure 2 Mode Configuration Interface Reset Sequence

There is no special requirement for how fast Vcc ramps up to 3.3V. However, all timing references are based on Vcc stabilized at 3.3V ± 5%.

AC Timing Characteristics — RC32134

(Tc = 0°C to +90°C Commercial, Tc = -40°C to +90°C Industrial, V_{cc} Core = +3.3V±5%)

Signal	Symbol	Reference Edge	75MHz		Unit	User Manual Timing Diagram Reference
			Min	Max		
Local Memory/ Peripheral Bus						
cpu_ad[31:0] (address phase), cpu_addr[3:2]	Tsu1	cpu_ale falling	3	—	ns	**Chapter 3, Figure 3.6 Figure 3.7 Figure 3.8 Figure 3.9 Figure 5.4 Figure 8.8 Figure 8.9**
cpu_ad[31:0] (address phase), cpu_addr[3:2]	Thld1	cpu_ale falling	3	—	ns	
cpu_ad[31:0] (data phase)	Tsu2	cpu_masterclk rising	5.5	—	ns	
cpu_ad[31:0] (data phase)	Thld2	cpu_masterclk rising	0.7	—	ns	
cpu_ale rising	Tsu3	cpu_masterclk falling	0	—	ns	
cpu_ale falling (ale pulse width)	Tale high	cpu_ale rising	4	—	ns	
cpu_busgnt_n, cpu_wr_n, cpu_be_n[3:0], cpu_last_n	Tsu4	cpu_masterclk rising	5	—	ns	
cpu_busgnt_n, cpu_wr_n, cpu_be_n[3:0], cpu_reset_n, cpu_last_n	Thld4	cpu_masterclk rising	0.7	—	ns	
cpu_cip_n	Tsu5	cpu_masterclk rising	5	—	ns	
cpu_cip_n	Thld5	cpu_masterclk rising	0.7	—	ns	
cpu_ack_n, cpu_buserr_n, cpu_reset_n	Tdo1	cpu_masterclk rising	—	8	ns	
cpu_busreq_n, cpu_int_n	Tdo2	cpu_masterclk rising	—	8	ns	
cpu_dt_r_n	Tdo3	cpu_masterclk rising	—	8	ns	
cpu_ad[31:0]	Tdo4	cpu_masterclk rising	—	8	ns	
cpu_ad[31:0] output hold time	Tdoh1	cpu_masterclk rising	1[1]	—	ns	
cpu_ack_n, cpu_buserr_n, cpu_reset_n, cpu_busreq_n, cpu_int_n	Tdoh2	cpu_masterclk rising	0.5	—	ns	
DMA						
dma_ready_n[1:0], dma_done_n[1:0]	Tsu7	cpu_masterclk rising	3	—	ns	**Chapter 9, Figures 9.6 & 9.7**
dma_ready_n[1:0], dma_done_n[1:0]	Thld9	cpu_masterclk rising	0.5	—	ns	
Memory-I/O Controller						
mem_wait_n	Tsu6	cpu_masterclk rising	3	—	ns	**Chapter 3, Figure 3.6 Figure 3.7 Figure 3.8**
mem_wait_n	Thld8	cpu_masterclk rising	0.5	—	ns	
mem_addr[22:2]	Tdo5	cpu_masterclk rising	—	8	ns	
mem_cs_n[5:0]	Tdo6	cpu_masterclk rising	—	8	ns	
mem_oe_n, mem_we_[3:0], mem_245_dt_r_n, mem_245_oe_n	Tdo7	cpu_masterclk rising	—	8	ns	
mem_addr[22:2] mem_cs_n[5:0] mem_oe_n, mem_we_[3:0], mem_245_dt_r_n, mem_245_oe_n	Tdoh3	cpu_masterclk rising	0.5	—	ns	

Signal	Symbol	Reference Edge	75MHz		Unit	User Manual Timing Diagram Reference
			Min	Max		
PCI						
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_idse, pci_perr_n, pci_serr_n, pci_rst_n, pci_devsel_n, pci_lock_n	T_su	pci_clk rising	7	—	ns	**Note: Refer to PCI Specification, Revision 2.1 for a detailed timing diagram.**
pci_gnt_n[0]	T_su(ptp)		10	—	ns	
pci_req_n[2:0]	T_su(ptp)		12	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_idse, pci_perr_n, pci_serr_n, pci_rst_n, pci_devsel_n, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_lock_n	T_h	pci_clk rising	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	10		ns	
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	10		ns	
pci_eeprom_mdo, pci-eeprom_cs	Tp	pci_clk rising, pci_eeprom_sk falling		10	ns	
pci_eeprom_sk	Tp	pci_clk rising		12	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_inta_n, pci_lock_n	T_val	pci_clk rising	2	11	ns	
pci_req_n[0], pci_gnt_n[2:0]	T_val(ptp)	pci_clk rising	2	12	ns	
SDRAM Controller						
sdram_245_dt_r_n, sdram_addr[15:2]	Tdo8	cpu_masterclk rising	—	8	ns	**Chapter 4, Figure 4.4**
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_bemask_n[3:0] sdram_cke	Tdo9	cpu_masterclk rising	—	8	ns	
sdram_addr_12	Tdo10	cpu_masterclk rising	—	8	ns	
sdram_245_oe_n	Tdo11	cpu_masterclk rising	—	8	ns	
sdram_245_dt_r_n, sdram_addr[15:2]	Tdoh4	cpu_masterclk rising	1[1]	—	ns	
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_bemask_n[3:0] sdram_cke sdram_addr_12 sdram_245_oe_n	Tdoh4	cpu_masterclk rising	1[1]	—	ns	
EDODDRAM Controller						
edodram_wait_n	Tsu7	cpu_masterclk rising	3	—	ns	**Chapter 5, Figure 5.3**
edodram_wait_n	Thld8	cpu_masterclk rising	0.5	—	ns	
edodram_addr[15:2], edodram_245_dt_r_n	Tdo12	cpu_masterclk rising	—	8	ns	
edodram_ras_n[3:0], edodram_cas_n[3:0], edodram_we_n, edodram_oe_n	Tdo13	cpu_masterclk rising	—	8	ns	
edodram_245_oe_n	Tdo14	cpu_masterclk rising	—	8	ns	

Signal	Symbol	Reference Edge	75MHz		Unit	User Manual Timing Diagram Reference
			Min	Max		
edodram_addr[15:2], edodram_245_dt_r_n edodram_ras_n[3:0], edodram_cas_n[3:0], edodram_we_n, edodram_oe_n edodram_245_oe_n	Tdoh5	cpu_masterclk rising	1[1]	—	ns	**Chapter 5, Figure 5.3** (Continued)
Timer						
timer_tc_n[1:0], timer_gate_n[1:0]	Tsu8	cpu_masterclk rising	3	—	ns	**Chapter 10, Figures 10.6 and 10.7**
timer_tc_n[1:0], timer_gate_n[1:0]	Thld10	cpu_masterclk rising	0.5	—	ns	
timer_tc_n[1:0], timer_gate_n[1:0]	Tdo15	cpu_masterclk rising	—	8	ns	
timer_tc_n[1:0], timer_gate_n[1:0]	Tdoh6	cpu_masterclk rising	1[1]	—	ns	
PIO						
PIO[11:0]	Tsu7	cpu_masterclk rising	3	—	ns	**Chapter 9, Figures 9.6 and 9.7**
PIO[11:0]	Thld9	cpu_masterclk rising	0.5	—	ns	
PIO[11], PIO[9:0]	Tdo16	cpu_masterclk rising	—	10	ns	
PIO[10]	Tdo19	cpu_masterclk rising	—	12	ns	
PIO[11], PIO[9:0]	Tdoh7	cpu_masterclk rising	1[1]	—	ns	
PIO[10]	Tdoh7	cpu_masterclk rising	1[1]	—	ns	
UARTs						
uart_rx[1:0], uart_tx[1:0]	Tsu9	cpu_masterclk rising	10		ns	**Chapter 11, Figure 11.15**
uart_rx[1:0], uart_tx[1:0]	Thld11	cpu_masterclk rising	10		ns	
uart_rx[1:0], uart_tx[1:0]	Tdo16	cpu_masterclk rising	—	10	ns	
uart_rx[1:0], uart_tx[1:0]	Tdoh8	cpu_masterclk rising	1[1]	—	ns	
Interrupt Handling						
interrupt_n	Tdo2	cpu_masterclk rising	—	8	ns	**Chapter 8, Figures 8.8 and 8.9**
interrupt_n	Tdoh2	cpu_masterclk-rising	1[1]	—	ns	
Reset						
reset_boot_mode, reset_pci_host_mode	Tsu8	cpu_masterclk-rising	3		ns	**Chapter 2, Figure 2.6**
reset_boot_mode, reset_pci_host_mode	Thld12	cpu_masterclk-rising	0.5		ns	
JTAG Interface						
jtag_tms, jtag_tdi, jtag_trst_n	Tsu	jtag_tck rising	10		ns	**Refer to Figure 2 below**
jtag_tms, jtag_tdi, jtag_trst_n	Thld	jtag_tck rising	10		ns	
jtag_tdo	Tdo18	jtag_tck falling	—	10	ns	

Note: Tsu_x = input setup time to RC32134
$Thld_x$ = input hold time to RC32134
Tdo_x = output propagation time from RC32134
$Tdoh_x$ = output hold time from RC32134

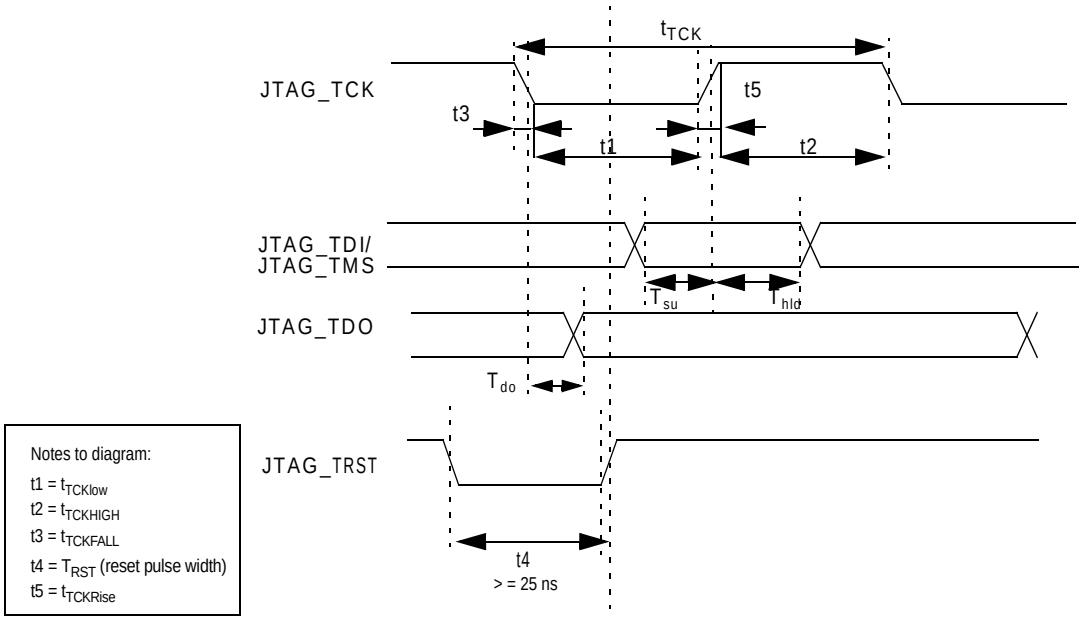
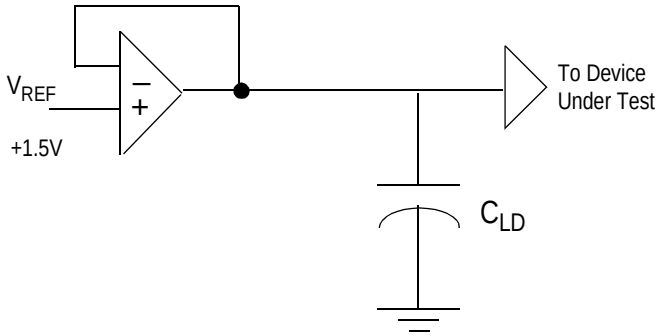


Figure 3 Standard JTAG timing

Output Loading for AC Testing (for non-PCI signals)



Signal	Cld
All Signals	50 pF

Note: PCI pins have been correlated to PCI 2.1.

Recommended Operation Temperature and Supply Voltage

Grade	Temperature	Gnd	VccIO	VccCore
Commercial	0°C to +90°C (Case)	0V	3.3V±5%	3.3V±5%
Industrial	-40° + 90°C (Case)	0V	3.3V±5%	3.3V±5%

Capacitive Load Deration

Refer to the IDT document “RC32134 IBIS Model” under sub-category RC32134 Integrated Processor on the company’s web page for Processors (http://www.idt.com/products/pages/Processors.html) .

DC Electrical Characteristics

Tc = 0°C to +90°C Commercial, Tc = -40°C to +90°C Industrial, V_{cc} Core = +3.3V±5%

	Parameter	RC32134 75MHz		Pin Numbers	Conditions
		Minimum	Maximum		
LOW Drive Pads	V_{OL}	—	0.4V	1, 2, 3, 4, 5, 8, 15, 18, 19, 20, 21, 22, 23, 24, 25, 28, 29, 30, 31, 104, 106, 118, 133, 137, 142, 161	$\|I_{OUT}\|$ = 10.8mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 7.8mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	V_{cc} + 2.0V		
HIGH Drive Pads	V_{OL}	—	0.4V	9, 10, 11, 12, 13, 107, 108, 109, 112, 113, 114, 115, 116, 117, 119, 122, 123, 124, 125, 126, 129, 132, 134, 135, 138, 139, 143, 144, 146, 147, 149, 152, 154, 155, 159, 160, 165, 167, 168, 169, 170, 171, 174, 175, 176, 177, 178, 179, 180, 181, 184, 185, 186, 187, 188, 189, 190, 191, 194, 195, 196, 197, 198, 199, 200, 201, 204, 205, 206, 207, 208	$\|I_{OUT}\|$ = 19mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 15.6mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	V_{cc} + 2.0V		
PCI Drive Pads	V_{OL}	—	0.4V	35, 39, 42, 43, 45, 48, 49, 50, 51, 52, 53, 54, 55, 56, 60, 61, 62, 63, 64, 65, 66, 67, 70, 71, 72, 73, 74, 75, 77, 80, 81, 82, 83, 84, 85, 86, 87, 90, 91, 92, 93, 94, 95, 96, 97, 100, 101, 102, 103	$\|I_{OUT}\|$ = 25mA
	V_{OH}	V_{cc} - 0.4V	—		$\|I_{OUT}\|$ = 19.5mA
	V_{IL}	—	0.8V		
	V_{IH}	2.0V	5.5		—
	C_{IN}	—	10pF	All Except 41, 57	—
	C_{IN}	5pf	12pF	41	Per PCI 2.1
	C_{IN}		8pF	57	Per PCI 2.1
	C_{OUT}	—	10pF	All output pads	—
	I/O_{LEAK}	—	20uA	All pins	Input/Output Leakage

Power Consumption—RC32134

Parameter	RC32134 75MHz	Conditions
Typical I_{CC} P_{typ}	360mA 1.2W	C_L = 50pF Ta= 25°C V_{cc} core = 3.3V V_{cc} IO = 3.3V cpu_masterclk = 75MHz pci_clk = 33MHz
Max I_{CC} P_{max}	460mA 1.6W	C_L = 50pF Ta= 55°C V_{cc} core = V_{cc} core Max V_{cc} IO = 3.47V cpu_masterclk = 75MHz pci_clk = 33MHz

Absolute Maximum Ratings

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	-0.3	4.0	V
Vi	Input Voltage	Gnd	5.5	V
Tstg	Storage Temperature	-40	125	degrees C
Ta	Ambient Temperature Value	0	70	degrees C

Package Pin-out - 208-PQFP

The following table lists the pin numbers and signal names for the RC32134. To maximize pin usage, several pins have alternate functions, as noted in the “Alt” column and described in “RC32134 Alternate Signal Functions” on page 22. Signal names ending with an _n are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
1	mem_cs_n[5]		53	pci_ad[26]		105	cpu_wr_n		157	cpu_coldreset_n	
2	mem_cs_n[4]		54	pci_ad[25]		106	cpu_reset_n		158	cpu_be_n[3]	
3	mem_cs_n[3]		55	pci_ad[24]		107	cpu_ad[21]		159	cpu_ad[20]	
4	mem_cs_n[2]		56	pci_cbe_n[3]		108	cpu_ad[9]		160	cpu_ad[11]	
5	mem_cs_n[1]		57	pci_req_n[2] (Host mode)	1	109	cpu_ad[22]		161	cpu_busreq_n	
6	Vcc I/O		58	V_{cc} I/O		110	V_{cc} I/O		162	V_{cc} I/O	
7	V_{ss}		59	V_{ss}		111	V_{ss}		163	V_{ss}	
8	mem_cs_n[0]		60	pci_ad[23]		112	cpu_ad[8]		164	cpu_addr[2]	
9	mem_oe_n		61	pci_ad[22]		113	cpu_ad[23]		165	cpu_ad[10]	
10	mem_we_n[3]		62	pci_ad[21]		114	cpu_ad[7]		166	cpu_addr[3]	
11	mem_we_n[2]		63	pci_ad[20]		115	cpu_ad[24]		167	mem_addr[22]	1
12	mem_we_n[1]		64	pci_ad[19]		116	cpu_ad[6]		168	mem_addr[21]	1
13	mem_we_n[0]		65	pci_ad[18]		117	cpu_ad[25]		169	mem_addr[20]	1
14	mem_wait_n	2	66	pci_ad[17]		118	cpu_dt_r_n	3	170	mem_addr[19]	
15	mem_245_oe_n		67	pci_ad[16]		119	cpu_ad[5]		171	mem_addr[18]	
16	V_{cc} I/O		68	V_{cc} I/O		120	V_{cc} I/O		172	V_{cc} I/O	
17	V_{ss}		69	V_{ss}		121	V_{ss}		173	V_{ss}	
18	dma_ready_n[1]	2	70	pci_cbe_n[2]		122	cpu_ad[26]		174	mem_addr[17]	
19	dma_ready_n[0]	2	71	pci_frame_n		123	cpu_ad[4]		175	mem_addr[16]	
20	timer_tc_n[1]	2	72	pci_irdy_n		124	cpu_ad[27]		176	mem_addr[15]	2
21	timer_tc_n[0]	2	73	pci_trdy_n		125	cpu_ad[3]		177	mem_addr[14]	2

Table 3: RC32134 208-pin QFP Package Pin-Out (Page 1 of 2)

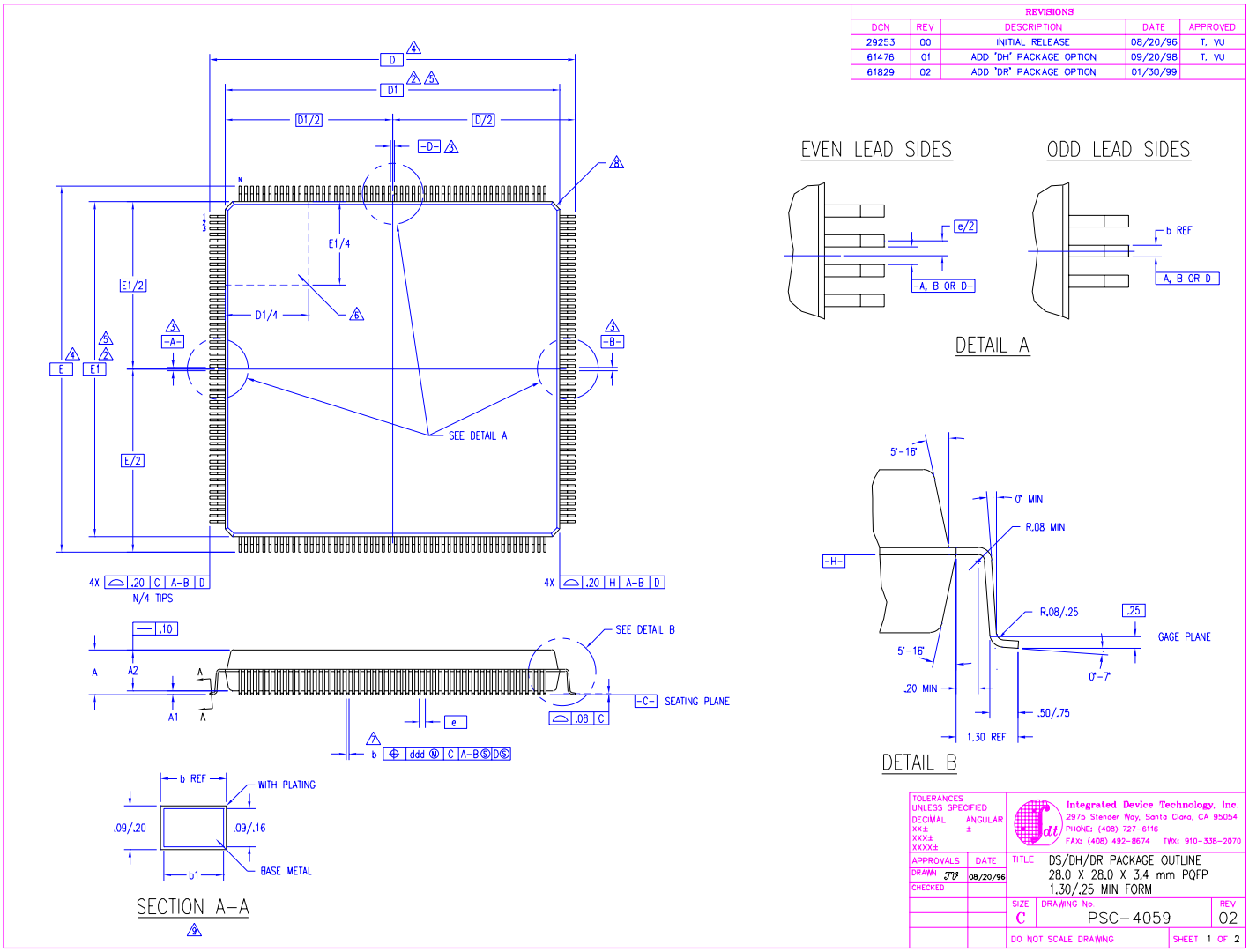
Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
22	uart_rx[1]	1	74	pci_devsel_n		126	cpu_ad[28]		178	mem_addr[13]	2
23	uart_tx[1]	1	75	pci_stop_n		127	cpu_cip_n		179	sdram_bemask_n[3]	1
24	uart_rx[0]	1	76	pci_lock_n		128	cpu_last_n		180	sdram_bemask_n[2]	1
25	uart_tx[0]	1	77	pci_perr_n		129	cpu_ad[2]		181	sdram_cs_n[3]	1
26	V_{cc} Core		78	V_{cc} Core		130	V_{cc} Core		182	V_{cc} Core	
27	V_{ss}		79	V_{ss}		131	V_{ss}		183	V_{ss}	
28	pci_eeprom_mdo	1	80	pci_serr_n		132	cpu_ad[29]		184	sdram_cs_n[2]	1
29	pci_eeprom_mdi	1	81	pci_par		133	cpu_buserr_n		185	sdram_cke	
30	pci_eeprom_sk	1	82	pci_cbe_n[1]		134	cpu_ad[1]		186	mem_addr[12]	1
31	sdram_addr_12	1	83	pci_ad[15]		135	cpu_ad[30]		187	mem_addr[11]	2
32	jtag_trst_n		84	pci_ad[14]		136	cpu_ale		188	mem_addr[10]	2
33	jtag_tck		85	pci_ad[13]		137	cpu_ack_n		189	mem_addr[9]	2
34	jtag_tms		86	pci_ad[12]		138	cpu_ad[0]		190	mem_addr[8]	2
35	jtag_tdo		87	pci_ad[11]		139	cpu_ad[31]		191	mem_addr[7]	2
36	V_{cc} I/O		88	V_{cc} I/O		140	V_{cc} I/O		192	V_{cc} I/O	
37	V_{ss}		89	V_{ss}		141	V_{ss}		193	V_{ss}	
38	jtag_tdi		90	pci_ad[10]		142	cpu_masterclk	1	194	mem_addr[6]	2
39	pci_gnt_n[2] (Host mode)	1	91	pci_ad[9]		143	cpu_ad[15]		195	mem_addr[5]	2
40	pci_rst_n		92	pci_ad[8]		144	cpu_ad[16]		196	mem_addr[4]	2
41	pci_clk		93	pci_cbe_n[0]		145	cpu_be_n[0]		197	mem_addr[3]	2
42	pci_gnt_n[1] (Host mode)	1	94	pci_ad[7]		146	cpu_ad[17]		198	mem_addr[2]	2
43	pci_gnt_n[0]		95	pci_ad[6]		147	cpu_ad[14]		199	sdram_ras_n	1
44	pci_req_n[1] (Host mode)	1	96	pci_ad[5]		148	cpu_be_n[1]		200	sdram_cs_n[1]	1
45	pci_req_n[0]		97	pci_ad[4]		149	cpu_ad[18]		201	sdram_cs_n[0]	1
46	V_{cc} I/O		98	V_{cc} I/O		150	V_{cc} I/O		202	V_{cc} I/O	
47	V_{ss}		99	V_{ss}		151	V_{ss}		203	V_{ss}	
48	pci_ad[31]		100	pci_ad[3]		152	cpu_ad[13]		204	sdram_bemask_n[1]	1
49	pci_ad[30]		101	pci_ad[2]		153	cpu_be_n[2]		205	sdram_bemask_n[0]	1
50	pci_ad[29]		102	pci_ad[1]		154	cpu_ad[19]		206	sdram_cas_n	
51	pci_ad[28]		103	pci_ad[0]		155	cpu_ad[12]		207	sdram_we_n	1
52	pci_ad[27]		104	cpu_int_n[3]	1	156	cpu_busgnt_n		208	sdram_245_oe_n	2

Table 3: RC32134 208-pin QFP Package Pin-Out (Page 2 of 2)

RC32134 Alternate Signal Functions

Pin	Alt #1	Alt #2	Alt #3	Pin	Alt #1	Alt #2	Alt #3
14	sdram_wait_n	edodram_wait_n	NA	169	reset_pci_host_mode	NA	NA
18	dma_done_n[1]	pio[0]	NA	179	edodram_cas_n[3]	NA	NA
19	dma_done_n[0]	pio[1]	NA	180	edodram_cas_n[2]	NA	NA
20	timer_gate_n[1]	pio[2]	NA	181	edodram_ras_n[3]	NA	NA
21	timer_gate_n[0]	pio[3]	NA	184	edodram_ras_n[2]	NA	NA
22	pio[5]	NA	NA	186	edodram_addr[12]	NA	NA
23	pio[4]	NA	NA	187	sdram_addr[11]	edodram_addr[11]	NA
24	pio[7]	NA	NA	188	sdram_addr[10]	edodram_addr[10]	NA
25	pio[6]	NA	NA	189	sdram_addr[9]	edodram_addr[9]	NA
28	pio[11]	NA	NA	190	sdram_addr[8]	edodram_addr[8]	NA
29	pio[8]	NA	NA	191	sdram_addr[7]	edodram_addr[7]	NA
30	pio[10]	NA	NA	194	sdram_addr[6]	edodram_addr[6]	NA
31	pio[9]	NA	NA	195	sdram_addr[5]	edodram_addr[5]	NA
39	pci_inta_n Satellite	NA	NA	196	sdram_addr[4]	edodram_addr[4]	NA
42	NA	pci_eeprom_cs (Satellite)	NA	197	sdram_addr[3]	edodram_addr[3]	NA
44	unused (Satellite)	NA	NA	198	sdram_addr[2]	edodram_addr[2]	NA
57	pci_idsel (Satellite)	NA	NA	199	edodram_oe_n	NA	NA
104	interrrupt_n	NA	NA	200	edodram_ras_n[1]	NA	NA
118	mem_245_dt_r_N	sdram_245_dt_r_n	edodram_245_dt_r_n	201	edodram_ras_n[0]	NA	NA
142	sdram_clk		NA	207	edodram_we_n	NA	NA
167	reset_boot_mode[1]		NA	208	edodram_245_oe_n	edodram_oe_n	NA
168	reset_boot_mode[0]		NA				

Package Drawing - 208-pin PQFP

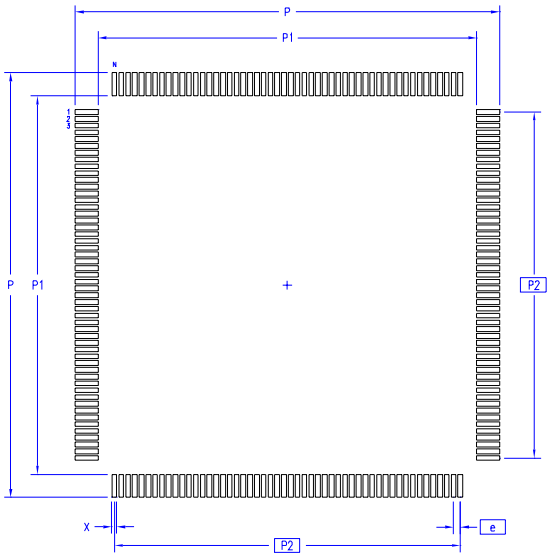


Package Drawing - page two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
29253	00	INITIAL RELEASE	08/20/96	T. VU
61476	01	ADD "DH" PACKAGE OPTION	09/20/98	T. VU
61829	02	ADD "DR" PACKAGE OPTION	01/30/99	

DWG #	DS/DH/DR208-1			
SYMBOL	JEDEC VARIATION FA-1			NOTE
	MIN	NOM	MAX	
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D	30.60 BSC			4
D1	28.00 BSC			5,2
E	30.60 BSC			4
E1	28.00 BSC			5,2
N	208			
e	.50 BSC			
b	.17	–	.27	7
b1	.17	.20	.23	
ddd	–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS | DATE
DRAWN STB 08/20/96
CHECKED

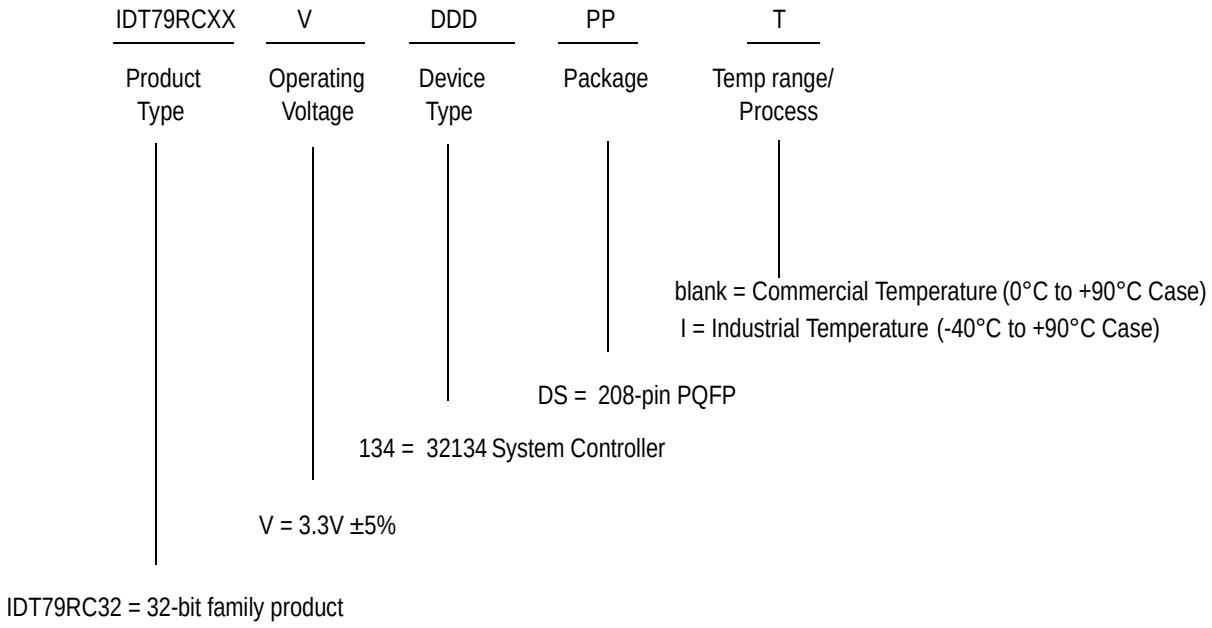
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE: DS/DH/DR PACKAGE OUTLINE
28.0 X 28.0 X 3.4 mm PQFP
1.30/.25 MIN FORM

SIZE C | DRAWING No. PSC-4059 | REV 02

DO NOT SCALE DRAWING | SHEET 2 OF 2

Ordering Information



Valid Combinations

IDT79RC32V134 DS	208-pin PQFP package - Commercial Temperature
IDT79RC32V134 DSI	208-pin PQFP package - Industrial Temperature

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