- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 34 µA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
  850 µV Max at T_A = 25°C
- **Wide Supply Voltage Range**
  2.7 V to 8 V
- **Macromodel Included**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLV2252 and TLV2254 are dual and quadruple low-voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV225x family consumes only 34 µA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. The TLV225x has a noise level of 19 nV/√Hz at 1kHz, four times lower than competitive micropower solutions.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

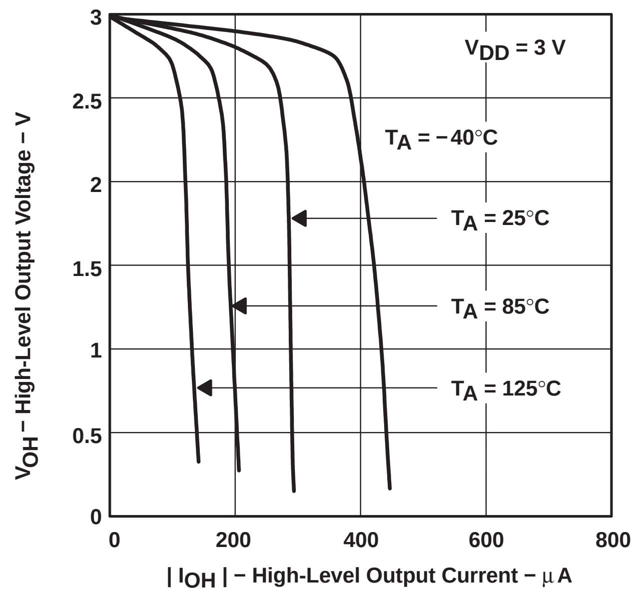


Figure 1

The TLV225x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV225xA family is available and has a maximum input offset voltage of 850 µV.

The TLV2252/4 also make great upgrades to the TLV2322/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

TLV2252 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP‡ (PW)	CERAMIC FLATPACK (U)
−40°C to 125°C	850 µV 1500 µV	TLV2252AID TLV2252ID	— —	— —	TLV2252AIP TLV2252IP	TLV2252AIPWLE —	— —
−40°C to 125°C	850 µV 1500 µV	TLV2252AQD TLV2252QD	— —	— —	— —	— —	— —
−55°C to 125°C	850 µV 1500 µV	— —	TLV2252AMFK TLV2252MFK	TLV2252AMJG TLV2252MJG	— —	— —	TLV2252AMU TLV2252MU

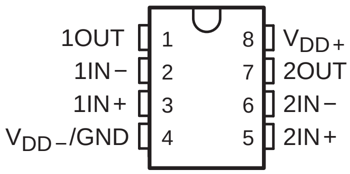
† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2252CDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.

TLV2254 AVAILABLE OPTIONS

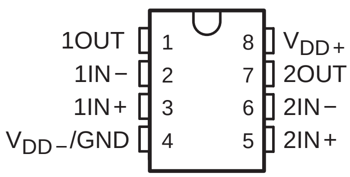
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP‡ (PW)	CERAMIC FLATPACK (W)
−40°C to 125°C	850 µV 1500 µV	TLV2254AID TLV2254ID	— —	— —	TLV2254AIN TLV2254IN	TLV2254AIPWLE —	— —
−40°C to 125°C	850 µV 1500 µV	TLV2254AQD TLV2254QD	— —	— —	— —	— —	— —
−55°C to 125°C	850 µV 1500 µV	— —	TLV2254AMFK TLV2254MFK	TLV2254AMJ TLV2254MJ	— —	— —	TLV2254AMW TLV2254MW

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2254CDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.

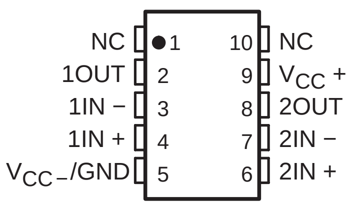
TLV2252I, TLV2252AI
TLV2252Q, TLV2252AQ
D, P, OR PW PACKAGE
(TOP VIEW)



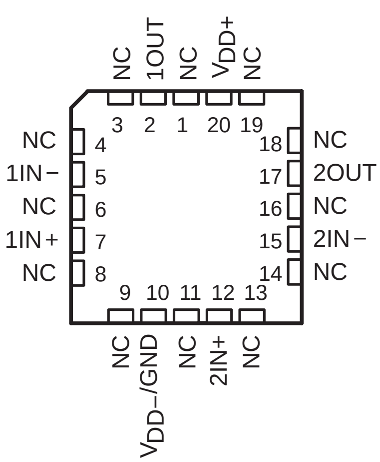
TLV2252M, TLV2252AM . . . JG PACKAGE
(TOP VIEW)



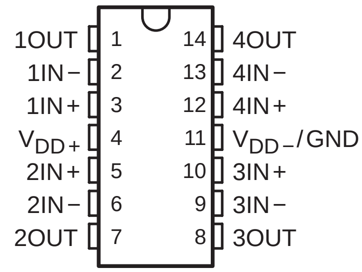
TLV2252M, TLV2252AM . . . U PACKAGE
(TOP VIEW)



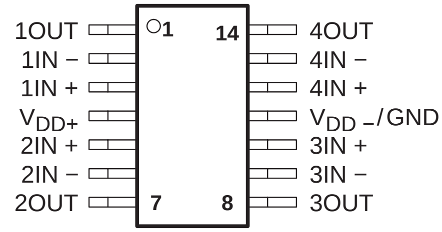
TLV2252M, TLV2252AM . . . FK PACKAGE
(TOP VIEW)



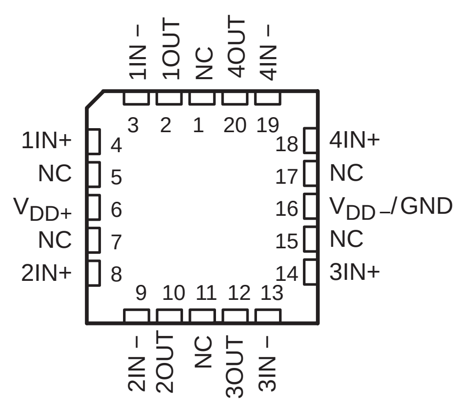
TLV2254I, TLV2254AI, TLV2254Q, TLV2254AQ . . . D OR N PACKAGE
TLV2254M, TLV2254AM . . . J OR W PACKAGE
(TOP VIEW)



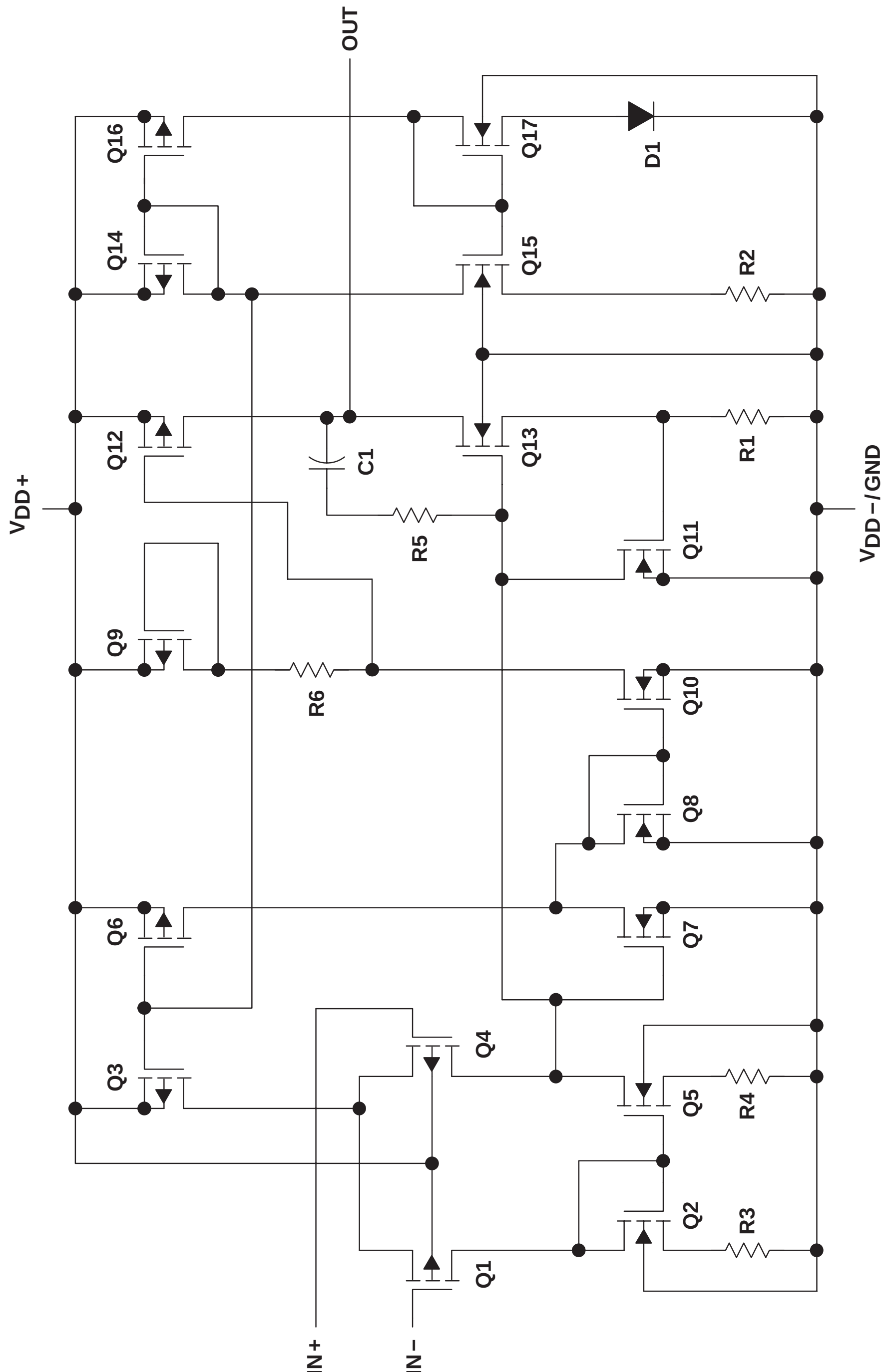
TLV2254I, TLV2254AI . . . PW PACKAGE
(TOP VIEW)



TLV2254M, TLV2254AM . . . FK PACKAGE
(TOP VIEW)



equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLV2252	TLV2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 16 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . . . $V_{DD-} - 0.3$ V to V_{DD+}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: I Suffix . . . . . −40°C to 125°C
Q Suffix . . . . . −40°C to 125°C
M Suffix . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, and PW packages . . . . . 260°C
J, JG, U, and W packages . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D−8	725 mW	5.8 mW/°C	377 mW	145 mW
D−14	950 mW	7.6 mW/°C	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
J	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
N	1150 mW	9.2 mW/°C	598 mW	230 mW
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW−8	525 mW	4.2 mW/°C	273 mW	105 mW
PW−14	700 mW	5.6 mW/°C	364 mW	140 mW
U	700 mW	5.5 mW/°C	370 mW	150 mW
W	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

	TLV225xI		TLV225xQ		TLV225xM		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	8	2.7	8	2.7	8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	−40	125	−40	125	−55	125	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

TLV2252I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2252I			TLV2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\|$ ≤5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.98			2.98		V
		I_{OH} = −75 μA		25°C	2.9			2.9			
				Full range	2.8			2.8			
		I_{OH} = −150 μA		25°C	2.8			2.8			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
				Full range			80			80	
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 100 kΩ‡	25°C	100	250		100	250		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		800			800		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			

† Full range is − 40°C to 125°C.
‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2252I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2252I			TLV2252AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		68	125		68	125	μA
			Full range			150			150	

† Full range is − 40°C to 125°C.

TLV2252I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	T_A†	TLV2252I			TLV2252AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, R_L = 100 kΩ‡, C_L = 100 pF‡	25°C	0.07	0.1		0.07	0.1		V/μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		35			35		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA /√Hz
	Gain-bandwidth product	f = 1 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		0.187			0.187		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		60			60		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is −40°C to 125°C.
‡ Referenced to 1.5 V

TLV2252I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2252I MIN	TLV2252I TYP	TLV2252I MAX	TLV2252AI MIN	TLV2252AI TYP	TLV2252AI MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.98			4.98		V
		I_{OH} = −75 μA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 μA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
				Full range			0.06			0.06	
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2252I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2252I			TLV2252AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		70	125		70	125	μA
			Full range			150			150	

† Full range is − 40°C to 125°C.

TLV2252I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2252I			TLV2252AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, R_L = 100 kΩ‡, C_L = 100 pF‡		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡		25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V

TLV2254I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254I			TLV2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\|$ ≤5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.98			2.98		V
		I_{OH} = −75 µA		25°C	2.9			2.9			
				Full range	2.8			2.8			
		I_{OH} = −150 µA		25°C	2.8			2.8			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		10			10		mV
				Full range			80			80	
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 100 kΩ‡	25°C	100	225		100	225		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		800			800		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	65	75		65	77		dB
				Full range	60			60			

† Full range is − 40°C to 125°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2254I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2254I			TLV2254AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	100		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V, No load	25°C		135	250		135	250	μA
			Full range			300			300	

† Full range is − 40°C to 125°C.

TLV2254I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	T_A†	TLV2254I			TLV2254AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.7 V to 1.7 V, R_L = 100 kΩ‡, C_L = 100 pF‡	25°C	0.07	0.1		0.07	0.1		V/μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		35			35		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 1 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		0.187			0.187		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		60			60		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is − 40°C to 85°C.
‡ Referenced to 1.5 V

TLV2254I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254I MIN	TLV2254I TYP	TLV2254I MAX	TLV2254AI MIN	TLV2254AI TYP	TLV2254AI MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				−40°C to 85°C			150			150	
				Full range			1000			1000	
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO} \rvert$ ≤5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.98			4.98		V
		I_{OH} = −75 μA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 μA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
				Full range			0.06			0.06	
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2254I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2254I			TLV2254AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V, No load	25°C		140	250		140	250	µA
			Full range			300			300	

† Full range is − 40°C to 125°C.

TLV2254I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2254I			TLV2254AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 100 kΩ‡,	25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA /√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V

TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			1000			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω, $\|V_{IO}\|$ ≤5 mV		25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.98			2.98		V
		I_{OH} = −75 µA		25°C	2.9			2.9			
				Full range	2.8			2.8			
		I_{OH} = −150 µA		25°C	2.8			2.8			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_{OL} = 50 µA		25°C		10			10		mV
		V_{IC} = 1.5 V, I_{OL} = 500 µA		25°C		100	150		100	150	
				Full range			165			165	
		V_{IC} = 1.5 V, I_{OL} = 1 mA		25°C		200	300		200	300	
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 100 kΩ‡	25°C	100	250		100	250		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		800			800		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz, P package		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz, A_V = 10		25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		80	100		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V, No load		25°C		68	125		68	125	µA
				Full range			150			150	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2252Q, and TLV2252M operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	T_A†	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.8 V to 1.4 V, R_L = 100 kΩ‡, C_L = 100 pF‡	25°C	0.07	0.1		0.07	0.1		V/μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		35			35		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 1 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		0.187			0.187		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		60			60		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			1000			1000	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.98			4.98		V
		I_{OH} = −75 μA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 μA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2252Q, and TLV2252M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		70	125		70	125	μA
			Full range			150			150	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2252Q, and TLV2252M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2252Q, TLV2252M			TLV2252AQ, TLV2252AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.25 V to 2.75 V, R_L = 100 kΩ‡, C_L = 100 pF‡		25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	µV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			1000			1000	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\|V_{IO}\|$ ≤5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.98			2.98		V
		I_{OH} = −75 µA		25°C	2.9			2.9			
				Full range	2.8			2.8			
		I_{OH} = −150 µA		25°C	2.8			2.8			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		100	150		100	150	
				Full range			165			165	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200	300		200	300	
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 100 kΩ‡	25°C	100	225		100	225		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		800			800		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V,	No load	25°C		135	250		135	250	µA
				Full range			300			300	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2254Q, and TLV2254M operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS	T_A†	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 1.7 V, R_L = 100 kΩ‡, C_L = 100 pF‡	25°C	0.07	0.1		0.07	0.1		V/µs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		35			35		nV/√Hz
		f = 1 kHz	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		0.6			0.6		µV
		f = 0.1 Hz to 10 Hz	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 1 kHz, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		0.187			0.187		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, A_V = 1, R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		60			60		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡, C_L = 100 pF‡	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		200	1500		200	850	μV
				Full range			1750			1000	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			1000			1000	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			1000			1000	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.98			4.98		V
		I_{OH} = −75 μA		25°C	4.9	4.94		4.9	4.94		
				Full range	4.8			4.8			
		I_{OH} = −150 μA		25°C	4.8	4.88		4.8	4.88		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 100 kΩ‡	25°C	100	350		100	350		V/mV
				Full range	10			10			
			R_L = 1 MΩ‡	25°C		1700			1700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 25 kHz,	A_V = 10	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 2.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2254Q, and TLV2254M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		140	250		140	250	µA
				Full range			300			300	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2254Q, and TLV2254M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2254Q, TLV2254M			TLV2254AQ, TLV2254AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 100 kΩ‡,	25°C	0.07	0.12		0.07	0.12		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		36			36		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.2%			0.2%		
			A_V = 10			1%			1%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

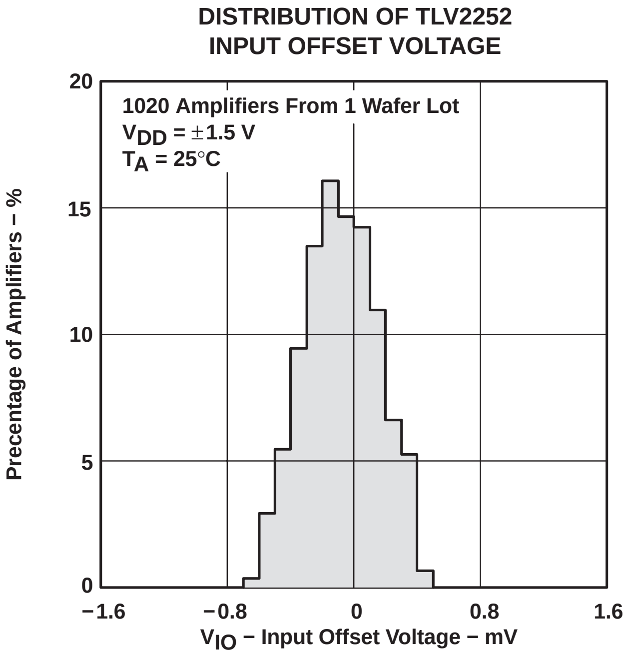


Figure 2

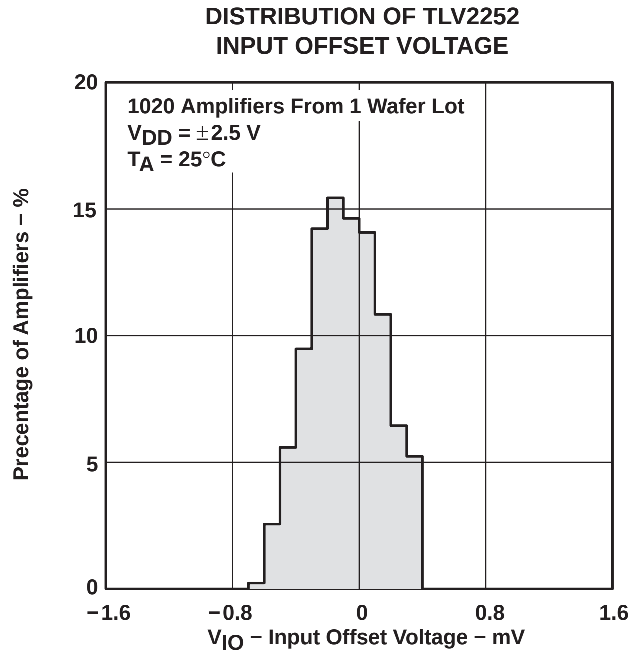


Figure 3

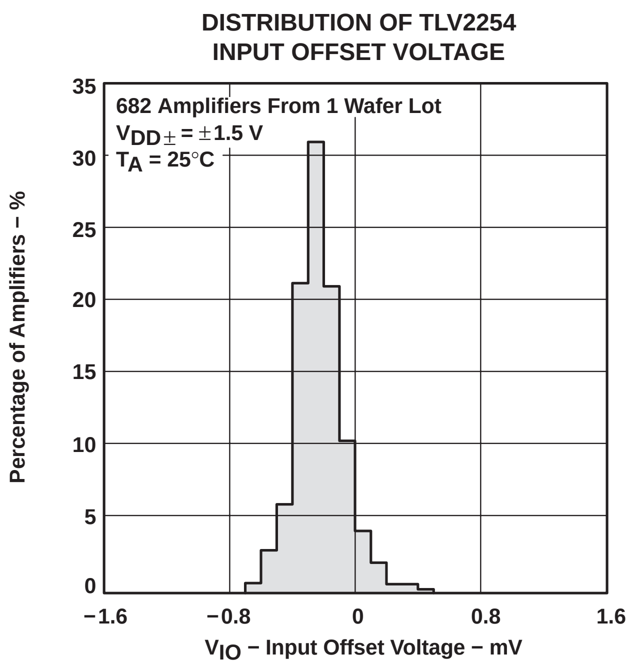


Figure 4

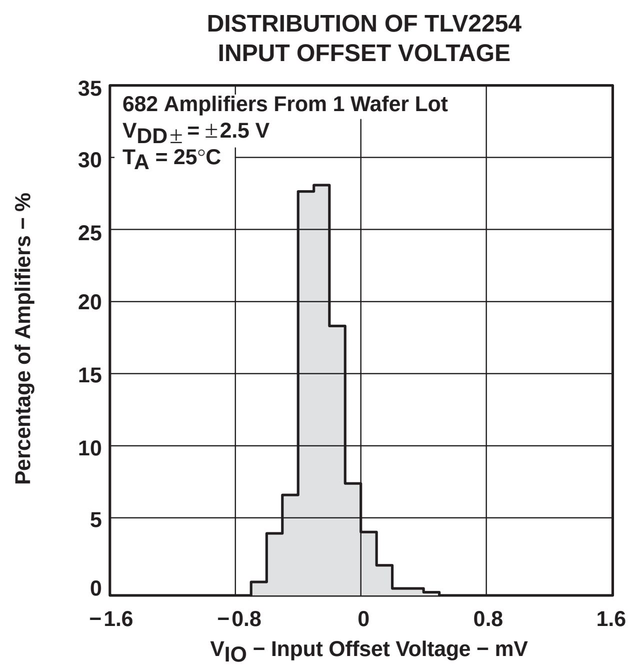


Figure 5

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE

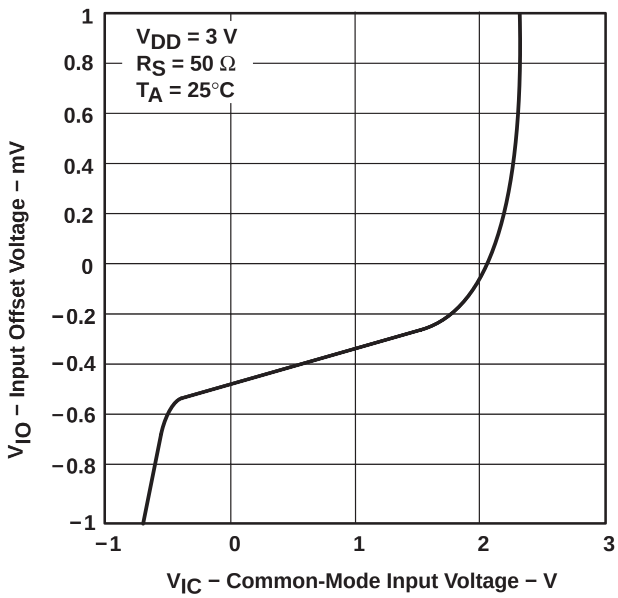


Figure 6

INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE

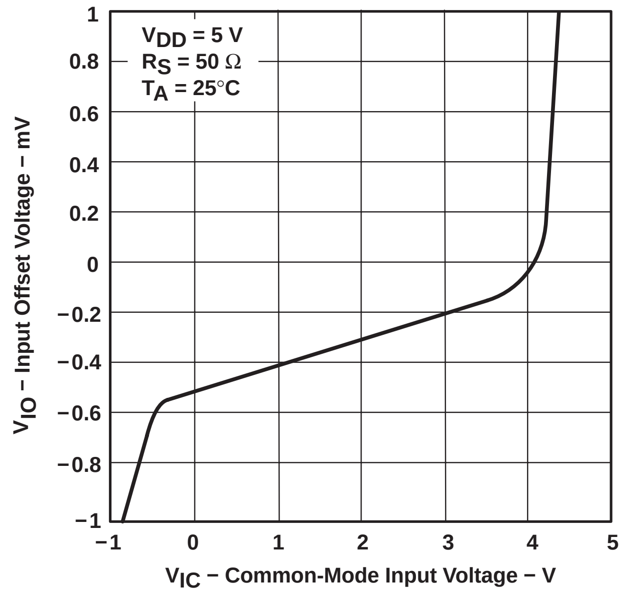


Figure 7

DISTRIBUTION OF TLV2252 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

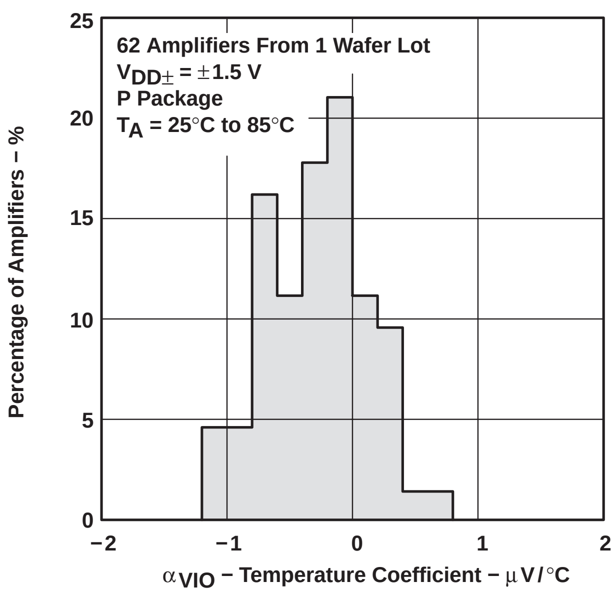


Figure 8

DISTRIBUTION OF TLV2252 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

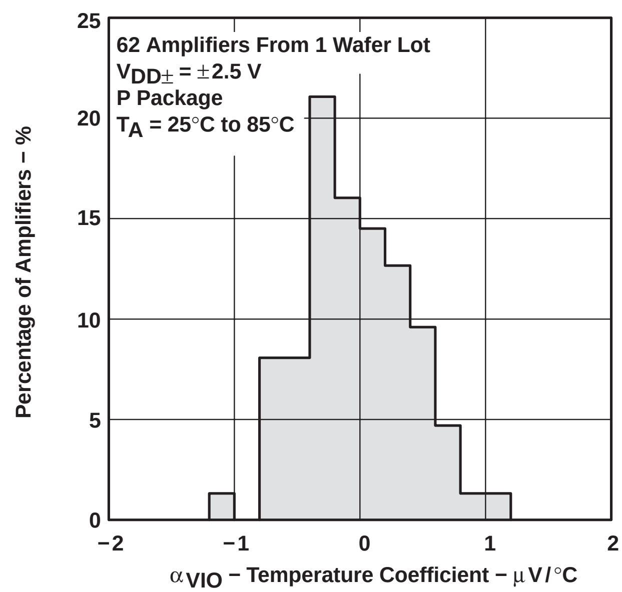


Figure 9

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

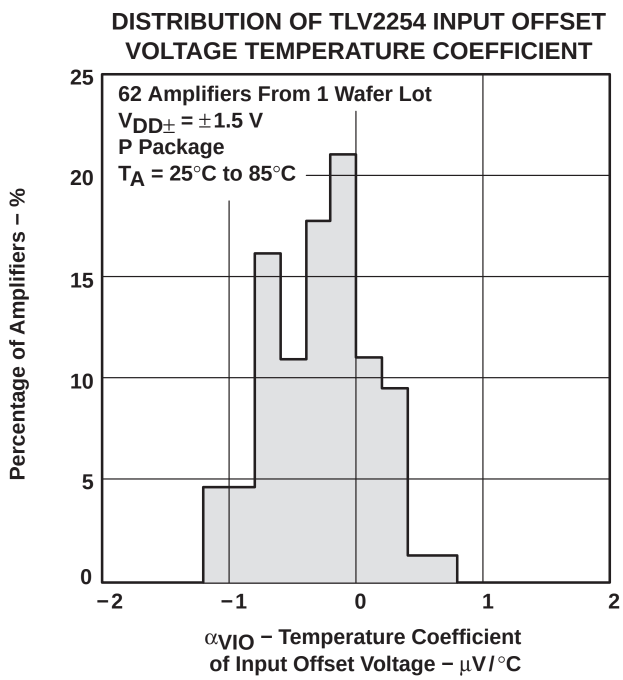


Figure 10

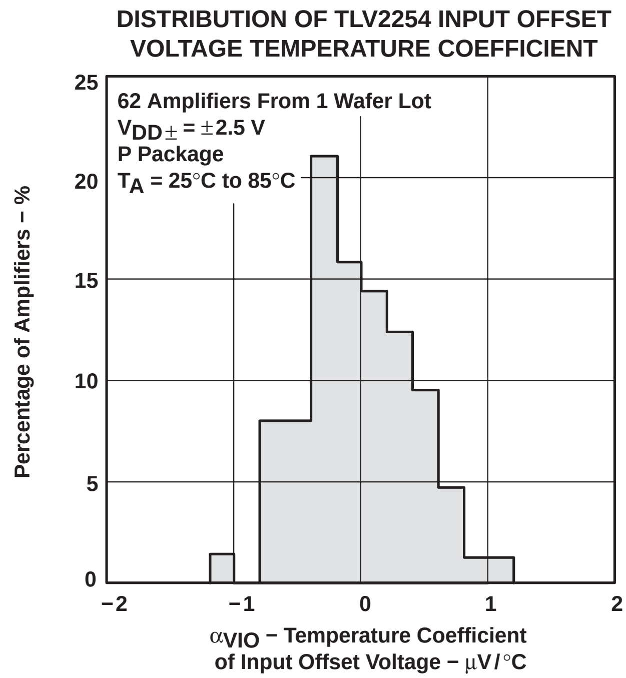


Figure 11

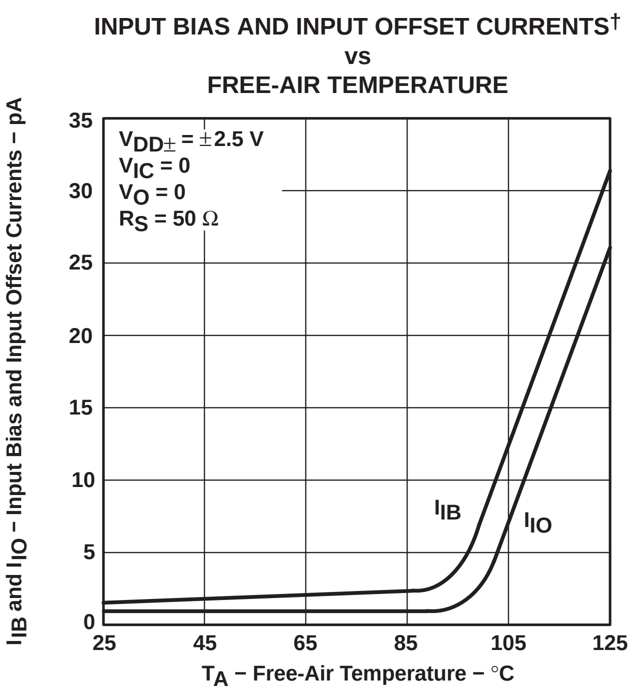


Figure 12

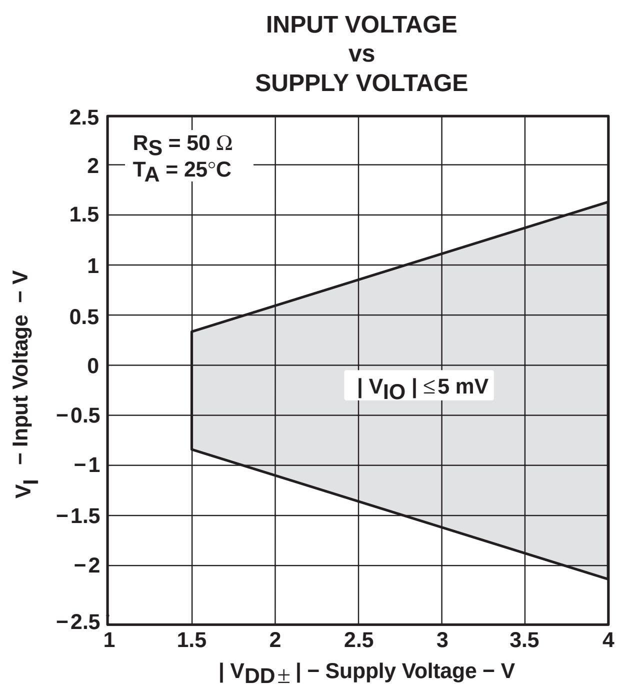


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE†‡
vs
FREE-AIR TEMPERATURE

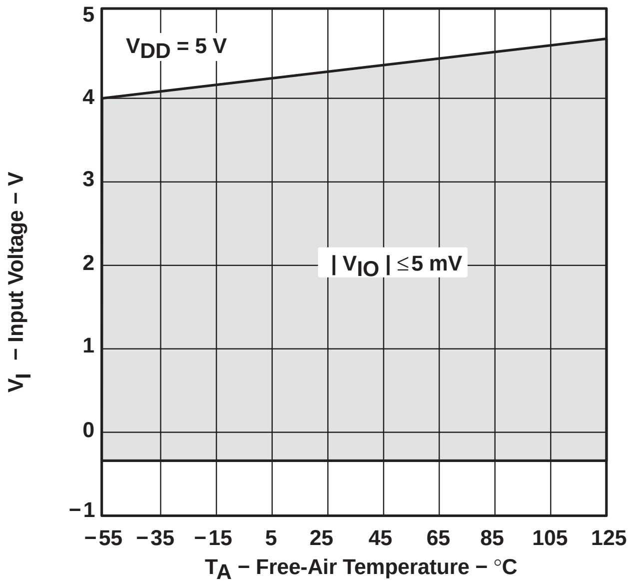


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

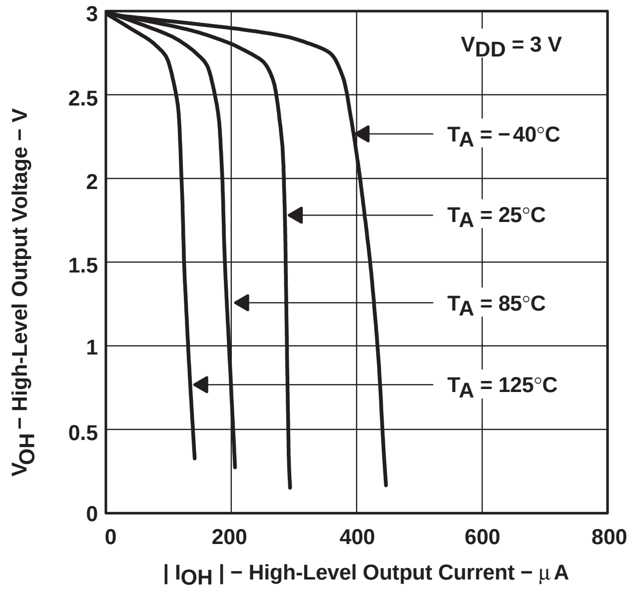


Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

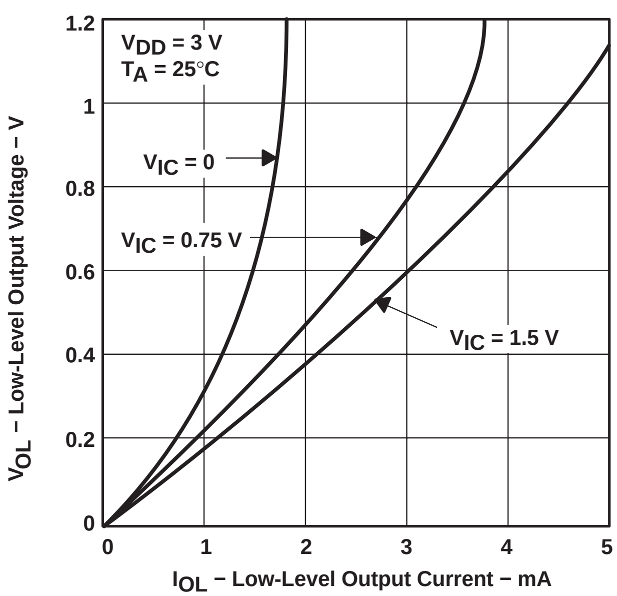


Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

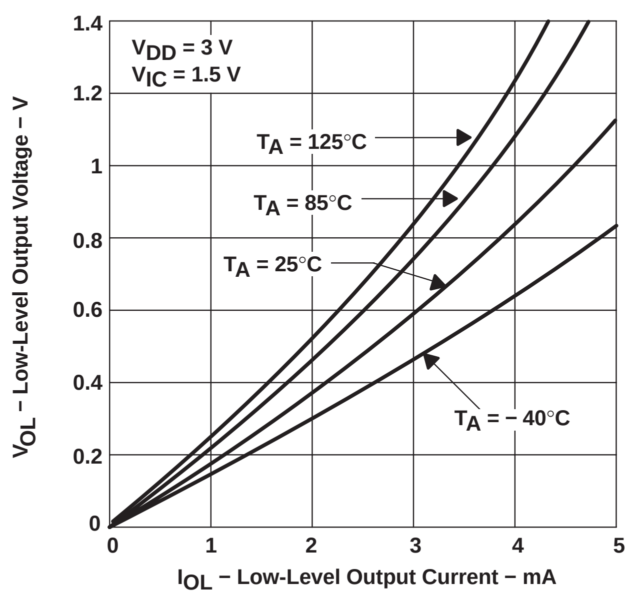


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT

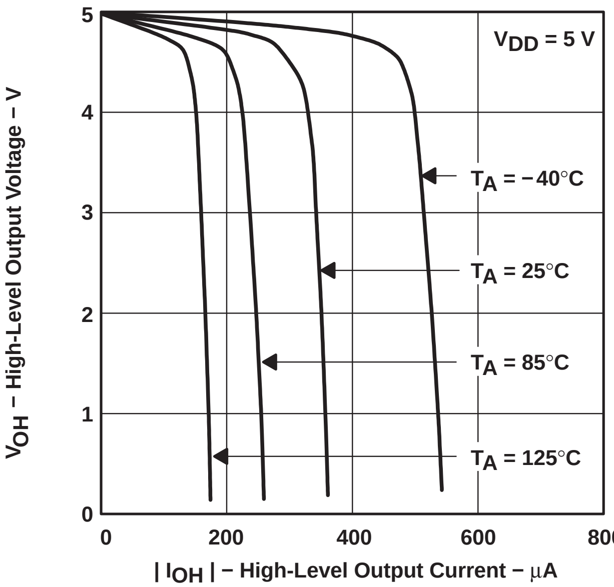


Figure 18

LOW-LEVEL OUTPUT VOLTAGE†‡ vs LOW-LEVEL OUTPUT CURRENT

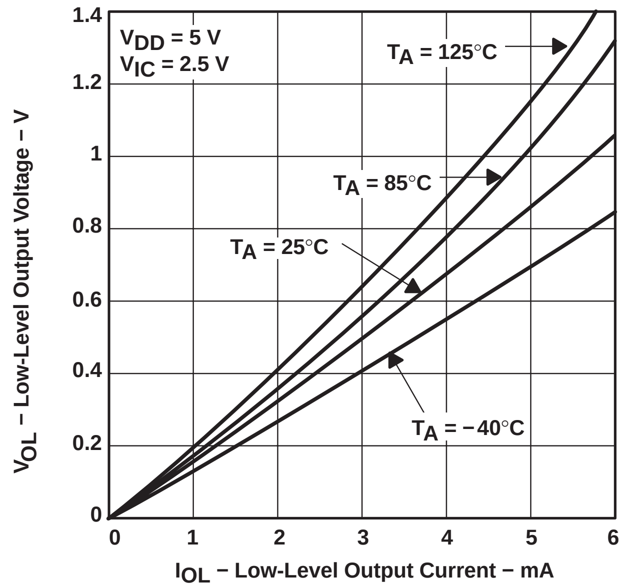


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡ vs FREQUENCY

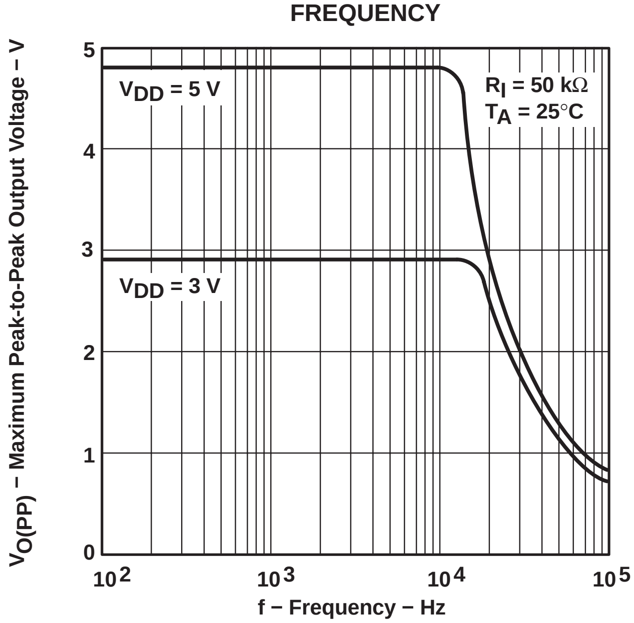


Figure 20

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

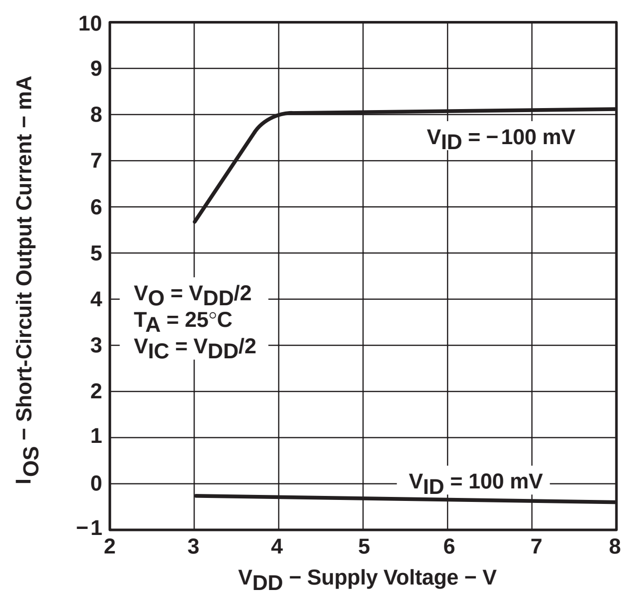


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†
vs
FREE-AIR TEMPERATURE

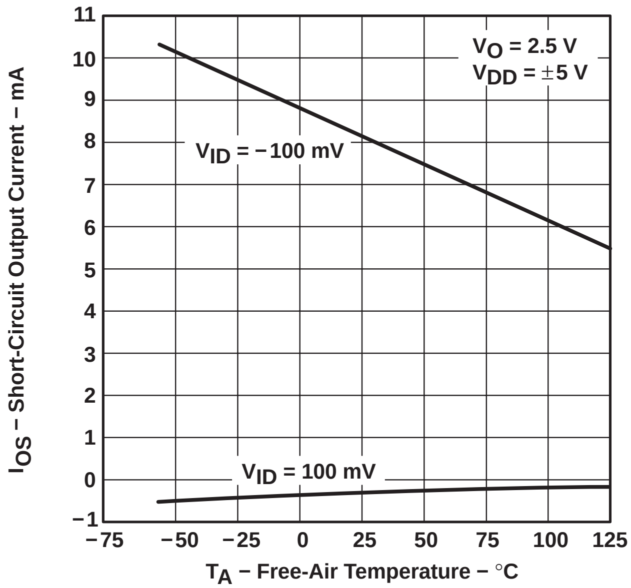


Figure 22

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

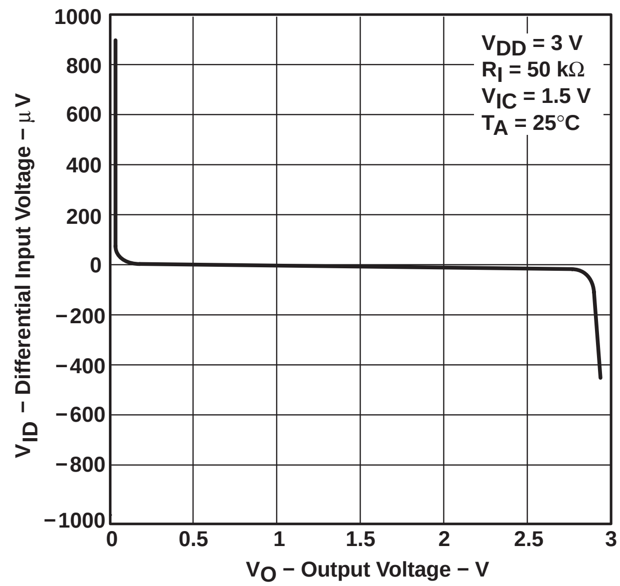


Figure 23

DIFFERENTIAL INPUT VOLTAGE‡
vs
OUTPUT VOLTAGE

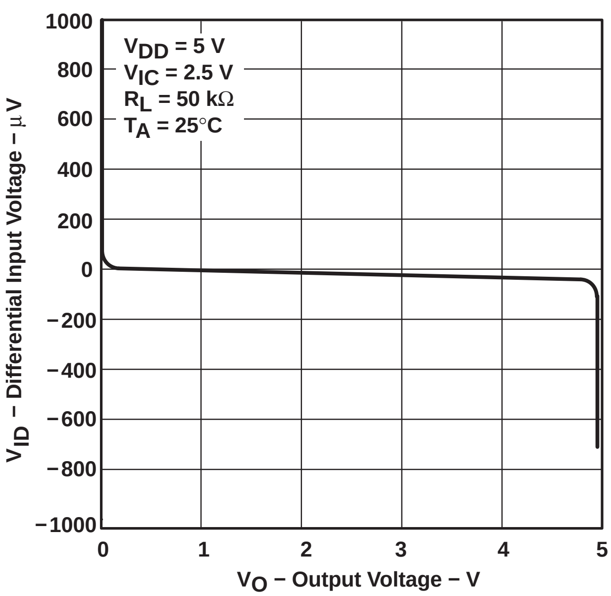


Figure 24

DIFFERENTIAL VOLTAGE AMPLIFICATION†‡
vs
LOAD RESISTANCE

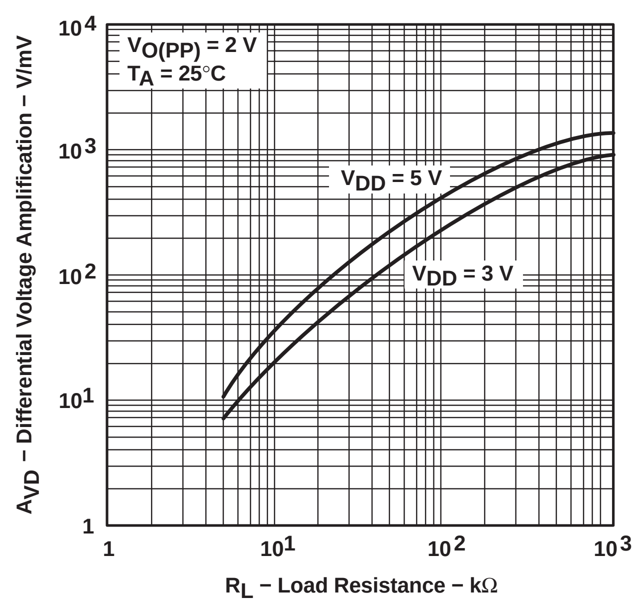


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

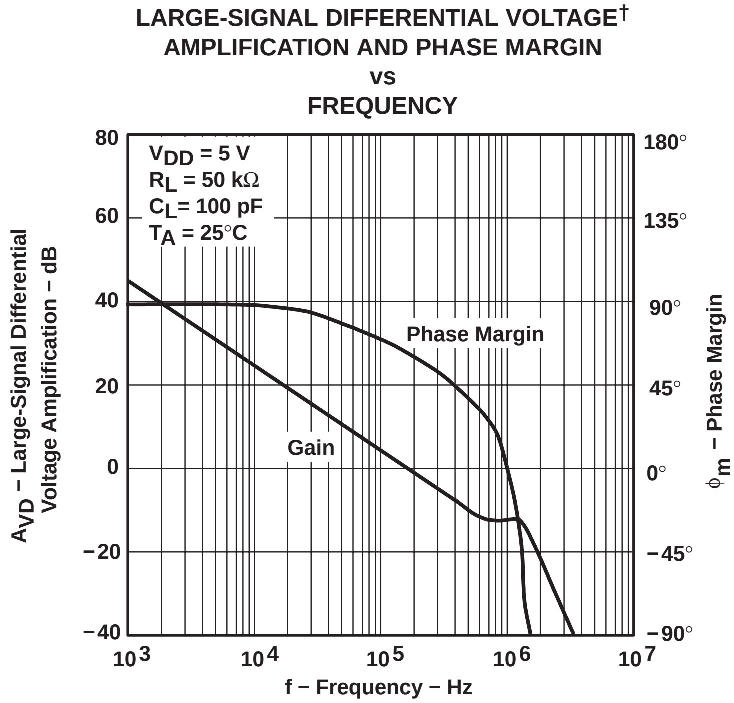


Figure 26

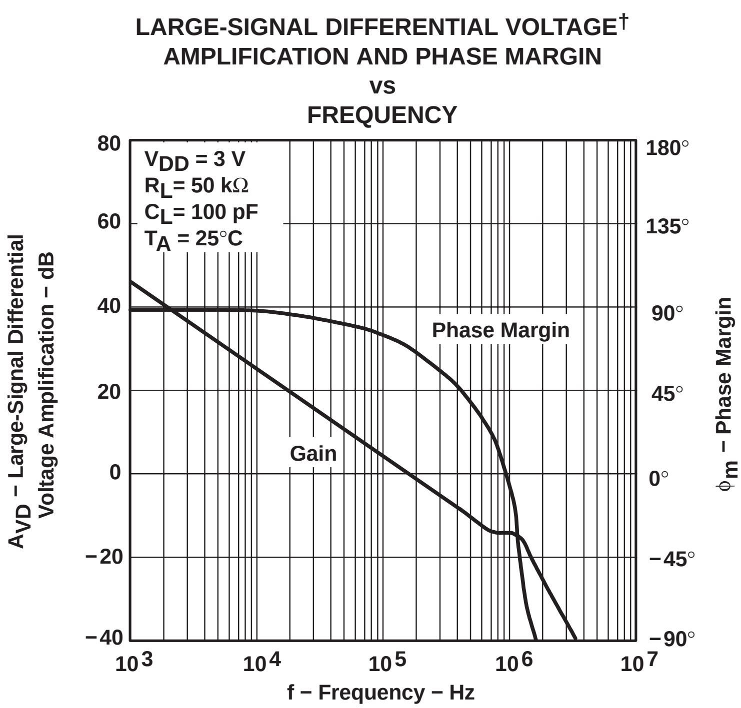


Figure 27

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE†‡

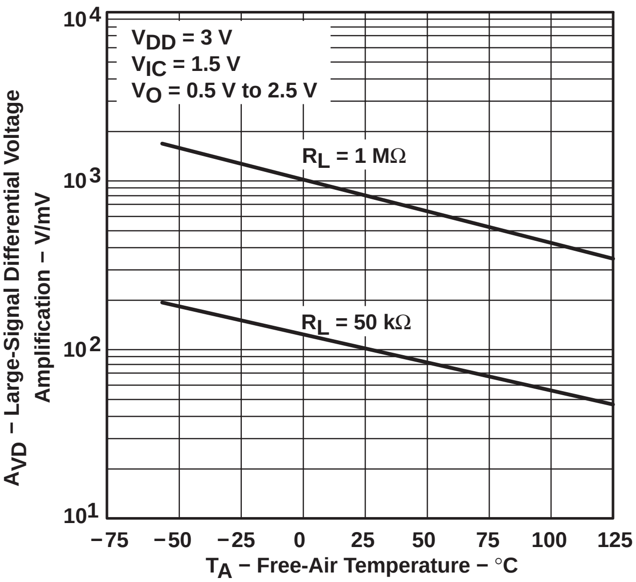


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE†‡

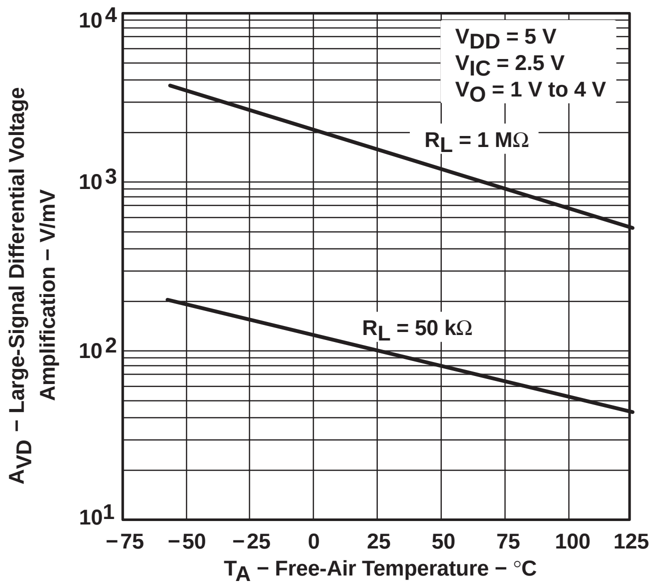


Figure 29

OUTPUT IMPEDANCE‡ vs FREQUENCY

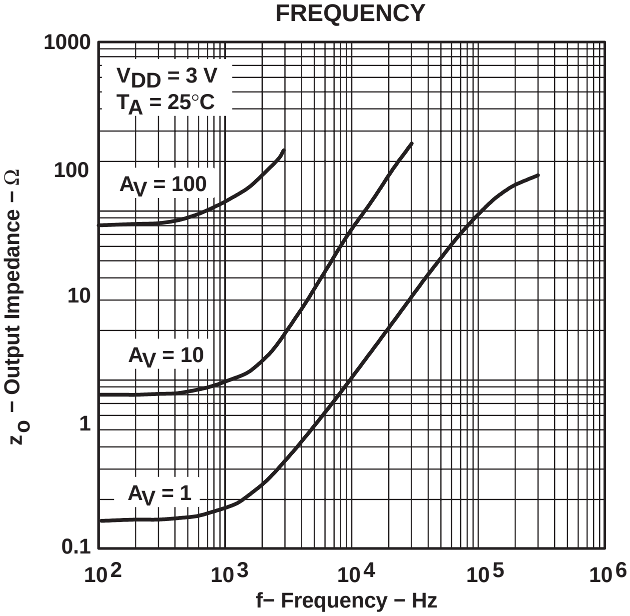


Figure 30

OUTPUT IMPEDANCE‡ vs FREQUENCY

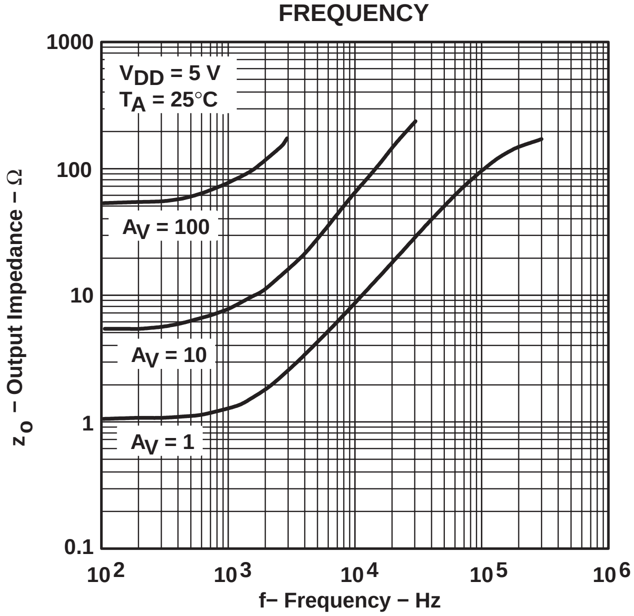


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO† vs FREQUENCY

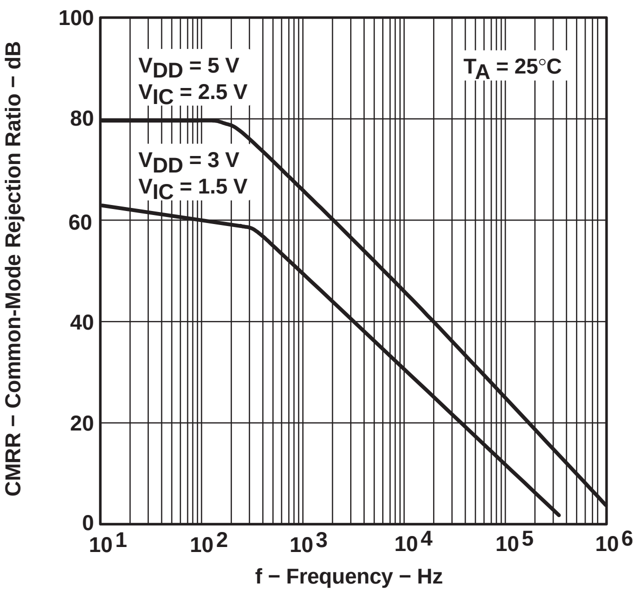


Figure 32

COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE

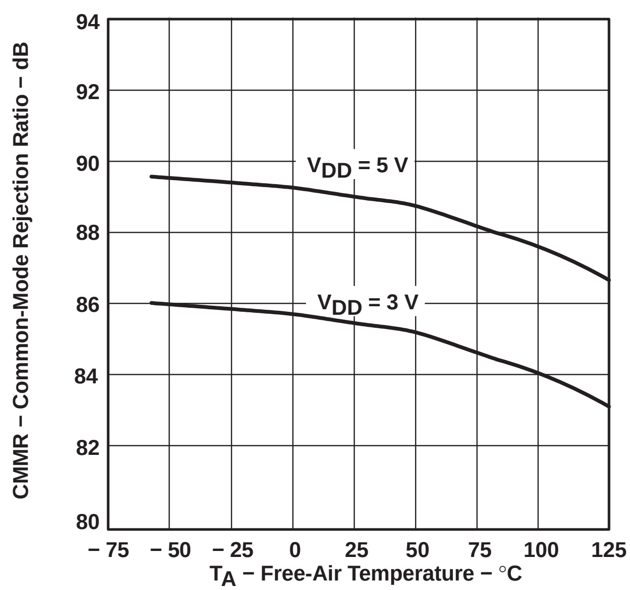


Figure 33

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

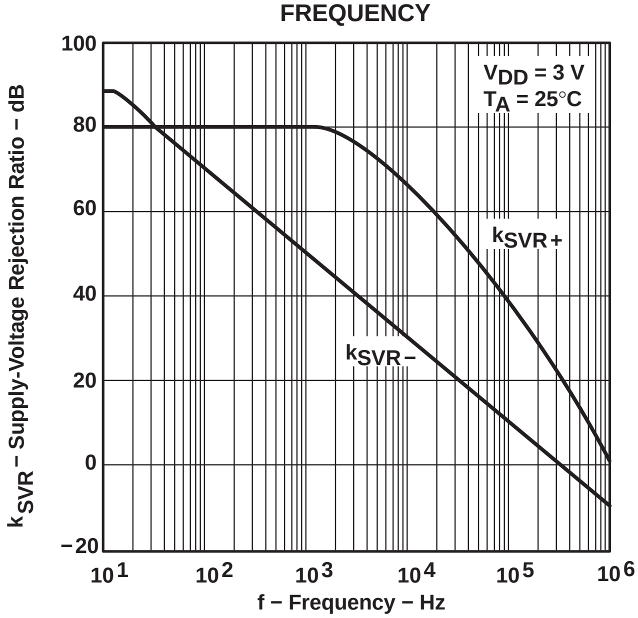


Figure 34

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

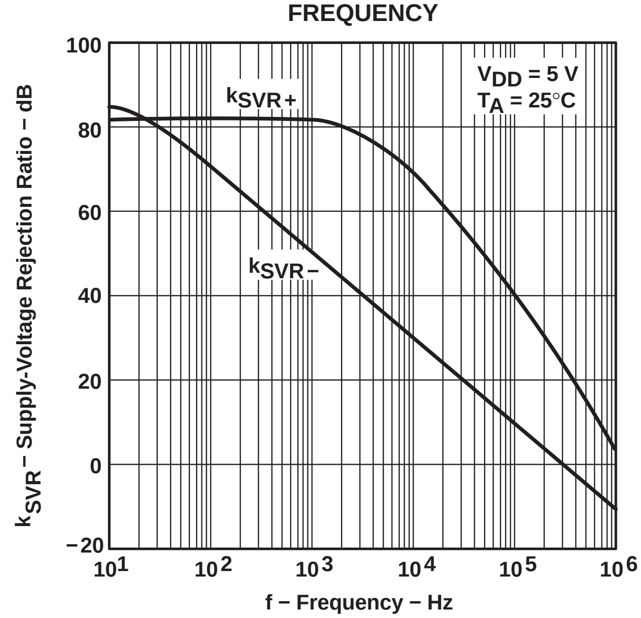


Figure 35

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

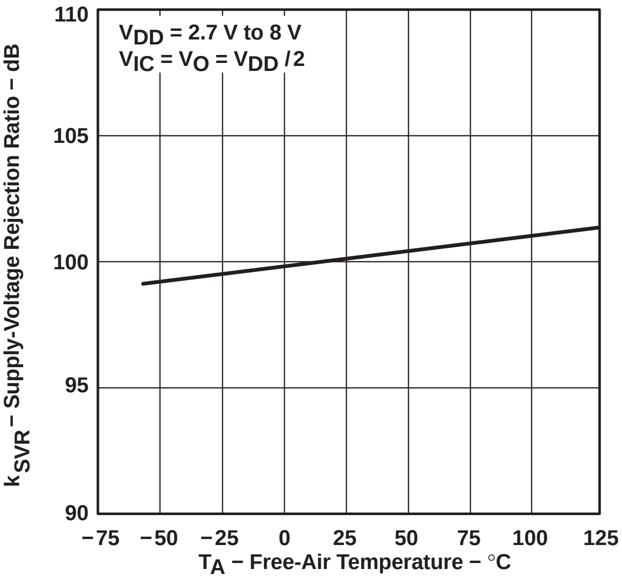


Figure 36

TLV2252
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

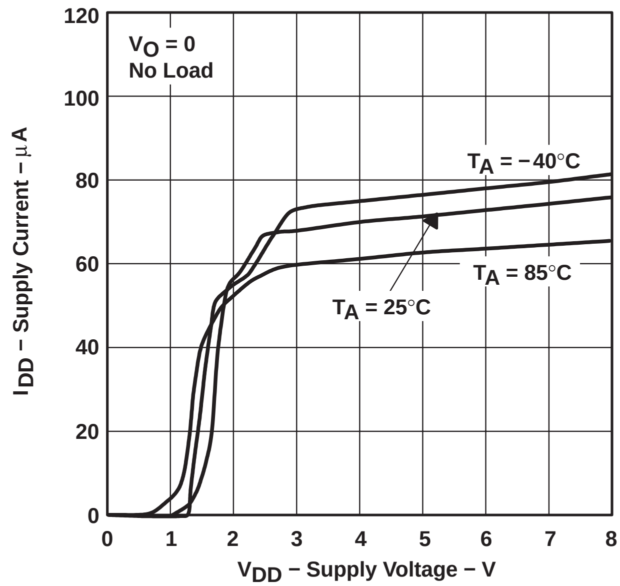


Figure 37

TLV2254
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

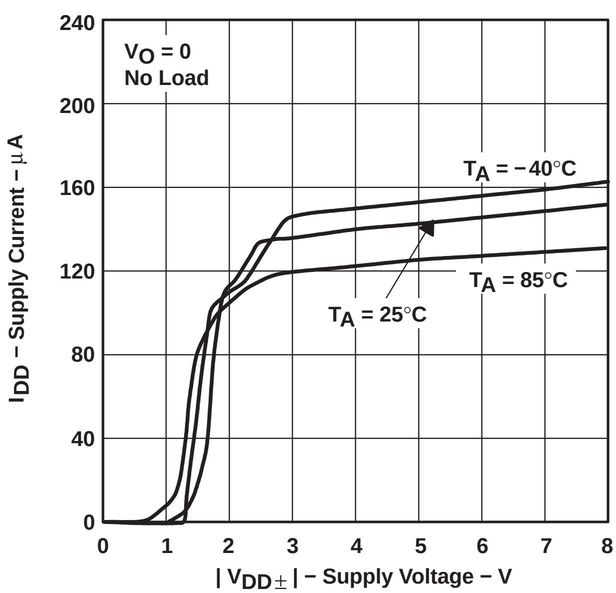


Figure 38

SLEW RATE‡
vs
LOAD CAPACITANCE

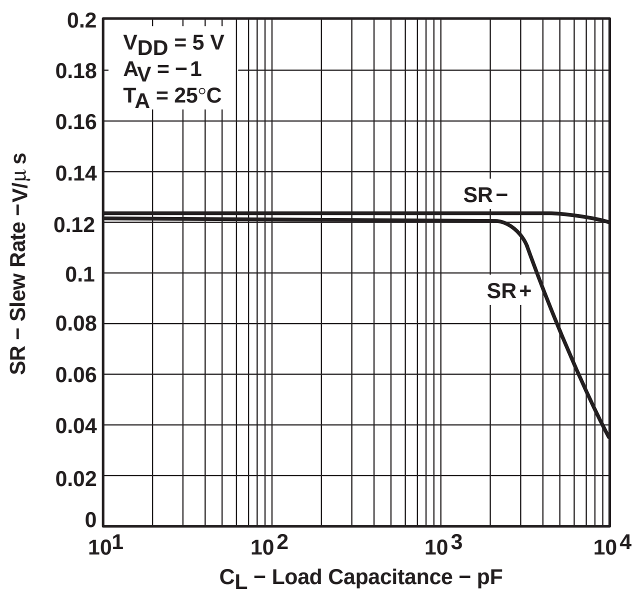


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SLEW RATE†‡ vs FREE-AIR TEMPERATURE

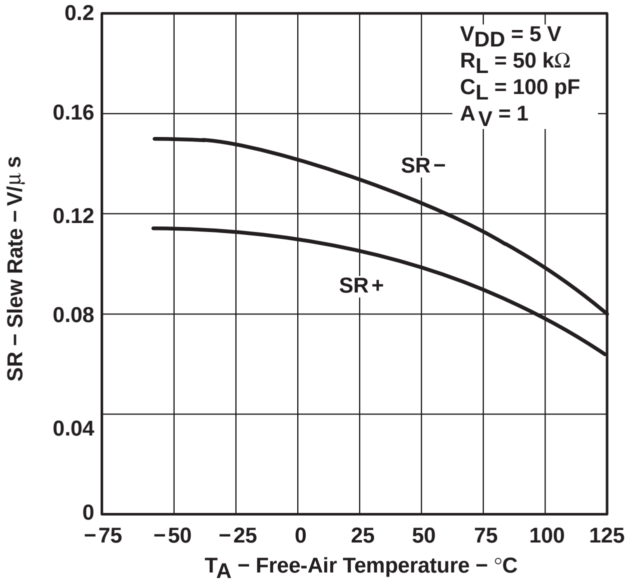


Figure 40

INVERTING LARGE-SIGNAL PULSE RESPONSE†

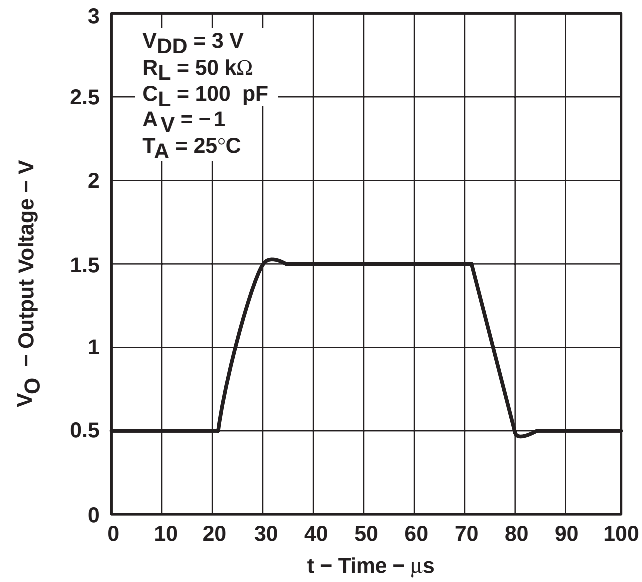


Figure 41

INVERTING LARGE-SIGNAL PULSE RESPONSE†

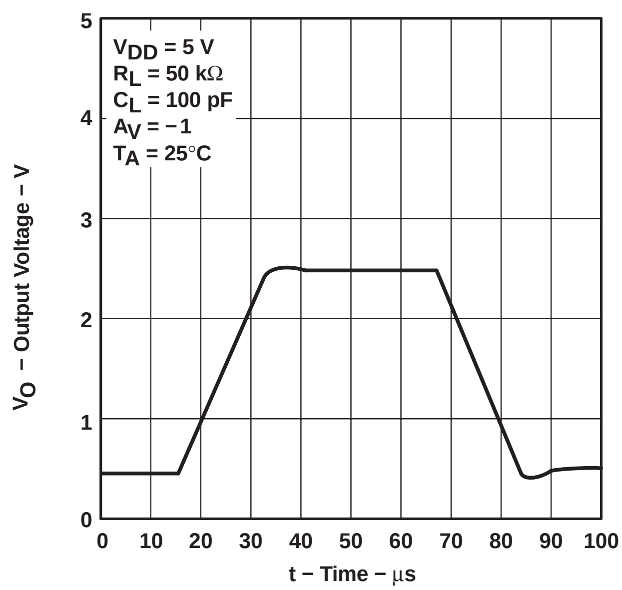


Figure 42

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

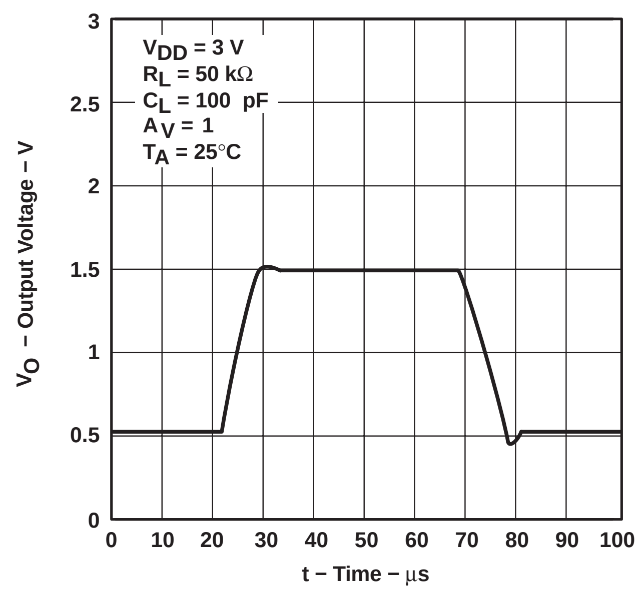


Figure 43

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

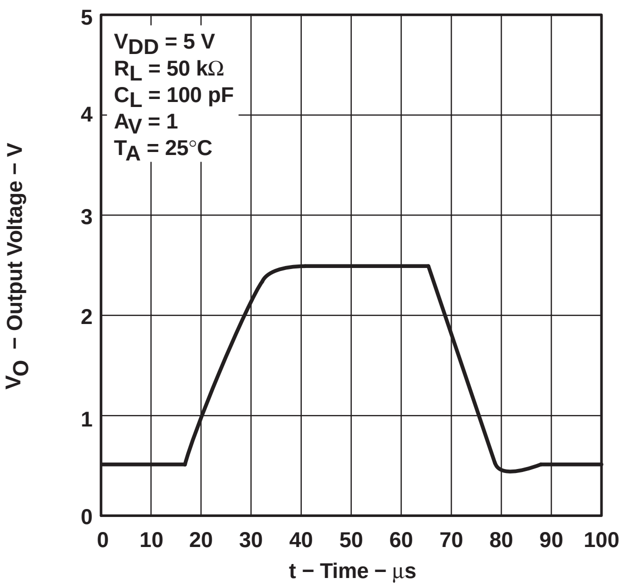


Figure 44

INVERTING SMALL-SIGNAL PULSE RESPONSE†

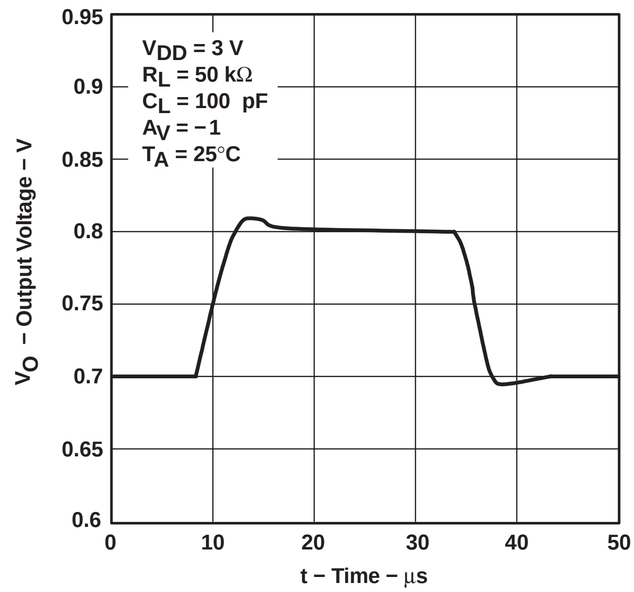


Figure 45

INVERTING SMALL-SIGNAL PULSE RESPONSE†

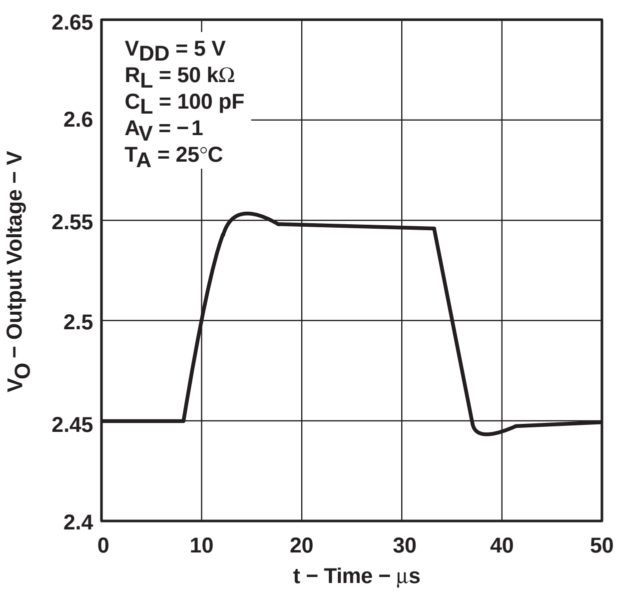


Figure 46

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

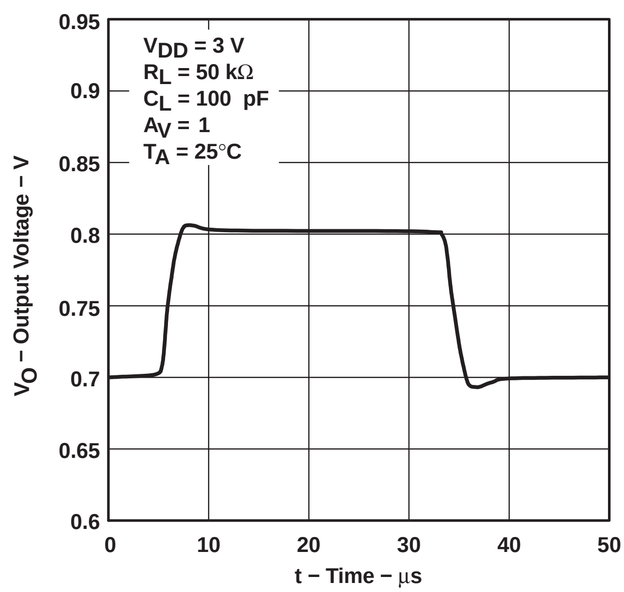


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

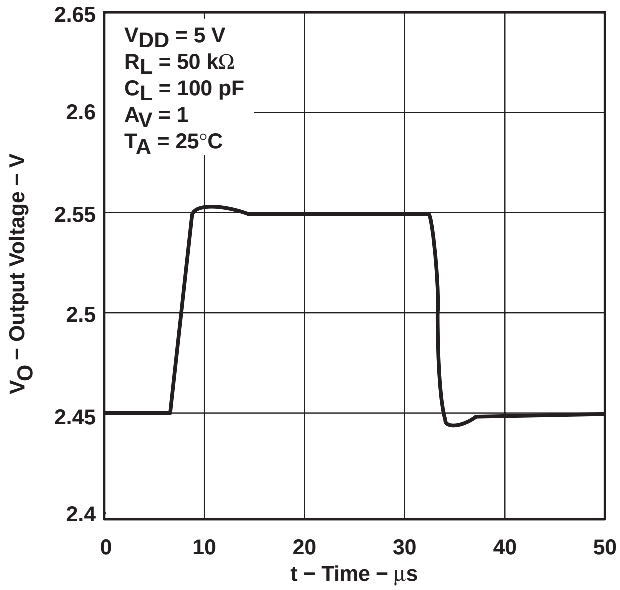


Figure 48

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

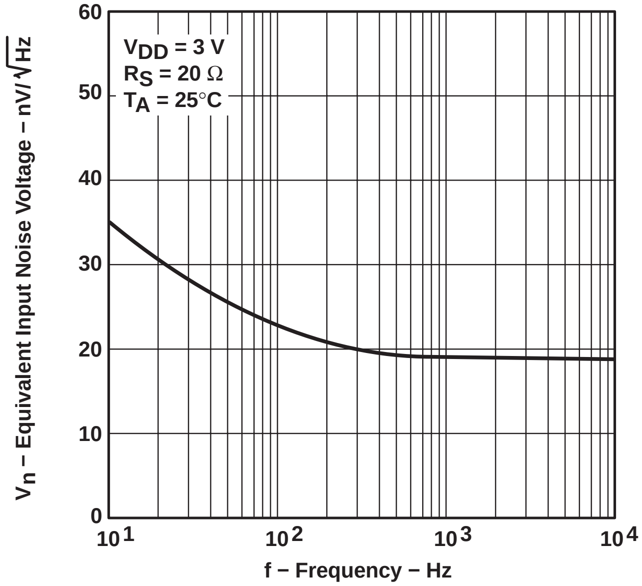


Figure 49

EQUIVALENT INPUT NOISE VOLTAGE† vs FREQUENCY

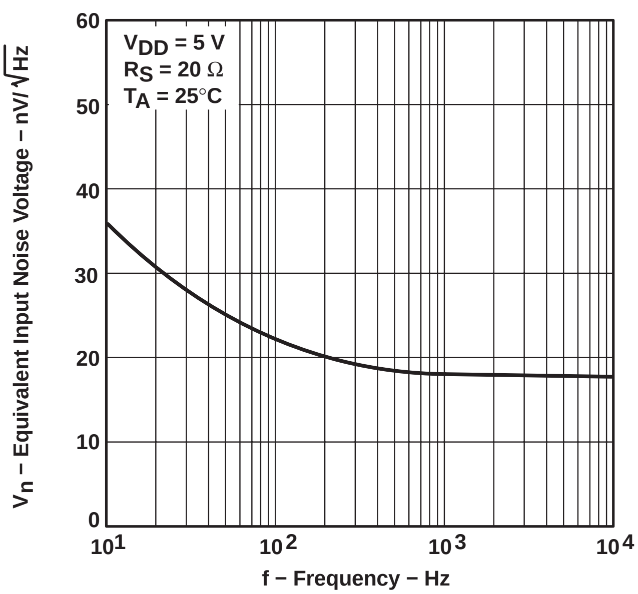


Figure 50

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD†

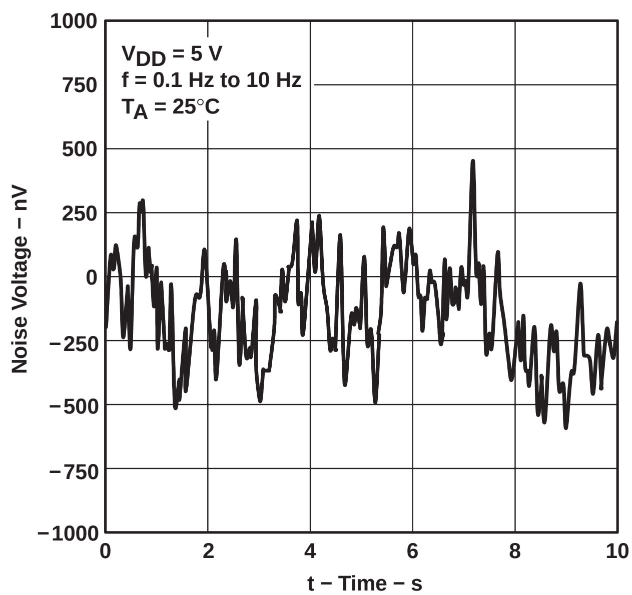


Figure 51

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INTEGRATED NOISE VOLTAGE†
vs
FREQUENCY

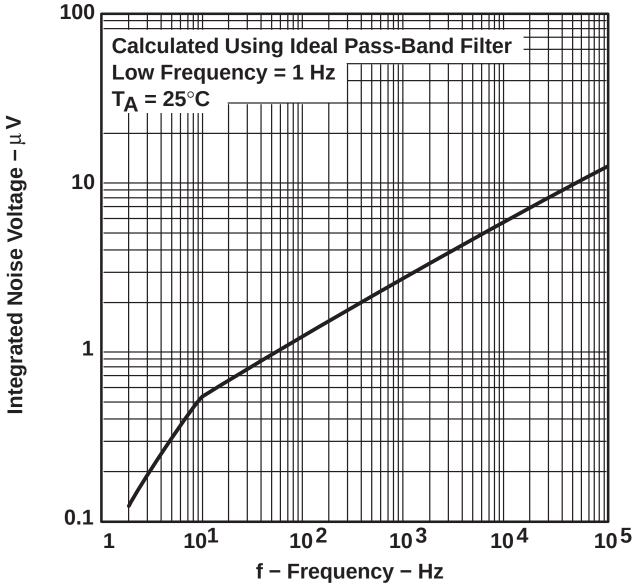


Figure 52

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY

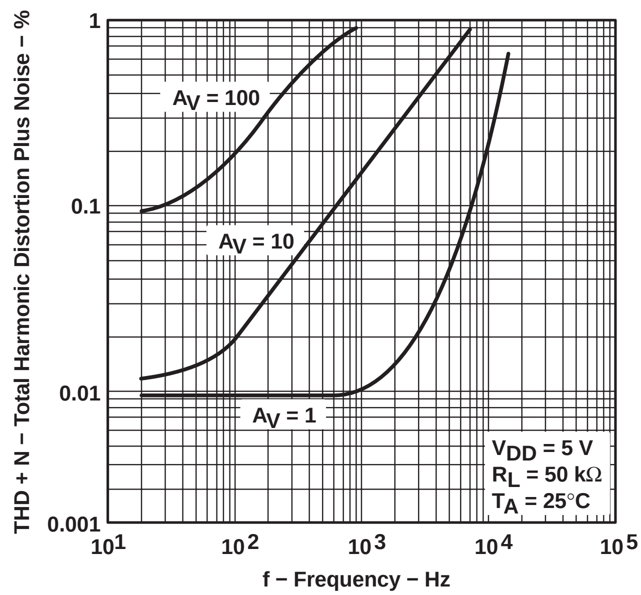


Figure 53

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

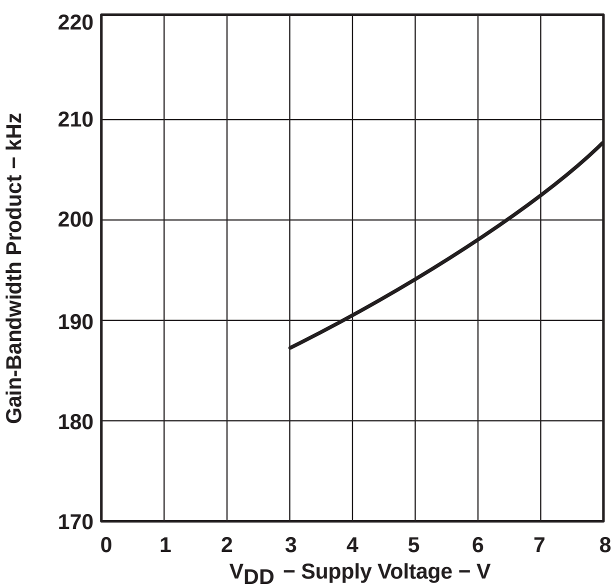


Figure 54

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

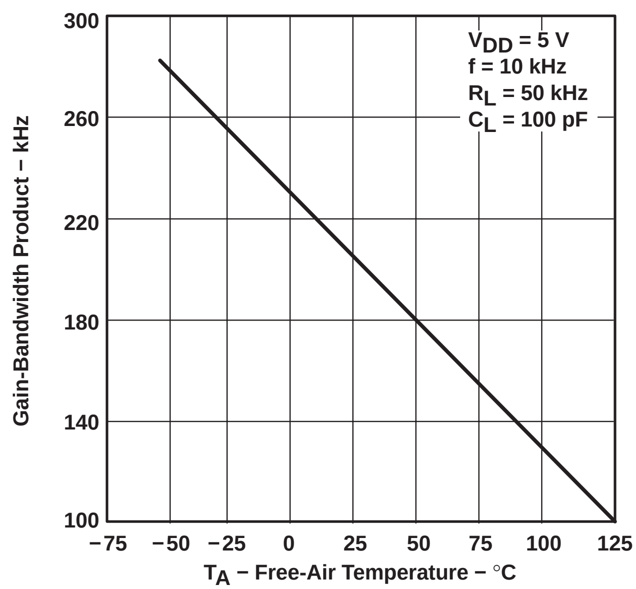


Figure 55

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

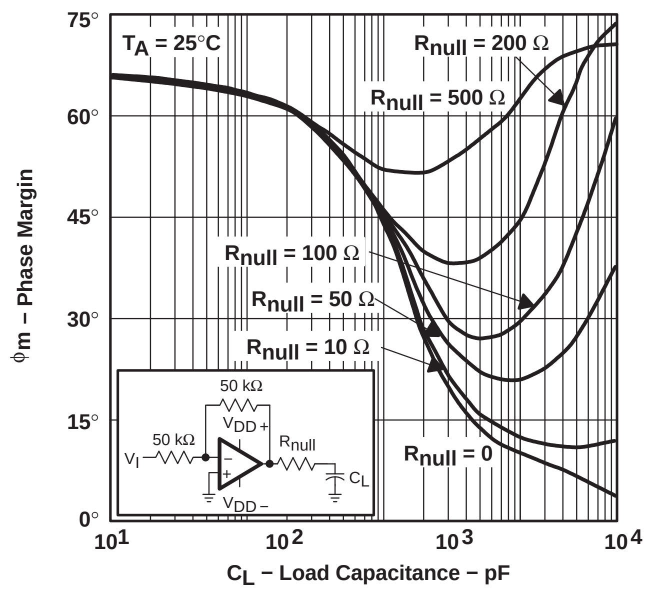


Figure 56

GAIN MARGIN vs LOAD CAPACITANCE

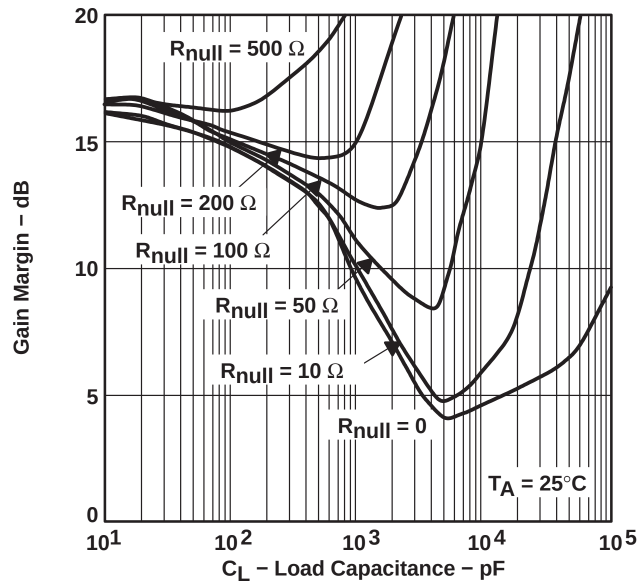


Figure 57

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

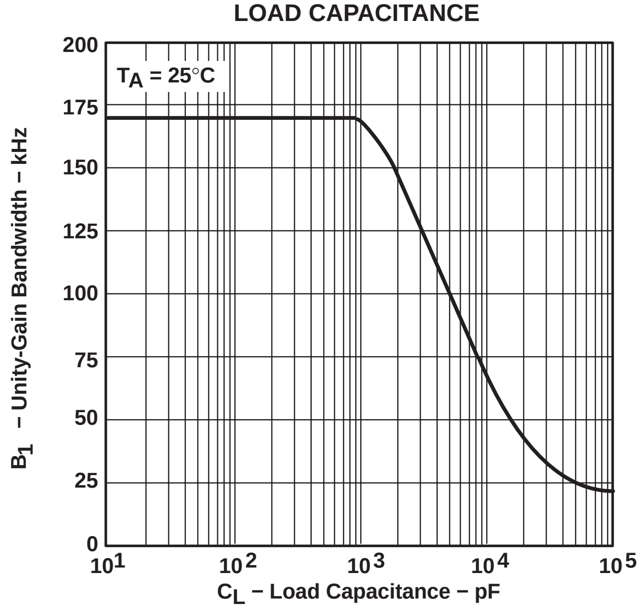
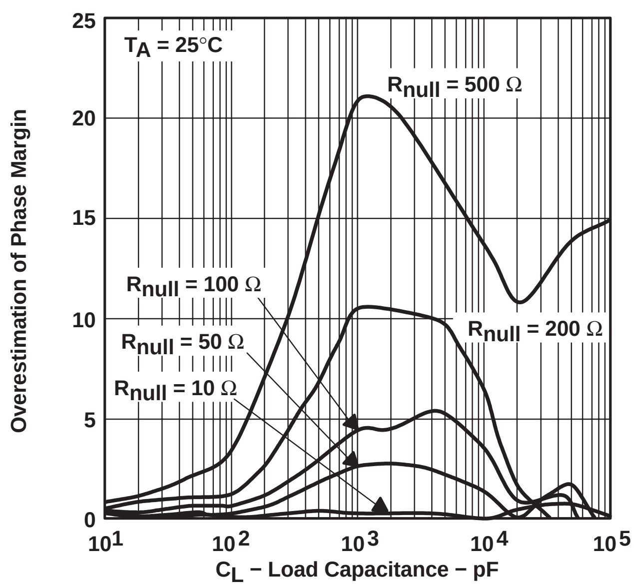


Figure 58

OVERESTIMATION OF PHASE MARGIN† vs LOAD CAPACITANCE



† See application information

Figure 59

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

driving large capacitive loads

The TLV2252 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 55 and Figure 56 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first adds a zero to the transfer function and the second reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \qquad (1)$$

Where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

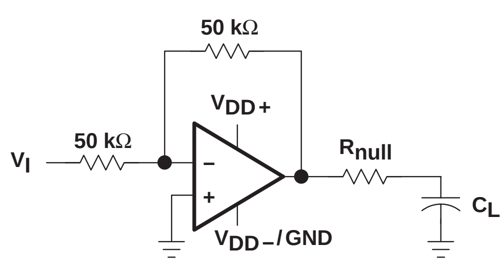


Figure 60. Series-Resistance Circuit

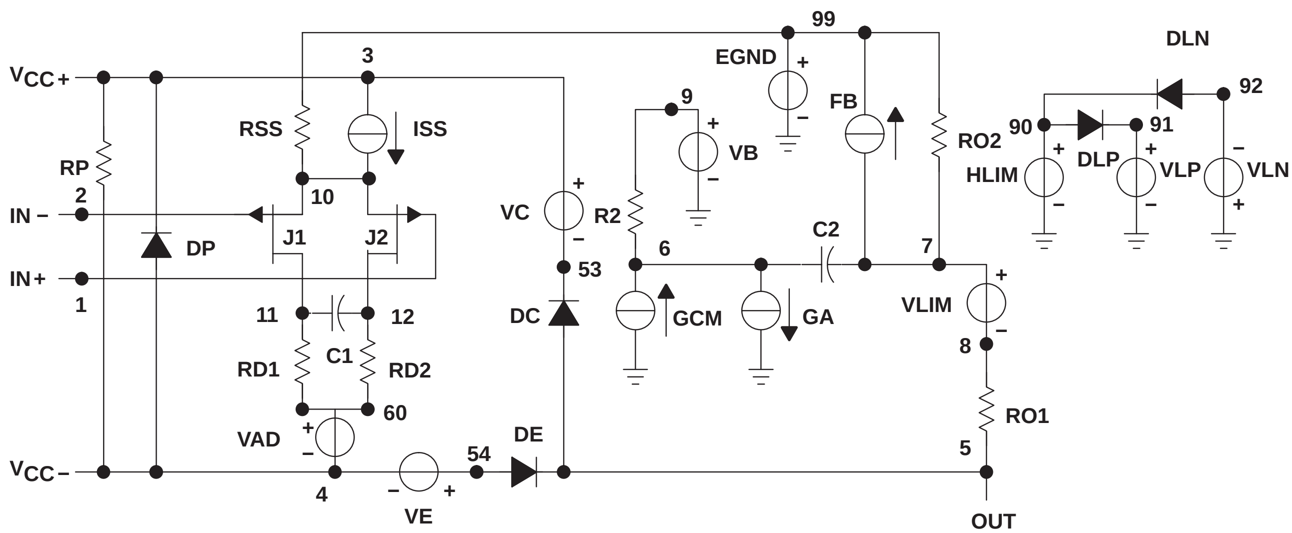
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLV2252 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV225x 1 2 3 4 5
        C1      11      12      6.369E−12
        C2      6       7       25.00E−12
        DC      5       53      DX
        DE      54      5       DX
        DLP     90      91      DX
        DLN     92      90      DX
        DP      4       3       DX
        EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7       99      POLY (5) VB VC VE VLP
        + VLN 0 57.62E6 −60E6 60E6 60E6 −60E6
        GA      6       0       11      12 26.86E−6
        GCM     0       6       10      99 2.686E−9
        ISS     3       10      DC 3.1E−6
        HLIM    90      0       VLIM 1K
        J1      11      2       10 JX
        J2      12      1       10 JX
        R2      6       9       100.0E3
RD1     60      11      37.23E3
RD2     60      12      37.23E3
R01     8       5       84
R02     7       99      84
RP      3       4       71.43E3
RSS     10      99      64.52E6
VAD     60      4       −.5
VB      9       0       DC 0
VC      3       53      DC .605
VE      54      4       DC .605
VLIM    7       8       DC 0
VLP     91      0       DC −0.235
VLN     0       92      DC 7.5
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=500.0E−15 BETA=139E−6
+ VTO=−.05)
.ENDS
```

Figure 61. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9550401Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9550401QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9550401QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9550403Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9550403QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9550403QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566601Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9566601QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566601QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566602Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9566602QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566602QDA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566603Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9566603QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566603QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566604Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9566604QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9566604QDA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2252AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AIP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2252AIPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2252AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AIPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLV2252AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2252AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2252AQD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2252AQDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2252CP	ACTIVE	PDIP	P	8		TBD	Call TI	Call TI

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV2252ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2252IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2252IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2252MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2252MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2252MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2252QD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2252QDR	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI
TLV2254AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2254AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2254AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2254AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2254AIN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2254AINE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2254AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2254AIPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2254AIPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TLV2254AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2254AIPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2254AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2254AMJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2254AMWB	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2254AQD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2254AQDR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2254ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2254IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2254IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV2254IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2254IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2254INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2254MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2254MJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2254MWB	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2254QD	ACTIVE	SOIC	D	14	50	TBD	Call TI	Call TI
TLV2254QDR	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI
TLV2262AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2262AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2262AMUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2262MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2262MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2262MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

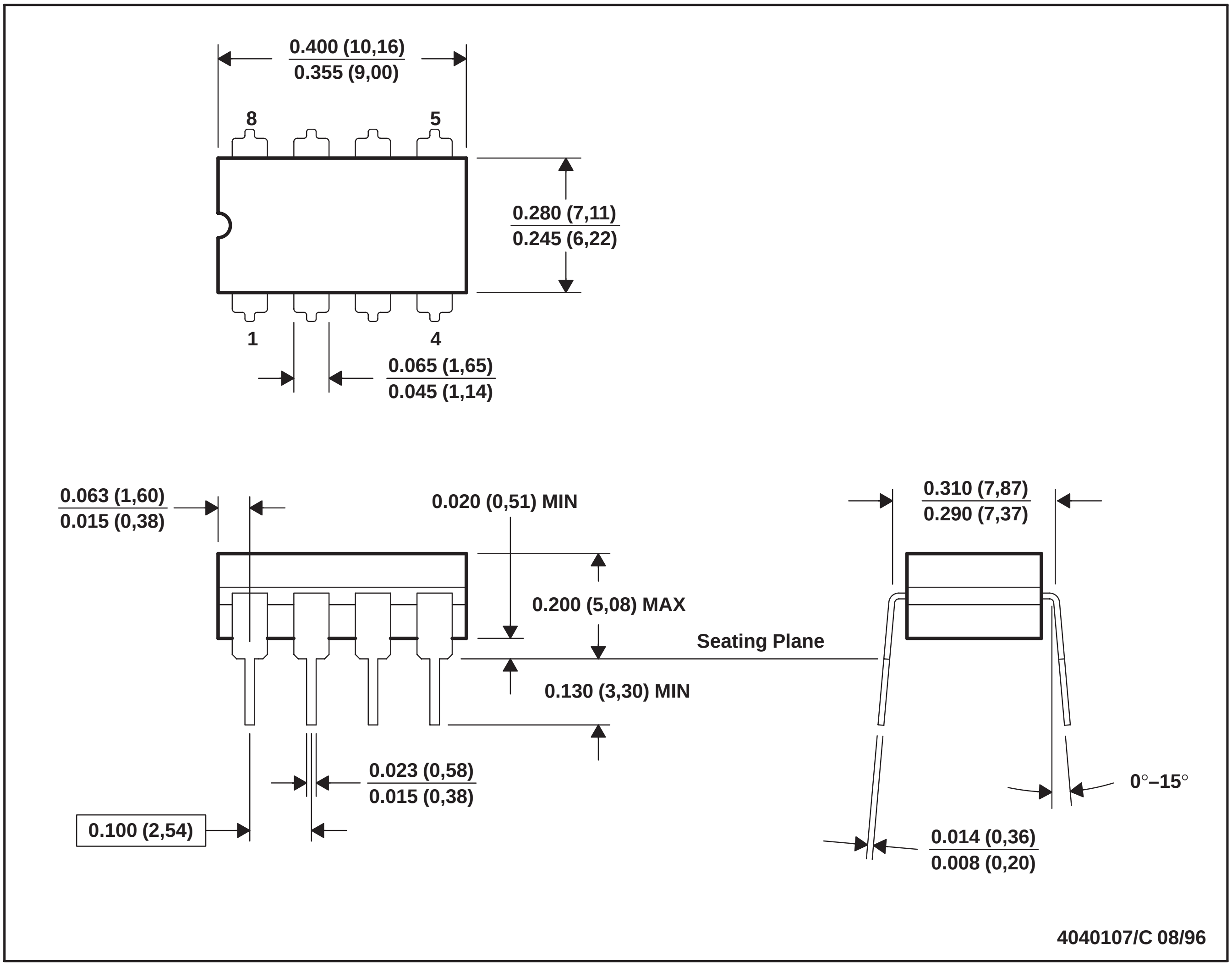
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

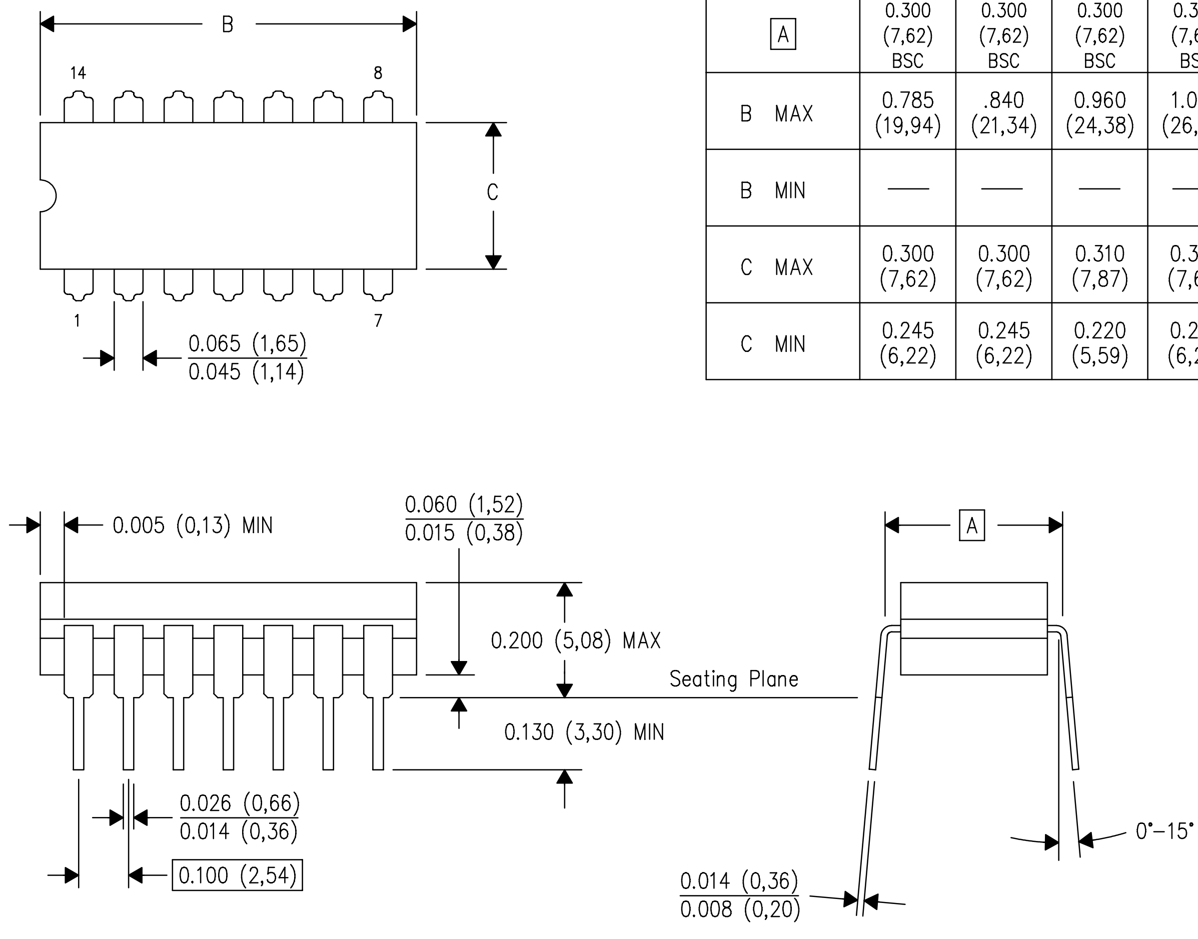


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

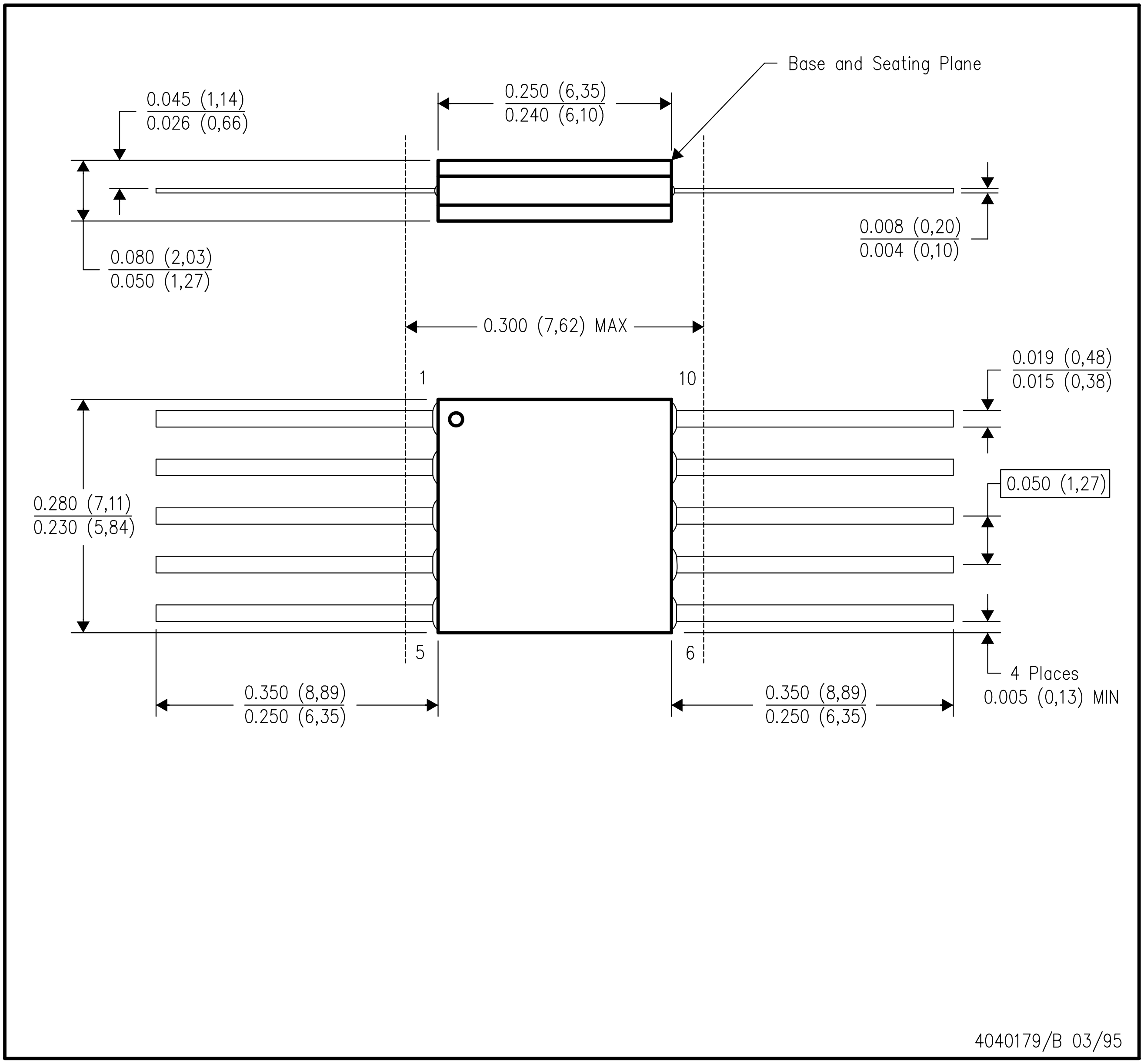
PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

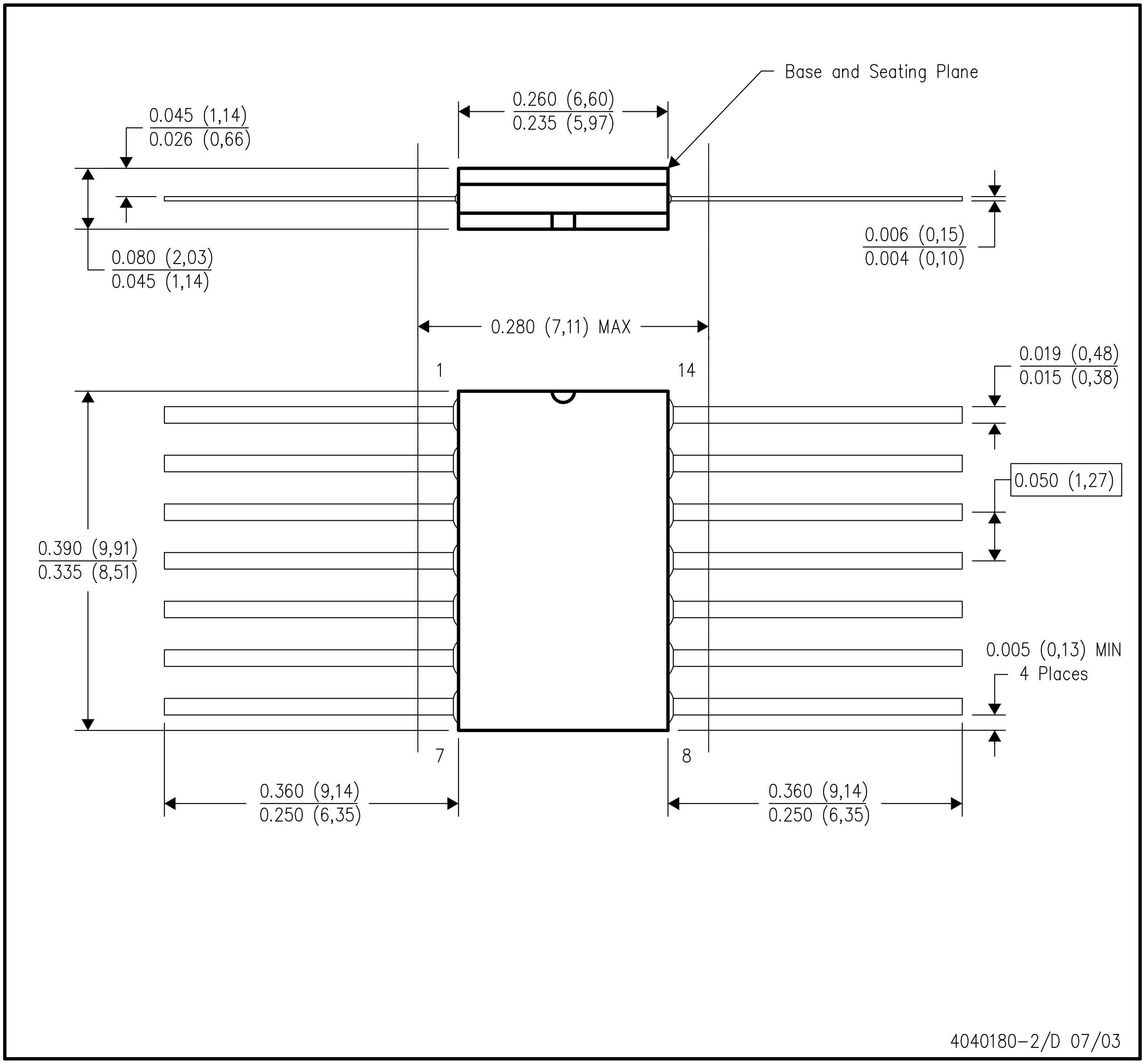
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

U (S-GDFP-F10) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

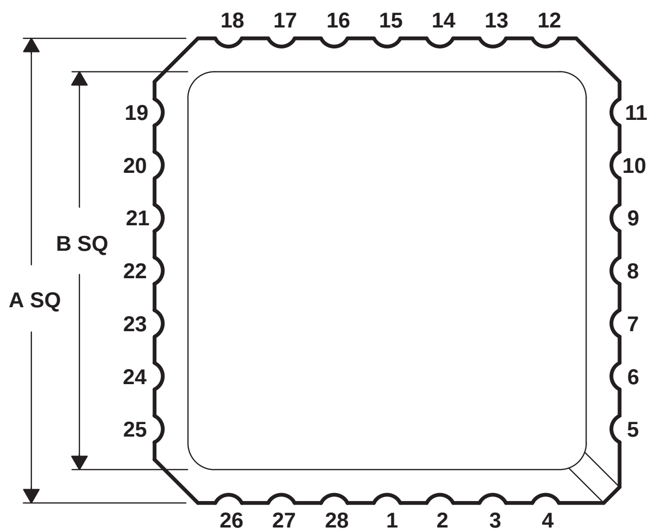
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



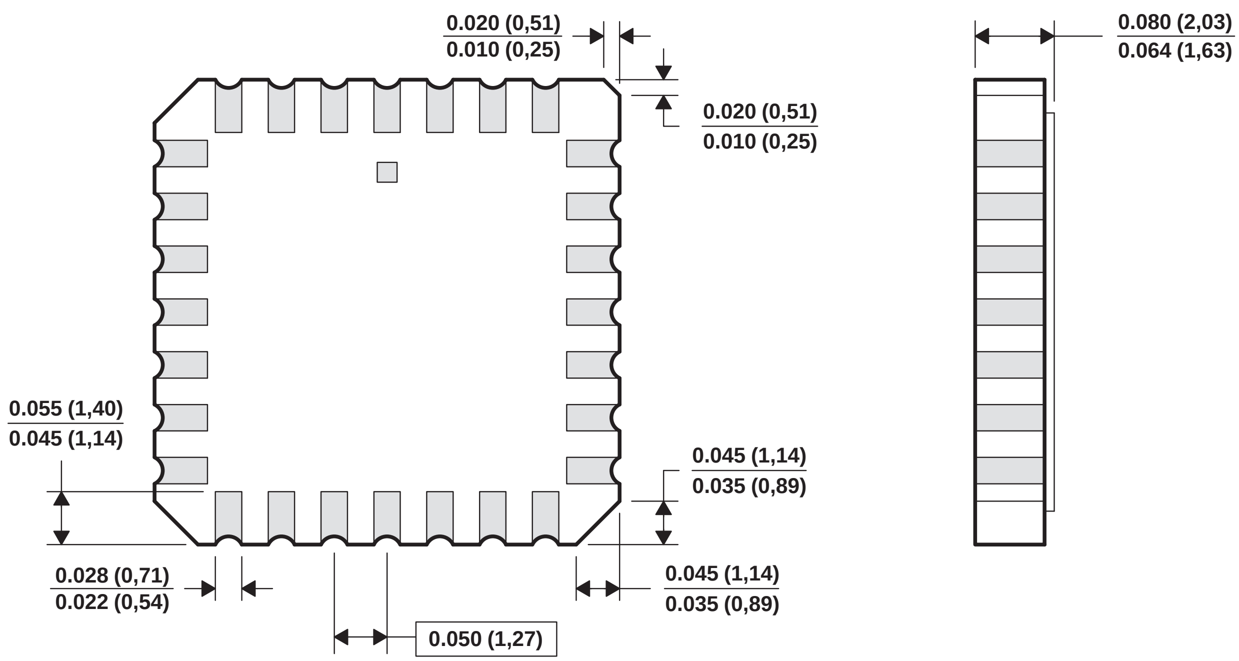
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



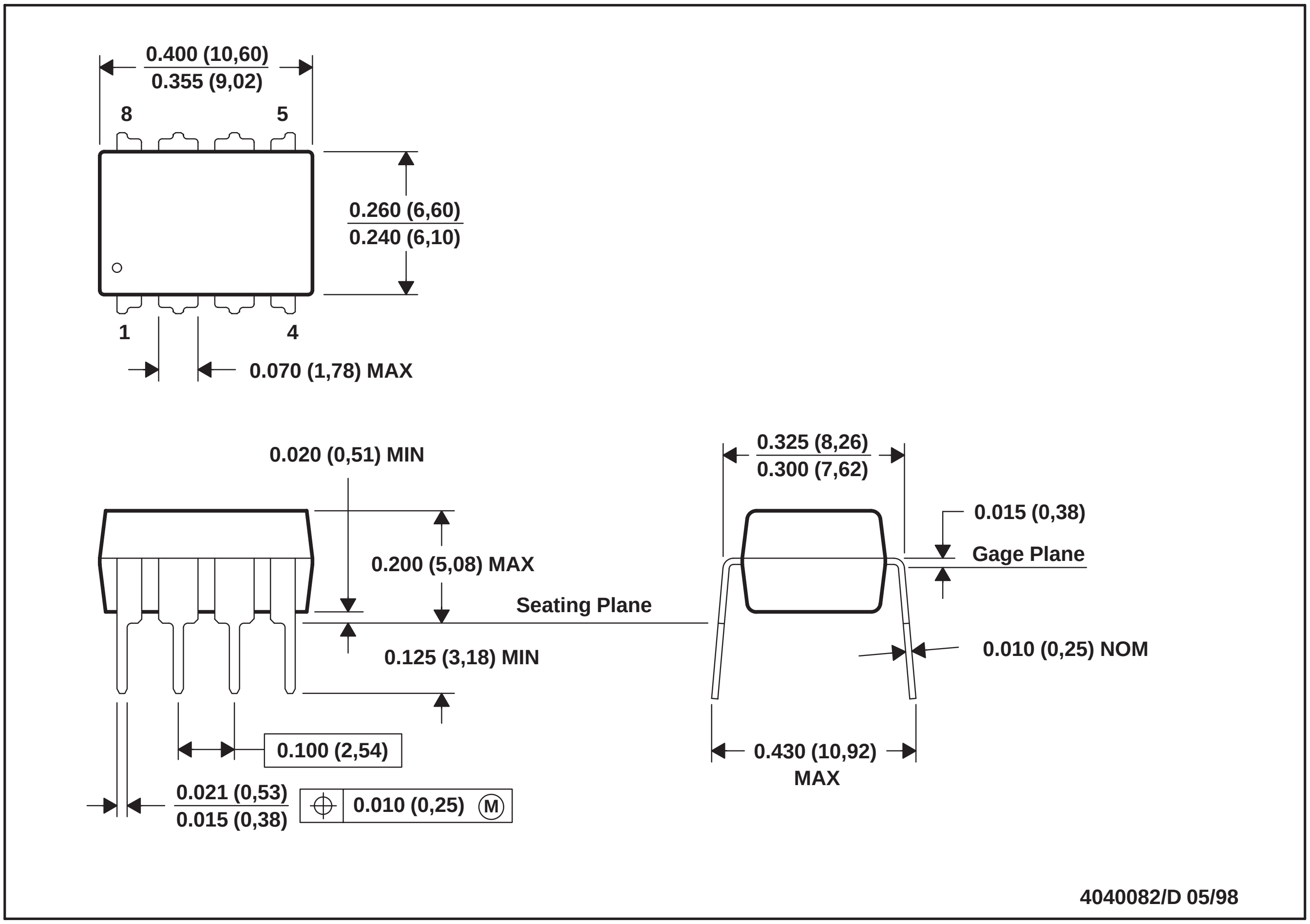
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

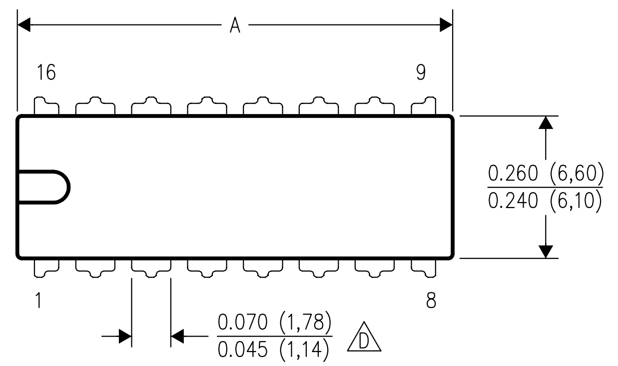
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



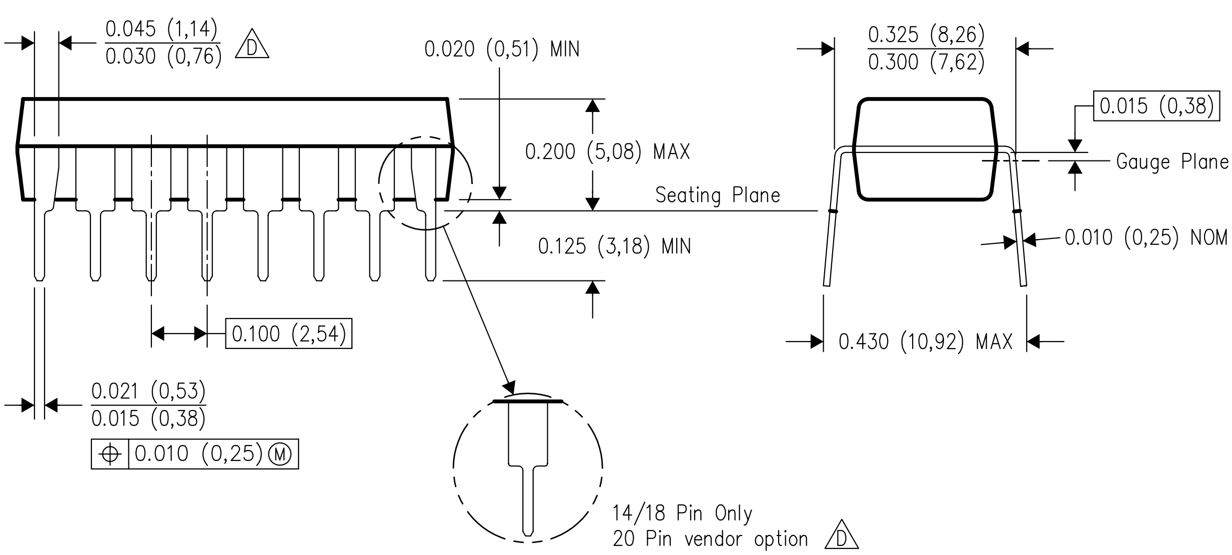
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



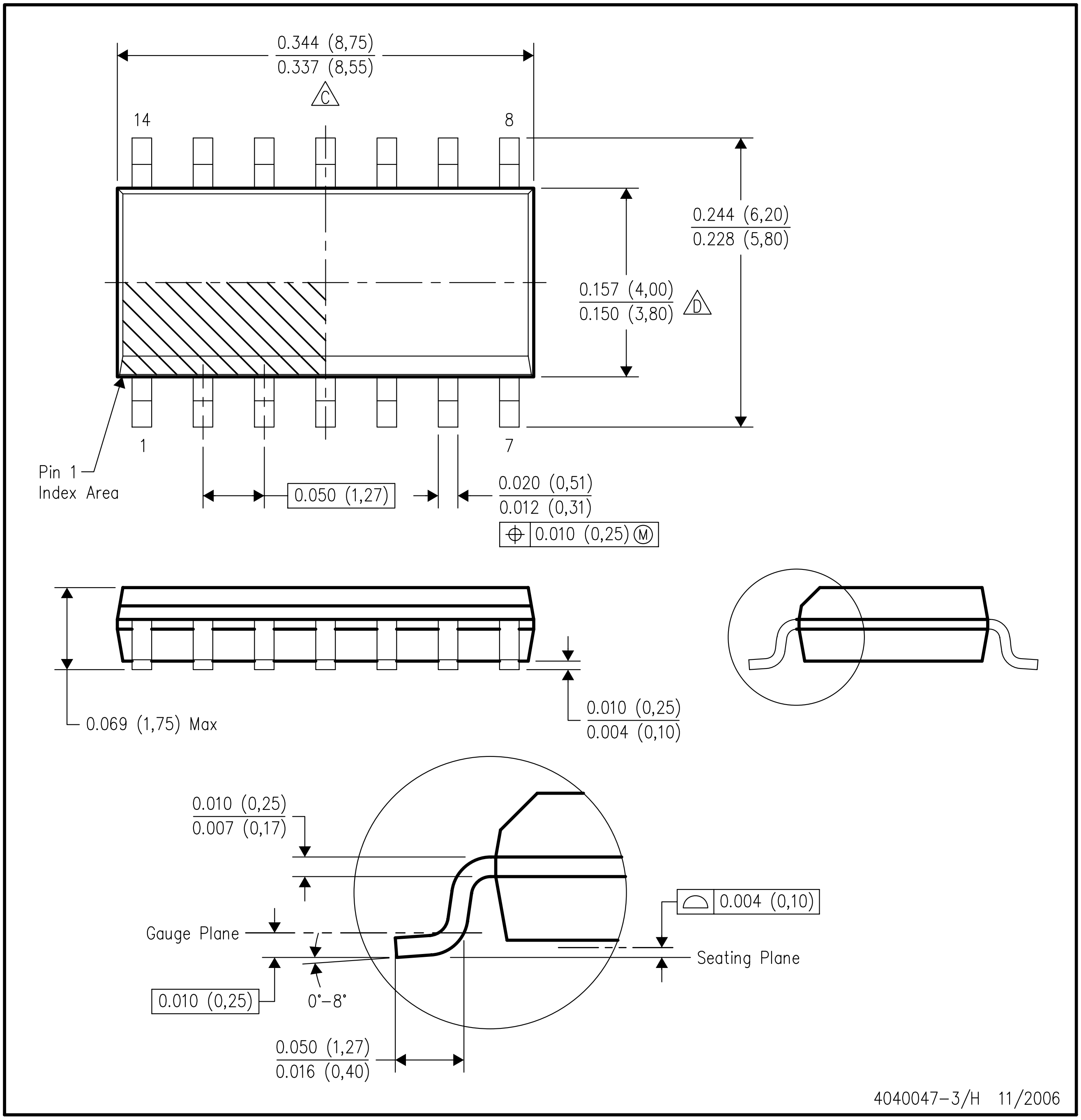
PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

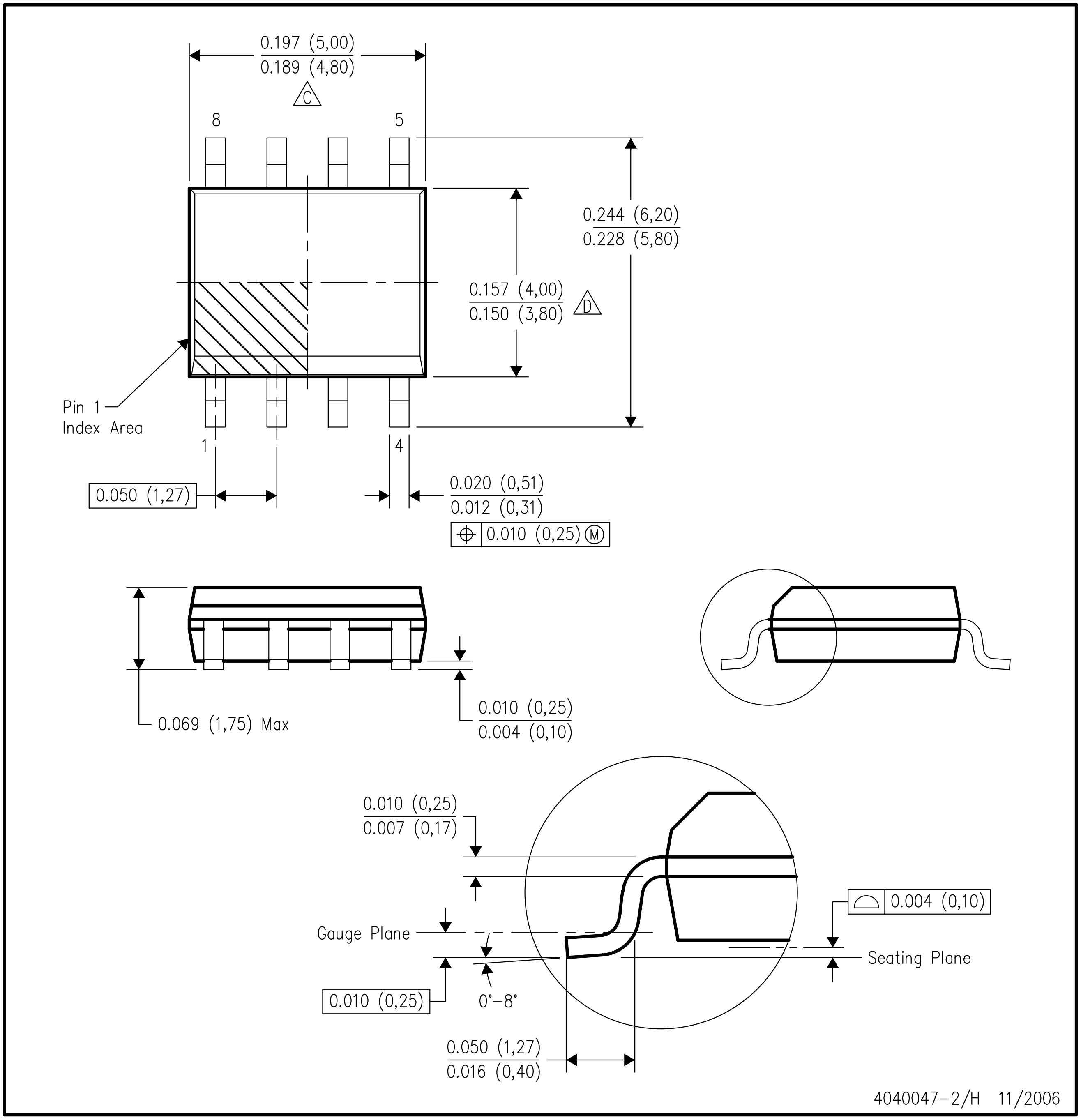
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- (C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AB.

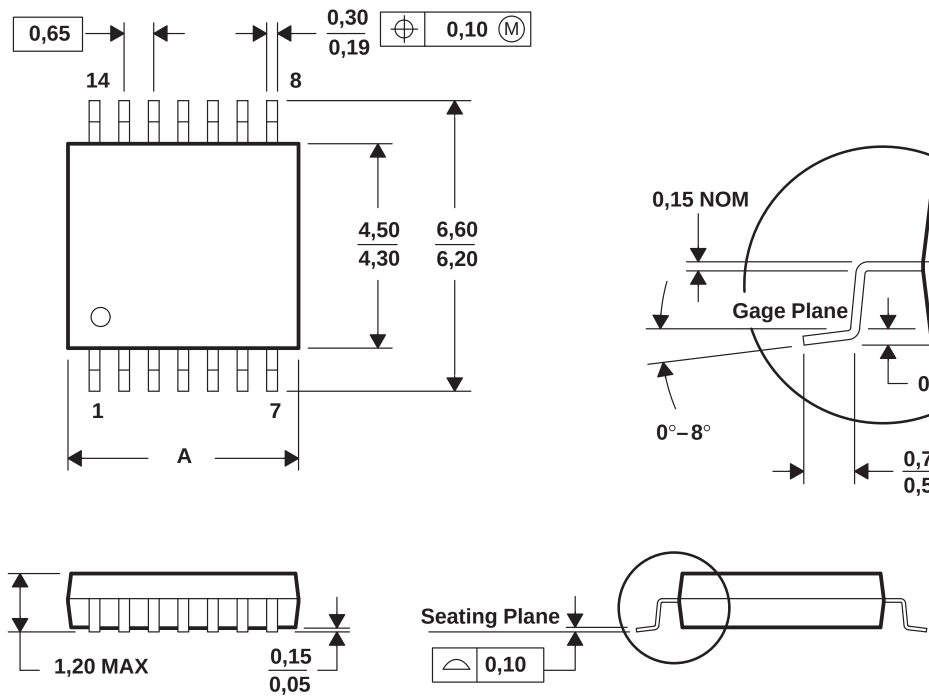
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153