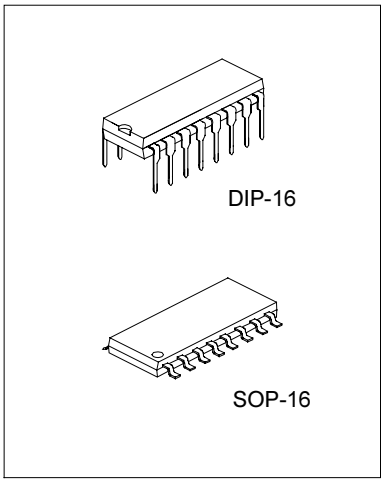
RADIO DATA SYSTEM (RDS) DEMODULATOR



DESCRIPTION

The integrated CMOS circuit SC6579 is an RDS demodulator. It recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting.

The data signal RDDA and the clock signal RDCL are provided as outputs for further processing by a suitable decoder (microcomputer).

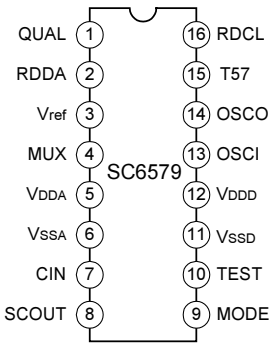
FEATURES

- Anti-aliasing filter (2nd order)
- Integrated 57 kHz band-pass filter (8th order)
- Reconstruction filter (2nd order)
- Clocked comparator with automatic offset compensation
- 57 kHz carrier regeneration
- Synchronous demodulator for 57 kHz modulated RDS signals
- Selectable 4.332/8.664 MHz crystal oscillator with variable dividers
- Clock regeneration with lock on bi-phase data rate
- Bi-phase symbol decoder with integrate and dump functions
- Differential decoder
- Signal quality detector
- Subcarrier output.

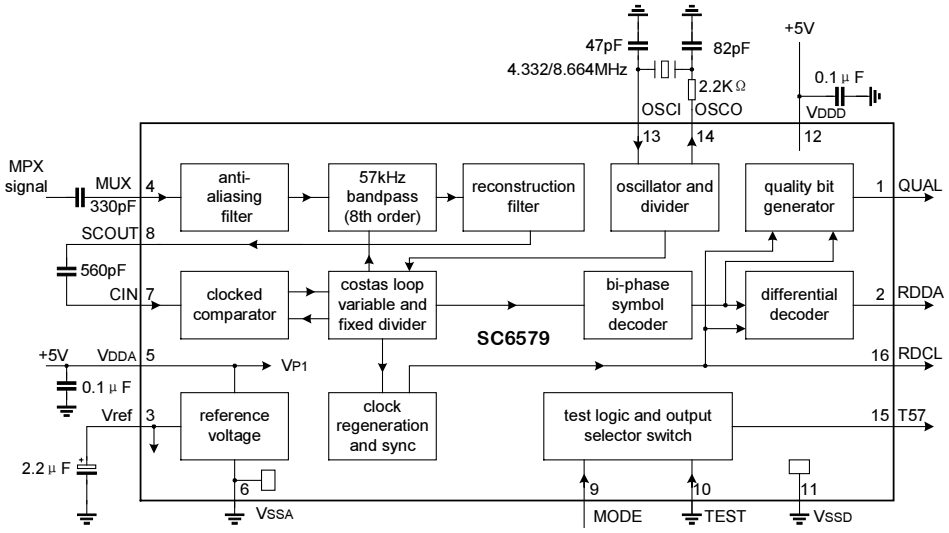
ORDERING INFORMATION

Device	Package
SC6579	DIP16-300-2.54
SC6579S	SOP-16-225-1.27

PIN CONFIGURATION



BLOCK DIAGRAM



Via pin MODE two different crystal frequencies can be used.

MODE	CRYSTAL CLOCK
LOW	4.332 MHz
HIGH	8.664 MHz

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Analog Supply Voltage (pin 5)	V_{DDA}	0~ 6	V
Digital Supply Voltage (pin 12)	V_{DDD}	0~ 6	V
Voltage on All Pins; Grounds Excluded	V_n	-0.5 ~ V_{DD} + 0.5	V
Storage Temperature	T_{stg}	-40 ~+150	°C
Operating Ambient Temperature	T_{amb}	-40 ~+85	°C
Electrostatic Handling for All Pins Except	V_{ESD}	±300 note 1	V
Pins 9 and 10		+1500 ~-3000 note 2	V

Notes：1. Equivalent to discharging a 200 pF capacitor via a 0 Ω series resistor.

2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

ELECTRICAL CHARACTERISTICS

(V_{DDA} =V_{DDD} =5 V; T_{amb} =25°C and measurements taken in Fig.1; unless otherwise specified.)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Analog Supply Voltage (pin 5)	V_{DDA}		3.6	5.0	5.5	V
Digital Supply Voltage (pin 12)	V_{DDD}		3.6	5.0	5.5	V
Total Supply Current	I_{tot}	$I_5 + I_{12}$	~	6	~	mA
Reference Voltage (pin 3)	V_{ref}	V_{DDA} = 5 V	~	2.5	~	V
MPX input (signal before the capacitor on pin 4)						
RDS Amplitude (RMS value)	$V_{i\ MPX\ (rms)}$	Δf ±1.2 kHz RDS; Δf ±3.5 kHz ARI; see Fig.5	1	--	--	mV
Maximum Input Signal Capability (peak-to-peak value)	$V_{i\ MPX\ (p-p)}$	f = 5±2 kHz	200	--	--	mV
		f < 50 kHz	1.4	--	--	V
		f < 15 kHz	2.8	--	--	V
		f > 70 kHz	3.5	--	--	V
Input Resistance	R4-6	f = 0 to 100kHz	40	--	--	kΩ
Signal Gain	G8-4	f = 57 kHz	17	20	23	dB
57 kHz band-pass filter						
Center Frequency	fc	T_{amb} = -40 to +85 °C	56.5	57.0	57.5	kHz
-3 dB Bandwidth	B		2.5	3.0	3.5	kHz
Stop Band Gain	G	Δf =±7 kHz	31	--	--	dB
		f < 45 kHz	40	--	--	dB
		f < 20 kHz	50	--	--	dB
		f > 70 kHz	40	--	--	dB
Output Resistance (pin 8)	$R_{o(8)}$	f = 57 kHz	--	26	--	Ω
Comparator input (pin 7)						
Minimum Input Level (RMS value)	$V_{i(rms)}$	f = 57 kHz	--	1	10	mV
Input Resistance	R_i		70	110	150	kΩ
Oscillator input (pin 13)						
HIGH-level Input Voltage	V_{IH}	V_{DDD} = 5.0 V	4.0	--	--	V
LOW-level Input Voltage	V_{IL}	V_{DDD} = 5.0 V	--	--	1.0	V
Input Current	I_I	V_{DDD} = 5.5 V	--	--	±I	μA

（To be continued）

(Continued)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Digital demodulator and outputs QUAL, RDDA, T57, OSCO and RDCL (pins 1, 2, 14, 15 and 16)						
HIGH-level output voltage	V_{OH}	I_Q = -20 mA; V_{DDD} = 4.5 V	4.4	--	--	V
LOW-level output voltage	V_{OL}	I_Q = 3.2 mA; V_{DDD} = 5.5 V	--	--	0.4	V
Nominal Clock Frequency RDCL	f_{RDCL}		--	1187.5	--	Hz
Jitter of RDCL	Δt_{RDCL}		--	--	18	μs
Nominal Subcarrier Frequency T57	f_{T57}	note 1	--	57.0	--	kHz
Output Current OSCO (pin 14)	I_O	V_{DDD} = 4.5 V; V_{14} = 0.4 V	1.5	--	--	mA
		V_{DDD} = 4.5 V; V_{14} = 4.1 V	-1.6	--	--	mA
Output Current QUAL, RDDA, T57, RDCL (pins 1, 2, 15 and 16)		V_{DDD} = 4.5 V; V_O = 0.4 V	5.9	--	--	mA
		V_{DDD} = 4.5 V; V_O = 4.1 V	-5.3	--	--	mA
4.332 MHz crystal parameters						
XTAL Frequency	f_0		--	4.332	--	MHz
Maximum Permitted Tolerance	Δf_{max}			±50		10^{-6}
Adjustment Tolerance of f0	Δf_o	T_{amb} =25°C	--	--	±20	10^{-6}
		T_{amb} = -40 to +85 °C	--	--	±25	10^{-6}
Load Capacitance	C_L		--	30	--	pF
Resonance Resistance	R_{xtal}		--	--	60	Ω
8.664 MHz crystal parameters						
XTAL Frequency	f_0		--	8.664	--	MHz
Maximum Permitted Tolerance	Δf_{max}		--	±50	--	10^{-6}
Adjustment Tolerance of f0	Δf_o	T_{amb} =25°C	--	--	±30	10^{-6}
		T_{amb} = -40 to +85 °C	--	--	±30	10^{-6}
Load Capacitance	C_L		--	30	--	. pF
Resonance Resistance	R_{xtal}		--	--	60	Ω

Note1. The signal T57 has a phase lead of 123° (±180°) relative to the ARI carrier at output SCOUT.

PIN DESCRIPTION

Pin no.	Symbol	Function
1	QUAL	Quality indication output
2	RDDA	RDS data output
3	V_{ref}	Reference voltage output (0.5 V_{DDA})
4	MUX	Multiplex signal input
5	V_{DDA}	+5 V supply voltage for analog part
6	V_{SSA}	Ground for analog part (0V)
7	CIN	Subcarrier input to comparator
8	SCOUT	Subcarrier output of reconstruction filter
9	MODE	Oscillator mode/test control input
10	TEST	Test enable input
11	V_{SSD}	Ground for digital part (0V)
12	V_{DDD}	+5 V supply voltage for digital part
13	OSCI	Oscillator input
14	OSCO	Oscillator output
15	T57	57 kHz clock signal output
16	RDCL	RDS clock output

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	Analog Supply Voltage (pin 5)	3.6	5.0	5.5	V
V_{DDD}	Digital Supply Voltage (pin 12)	3.6	5.0	5.5	V
I_{tot}	Total Supply Current	--	6	--	mA
$V_{i(rms)}$	RDS Input Amplitude (RMS value; pin 4)	1	--	--	mV
V_{OH}	HIGH-level Output Voltage for Signals RDDA, RDCL, QUAL and T57	4.4	--	--	V
V_{OL}	LOW-level Output Voltage for Signals RDDA, RDCL, QUAL and T57	--	--	0.4	V
T_{amb}	Operating Ambient Temperature	-40	--	+85	°C

FUNCTION DESCRIPTION

The SC6579 is a demodulator circuit for RDS applications. It contains a 57 kHz bandpass filter and a digital demodulator to regenerate the RDS data stream out of the multiplex signal (MPX).

Filter part

The MUX signal is band-limited by a second-order anti-aliasing-filter and fed through a 57 kHz band-pass filter (8th order band-pass filter with 3 kHz bandwidth) to separate the RDS signals. This filter uses switched capacitor technique and is clocked by a clock frequency of 541.5 kHz derived from the 4.332/8.664 MHz crystal oscillator. Then the signal is fed to the reconstruction filter to smooth the sampled and filtered RDS signal before it is output on pin 8. The signal is AC-coupled to the comparator (pin 7). The comparator is clocked with a frequency of 228 kHz (synchronized by the 57 kHz of the demodulator).

Digital part

The synchronous demodulator (Costa's loop circuit) with carrier regeneration demodulates the internal coupled, digitized signal. The suppressed carrier is recovered from the two sidebands (Costa's loop). The demodulated signal is low-pass-filtered in such a way that the overall pulse shape (transmitter and receiver) approaches a cosinusoidal form in conjunction with the following Integrate and dump circuit.

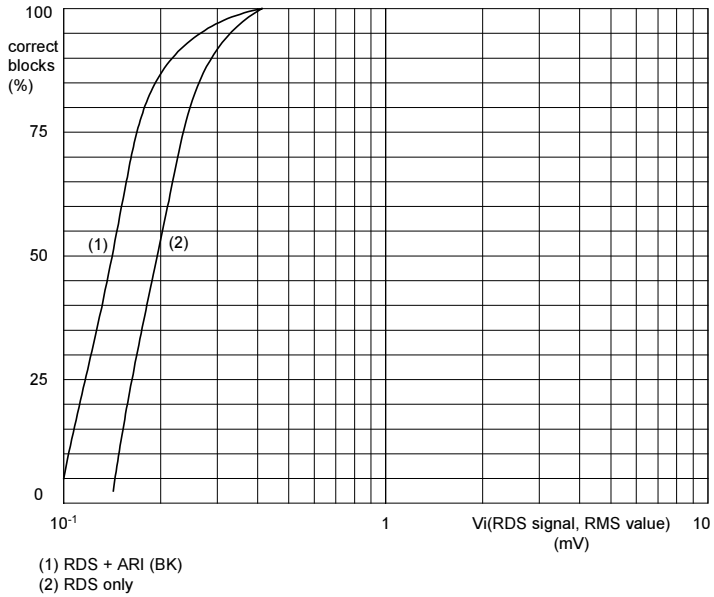
The data-spectrum shaping is split into two equal parts and handled in the transmitter and in the receiver. Ideally, the data filtering should be equal in both of these parts. The overall data-channel-spectrum shaping of the transmitter and the receiver is approximately 100% roll-off. The integrate and dump circuit performs an integration over a clock period. This results in a demodulated and valid RDS signal in form of bi-phase symbols being output from the integrate and dump circuit. The final stages of RDS data processing are the bi-phase symbol decoding and the differential decoding. After synchronization by data clock RDCL (pin 16) data appears on the RDDA output (pin 2). The output of the bi-phase symbol decoder is evaluated by a special circuit to provide an indication of good data (QUAL = HIGH) or corrupt data (QUAL = LOW).

Timing

Fixed and variable dividers are applied to the 4.332/8.664 MHz crystal oscillator to generate the 1.1875 kHz RDS clock RDCL, which is synchronized by the incoming data. Which ever clock edge is considered (positive or negative going edge) the data will remain valid for 399 μs after the clock transition. The timing of data change is 4 μs before a clock change. Which clock transition (positive or negative going clock) the data change occurs in, depends on the lock conditions and is arbitrary (bit slip).

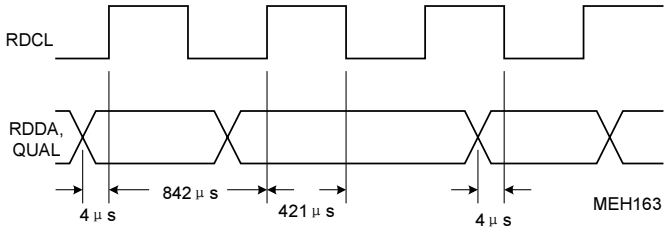
During poor reception it is possible that faults in phase occur, then the clock signal stays uninterrupted, and data is constant for 1.5 clock periods. Normally, faults in phase do not occur on a cyclic basis. If however, faults in phase occur in this way, the minimum spacing between two possible faults in phase depends on the data being transmitted. The minimum spacing cannot be less than 16 clock periods. The quality bit changes only at the time of a data change.

TYPICAL RDS SENSITIVITY (BLOCK)

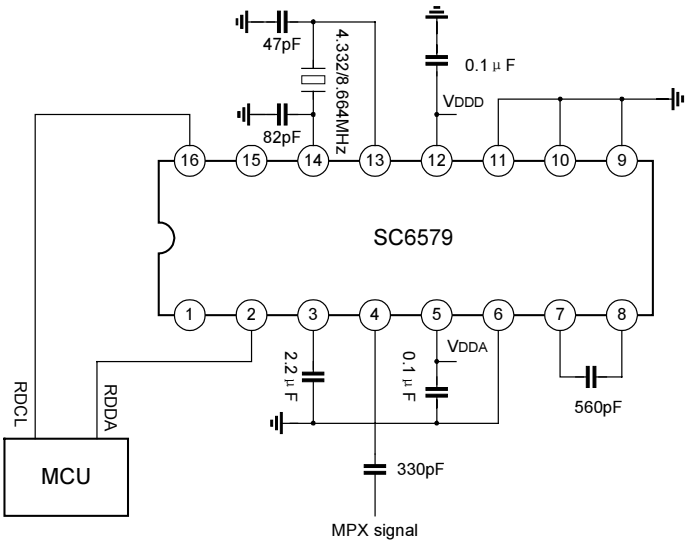


(1) RDS + ARI (BK)
(2) RDS only

TIMING DIAGRAM

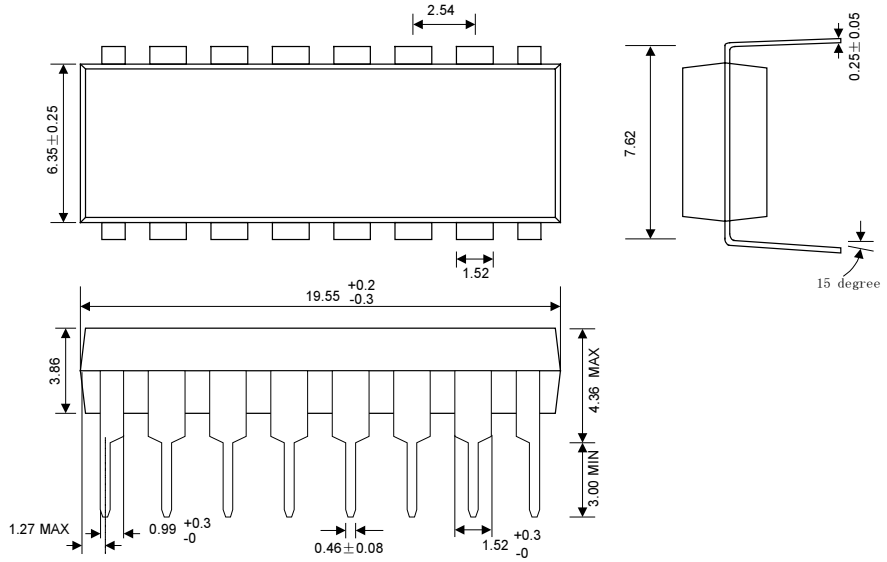


APPLICATION CIRCUIT



PACKAGE OUTLINE

DIP-16-300-2.54 UNIT: mm



SOP-16-225-1.27 UNIT:mm

