

Preliminary

GENERAL DESCRIPTION

EM56000A is a series of single chip dual channel IC with voice synthesizer. The dual channel can be (voice + voice) simultaneously. That contains some input and I/O ports, and a tiny controller. By programming through the tiny controller, user's application including section combination, trigger modes, control outputs, IR communication, and other logical function can be easily implemented.

FEATURES

	EM56001A	EM56101A	EM56200A	EM56300A	EM56400A	EM56500A	EM56600A
TOTAL ROM(bits)	10K x 10	16K x 10	32K x 10	64K x 10	128K x 10	256K x 10	512K x 10
PROGRAMROM(bits)	8K x 10		32K x 10				
RAM(nibbles)	32	64	128				
PORT1 [input](pins)	-		4				
PORT2 [I/O](pins)	2	4					
PORT3 [I/O](pins)	4						
VO(pins)	1		2				

- Single power supply 2.4 V ~ 5.5 V.
- Port1 and Port2 with wake-up function, Port3.2 with programmable IR (38 KHz carry) communication function.
- Power down mode for saving power consumption.
- Single ROM for voice program data.
- Readable ROM code data.
- One 6-bit timer overflow control.
- Two stacks for subroutine calling.
- Dual channel output simultaneously : (voice + voice).
- 5-bit ASPCM synthesizer.
- Multiple playing speeds in 2 KHz ~ 32 KHz for voice playback.
- Multiple levels of volume control.
- Fixed current D/A to drive external connected transistor for audio output.

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PIN DESCRIPTIONS

Symbol	I/O	Function
P1.0	I	Bit 0 of Port 1. (not for EM56001A, EM56101A)
P1.1	I	Bit 1 of Port 1. (not for EM56001A, EM56101A)
P1.2	I	Bit 2 of Port 1. (not for EM56001A, EM56101A)
P1.3	I	Bit 3 of Port 1. (not for EM56001A, EM56101A)
P2.0	I/O	Bit 0 of Port 2. (not for EM56001A)
P2.1	I/O	Bit 1 of Port 2. (not for EM56001A)
P2.2	I/O	Bit 2 of Port 2.
P2.3	I/O	Bit 3 of Port 2.
P3.0	I/O	Bit 0 of Port 3.
P3.1	I/O	Bit 1 of Port 3.
P3.2	I/O	Bit 2 of Port 3. The pin can generate 38KHz square wave.
P3.3	I/O	Bit 3 of Port 3. The pin can be treated as an LED output flashing with volume.
VDD	I	Positive power supply.
OSC	I	Oscillation component connection pin.
VSS	I	Negative power supply.
VO1	O	Audio1 output.
VO2	O	Audio2 output. (not for EM56001A, EM56101A)
TEST		For testing only

ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Min.	Max.	Unit
Supply Voltage	$V_{DD}-V_{SS}$	-0.3	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Operating Temperature	T_{OP}	-20	70	°C
Storage Temperature	T_{STG}	-55	+125	°C

ELECTRICAL CHARACTERISTICS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating voltage	V_{DD}	2.4	3.0	5.5	V	
Standby current	I_{DDS}	-	-	1.0	μA	$V_{DD}=3V$
Operating current	I_{DDO}	-	-	250	μA	$V_{DD}=3V$, No load
Drive current of P2,P3	I_{OD}	2.0	3.0	-	mA	$V_{DD}=3V$, $V_O=2.4V$
Sink current of P3	I_{OS}	2.3	3.5	-	mA	$V_{DD}=3V$, $V_O=0.4V$

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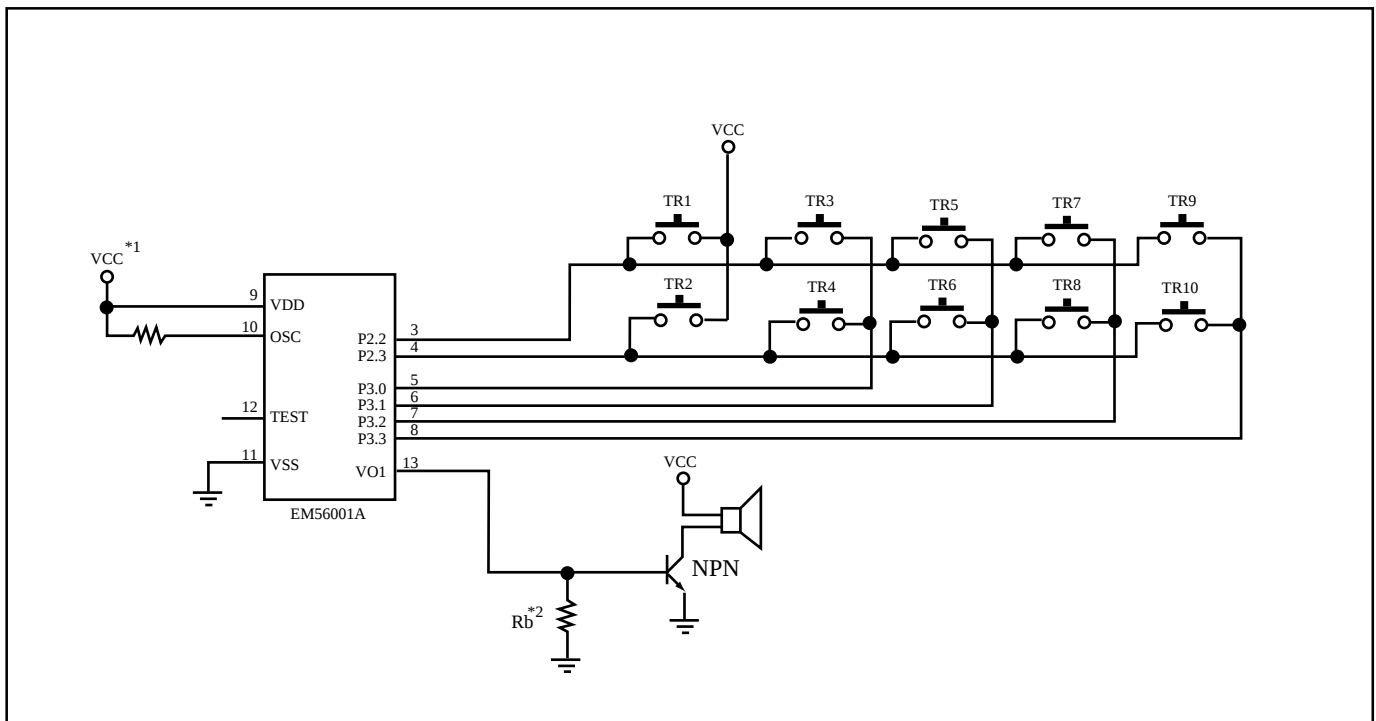
Parameter	Sym.	Min.	Typ.	Max.	Unit	Condition
Sink current of P2 (after KEYB)	I_{OS1}	2.3	3.5	-	mA	$V_{DD}=3V, V_O=0.4V$
Sink current of P2 (before KEYB)	I_{OS2}	-	3.0	10	μA	$V_{DD}=3V, V_O=0.4V$
Input current of P1	I_{IH}	-	3.0	10	μA	$V_{DD}=3V$
Output current of VO1, VO2	I_{VO}	4.0	5.0	6.0	mA	$V_{DD}=3V, V_O=0.7V$, two channel full scale output
Oscillation resistor	R_{OSC}	-	470	-	K Ω	$V_{DD}=2.4V \sim 5.5V$
Oscillation frequency	F_{OSC}	0.9	1.0	1.1	MHz	$V_{DD}=2.4V \sim 5.5V$
Oscillation frequency deviation	$\frac{\Delta F_{OSC}}{F_{OSC}}$	-10	0	10	%	$V_{DD}=2.4V \sim 5.5V$

APPLICATION CIRCUIT

In the following application circuits:

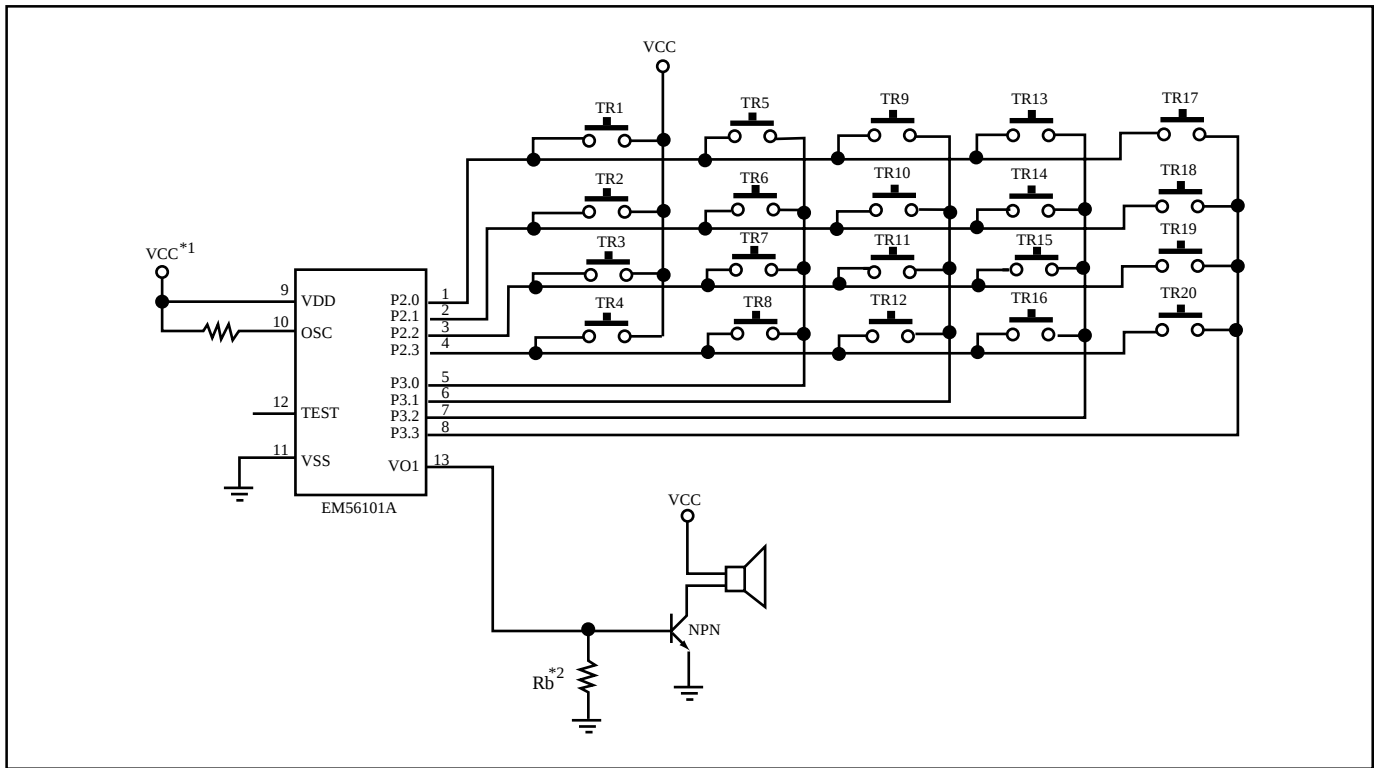
- *1 : For heavy loading application, adding an electrolytic capacitor between Vcc and Ground is recommended.
The recommended value for button cell application is 10 μF .
- *2 : The recommended value for button cell application is 750 Ω or less.

10-key Application Circuit For EM56001A

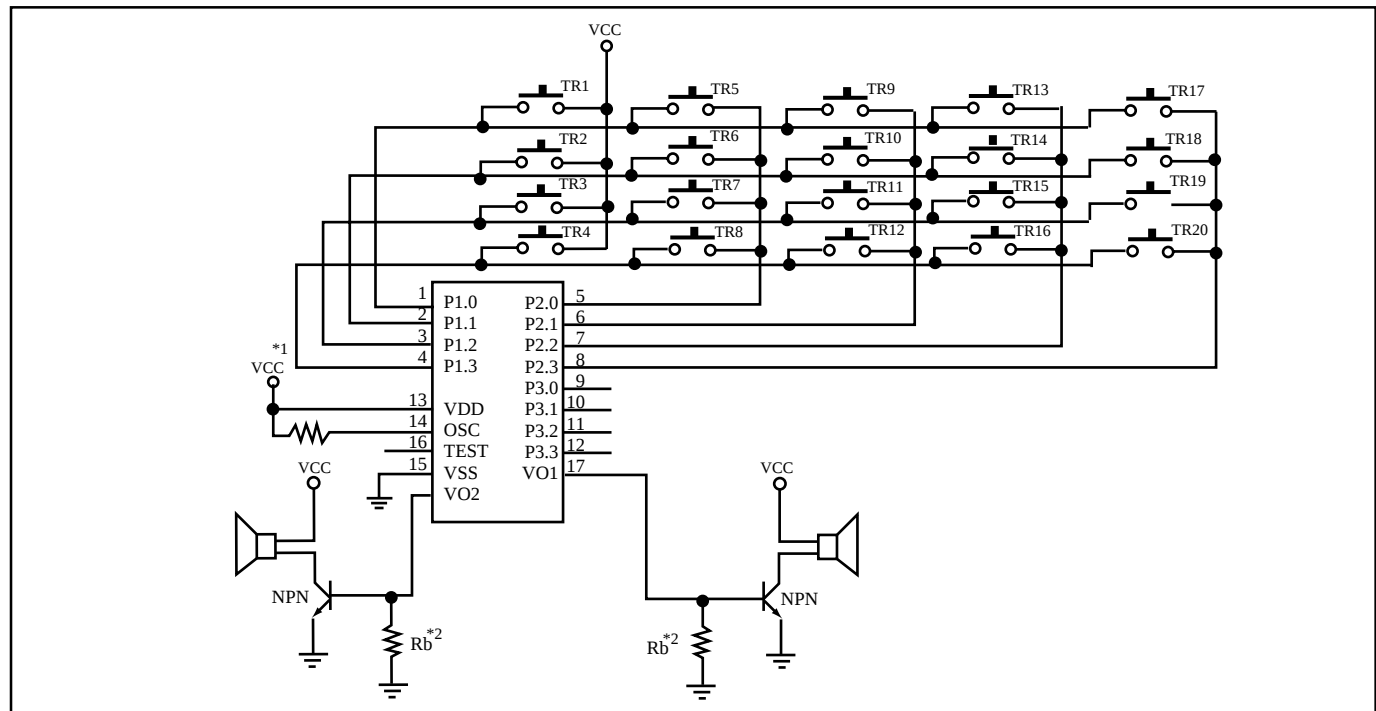


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20-key Application Circuit For EM56101A

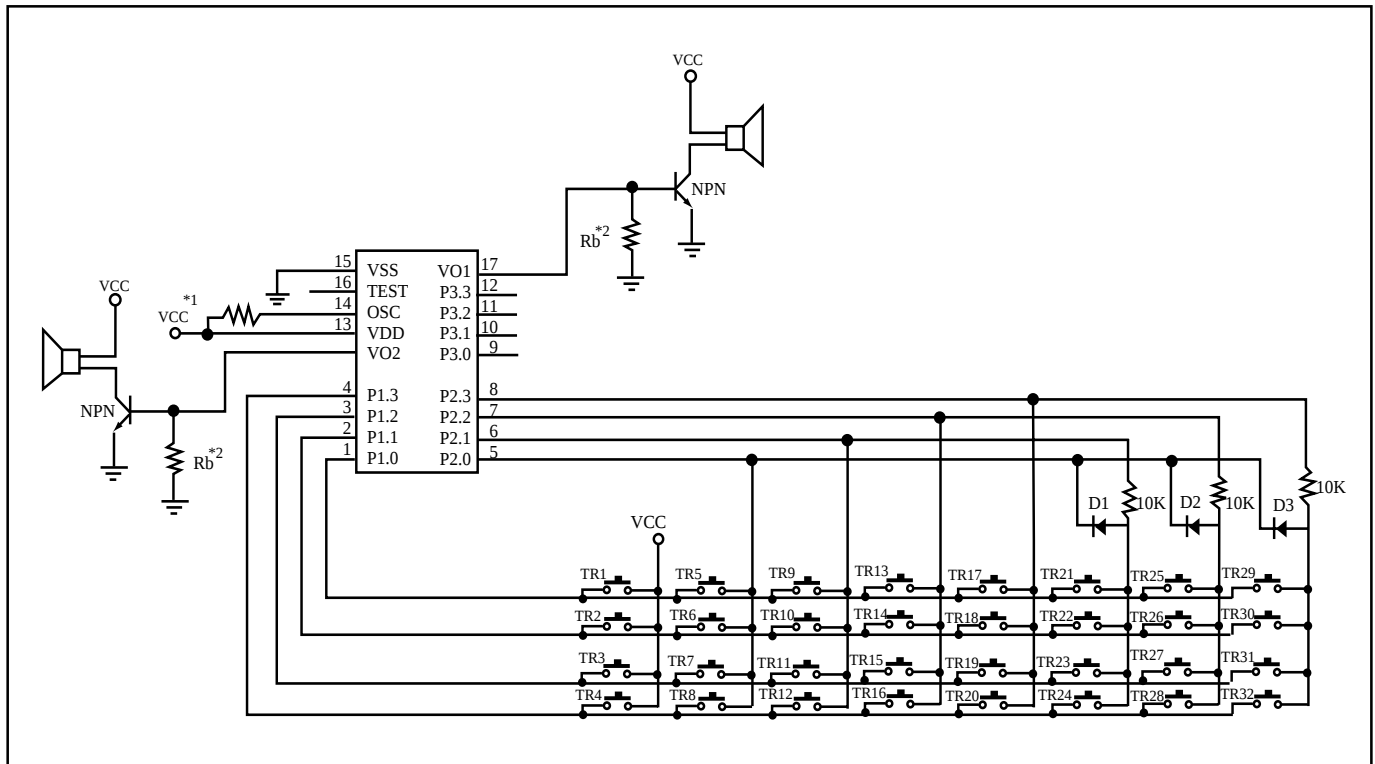


20-key Application Circuit For EM56200A~EM56600A

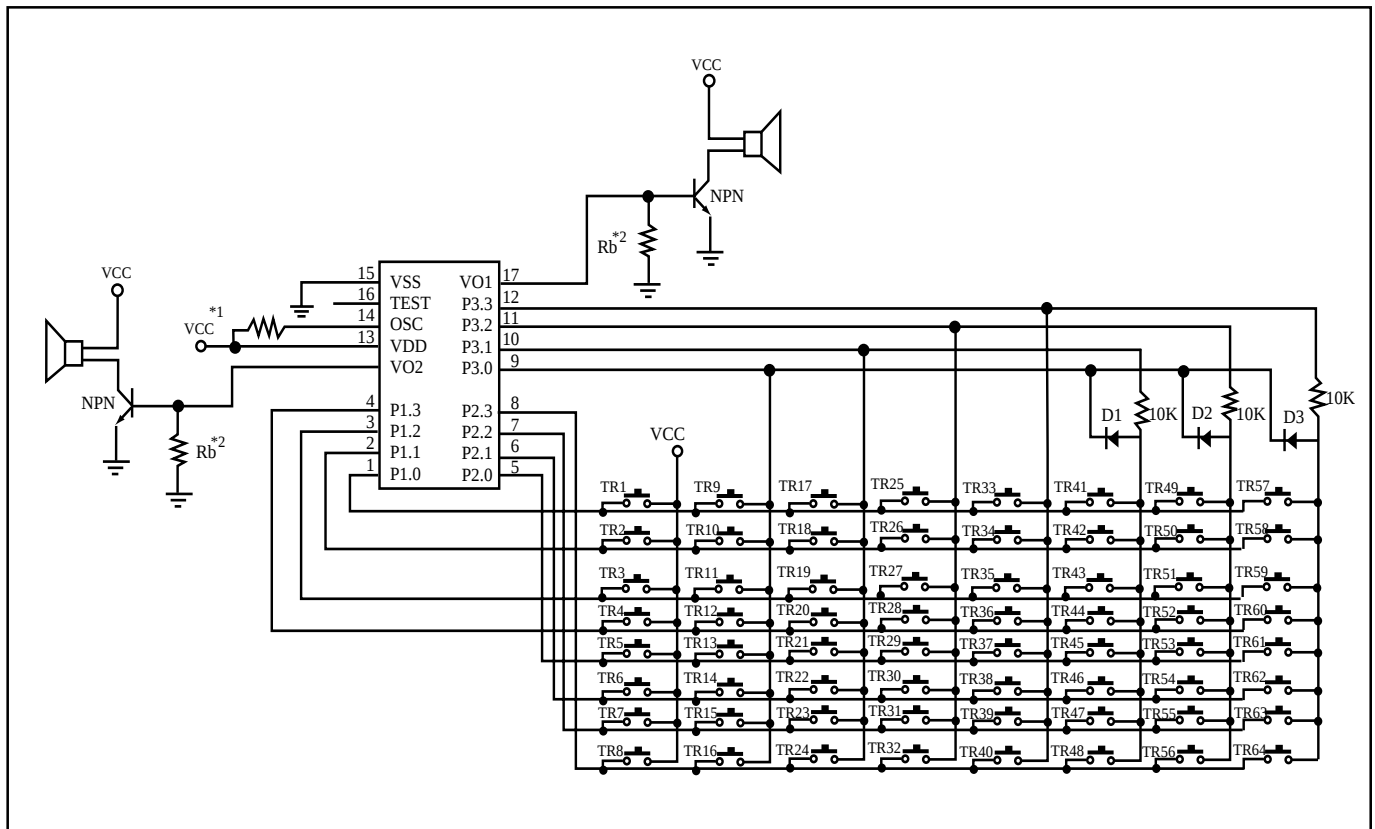


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32-key Application Circuit For EM56200A~EM56600A

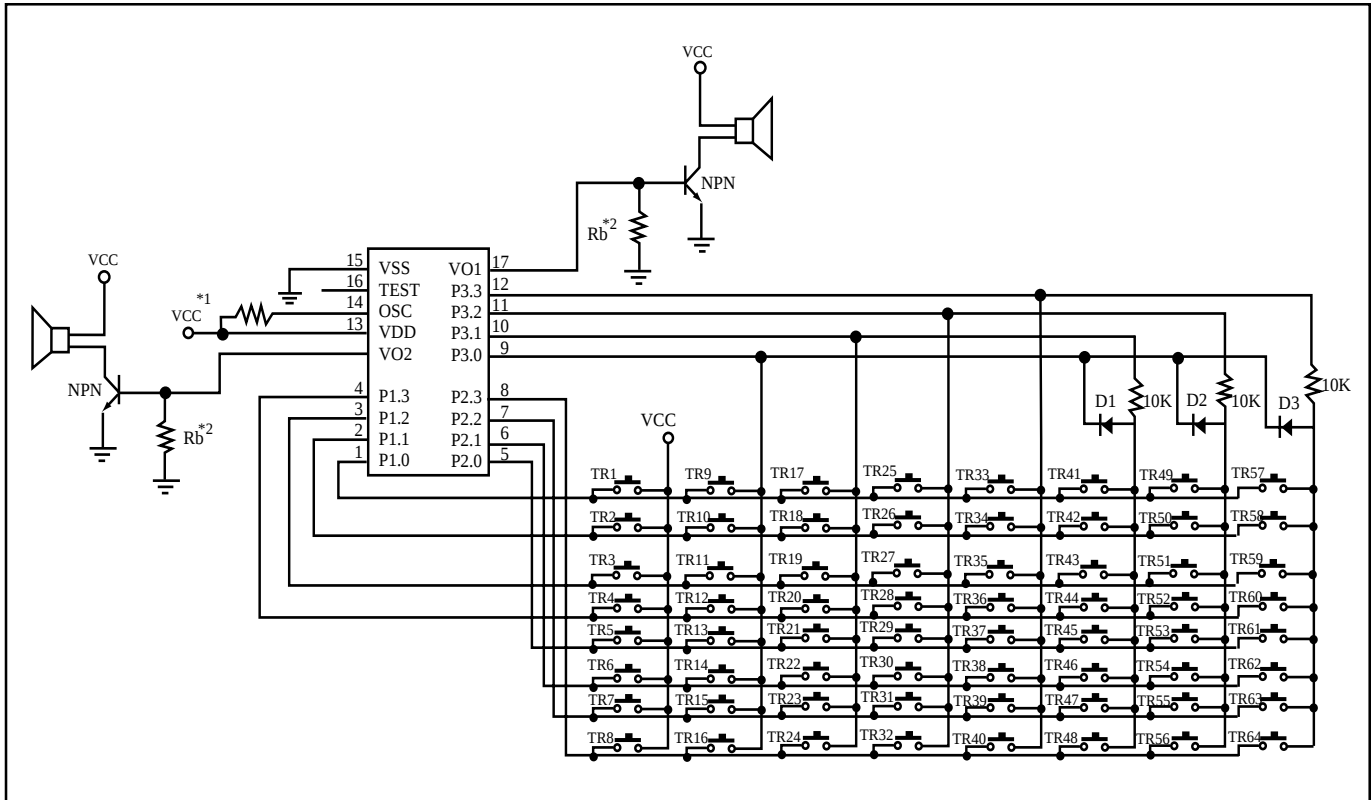


64-key Application Circuit For EM56200A~EM56600A

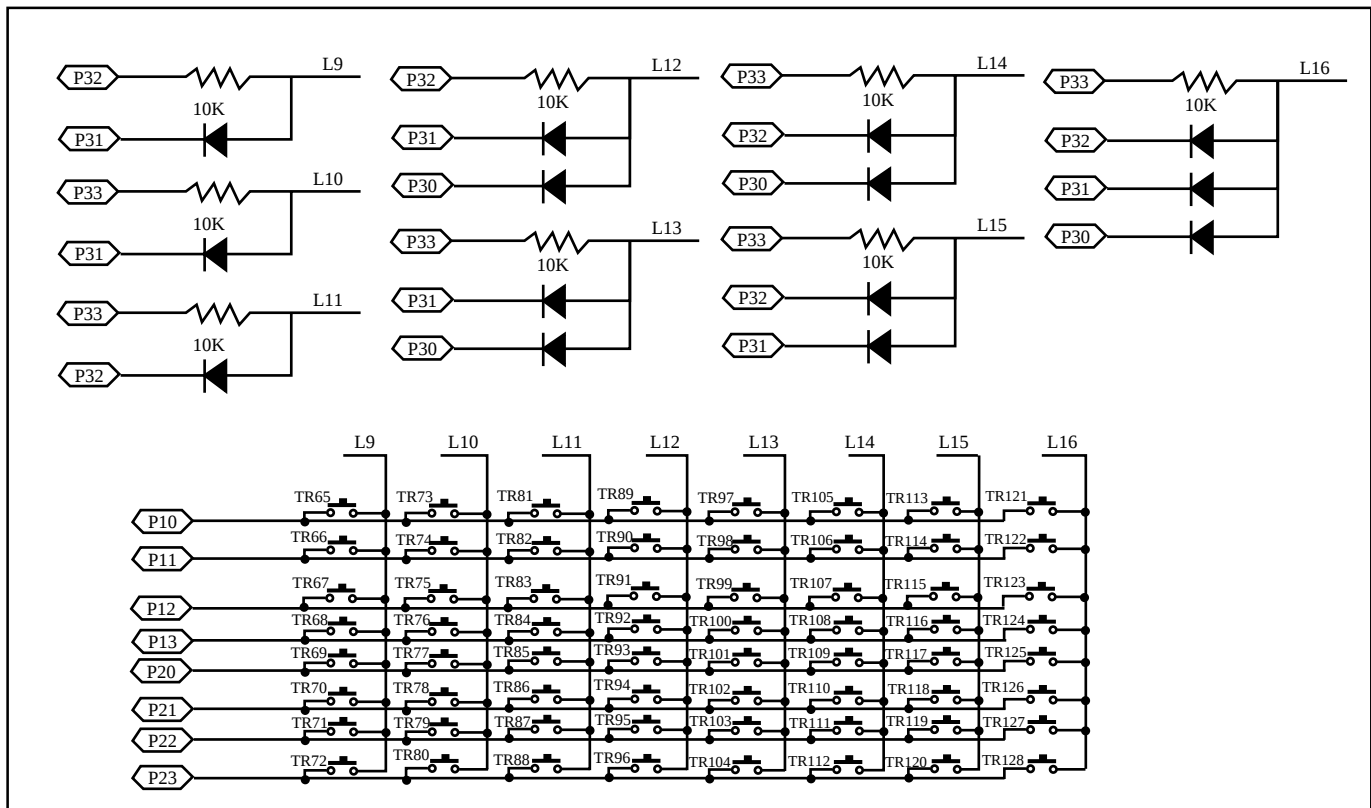


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128-key Application Circuit (A) For EM56200A~EM56600A

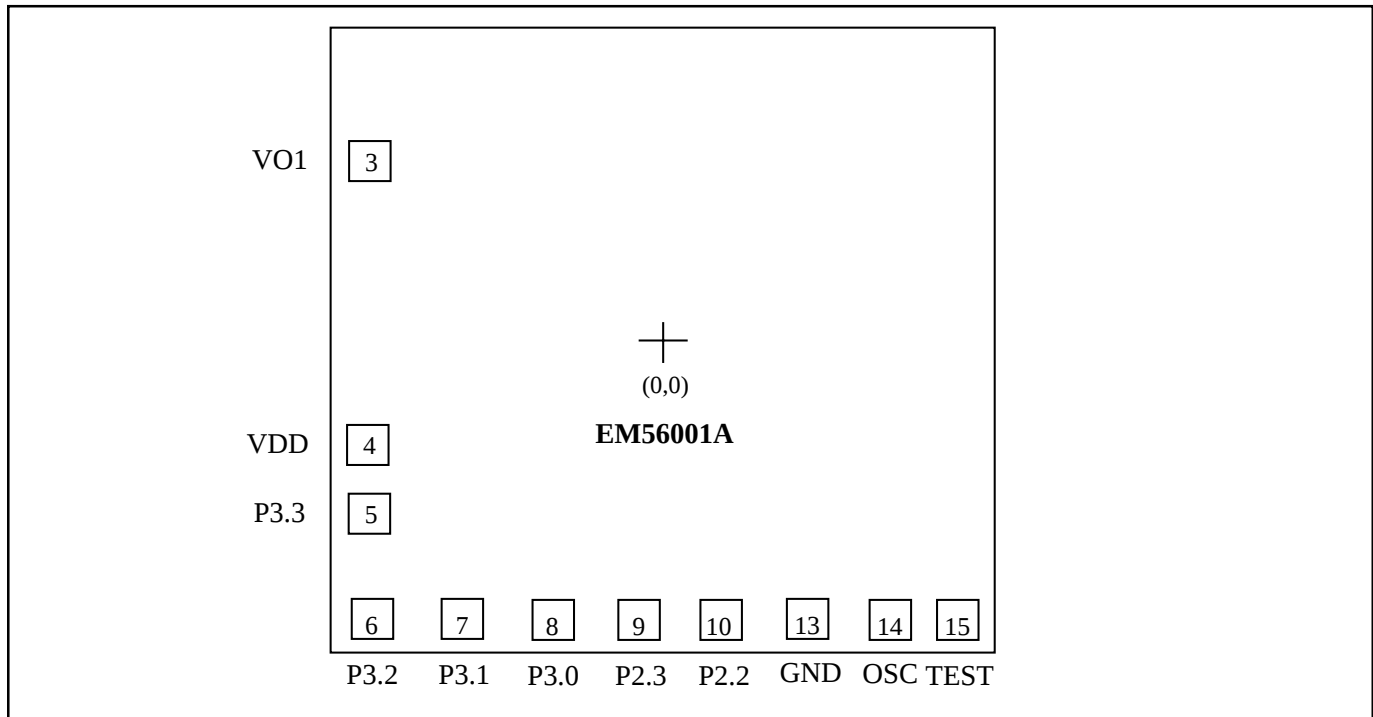


128-key Application Circuit (B) For EM56200A~EM56600A



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PAD DIAGRAM



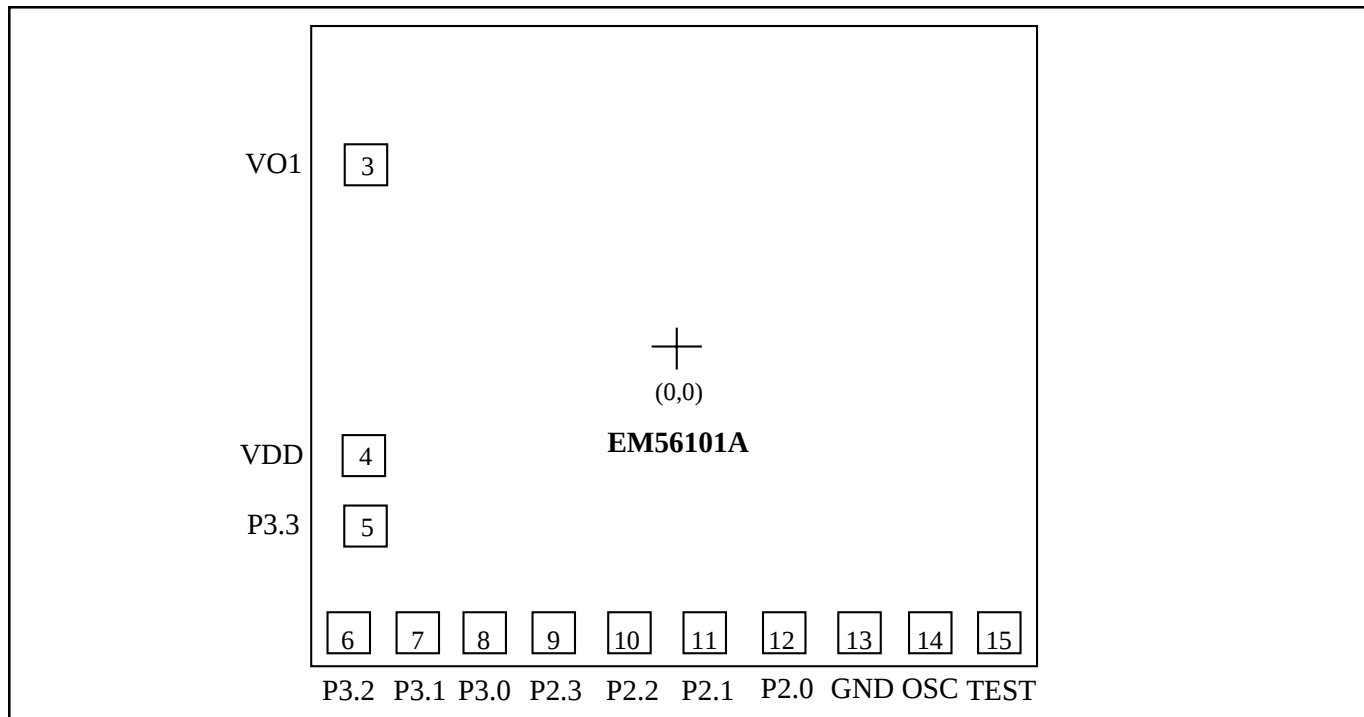
Chip Size : 1300 x 1500 um

For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	NC		
2	NC		
3	VO1	-402.0	421.4
4	VDD	-418.4	-125.4
5	P3.3	-418.4	-269.3
6	P3.2	-440.4	-523.4
7	P3.1	-318.8	-523.4
8	P3.0	-198.2	-523.4
9	P2.3	-76.1	-523.4
10	P2.2	46.3	-523.4
11	NC		
12	NC		
13	GND	190.5	-523.4
14	OSC	321.5	-523.4
15	TEST	442.7	-523.4
16	NC		
17	NC		
18	NC		
19	NC		
20	NC		

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PAD DIAGRAM



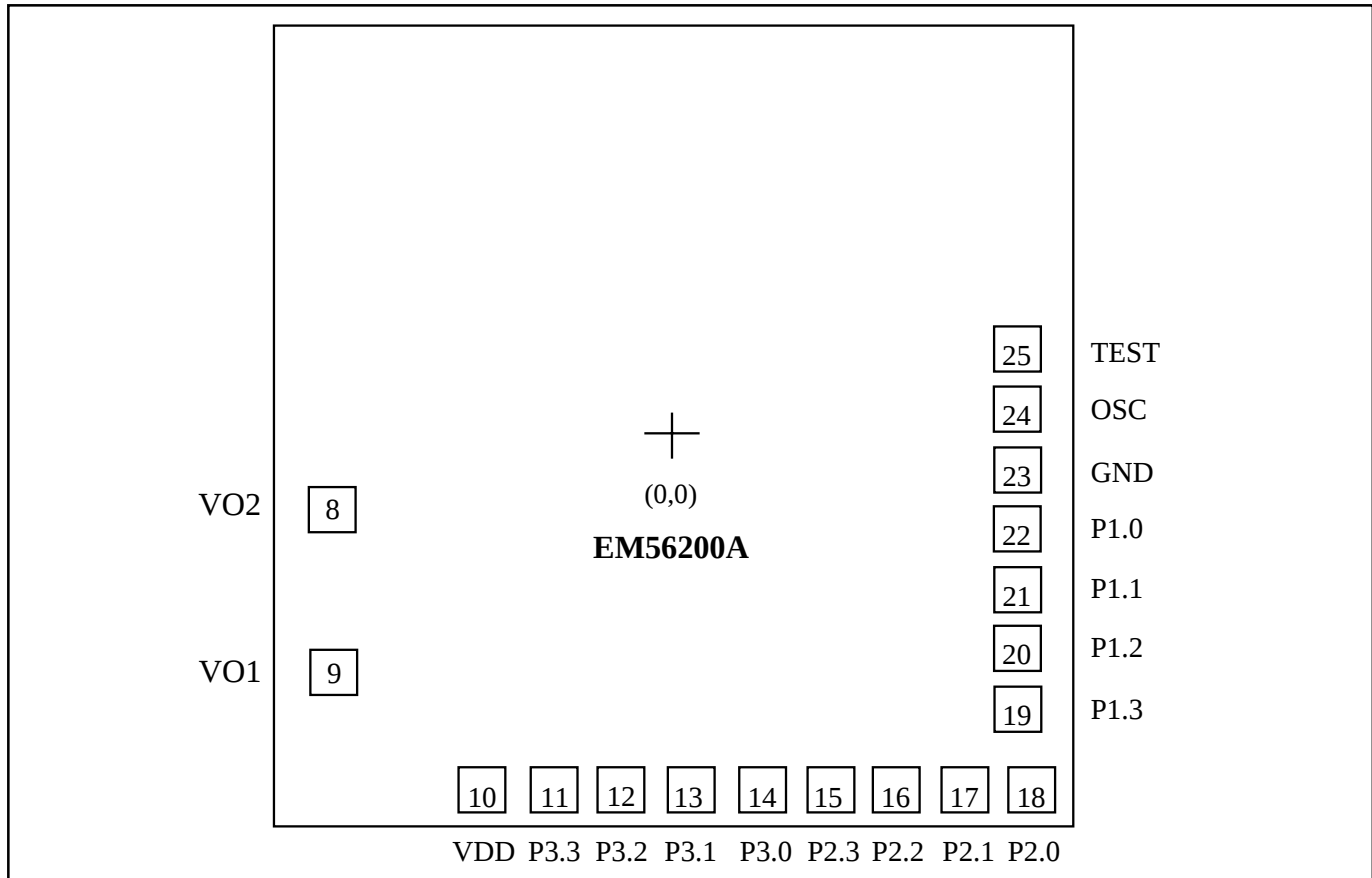
Chip Size : 1500 x 1400 um

For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	NC		
2	NC		
3	VO1	-512.0	391.0
4	VDD	-528.4	-153.7
5	P3.3	-528.4	-284.7
6	P3.2	-564.8	-498.4
7	P3.1	-443.9	-498.4
8	P3.0	-323.0	-498.4
9	P2.3	-200.9	-498.4
10	P2.2	-78.5	-498.4
11	P2.1	43.9	-498.4
12	P2.0	166.3	-498.4
13	GND	310.5	-498.4
14	OSC	441.5	-498.4
15	TEST	562.7	-498.4
16	NC		
17	NC		
18	NC		
19	NC		
20	NC		

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PAD DIAGRAM



Chip Size : 1700 x 1750 um

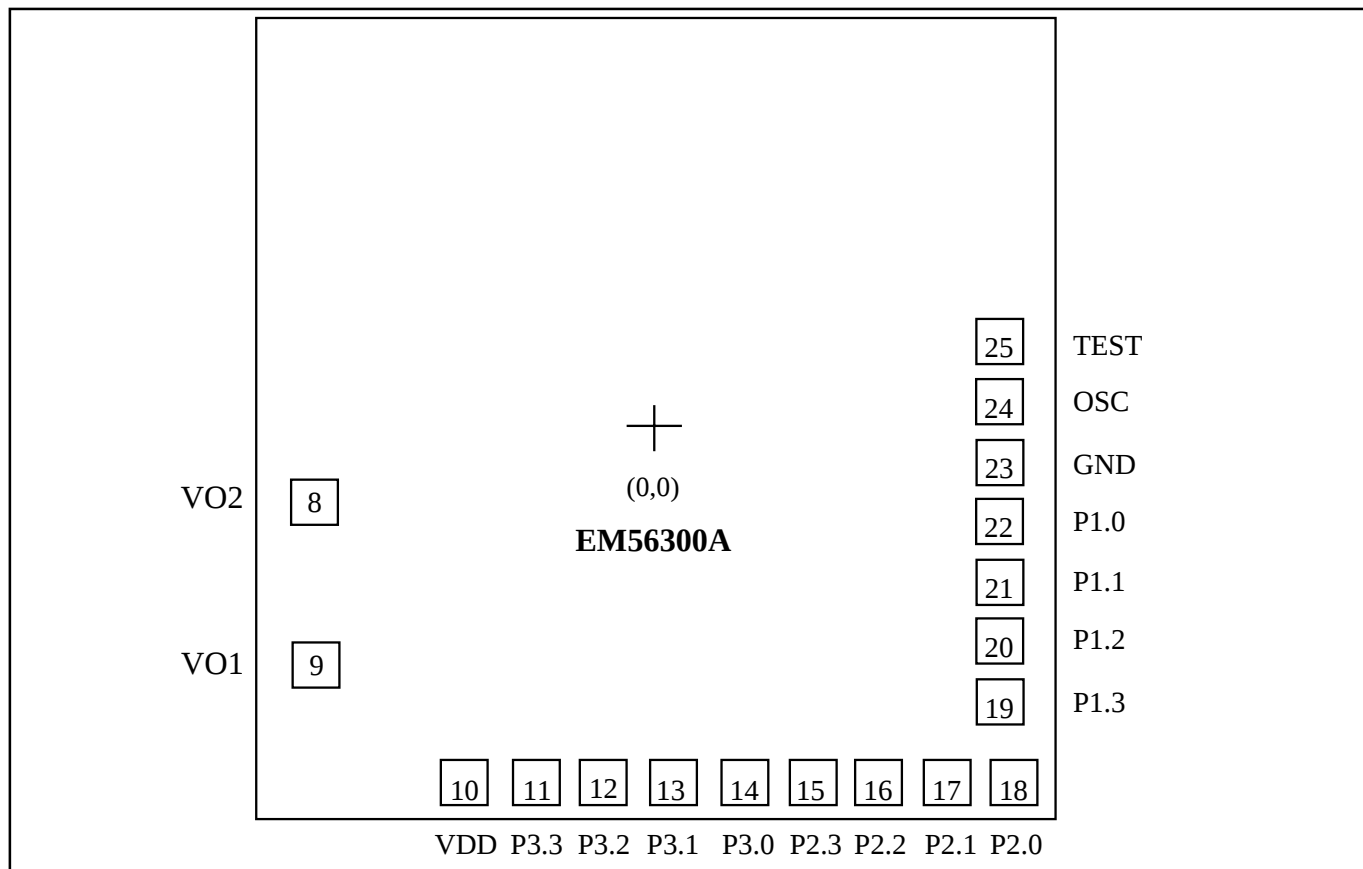
For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	NC		
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	VO2	-572.0	-17.2
9	VO1	-572.0	-401.5
10	VDD	-383.4	-628.4
11	P3.3	-252.4	-628.4
12	P3.2	-131.5	-628.4
13	P3.1	-10.6	-628.4
14	P3.0	110.3	-628.4

Pad No.	Symbol	X	Y
15	P2.3	232.4	-628.4
16	P2.2	354.8	-628.4
17	P2.1	477.2	-628.4
18	P2.0	599.6	-628.4
19	P1.3	588.4	-453.7
20	P1.2	588.4	-331.3
21	P1.1	588.4	-208.9
22	P1.0	588.4	-86.5
23	GND	588.4	57.7
24	OSC	588.4	188.7
25	TEST	588.4	309.9
26	NC		
27	NC		
28	NC		

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PAD DIAGRAM



Chip Size : 1700 x 2000 um

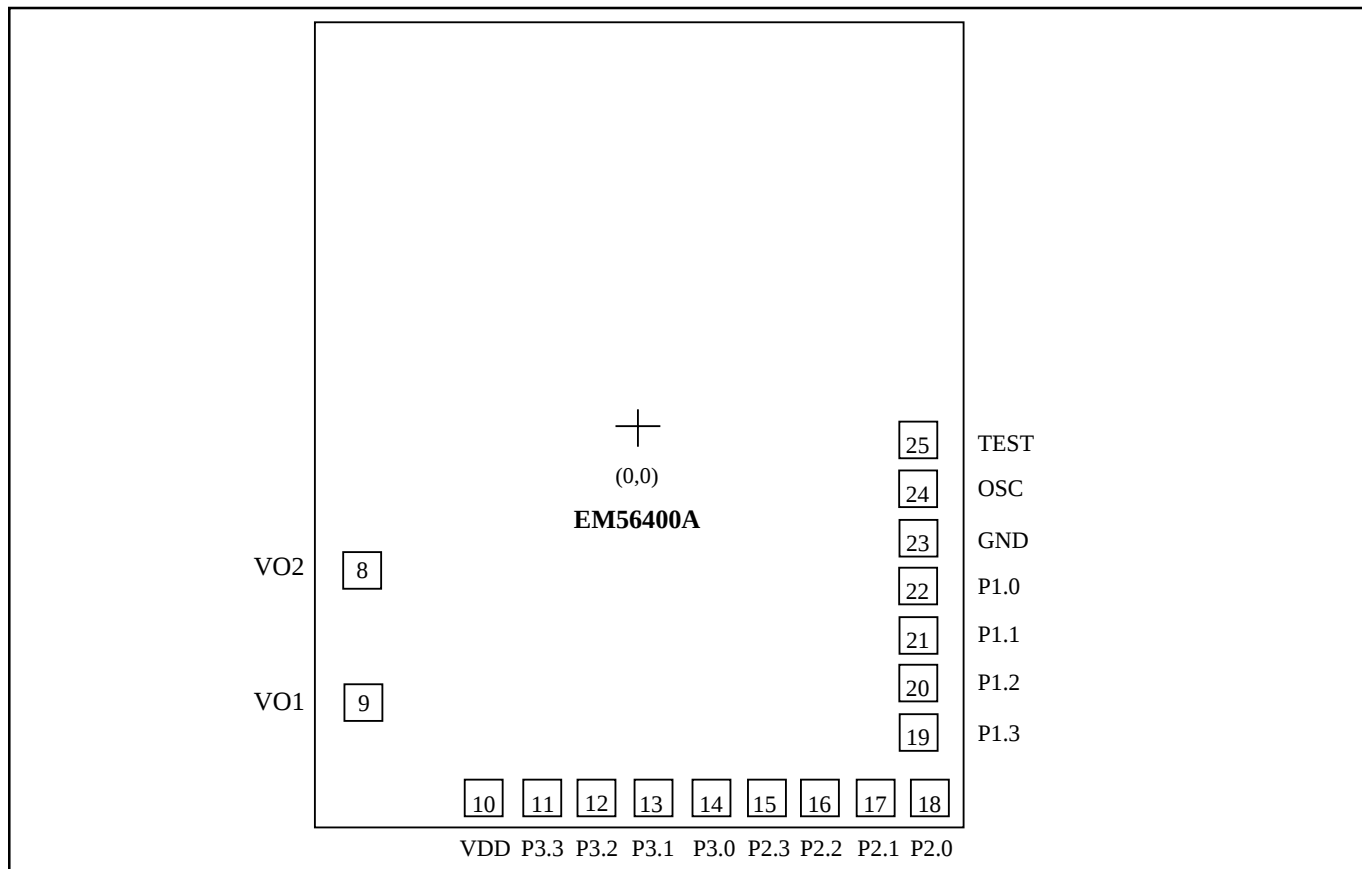
For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	NC		
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	VO2	-572.0	-147.2
9	VO1	-572.0	-531.6
10	VDD	-383.4	-758.4
11	P3.3	-252.4	-758.4
12	P3.2	-131.5	-758.4
13	P3.1	-10.6	-758.4
14	P3.0	110.3	-758.4

Pad No.	Symbol	X	Y
15	P2.3	232.4	-758.4
16	P2.2	354.8	-758.4
17	P2.1	477.2	-758.4
18	P2.0	599.6	-758.4
19	P1.3	588.4	-583.7
20	P1.2	588.4	-461.3
21	P1.1	588.4	-338.9
22	P1.0	588.4	-216.5
23	GND	588.4	-72.3
24	OSC	588.4	58.7
25	TEST	588.4	179.9
26	NC		
27	NC		
28	NC		

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PAD DIAGRAM



Chip Size : 1700 x 2500 um

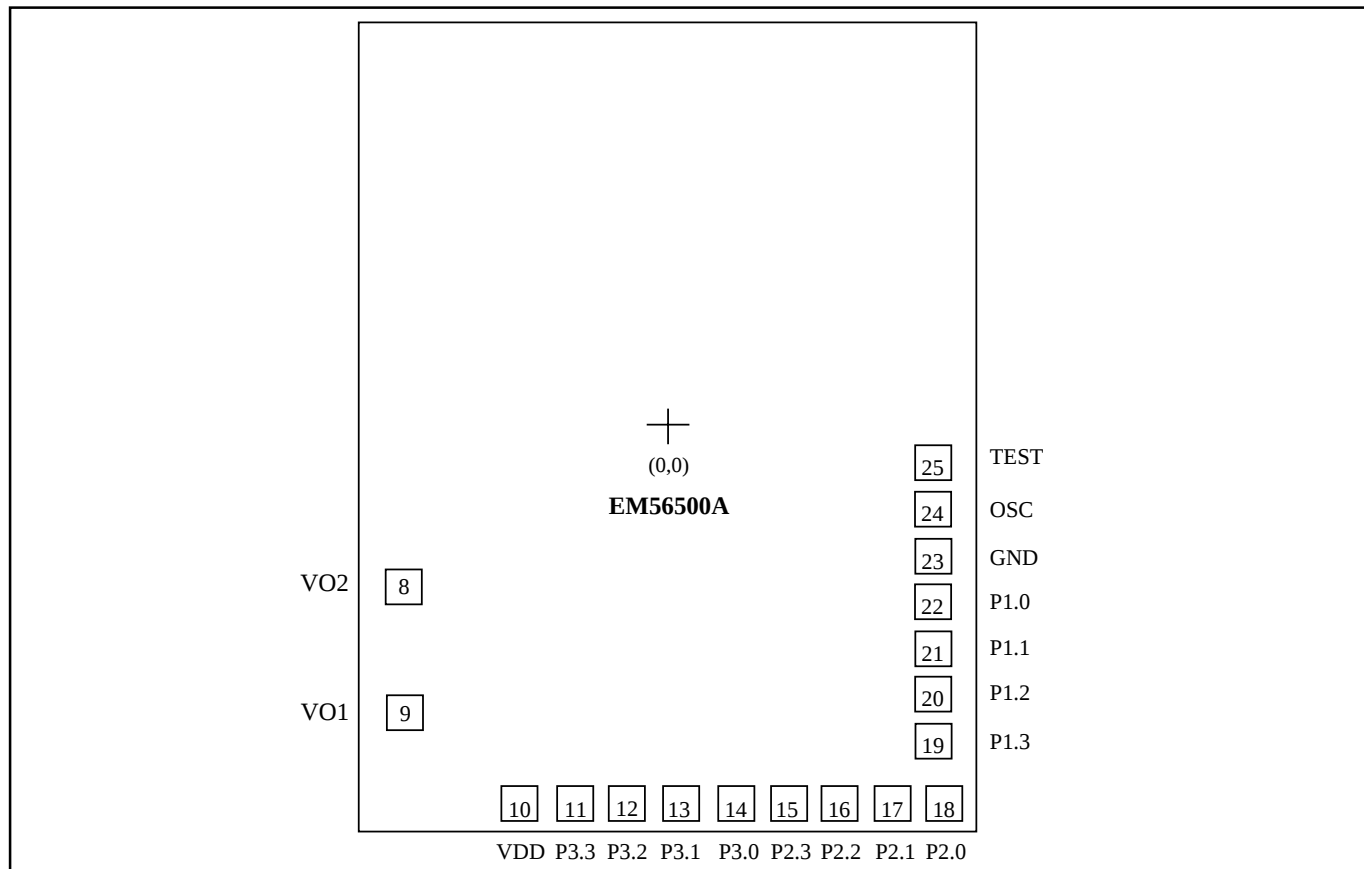
For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	NC		
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	VO2	-572.0	-412.2
9	VO1	-572.0	-796.5
10	VDD	-383.4	-1023.4
11	P3.3	-252.4	-1023.4
12	P3.2	-131.5	-1023.4
13	P3.1	-10.6	-1023.4
14	P3.0	110.3	-1023.4

Pad No.	Symbol	X	Y
15	P2.3	232.4	-1023.4
16	P2.2	354.8	-1023.4
17	P2.1	477.2	-1023.4
18	P2.0	599.6	-1023.4
19	P1.3	588.4	-848.7
20	P1.2	588.4	-726.3
21	P1.1	588.4	-603.9
22	P1.0	588.4	-481.5
23	GND	588.4	-337.3
24	OSC	588.4	-206.3
25	TEST	588.4	-85.1
26	NC		
27	NC		
28	NC		

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PAD DIAGRAM



Chip Size : 1700 x 3600 um

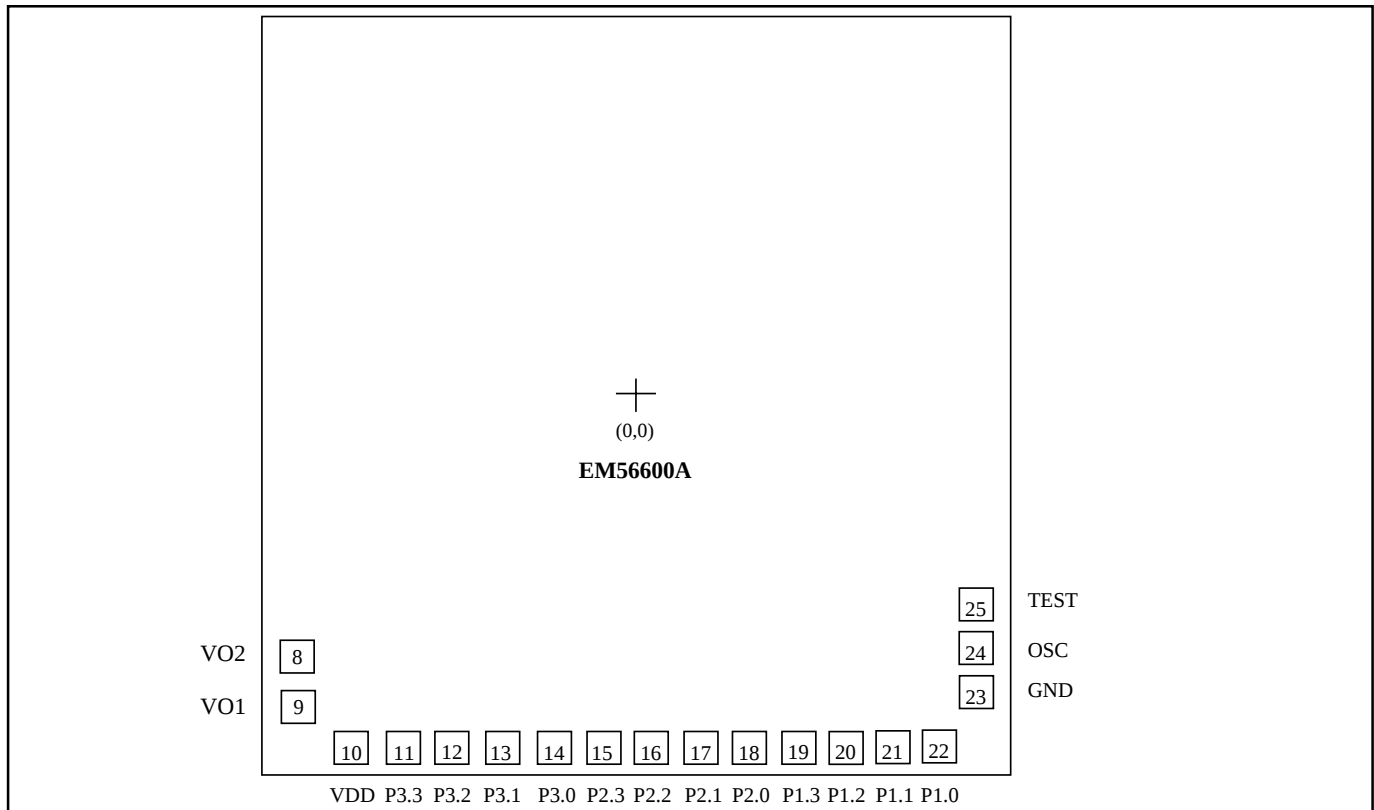
For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	NC		
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	VO2	-572.0	-932.2
9	VO1	-572.0	-1316.6
10	VDD	-383.4	-1543.4
11	P3.3	-252.4	-1543.4
12	P3.2	-131.5	-1543.4
13	P3.1	-10.6	-1543.4
14	P3.0	110.3	-1543.4

Pad No.	Symbol	X	Y
15	P2.3	232.4	-1543.4
16	P2.2	354.8	-1543.4
17	P2.1	477.2	-1543.4
18	P2.0	599.6	-1543.4
19	P1.3	588.4	-1368.7
20	P1.2	588.4	-1246.3
21	P1.1	588.4	-1123.9
22	P1.0	588.4	-1001.5
23	GND	588.4	-857.3
24	OSC	588.4	-726.3
25	TEST	588.4	-605.1
26	NC		
27	NC		
28	NC		

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PAD DIAGRAM



Chip Size : 3050 x 3100 um

For PCB layout, IC substrate must be connected to Vss.

Pad No.	Symbol	X	Y
1	NC		
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	VO2	-1285.0	-1111.6
9	VO1	-1285.0	-1241.6
10	VDD	-884.3	-1340.0
11	P3.3	-695.7	-1340.0
12	P3.2	-519.2	-1340.0
13	P3.1	-342.7	-1340.0
14	P3.0	-166.2	-1340.0
15	P2.3	15.0	-1340.0
16	P2.2	191.5	-1340.0

Pad No.	Symbol	X	Y
17	P2.1	377.4	-1340.0
18	P2.0	553.9	-1340.0
19	P1.3	739.8	-1340.0
20	P1.2	916.3	-1340.0
21	P1.1	1102.2	-1340.0
22	P1.0	1278.7	-1340.0
23	GND	1293.4	-1138.0
24	OSC	1293.4	-1007.0
25	TEST	1293.4	-885.8
26	NC		
27	NC		
28	NC		
29	NC		
30	NC		
31	NC		
32	NC		