BCM® in a VIA Package Bus Converter

BCM3814x60E10A5yzz

Isolated Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 150A continuous low voltage side current
- Fixed transformation ratio(K) of 1/6
- Up to 769W/in^3 power density
- 97.2% peak efficiency
- Integrated ceramic capacitance filtering
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 3814 package
- High MTBF
- Thermally enhanced VIA™ package
- PMBus™ management interface

Typical Applications

- DC Power Distribution
- Information and Communication Technology (ICT) Equipment
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Energy Systems
- Transportation

Product Ratings	
V_{HI} = 54V (36 – 60V)	I_{LO} = up to 150A
V_{LO} = 9V (6 – 10V) (NO LOAD)	K = 1/6

Product Description

The BCM in a VIA package is a high efficiency Bus Converter, operating from a 36 to 60V_{DC} high voltage bus to deliver an isolated 6 to 10V_{DC} unregulated, low voltage.

This unique ultra-low profile module incorporates DC-DC conversion, integrated filtering and PMBus™ commands and controls in a chassis or PCB mount form factor.

The BCM offers low noise, fast transient response and industry leading efficiency and power density. A low voltage side referenced PMBus™ compatible telemetry and control interface provides access to the BCM's internal controller configuration, fault monitoring, and other telemetry functions.

Leveraging the thermal and density benefits of Vicor's VIA packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances.

When combined with downstream Vicor DC-DC conversion components and regulators, the BCM allows the Power Design Engineer to employ a simple, low-profile design which will differentiate the end system without compromising on cost or performance metrics.

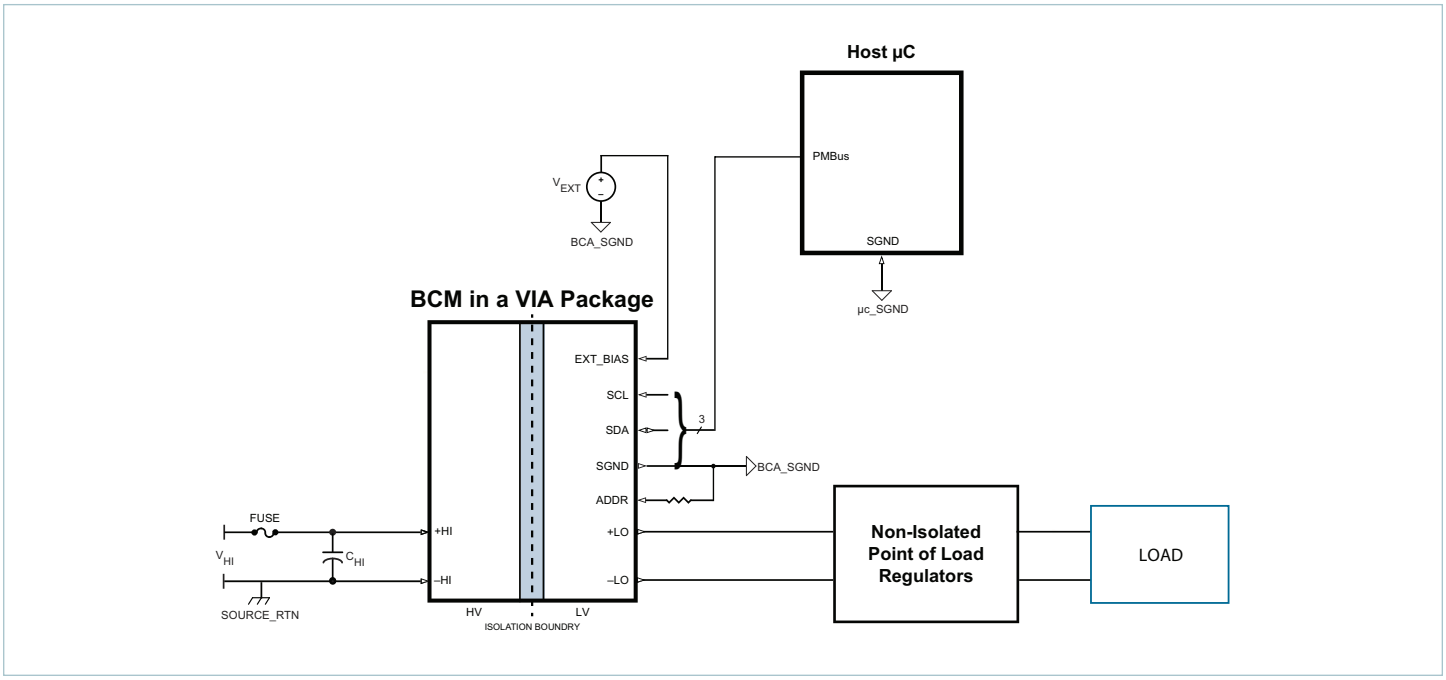
Size:
3.76 x 1.40 x 0.37 in
95.59 x 35.54 x 9.40 mm

Part Ordering Information

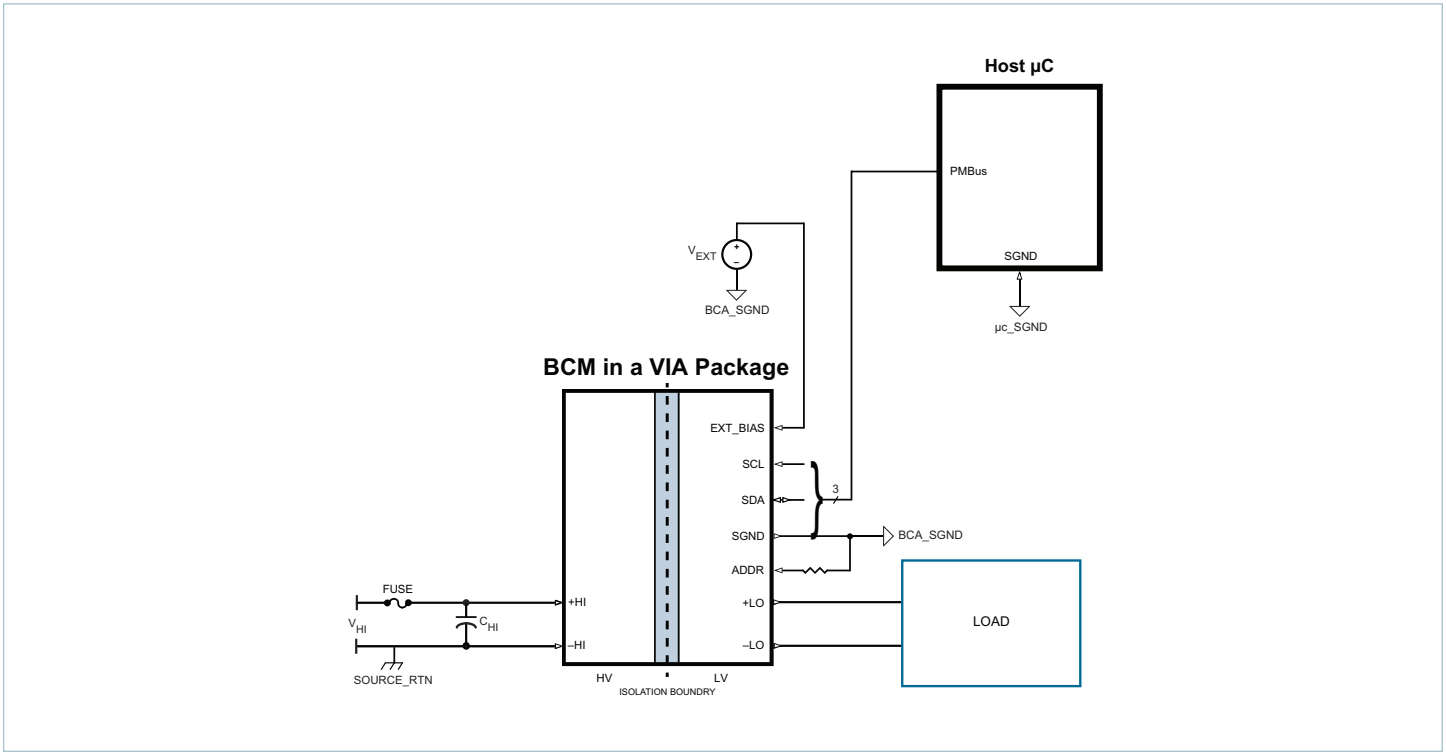
Product Function	Package Length	Package Width	Package Type	Max High Side Voltage	High Side Voltage Range Ratio	Max Low Side Voltage	Max Low Side Current	Product Grade (Case Temperature)	Option Field
BCM	38	14	x	60	E	10	A5	y	zz
BCM = Bus Converter Module	Length in Inches x 10	Width in Inches x 10	B = Board VIA V = Chassis VIA	Internal Reference				C = -20 to 100°C[1] T = -40 to 100°C[1]	02 = Chassis/PMBus 06 = Short Pin/PMBus 10 = Long Pin/PMBus

[1] High Temperature Current Derating may apply; See Figure 1, specified thermal operating area.

Typical Application

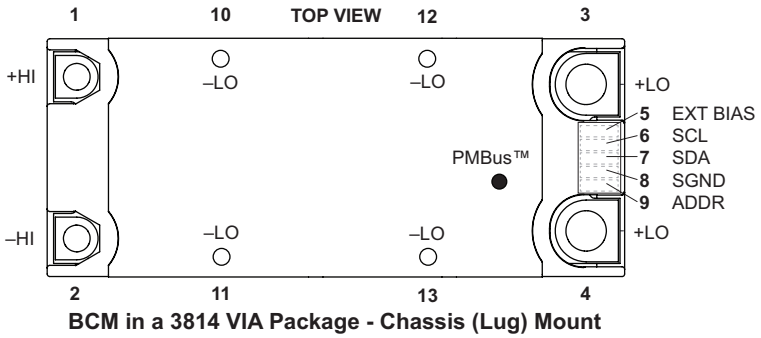


BCM3814x60E10A5yzz at point of load

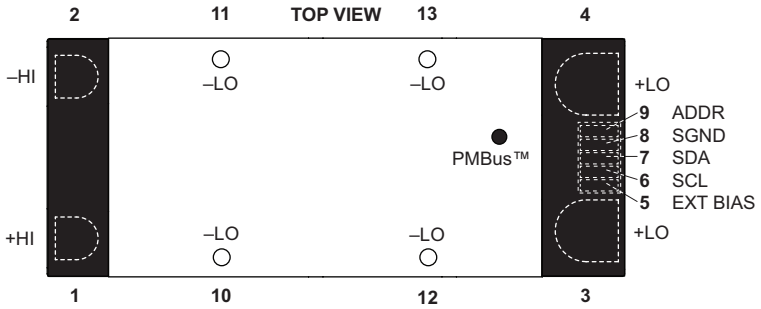


BCM3814x60E10A5yzz direct to load

Pin Configuration



BCM in a 3814 VIA Package - Chassis (Lug) Mount



BCM in a 3814 VIA Package - Board (PCB) Mount

Note: The dot on the VIA housing indicates the location of the signal pin 9.

Pin Descriptions

Pin Number	Signal Name	Type	Function
1	+HI	HIGH SIDE POWER	Positive transformer power terminal on high voltage side
2	–HI	HIGH SIDE POWER RETURN	Negative transformer power terminal on high voltage side
3, 4	+LO	LOW SIDE POWER	Positive transformer power terminal on low voltage side
5	EXT BIAS	INPUT	5V supply input
6	SCL	INPUT	I^2C Clock, PMBus™ Compatible
7	SDA	INPUT/OUTPUT	I^2C Data, PMBus™ Compatible
8	SGND	LOW SIDE SIGNAL RETURN	Signal Ground
9	ADDR	INPUT	Address assignment - Resistor based
10, 11, 12, 13	–LO	LOW SIDE POWER RETURN	Negative transformer power terminal on low voltage side

Notes: All signal pins (5, 6, 7, 8, 9) are referenced to low voltage side and isolated from the high voltage side.
Keep SGND Signal of the BCM in a VIA package separated from the low voltage side power return terminal (–LO) in electrical design.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+HI to –HI		-1	80	V
HI_DC or LO_DC slew rate			1	V/µs
+LO to –LO		-1	15	V
EXT BIAS to SGND		-0.3	10	V
			0.15	A
SCL to SGND		-0.3	5.5	V
SDA to SGND		-0.3	5.5	V
ADDR to SGND		-0.3	3.6	V
Dielectric Withstand*	See note below			
High Voltage Side to Case	Basic Insulation	1500		V_{DC}
High Voltage Side to Low voltage Side	Basic Insulation	1500		V_{DC}
Low Voltage Side to Case	Functional Insulation	N/A		V_{DC}

* The SELV side (-LO) is directly connected to the case of the BCM in a VIA package.

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain High Voltage Side to Low Voltage Side Specification (Forward Direction)						
High Side Input Voltage range, continuous	V_{HI_DC}		**36**		**60**	V
V_{HI} µController	$V_{\mu C\_ACTIVE}$	V_{HI_DC} voltage where µC is initialized, (powertrain inactive)			14	V
HI to LO Input Quiescent Current	I_{HI_Q}	Disabled, V_{HI_DC} = 54V		5		mA
		T_{CASE} ≤ 100°C			10	
HI to LO No Load Power Dissipation	P_{HI_NL}	V_{HI_DC} = 54V, T_{CASE} = 25°C		7.2	9	W
		V_{HI_DC} = 54V	**5**		**14**	
		V_{HI_DC} = 36V to 60V, T_{CASE} = 25 °C			12	
		V_{HI_DC} = 36V to 60V			**17**	
HI to LO Inrush Current Peak	$I_{HI\_INR\_PK}$	V_{HI_DC} = 60V, C_{LO_EXT} = 4000 µF, R_{LOAD_LO} = 20% of full load current		30		A
		T_{CASE} ≤ 100°C			35	
DC High Side Input Current	$I_{HI\_IN\_DC}$	At $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} ≤ 85°C			25.5	A
Transformation Ratio	K	High voltage to low voltage, K = V_{LO_DC} / V_{HI_DC}, at no load		1/6		V/V
Low Side Output Current (continuous)	$I_{LO\_OUT\_DC}$	T_{CASE} ≤ 85°C			150	A
Low Side Output Current (pulsed)	$I_{LO\_OUT\_PULSE}$	10 ms pulse, 25% Duty cycle, $I_{LO\_OUT\_AVG}$ ≤ 50% rated $I_{LO\_OUT\_DC}$			180	A
HI to LO Efficiency (ambient)	η_{AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A	95.2	95.8		%
		V_{HI_DC} = 36V to 60V, $I_{LO\_OUT\_DC}$ = 150A	93.6			
		V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 75A	96.7	97.2		
HI to LO Efficiency (hot)	η_{HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = 85°C	95.4	95.6		%
HI to LO Efficiency (over load range)	$\eta_{20\%}$	30A < $I_{LO\_OUT\_DC}$ < 150A	93			%
HI to LO Output Resistance	R_{LO_COLD}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = -40°C	0.9	1.7	2.1	mΩ
	R_{LO_AMB}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A	2	2.1	2.4	
	R_{LO_HOT}	V_{HI_DC} = 54V, $I_{LO\_OUT\_DC}$ = 150A, T_{CASE} = 85°C	1.6	2.3	2.6	
Switching Frequency	F_{SW}	Frequency of the LO Side Voltage Ripple = 2x F_{SW}	**0.85**	0.90	**0.95**	MHz
Low Side Output Voltage Ripple	$V_{LO\_OUT\_PP}$	C_{LO_EXT} = 0µF, $I_{LO\_OUT\_DC}$ = 150A, V_{HI_DC} = 54V, 20MHz BW		120		mV
		T_{CASE} ≤ 100°C			200	

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
General Powertrain High Voltage Side to Low Voltage Side Specification (Forward Direction) Cont.						
Effective HI Side Capacitance (Internal)	C_{HI_INT}	Effective Value at $54V_{HI\_DC}$		11.2		µF
Effective LO Side Capacitance (Internal)	C_{LO_INT}	Effective Value at $9V_{LO\_DC}$		202		µF
Effective LO Side Output Capacitance (External)	$C_{LO\_OUT\_EXT}$	Excessive capacitance may drive module into SC protection			**6000**	µF
Effective LO Side Output Capacitance (External)	$C_{LO\_OUT\_AEXT}$	$C_{LO\_OUT\_AEXT}$ Max = N * 0.5 * $C_{LO\_OUT\_EXT\ MAX}$, where N = the number of units in parallel				
Powertrain Protection High Voltage Side to Low Voltage Side (Forward Direction)						
Auto Restart Time	$t_{AUTO\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given $V_{HI\_DC} > V_{HI\_UVLO+}$	**490**		**560**	ms
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**63**	67	**71**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**61**	65	**69**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			2		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Soft-Start Time	$t_{HI\_SOFT-START}$	From powertrain active. Fast Current limit protection disabled during Soft-Start		1		ms
LO Side Output Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**180**	204	**240**	A
LO Side Output Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3		ms
LO Side Output Short Circuit Protection Trip Threshold	$I_{LO\_OUT\_SCP}$		**195**			A
LO Side Output Short Circuit Protection Response Time	$t_{LO\_OUT\_SCP}$			1		µs
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC (Internal Temperature)	**125**			°C

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Supervisory Limits HIGH VOLTAGE SIDE to LOW VOLTAGE SIDE (Forward Direction)						
HI Side Overvoltage Lockout Threshold	V_{HI_OVLO+}		**64**	66	**68**	V
HI Side Overvoltage Recovery Threshold	V_{HI_OVLO-}		**60**	64	**66**	V
HI Side Overvoltage Lockout Hysteresis	$V_{HI\_OVLO\_HYST}$			2		V
HI Side Overvoltage Lockout Response Time	t_{HI_OVLO}			100		µs
HI Side Undervoltage Lockout Threshold	V_{HI_UVLO-}		**26**	28	**30**	V
HI Side Undervoltage Recovery Threshold	V_{HI_UVLO+}		**28**	30	**32**	V
HI Side Undervoltage Lockout Hysteresis	$V_{HI\_UVLO\_HYST}$			2		V
HI Side Undervoltage Lockout Response Time	t_{HI_UVLO}			100		µs
HI Side Undervoltage Startup Delay	$t_{HI\_UVLO+\_DELAY}$	From V_{HI_DC} = V_{HI_UVLO+} to powertrain active, (i.e One time Startup delay form application of V_{HI_DC} to V_{LO_DC})		20		ms
LO Side Output Overcurrent Trip Threshold	$I_{LO\_OUT\_OCP}$		**193**	204	**215**	A
LO Side Output Overcurrent Response Time Constant	$t_{LO\_OUT\_OCP}$	Effective internal RC filter		3		ms
Overtemperature Shutdown Threshold	t_{OTP+}	Temperature sensor located inside controller IC (Internal Temperature)	**125**			°C
Overtemperature Recovery Threshold	t_{OTP-}	Temperature sensor located inside controller IC (Internal Temperature)	105	110	115	°C
Undertemperature Shutdown Threshold	t_{UTP}	Temperature sensor located inside controller IC; Protection not available for M-Grade units.			-45	°C
Undertemperature Restart Time	$t_{UTP\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given V_{HI_DC} > V_{HI_UVLO+}		3		s

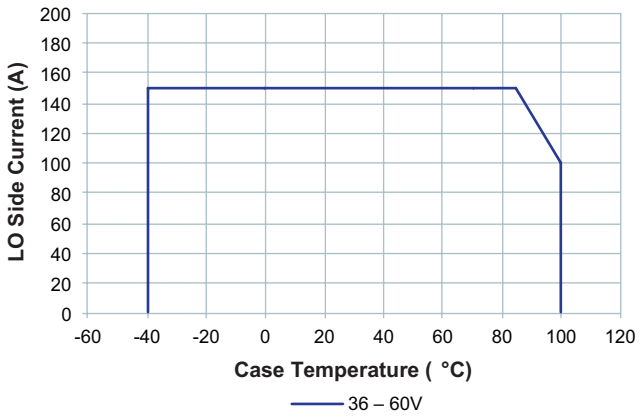


Figure 1 *— Specified thermal operating area*

1. The BCM in a VIA Package is cooled through bottom case (bottom housing).
2. The thermal rating of the BCM in a VIA Package is based on typical measured device efficiency.
3. The case temperature in the graph is the measured temperature of the bottom housing, such that operating internal junction temperature of the BCM in a VIA Package does not exceed 125°C.

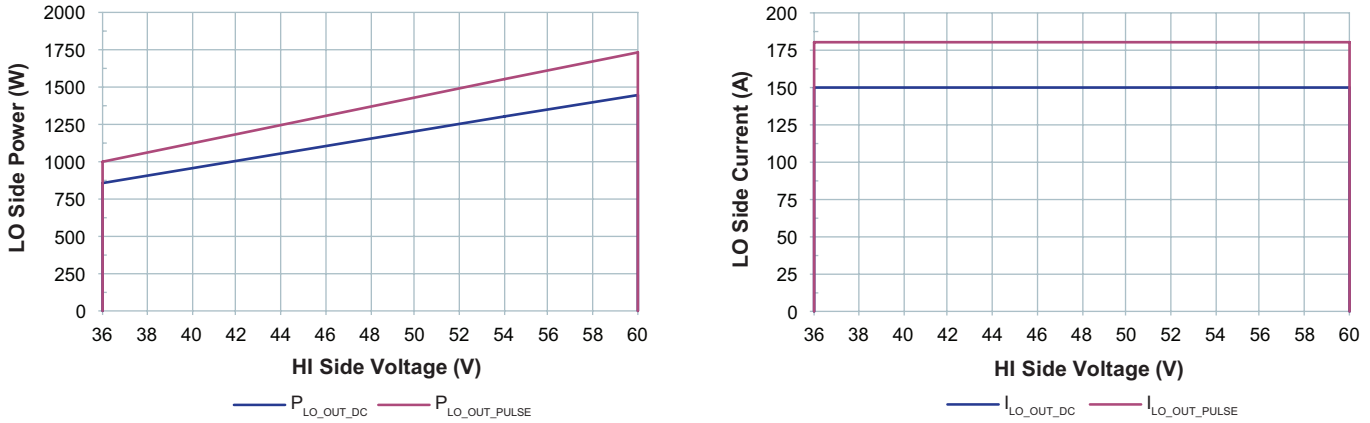


Figure 2 *— Specified electrical operating area using rated R_{LO_HOT}*

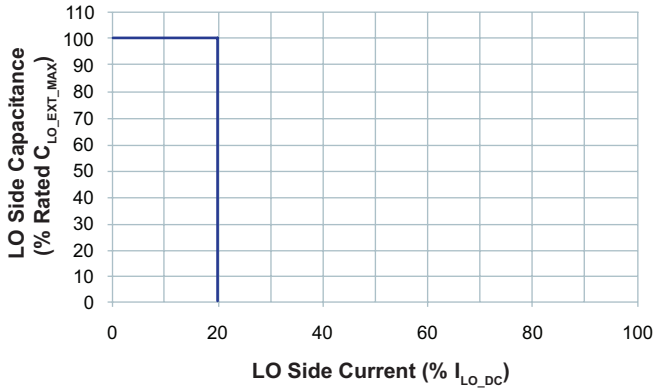


Figure 3 *— Specified HI side start-up into load current and external capacitance*

PMBus™ Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted.

Monitored Telemetry					
• **The BCM communication version is not intended to be used without a Digital Supervisor.**					
ATTRIBUTE	**DIGITAL SUPERVISOR PMBus™ READ COMMAND**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**UPDATE RATE**	**REPORTED UNITS**
HI Side Voltage	(88h) READ_VIN	± 5%(LL - HL)	28V to 66V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
HI Side Current	(89h) READ_IIN	± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	-1A to 34A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Voltage[1]	(8Bh) READ_VOUT	± 5%(LL - HL)	4.7V to 11V	100µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
LO Side Current	(8Ch) READ_IOUT	± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	-6A to 204A	100µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
LO Side Resistance	(D4h) READ_ROUT	± 5%(50 - 100% of FL) at NL ± 10%(50 - 100% of FL)(LL - HL)	500u to 3000u	100ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature[2]	(8Dh) READ_TEMPERATURE_1	± 7°C(Full Range)	- 55°C to 130°C	100ms	$T_{ACTUAL} = T_{REPORTED}$

[1] Default READ LO Side Voltage returned when unit is disabled = -300V.
[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameter					
• Factory setting of all below Thresholds and Warning limits are 100% of listed protection values. • Variables can be written only when module is disabled either EN pulled low or $V_{HI} < V_{HI\_UVLO-}$. • Module must remain in a disabled mode for 3ms after any changes to the below variables allowing ample time to commit changes to EEPROM.					
ATTRIBUTE	**DIGITAL SUPERVISOR PMBus™ COMMAND [3]**	**CONDITIONS / NOTES**	**ACCURACY (RATED RANGE)**	**FUNCTIONAL REPORTING RANGE**	**DEFAULT VALUE**
HI Side Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{HI_OVLO-} is automatically 3% lower than this set point	± 5%(LL - HL)	28V to 66V	100%
HI Side Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5%(LL - HL)	28V to 66V	100%
HI Side Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5%(LL - HL)	28V or 66V	100%
HI Side Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	0 to 34A	100%
HI Side Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 20%(10 - 20% of FL) ± 5%(20 - 133% of FL)	0 to 34A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal Temperature	± 7°C(Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal Temperature	± 7°C(Full Range)	0 to 125°C	100%
Turn on Delay	(60h) TON_DELAY	Additional time delay to the Undervoltage Startup Delay	± 50µs	0 to 100ms	0ms

[3] Refer to internal µc datasheet for complete list of supported commands.

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); all other specifications are at T_{CASE} = 25°C unless otherwise noted. **Please note:** For chassis mount model, Vicor part number 42550 will be needed for applications requiring the use of the signal pins. Signal cable 42550 is rated up to five insertions and extractions. To avoid unnecessary stress on the connector, the cable should be tied to the chassis.

EXT. BIAS (VDDB) Pin

- 5V supply input, required to power the circuitry internal to the BCM in a VIA package for communication signals such as SCL, SDA, ADDR etc
- Voltage to EXT BIAS pin is needed for PMBus™ enable and disable control. It is not needed for PMBus monitoring voltage, current, power or temperature. Lower voltage is better. It will help to lower the power dissapation in the internal regulator that is generating 3.3V voltage for communication circuits.
- Apply voltage to this pin between 4.5V and 9V. The nominal voltage is 5V.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4.5	5	9	V
		VDDB Current consumption	I_{VDDB}				50	mA
	Startup	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} Slew Rate = 1V/µs		3.5		A
		Turn on time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

SGND Pin

- This pin is supply return pin for Ext. Bias (VDDB) pin.
- All input and output signals (SCL, SDA, ADDR) are referenced to SGND pin.

Note: Keep SGND Signal of the BCM in a VIA package separated from the low voltage side power return terminal (–LO) in electrical design.

Address (ADDR) Pin

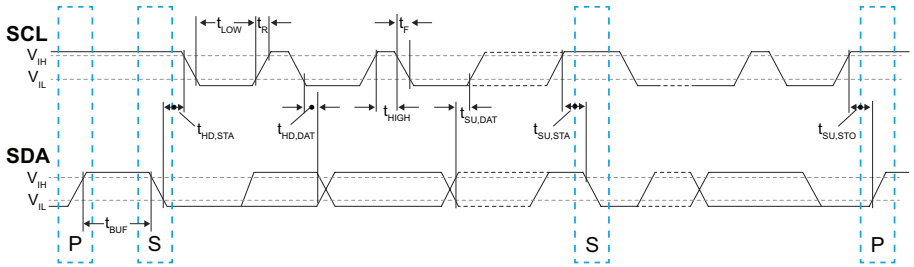
- This pin programs only a Fixed and Persistent slave address for BCM in a VIA package.
- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during startup and is used until power is reset.
- This pin has 10kΩ pullup resistor internally between ADDR pin and internal VDD.
- 16 addresses are available. Relative to nominal value of internal VDD (V_{VDD_NOM} = 3.3V), a 206.25mV range per address.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MULTI-LEVEL INPUT	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR leakage current	I_{SADDR}	Leakage current			1	µA
	Startup	ADDR registration time	t_{SADDR}	From $V_{VDD\_IN\_MIN}$		1		ms

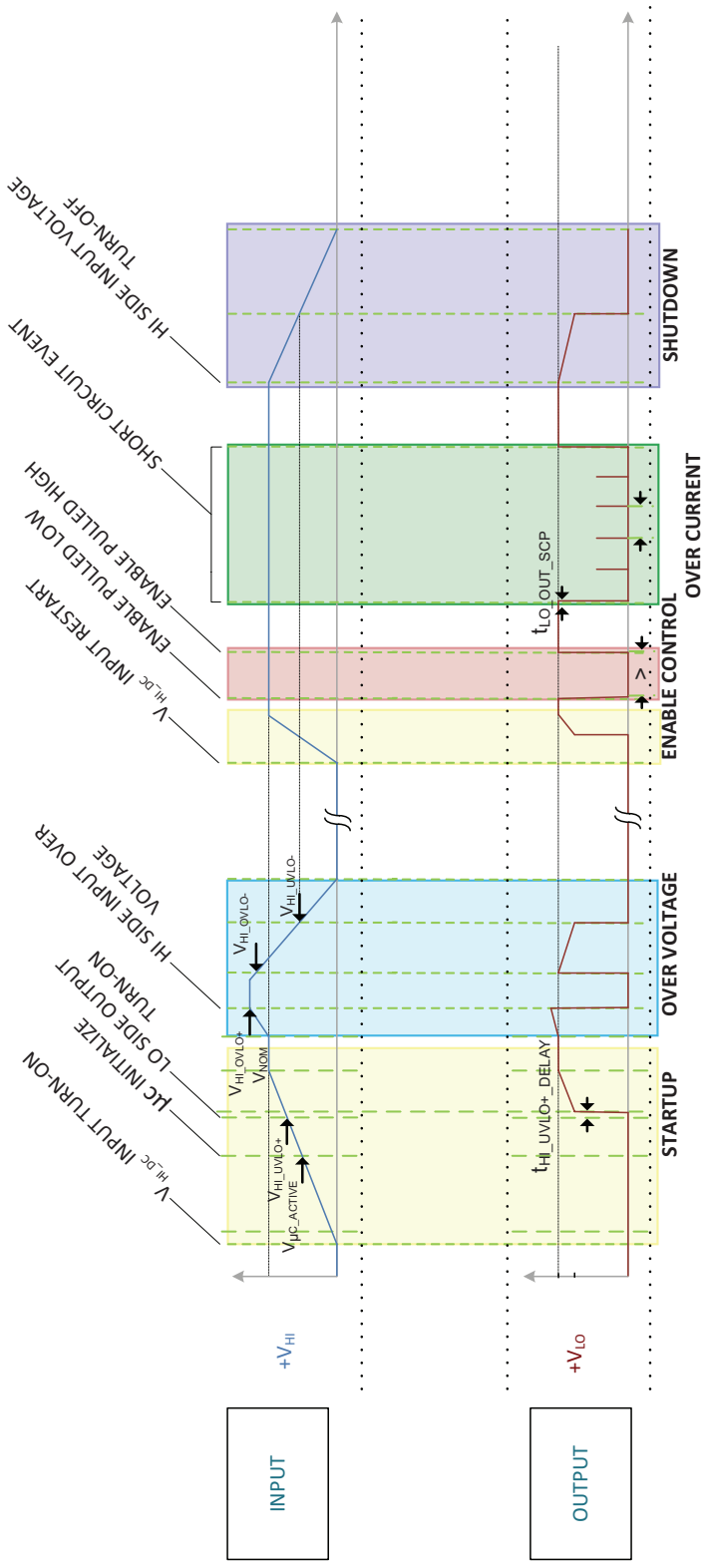
Serial Clock input (SCL) AND Serial Data (SDA) Pins

- High‑power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is signal not supported.
- PMBus™ command compatible.
- The internal µC requires the use of a flip‑flop to drive SSTOP. See system diagram section for more details.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}	V_{VDD_IN} = 3.3V	2.1			V
			V_{IL}	V_{VDD_IN} = 3.3V			0.8	V
		Output Voltage Threshold	V_{OH}	V_{VDD_IN} = 3.3V	3			V
			V_{OL}	V_{VDD_IN} = 3.3V			0.4	V
		Leakage current	I_{LEAK_PIN}	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10MHz to 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	KHz
		Free time between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold time after Start or Repeated Start condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup time	$t_{SU:STA}$		0.6			µs
		Stop Condition setup time	$t_{SU:STO}$		0.6			µs
		Data Hold time	$t_{HD:DAT}$		300			ns
		Data Setup time	$t_{SU:DAT}$		100			ns
		Clock low time out	$t_{TIMEOUT}$		25		35	ms
		Clock low period	t_{LOW}		1.3			µs
		Clock high period	t_{HIGH}		0.6		50	µs
		Cumulative clock low extend time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall time	t_F	Measured from (V_{IL_MAX} ‑0.15) to (V_{IH_MIN} + 0.15)	20		300	ns
		Clock or Data Rise time	t_R	0.9 • $V_{VDD\_IN\_MAX}$ to (V_{IL_MAX} ‑0.15)	20		300	ns



Timing diagram (Foward Direction)



Application Characteristics

Product is mounted and temperature controlled via top side cold plate, unless otherwise noted. All data presented in this section are collected data from high voltage side sourced units processing power in forward direction.See associated figures for general trend data.

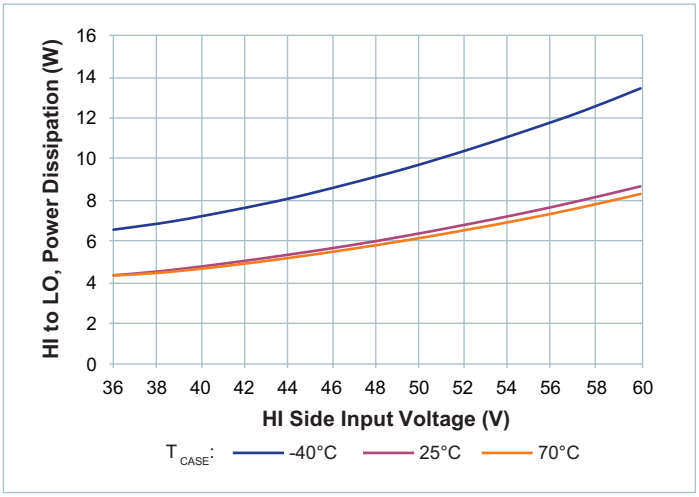


Figure 4 *— No load power dissipation vs. V_{HI_DC}*

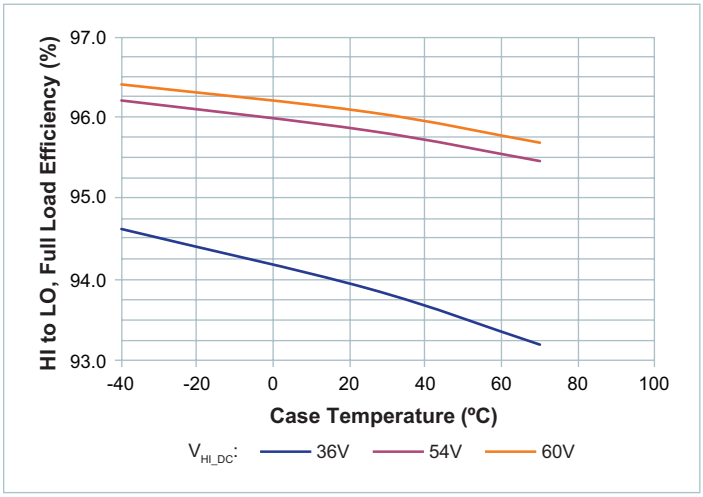


Figure 5 *— Full load efficiency vs. temperature; V_{HI_DC}*

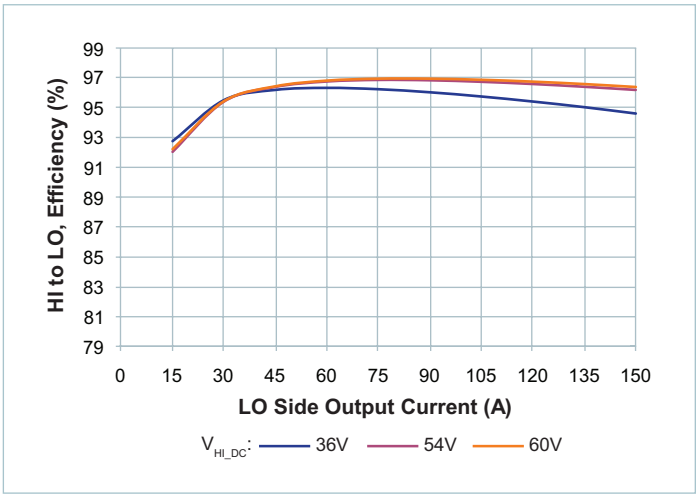


Figure 6 *— Efficiency at T_{CASE} = -40°C*

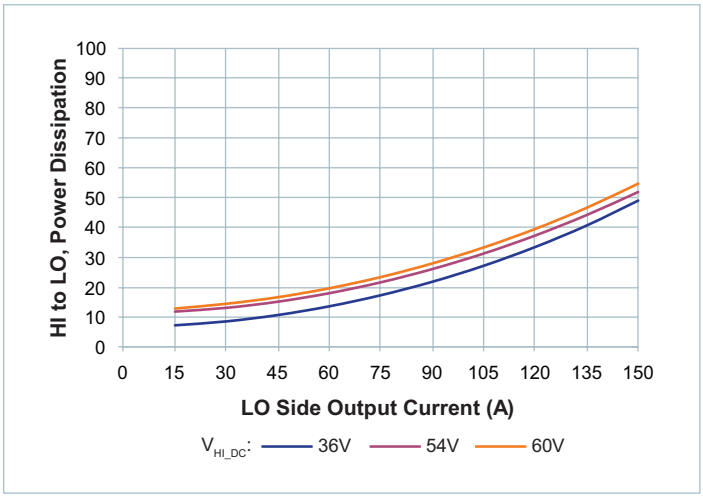


Figure 7 *— Power dissipation at T_{CASE} = -40°C*

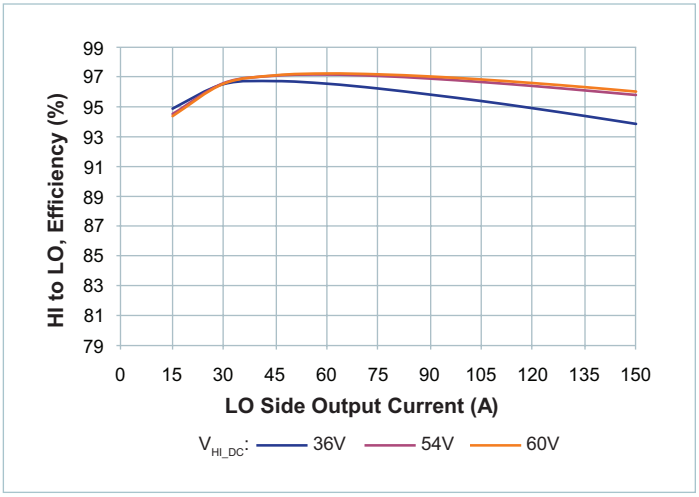


Figure 8 *— Efficiency at T_{CASE} = 25°C*

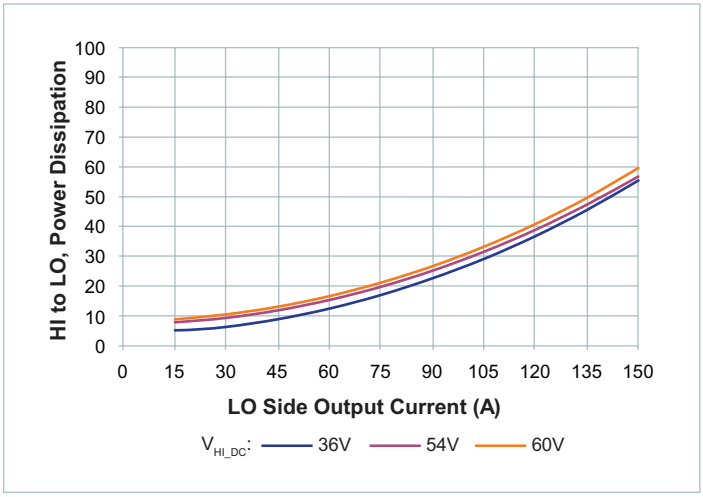


Figure 9 *— Power dissipation at T_{CASE} = 25°C*

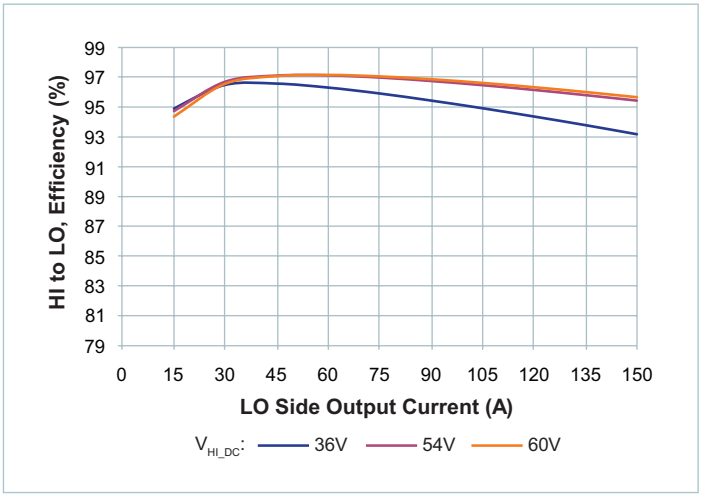


Figure 10 *— Efficiency at T_{CASE} = 70°C*

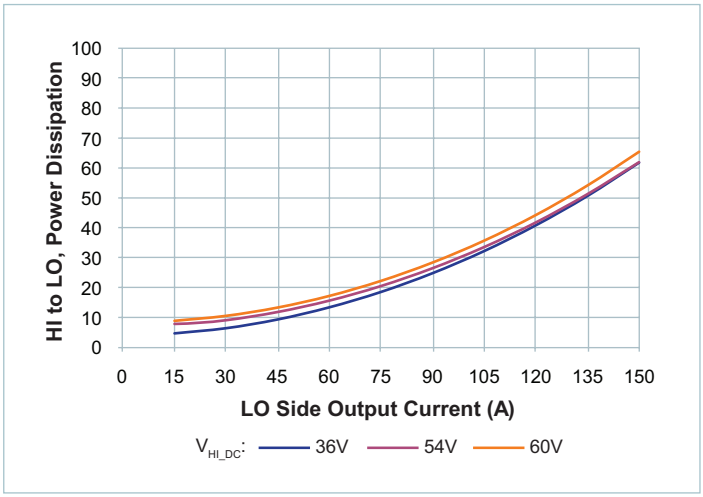


Figure 11 *— Power dissipation at T_{CASE} = 70°C*

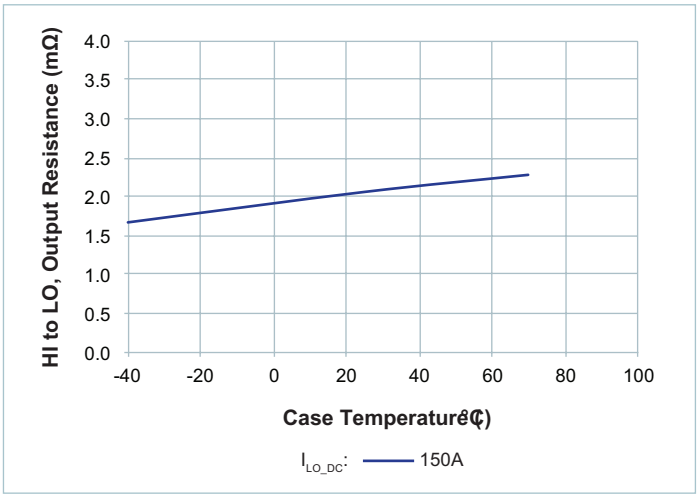


Figure 12 *— R_{LO} vs. temperature; Nominal V_{HI_DC} I_{LO_DC} = 150A at T_{CASE} = 70°C*

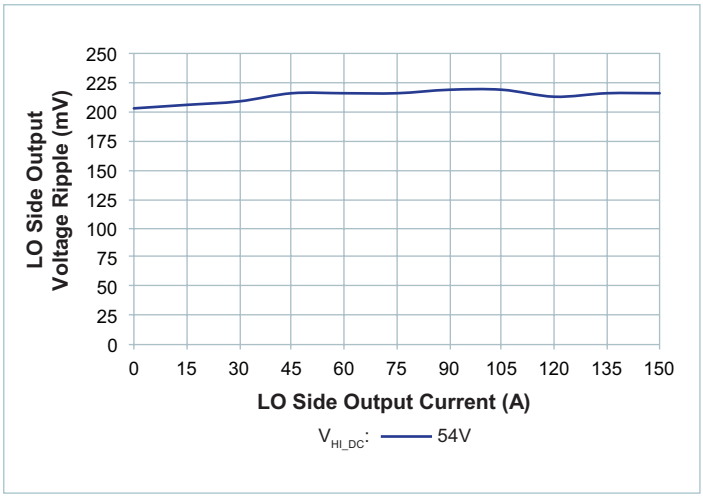


Figure 13 *— $V_{LO\_OUT\_PP}$ vs. I_{LO_DC} ; No external $C_{LO\_OUT\_EXT.}$ Board mounted module, scope setting : 20MHz analog BW*

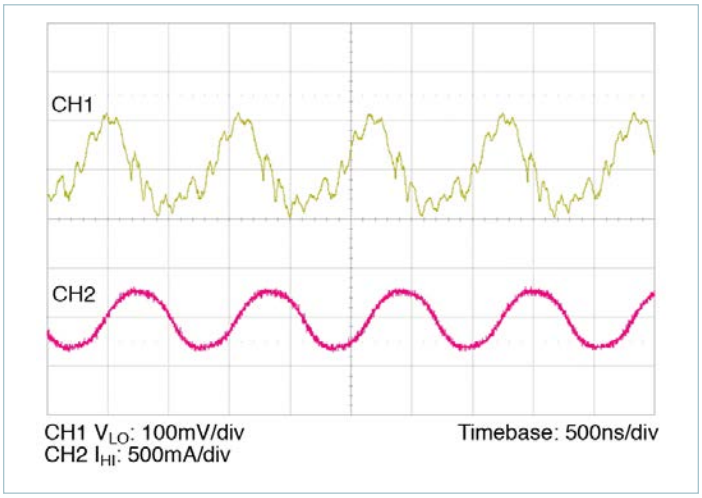


Figure 14 — *Full load ripple, 300µF $C_{HI\_IN\_EXT}$; No external $C_{LO\_OUT\_EXT}$. Board mounted module, scope setting : 20MHz analog BW*

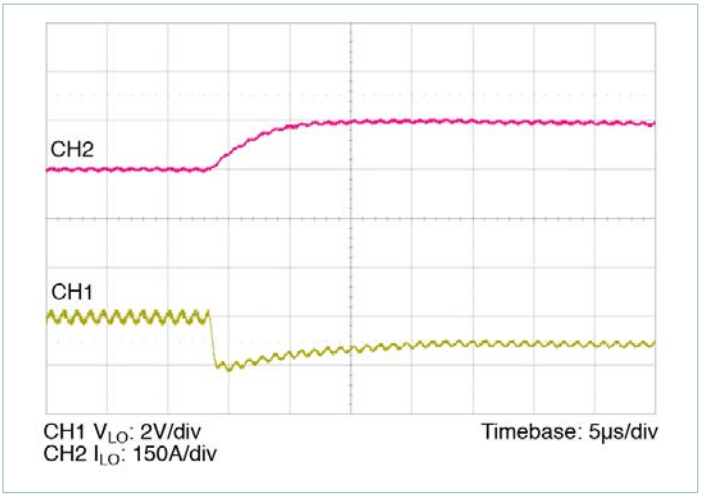


Figure 15 — *0 A– 150A transient response: $C_{HI\_IN\_EXT}$ = 300µF, no external $C_{LO\_OUT\_EXT}$*

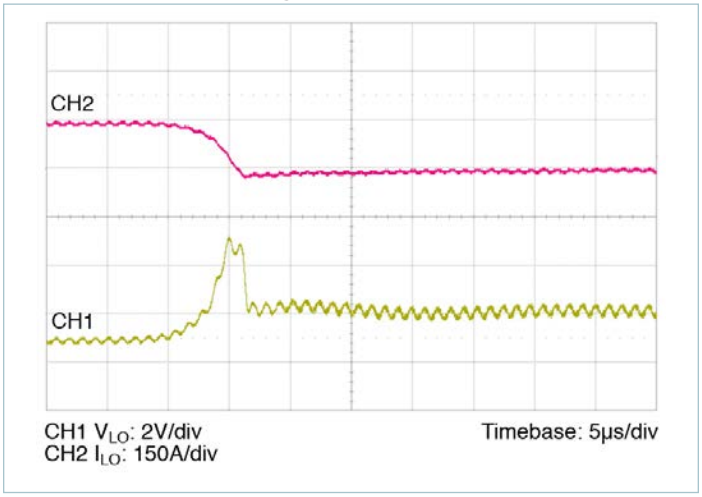


Figure 16 — *150A – 0A transient response: $C_{HI\_IN\_EXT}$ = 300µF, no external $C_{LO\_OUT\_EXT}$*

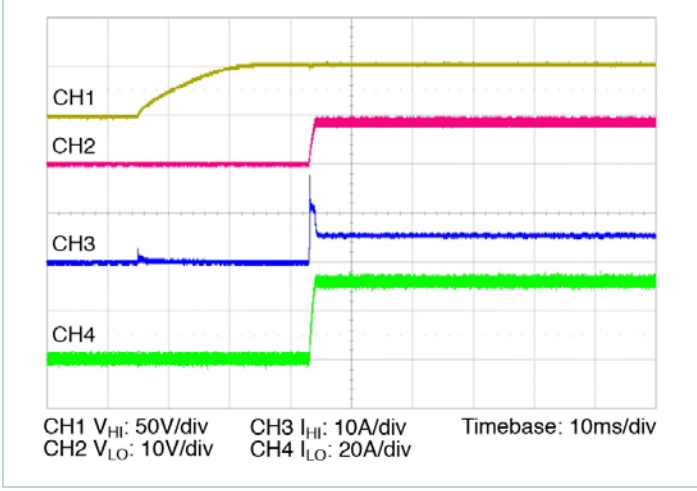


Figure 17 — *Start up from application of V_{HI_DC} = 54V, 20% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

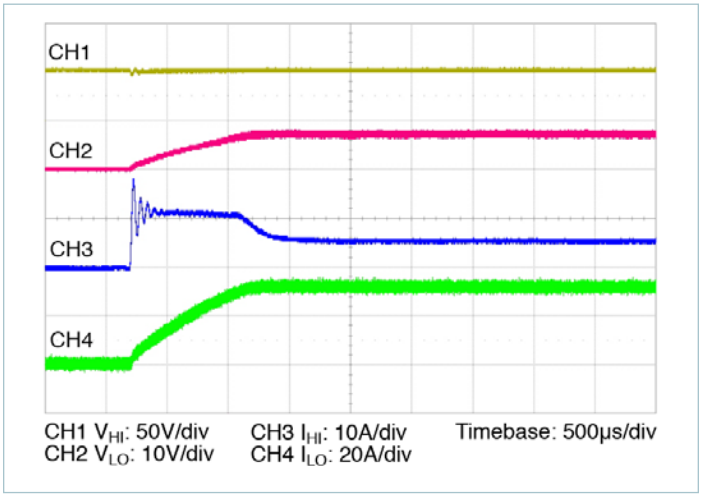


Figure 18 — *Start up from application of EN with pre-applied V_{HI_DC} = 54V, 20% I_{LO_DC}, 100% $C_{LO\_OUT\_EXT}$*

General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤100°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Lug (Chassis) Mount	95.34 / [3.75]	95.59 / [3.76]	95.84 / [3.77]	mm / [in]
Length	L	PCB (Board) Mount	97.55 / [3.84]	97.80 / [3.85]	98.05 / [3.86]	mm / [in]
Width	W		35.29 / [1.39]	35.54 / [1.40]	35.79 / [1.41]	mm / [in]
Height	H		9.019 / [0.355]	9.40 / [0.37]	9.781 / [0.385]	mm / [in]
Volume	Vol	Without heatsink		31.93 / [1.95]		cm^3/ [in^3]
Weight	W			130.4 / [4.6]		g / [oz]
Pin Material		C145 copper, 1/2 hard				
Underplate		Low stress ductile Nickel	50		100	µin
Pin Finish		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Thermal						
Operating junction temperature	$T_{INTERNAL}$	BCM3814x60E10A5yzz (T-Grade)	-40		125	°C
		BCM3814x60E10A5yzz (C-Grade)	-20		125	
Operating case temperature	T_{CASE}	BCM3814x60E10A5yzz (T-Grade), derating applied, see safe thermal operating area	-40		100	
		BCM3814x60E10A5yzz (C-Grade), derating applied, see safe thermal operating area	-20		100	
Thermal resistance top side	R_{JC_TOP}	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.33		°C/W
Thermal Resistance Coupling between top case and bottom case	R_{HOU}	Estimated thermal resistance of thermal coupling between the top and bottom case surfaces		0.49		°C/W
Thermal resistance bottom side	R_{JC_BOT}	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		0.71		°C/W
Thermal capacity				52		Ws/°C
Assembly						
Storage Temperature	T_{ST}	BCM3814x60E10A5yzz (T-Grade)	-40		125	°C
		BCM3814x60E10A5yzz (C-Grade)	-40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2 kV)	1000			
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)	200			

General Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T^{CASE} ≤ 125°C (T-Grade); All other specifications are at T_{CASE} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Isolation capacitance	C_{HI_LO}	Unpowered unit	**620**	**780**	**940**	pF
Isolation resistance	R_{HI_LO}	At $500V_{DC}$	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		2.2		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.6		MHrs
Agency approvals / standards						
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

BCM in a VIA Package

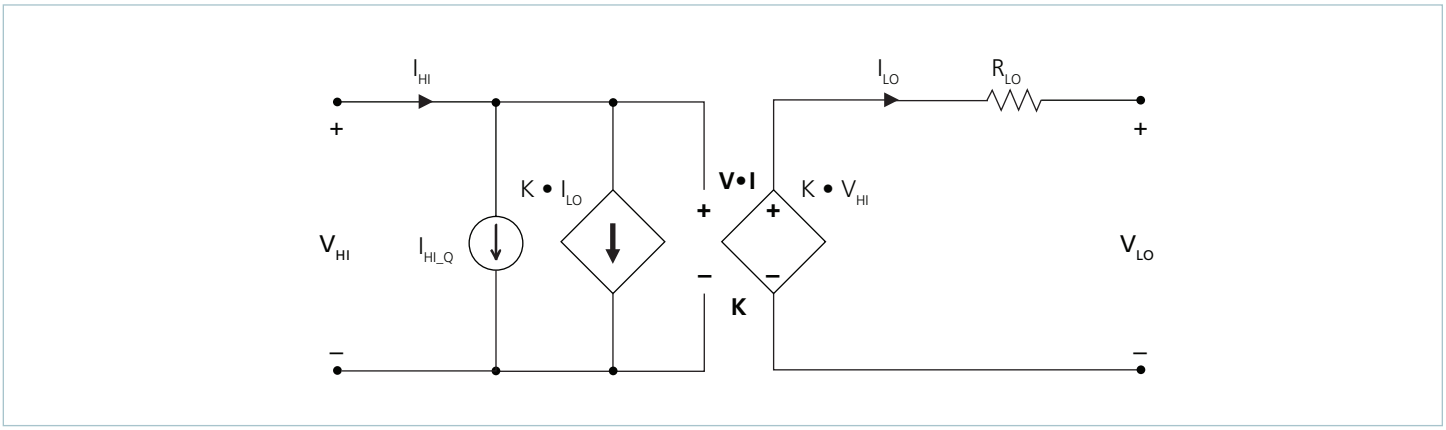


Figure 19 *— BCM DC model (Forward Direction)*

The BCM in a VIA package uses a high frequency resonant tank to move energy from high voltage side to low voltage side and vice versa. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of HI side voltage and LO side current. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM3814x60E10A5yzz can be simplified into the preceeding model.

At no load:

$$V_{LO} = V_{HI} \bullet K \qquad (1)$$

K represents the "turns ratio" of the BCM.
Rearranging Eq (1):

$$K = \frac{V_{LO}}{V_{HI}} \qquad (2)$$

In the presence of load, V_{LO} is represented by:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R_{LO} \qquad (3)$$

and I_{LO} is represented by:

$$I_{LO} = \frac{I_{HI} - I_{HI\_Q}}{K} \qquad (4)$$

R_{LO} represents the impedance of the BCM, and is a function of the R_{DS_ON} of the HI side and LO side MOSFETs, PC board resistance of HI side and LO side boards and the winding resistance of the power transformer. I_{HI_Q} represents the HI side quiescent current of the BCM control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{LO} = 0\Omega$ and $I_{HI\_Q} = 0A$, Eq. (3) now becomes Eq. (3) and is essentially load independent, resistor R is now placed in series with V_{HI}.

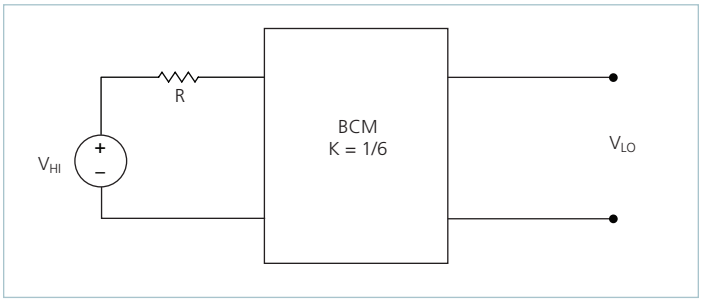


Figure 20 *— K = 1/6 BCM with series HI side resistor*

The relationship between V_{HI} and V_{LO} becomes:

$$V_{LO} = (V_{HI} - I_{HI} \bullet R) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_{HI_Q} is assumed = 0A) into Eq. (5) yields:

$$V_{LO} = V_{HI} \bullet K - I_{LO} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{LO} is used to represent the characteristic impedance of the BCM. However, in this case a real R on the high voltage side of the BCM is effectively scaled by K^2 with respect to the low voltage side.

Assuming that R = 1Ω, the effective R as seen from the low voltage side is 28mΩ, with K = 1/6.

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the high voltage side of the BCM. A switch in series with V_{HI} is added to the circuit. This is depicted in Figure 21.

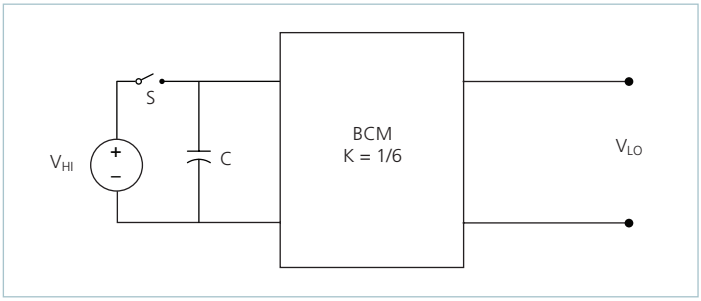


Figure 21 *— BCM with HI side capacitor*

A change in V_{HI} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{HI}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{HI}, the switch is opened and the capacitor is discharged through the idealized BCM. In this case,

$$I_C = I_{LO} \bullet K \qquad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{LO} = \frac{C}{K^2} \bullet \frac{dV_{LO}}{dt} \qquad (9)$$

The equation in terms of the LO side has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the low voltage side when expressed in terms of the high voltage side. With a K = 1/6 as shown in Figure 21, C = 1µF would appear as C = 36µF when viewed from the low voltage side.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a BCM between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the BCM is too high. The impedance of the BCM must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the BCM low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{HI_NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss ($P_{R_{LO}}$): refers to the power loss across the BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{HI\_NL} + P_{R_{LO}} \qquad (10)$$

Therefore,

$$P_{LO\_OUT} = P_{HI\_IN} - P_{DISSIPATED} = P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{LO\_OUT}}{P_{HI\_IN}} = \frac{P_{HI\_IN} - P_{HI\_NL} - P_{R_{LO}}}{P_{HI\_IN}} \qquad (12)$$

$$= \frac{V_{HI} \bullet I_{HI} - P_{HI\_NL} - (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}$$

$$= 1 - \left(\frac{P_{HI\_NL} + (I_{LO})^2 \bullet R_{LO}}{V_{HI} \bullet I_{HI}}\right)$$

Filter Design

A major advantage of BCM systems versus conventional PWM converters is that the transformer based BCM does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of HI side voltage and LO side current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the high voltage side and low voltage side stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:

  To take full advantage of the BCM module's dynamic response, the impedance presented to its HI side terminals must be low from DC to approximately 5MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100nH, the HI side should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200nH, the RC damper may be as high as 1µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- Further reduce HI side and/or LO side voltage ripple without sacrificing dynamic response:

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the LO side of the module multiplied by its K factor.

- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:

  The module high side/low side voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating HI side range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Total load capacitance at the LO side of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and small LO side impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the HI side of the module. At frequencies <500kHz the module appears as an impedance of R_{LO} between the source and load.

Within this frequency range, capacitance at the HI side appears as effective capacitance on the LO side per the relationship defined in Eq. (13).

$$C_{LO\_EXT} = \frac{C_{HI\_EXT}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The VIA™ package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the top surface, the bottom surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a VIA, as can be seen from specified thermal operating area in Figure 1. Since the VIA has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. To this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 22 shows the "thermal circuit" for the VIA module.

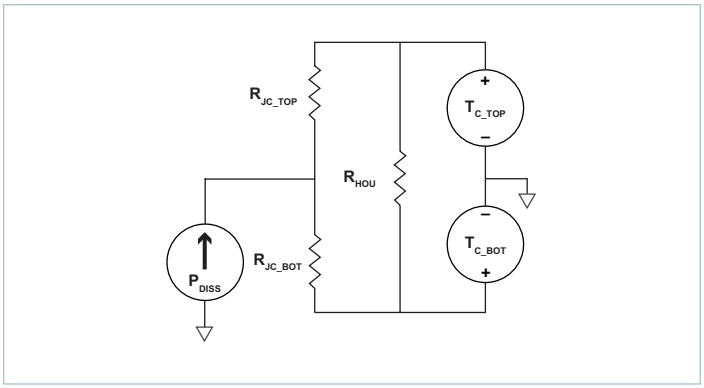


Figure 22 *— Double sided cooling VIA thermal model*

In this case, the internal power dissipation is P_{DISS}, R_{JC_TOP} and R_{JC_BOT} are thermal resistance characteristics of the VIA module and the top and bottom surface temperatures are represented as T_{C_TOP}, and T_{C_BOT}. It is interesting to notice that the package itself provides a high degree of thermal coupling between the top and bottom case surfaces (represented in the model by the resistor R_{HOU}). This feature enables two main options regarding thermal designs:

- Single side cooling: the model of Figure 22 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for bottom side cooling only is shown in Figure 23.

In this case, R_{JC} can be derived as following:

$$R_{JC} = \frac{(R_{JC\_TOP} + R_{HOU}) \bullet R_{JC\_BOT}}{R_{JC\_TOP} + R_{HOU} + R_{JC\_BOT}} \qquad (14)$$

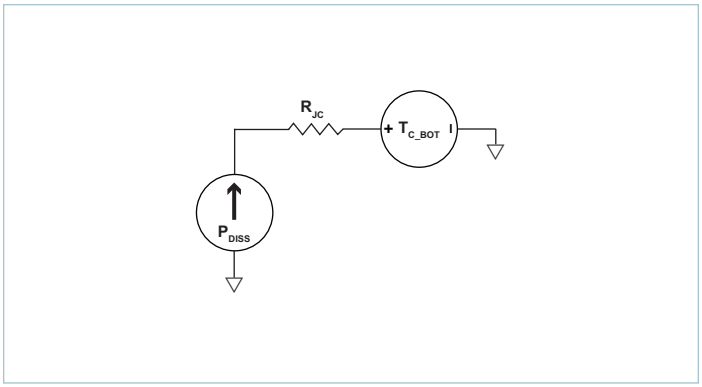


Figure 23 – *Single-sided cooling VIA thermal model*

- Double side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, like for example heatsinks with independent airflows or a combination of chassis/air cooling.

Current Sharing

The performance of the BCM in a VIA package is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes/wires within the PCB/Chassis to deliver and return the current to the VIA modules.
- Provide as symmetric a PCB/Wiring layout as possible among VIA™ modules

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

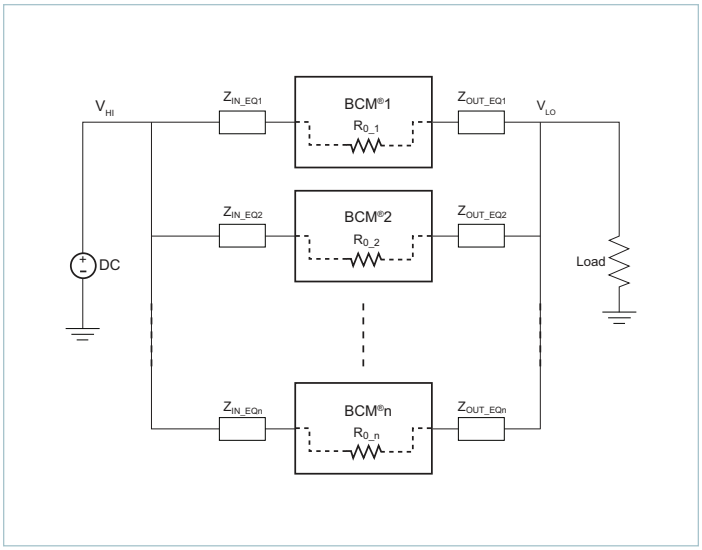


Figure 24 — *BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems, BCM in a VIA package modules are not internally fused. Input line fusing of BCM in a VIA package products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤40A Littlefuse 456 Series (HI side)

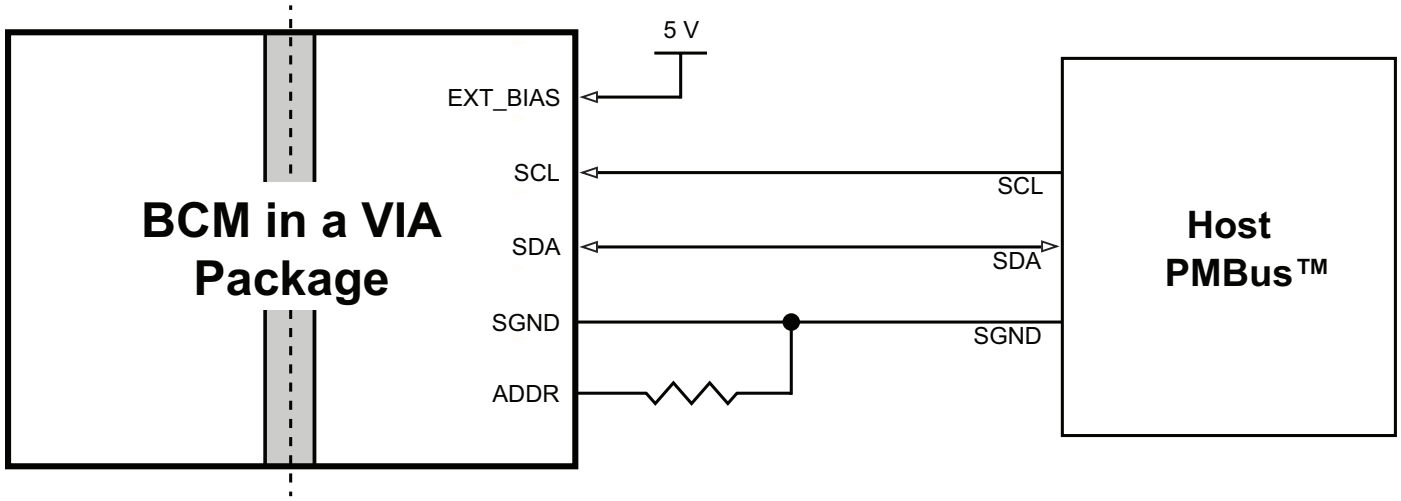
Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from low voltage side back to the high voltage side whenever the low side voltage exceeds $V_{HI} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

The BCM3814x60E10A5yzz has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the low voltage side and transient voltages appear on the high voltage side.

System Diagram for PMBus™ Interface



The BCM in a VIA package provides accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags.

The BCM's internal µC is referenced to low voltage side signal ground.

The BCM provides the host system µC with access to standalone BCM. The standalone BCM is constantly polled for status by the internal µC. Direct communication to BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the internal µC data and pages (0x01) prior to a telemetry inquiry points to the BCM connected data. The BCM constantly polls it's data through the PMBus.

The BCM enables the PMBus compatible host interface with an operating bus speed of up to 400kHz. The BCM follows the PMBus command structure and specification.

PMBus™ Interface

Refer to "PMBus Power System Management Protocol Specification Revision 1.2, Part I and II" for complete PMBus specifications details visit http://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of a predetermined 16 possible addresses shown in the table below using a resistor between ADDR pin and SGND pin.

The BCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power up, the BCM internal µC will sample the address pin voltage, and will hold this address until device power is removed.

ID	Slave Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The BCM internal µC employs a direct data format where all reported internal µC measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the Coefficients command is not supported:

$$X = \left(\frac{1}{m}\right) \bullet (Y \bullet 10^{-R} - b)$$

Where:

X, is a "real world" value in units (A, V, °C, s)

Y, is a two's complement integer received from the internal µC

m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_IIN	89h	1	2	0
READ_VOUT	8Bh	1	1	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1	8Dh	1	0	0
READ_POUT	96h	1	0	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0
READ_BCM_ROUT	D4h	1	5	0

[1] Default READ LO side voltage returned when BCM unit is disabled = -300V.
[2] Default READ Temperature returned when BCM unit is disabled = -273°C.

No special formatting is required when lowering the supervisory limits and warnings.

Supported Command List

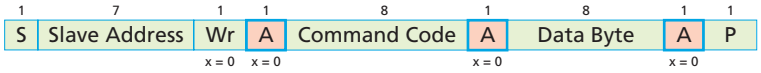
Command	Code	Function	Default Data Content	Data Bytes
PAGE	00h	Access BCM stored information for all connected devices	00h	1
OPERATION	01h	Turn BCMs on or off	80h	1
ON_OFF_CONFIG	02h	Defines startup when power is applied as well as immediate on/off control over the BCMs	1Dh	1
CLEAR_FAULTS	03h	Clear all BCM and all internal µC faults	N/A	None
CAPABILITY	19h	Internal µC PMBus™ key capabilities set by factory	20h	1
OT_FAULT_LIMIT	4Fh[1]	BCM over temperature protection	64h	2
OT_WARN_LIMIT	51h[1]	BCM over temperature warning	64h	2
VIN_OV_FAULT_LIMIT	55h[1]	BCM V_{HI} overvoltage warning	64h	2
VIN_OV_WARN_LIMIT	57h[1]	BCM V_{HI} overvoltage protection	64h	2
IIN_OC_FAULT_LIMIT	5Bh[1]	BCM I_{LO} overcurrent protection	64h	2
IIN_OC_WARN_LIMIT	5Dh[1]	BCM I_{LO} overcurrent warning	64h	2
TON_DELAY	60h[1]	Startup delay additional to any BCM fixed delays	00h	2
STATUS_BYTE	78h	Summary of BCM faults	00h	1
STATUS_WORD	79h	Summary of BCM fault conditions	00h	2
STATUS_IOUT	7Bh	BCM overcurrent fault status	00h	1
STATUS_INPUT	7Ch	BCM overvoltage and under voltage fault status	00h	1
STATUS_TEMPERATURE	7Dh	BCM over temperature and under temperature fault status	00h	1
STATUS_CML	7Eh	Internal µC PMBus Communication fault	00h	1
STATUS_MFR_SPECIFIC	80h	Other BCM status indicator	00h	1
READ_VIN	88h	Reads HI side voltage	FFFFh	2
READ_IIN	89h	Reads HI side current	FFFFh	2
READ_VOUT	8Bh	Reads LO side voltage	FFFFh	2
READ_IOUT	8Ch	Reads LO side current	FFFFh	2
READ_TEMPERATURE_1	8Dh	BCM temperature	FFFFh	2
READ_POUT	96h	Reads LO side power	FFFFh	2
PMBUS_REVISION	98h	Internal µC PMBus compatible revision	22h	1
MFR_ID	99h	Internal µC ID	"VI"	2
MFR_MODEL	9Ah	Internal µC or BCM model	Part Number	18
MFR_REVISION	9Bh	Internal µC or BCM revision	FW and HW revision	18
MFR_LOCATION	9Ch	Internal µC or BCM factory location	"AP"	2
MFR_DATE	9Dh	Internal µC or BCM manufacturing date	"YYWW"	4
MFR_SERIAL	9Eh	Internal µC or BCM serial number	Serial Number	16
MFR_VIN_MIN	A0h	BCM Minimum rated V_{HI}	Varies per BCM	2
MFR_VIN_MAX	A1h	BCM Maximum rated V_{HI}	Varies per BCM	2
MFR_VOUT_MIN	A4h	BCM Minimum rated V_{LO}	Varies per BCM	2
MFR_VOUT_MAX	A5h	BCM Maximum rated V_{LO}	Varies per BCM	2
MFR_IOUT_MAX	A6h	BCM Maximum rated I_{LO}	Varies per BCM	2
MFR_POUT_MAX	A7h	BCM Maximum rated P_{LO}	Varies per BCM	2
BCM_EN_POLARITY	D0h[1]	Set BCM EN pin polarity	02h	1
READ_K_FACTOR	D1h	BCM K factor	Varies per BCM	2
READ_BCM_ROUT	D4h	BCM R_{LO}	Varies per BCM	2
SET_ALL_THRESHOLDS	D5h[1]	Set BCM supervisory warning and protection thresholds	646464646464h	6
DISABLE_FAULT	D7h[1]	Disable BCM overvoltage, overcurrent or under voltage supervisory faults	00h	2

[1] The BCM must be in a disabled state during a write message.

Command Structure Overview

Write Byte protocol:

The Host always initiates PMBus™ communication with a START bit. All messages are terminated by the Host with a STOP bit. In a write message, the master sends the slave device address followed by a write bit. Once the slave acknowledges, the master proceeds with the command code and then similarly the data byte.



S Start Condition

Sr Repeated start Condition

Rd Read

Wr Write

X Indicated that field is required to have the value of x

A Acknowledge (bit may be 0 for an ACK or 1 for a NACK)

P Stop Condition

From Master to Slave

From Slave to Master

... Continued next line

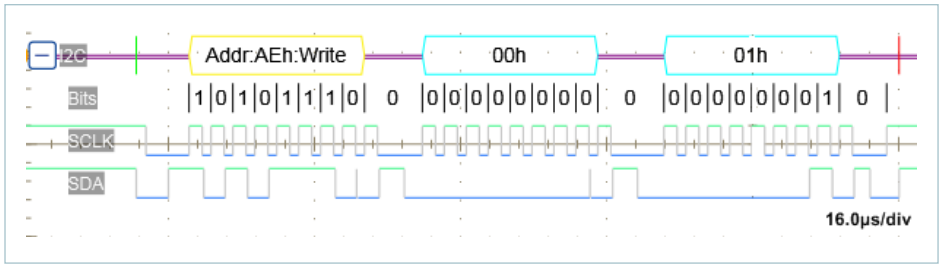
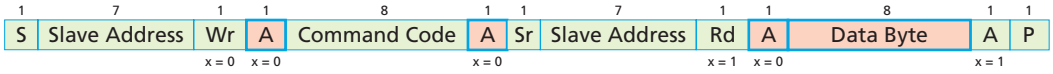


Figure 1 *— PAGE COMMAND (00h), WRITE BYTE PROTOCOL*

Read Byte protocol:

A Read message begins by first sending a Write Command, followed by a REPEATED START Bit and a slave Address. After receiving the READ bit, the internal µC begins transmission of the Data responding to the Command. Once the Host receives the requested Data, it terminates the message with a NACK preceding a stop condition signifying the end of a read transfer.



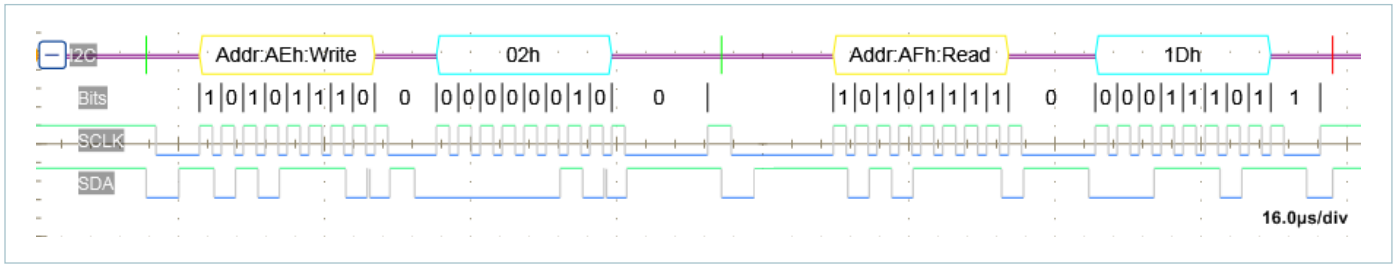
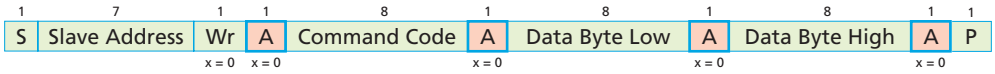


Figure 2 *— ON_OFF_CONFIG COMMAND (02h), READ BYTE PROTOCOL*

Write Word protocol:

When transmitting a word, the lowest order byte leads the highest order byte. Furthermore, when transmitting a Byte, the least significant bit (LSB) is sent last. Refer to System Management Bus (SMBus) specification version 2.0 for more details.

Note: Extended command and Packet Error Checking Protocols are not supported.



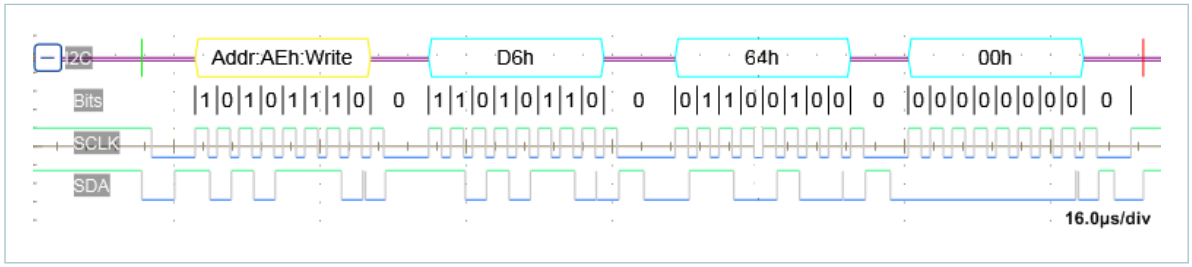
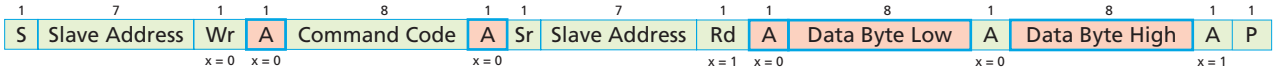


Figure 3 *— TON_DELAY COMMAND (60h)_WRITE WORD PROTOCOL*

Read Word protocol:



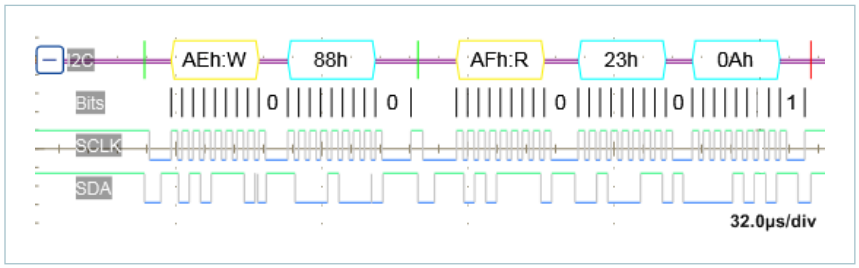
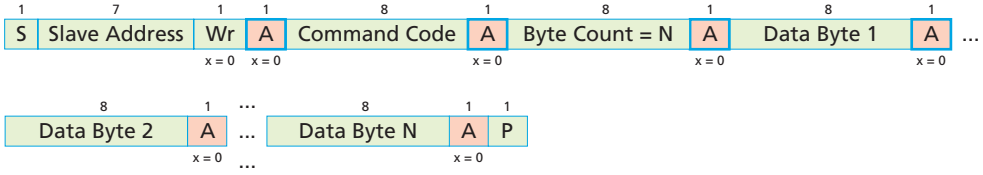


Figure 4 *— MFR_VIN_MIN COMMAND (A0h)_READ WORD PROTOCOL*

Write Block protocol:



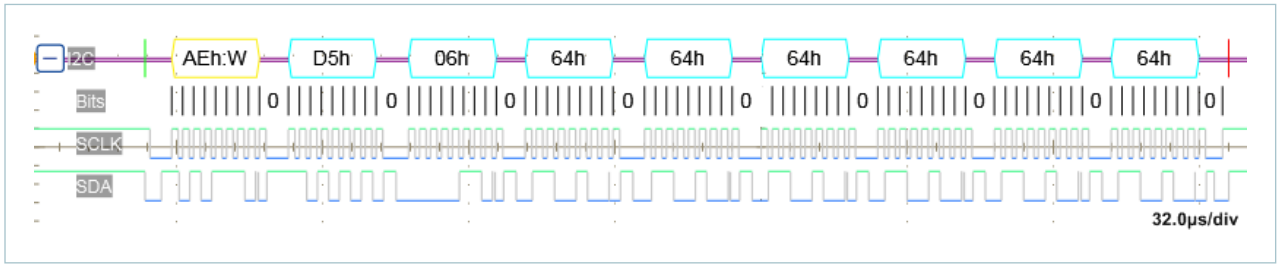
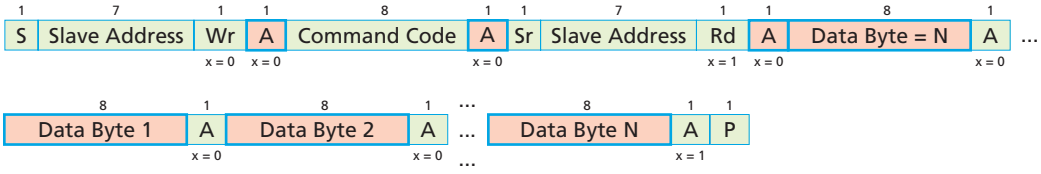


Figure 5 *— SET_ALL_THRESHOLDS COMMAND (D5h)_WRITE BLOCK PROTOCOL*

Read Block protocol:



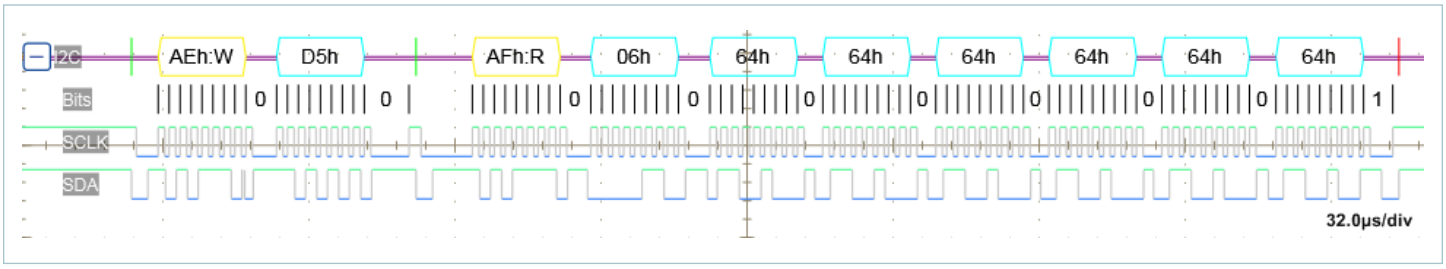
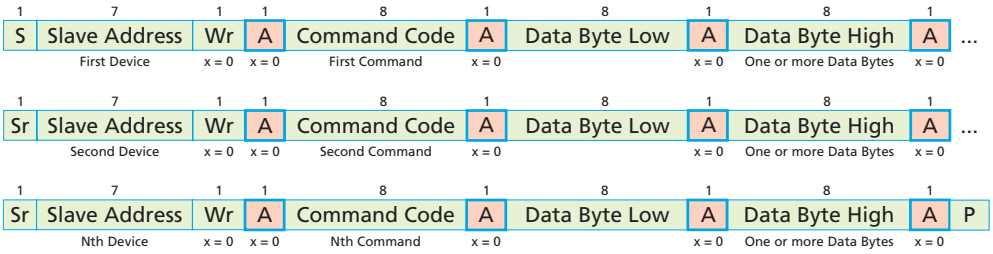


Figure 6 *— SET_ALL_THRESHOLDS COMMAND (D5h)_READ BLOCK PROTOCOL*

Write Group Command protocol:

Note that only one command per device is allowed in a group command.



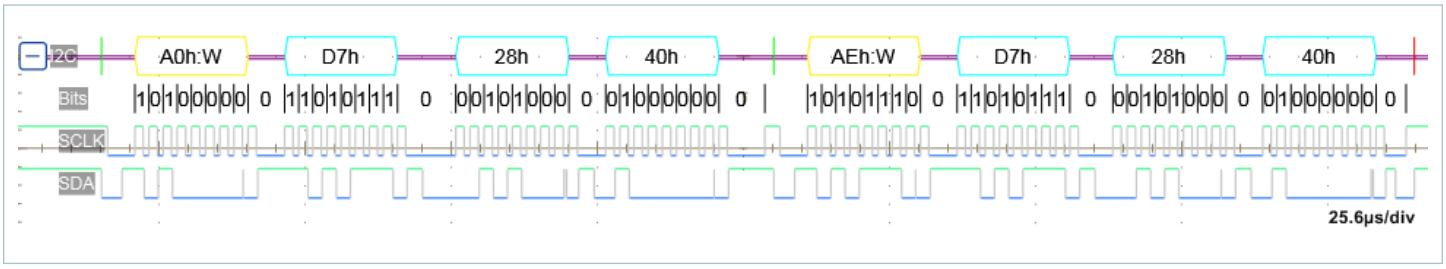


Figure 7 *— DISABLE_FAULT COMMAND (D7h)_WRITE*

Supported Commands Transaction Type

A direct communication to the BCM internal µC and a simulated communication to non-PMBus™ devices is enabled by a page command. Supported command access privileges with a pre-selected PAGE are defined in the following table. Deviation from this table generates a communication error in STATUS_CML register.

Command	Code	PAGE Data Byte Access Type	
		00h	01h
PAGE	00h	R/W	R/W
OPERATION	01h	R	R/W
ON_OFF_CONFIG	02h		R
CLEAR_FAULTS	03h	W	W
CAPABILITY	19h	R	
OT_FAULT_LIMIT	4Fh		R/W
OT_WARN_LIMIT	51h		R/W
VIN_OV_FAULT_LIMIT	55h		R/W
VIN_OV_WARN_LIMIT	57h		R/W
IIN_OC_FAULT_LIMIT	5Bh		R/W
IIN_OC_WARN_LIMIT	5Dh		R/W
TON_DELAY	60h		R/W
STATUS_BYTE	78h	R/W	R
STATUS_WORD	79h	R	R
STATUS_IOUT	7Bh	R	R/W
STATUS_INPUT	7Ch	R	R/W
STATUS_TEMPERATURE	7Dh	R	R/W
STATUS_CML	7Eh	R/W	
STATUS_MFR_SPECIFIC	80h	R	R/W
READ_VIN	88h		R
READ_IIN	89h	R	R
READ_VOUT	8Bh		R
READ_IOUT	8Ch	R	R
READ_TEMPERATURE_1	8Dh	R	R
READ_POUT	96h	R	R
PMBUS_REVISION	98h	R	
MFR_ID	99h	R	
MFR_MODEL	9Ah	R	R
MFR_REVISION	9Bh	R	R
MFR_LOCATION	9Ch	R	R
MFR_DATE	9Dh	R	R
MFR_SERIAL	9Eh	R	R
MFR_VIN_MIN	A0h	R	R
MFR_VIN_MAX	A1h	R	R
MFR_VOUT_MIN	A4h	R	R
MFR_VOUT_MAX	A5h	R	R
MFR_IOUT_MAX	A6h	R	R
MFR_POUT_MAX	A7h	R	R
BCM_EN_POLARITY	D0h		R/W
READ_K_FACTOR	D1h		R
READ_BCM_ROUT	D4h		R
SET_ALL_THRESHOLDS	D5h		R/W
DISABLE_FAULT	D7h		R/W

Page Command (00h)

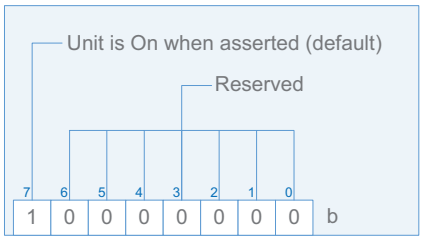
The page command data byte of 00h prior to a command call will address the internal µC specific data and a page data byte of FFh would broadcast to all of the connected BCMs. The value of the Data Byte corresponds to the pin name trailing number with the exception of 00h and FFh.

Data Byte	Description
00h	µC
01h	BCM

OPERATION Command (01h)

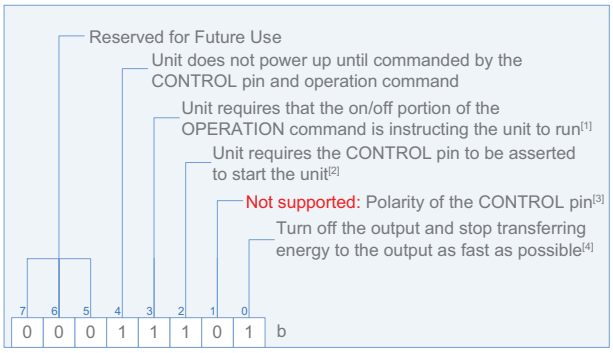
The Operation command can be used to turn on and off the connected BCM. Note that the host OPERATION command will not enable the BCM if the BCM EN pin is disabled in hardware with respect to the preset pin polarity. Only with the EN pin active, will the OPERATION command provide ON/OFF control.

If synchronous startup is required in the system, it is recommended to use the command from host PMBus in order to achieve simultaneous array startup.



This command accepts only two data values: 00h and 80h. If any other value is sent the command will be rejected and a CML Data error will result.

ON_OFF_CONFIG Command (02h)



[1] The BCM Enable pin is ALWAYS to be asserted for powerup. The BCM_EN_POLARITY command (D0h) bit[(1) defines the logic level required for the control pin (i.e BCM Enable pin) to be asserted.

[2] With respect to the BCM EN Control Pin if used in system

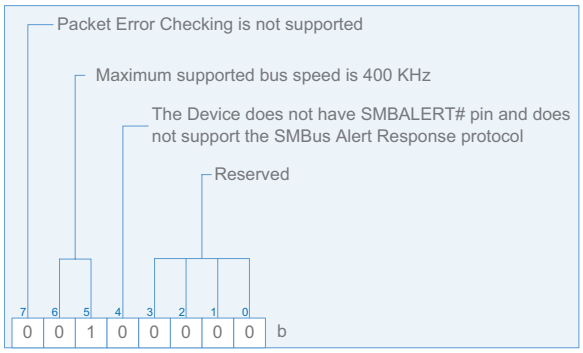
[3] See MFR_SPECIFIC_00 / BCM_EN_POLARITY to change the Polarity of the BCM Enable Pin

[4] The BCM powertrain once disabled cannot sink current

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are reasserted again once cleared. All faults are latched once asserted in the internal µC. Registered faults will not be cleared when shutting down the BCM powertrain by recycling the BCM high side voltage, or toggling the BCM EN pin, or sending the OPERATION command.

CAPABILITY Command (19h)



The internal µC returns a default value of 20h. This value indicates that the PMBus™ frequency supported is up to 400KHz and that both Packet Error Checking (PEC) and SMBALERT# are not supported.

OT_FAULT_LIMIT Command (4Fh), OT_WARN_ LIMIT Command (51h), VIN_OV_FAULT_ LIMIT Command (55h), VIN_OV_WARN_ LIMIT Command (57h), IIN_OC_FAULT_ LIMIT Command (5Bh), IIN_OC_WARN_ LIMIT Command (5Dh)

The values of these registers are set in nonvolatile memory and can only be written when the BCMs are disabled.

The values of the above mentioned fault and warning are set by default to a 100% of the respective BCM model supervisory limits. However these limits can be set to a lower value. For example: In order for a limit percentage to be set to 80% one would send a write command with a (50h) Data Word.

Any values outside the range of (00h – 64h) sent by a host will be rejected, will not override the currently stored value and will set the Unsupported Data bit in STATUS_CML.

The SET_ALL_THRESHOLDS COMMAND (D5h) combines in one block over temperature fault and warning limits, V_{HI} overvoltage fault and warning limits as well as I_{LO} overcurrent fault and warning limits. A delay prior to a read command of up to 200ms following a write of new value is required.

The VIN_UV_WARN_LIMIT (58h) and VIN_UV_FAULT_LIMIT (59h) are set by the factory and cannot be changed by the host. However, a host can disable the under voltage setting using the DISABLE_FAULT COMMAND (D7h).

All FAULT_RESPONSE commands are unsupported. The BCM powertrain supervisory limits and powertrain protection will behave as described in the BCM datasheet. In general, once a fault is detected, the BCM powertrain will shut down and attempt to autonrestart after a predetermined delay.

TON_DELAY Command (60h)

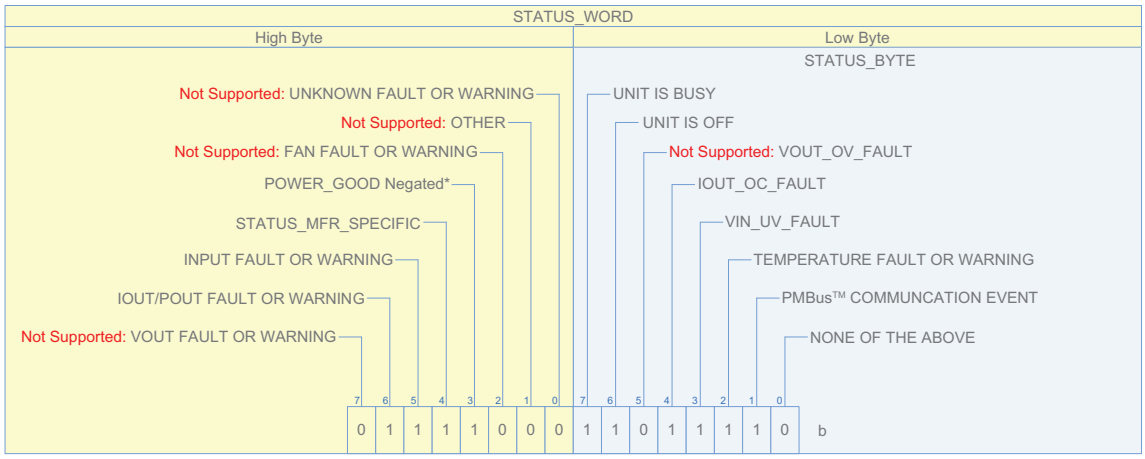
The value of this register word is set in nonvolatile memory and can only be written when the BCMs are disabled.

The maximum possible delay is 100ms. Default value is set to (00h). Follow this equation below to interpret the reported value.

$$TON\_DELAY_{ACTUAL} = t_{REPORTED} \bullet 10^{-3}(s)$$

Staggering startup in an array is possible with TON_DELAY Command. This delay will be in addition to any startup delay inherent in the BCM module. For example: startup delay from application of V_{HI} is typically 20ms whereas startup with EN pin is typically 250µs. When TON_DELAY is greater than zero, the set delay will be added to both.

STATUS_BYTE (78h) and STATUS_WORD (79h)



All fault or warning flags, if set, will remain asserted until cleared by the host or once the internal µC power is removed. This includes under voltage fault, overvoltage fault, overvoltage warning, overcurrent warning, over temperature fault, over temperature warning, under temperature fault, reverse operation, communication faults and analog controller shutdown fault.

Asserted status bits in all status registers, with the exception of STATUS_WORD and STATUS_BYTE, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Refer to the PMBus™ Power System Management Protocol Specification – Part II – Revision 1.2 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set anytime the BCM is not in the enabled state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared when the BCM completes the enabling state, 5 ms after the powertrain is activated allowing for soft-start to elapse. POWER_GOOD# and OFF bits cannot be cleared as they always reflect the current state of the device.

When Page (00h) is used the POWER_GOOD# bit reflects the OR-ing of all active BCMs' POWER_GOOD# bits. When Page (01h – 04h) is used POWER_GOOD# is clear only when the BCM is active.

When Page (00h) is used UNIT IS OFF is SET when all BCMs are not active. When Page (01h – 04h) is used UNIT IS OFF is clear only when the BCM is active.

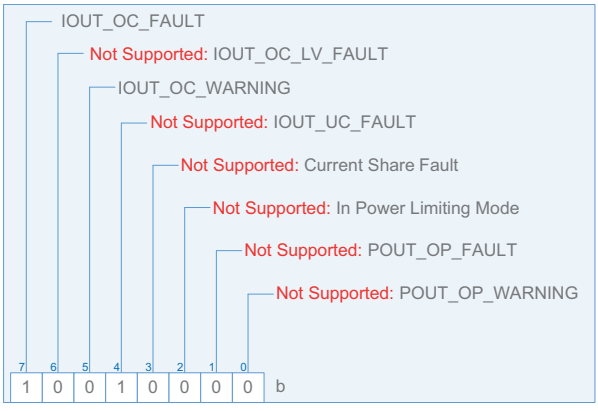
The Busy bit can be cleared using CLEAR_ALL Command (03h) or by writing either data value (40h, 80h) to PAGE (00h) using the STATUS_BYTE (78h).

Fault reporting, such as SMBALERT# signal output, and host notification by temporarily acquiring bus master status is not supported.

If the internal µC is still powered, it will retain the last status it received from the BCM and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard which requires that status bits remain set until specifically cleared. Note that in this case where the BCM V_{HI} is lost, the status will always indicate an under voltage fault, in addition to any other fault
that occurred.

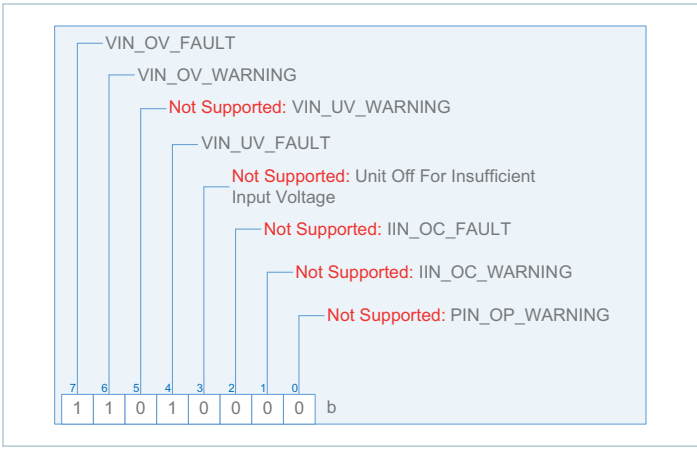
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_IOUT (7Bh)



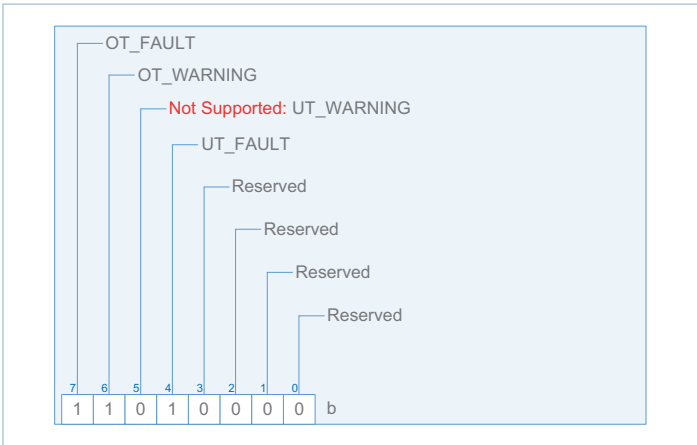
Unsupported bits are indicated above. A one indicates a fault.

STATUS_INPUT (7Ch)



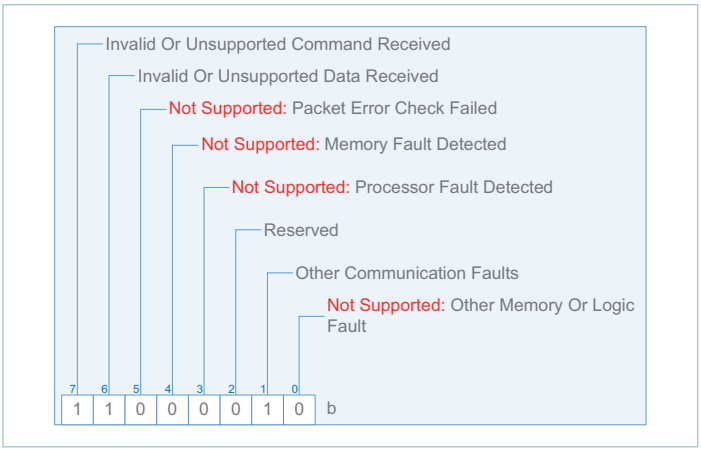
Unsupported bits are indicated above. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unsupported bits are indicated above. A one indicates a fault.

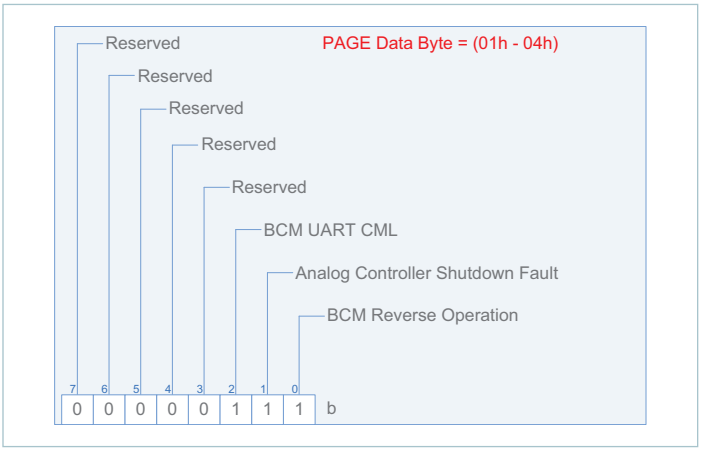
STATUS_CML (7Eh)



Unsupported bits are indicated above. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus™ command or data or other communication fault occured.

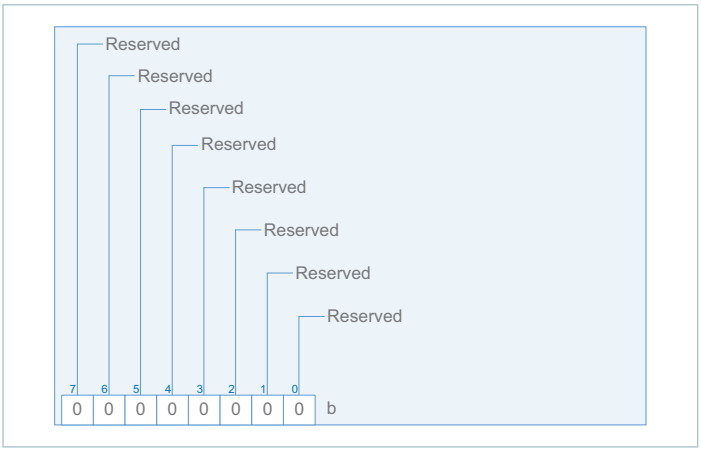
STATUS_MFR_SPECIFIC (80h)



The reverse operation bit, if asserted, indicates that the BCM is processing current in reverse. Reverse current reported value is not supported.

The BCM has analog protections and internal µC protections. The analog controller provides an additional layer of protection and has the fastest response time. The analog controller shutdown fault, when asserted, indicates that at least one of the powertrain protection faults is triggered. This fault will also be asserted if a disabled fault event occurs after asserting any bit using the DISABLE_FAULTS COMMAND.

The BCM UART is designed to operate with the internal µC UART. If the BCM UART CML is asserted, it may indicate a hardware or connection issue between both devices.



When PAGE COMMAND (00h) data byte is equal to (00h), the BCM Reverse operation, Analog Controller Shutdown Fault, and BCM UART CML bit will return OR-ing result of active BCMs. The BCM UART CML will also be asserted if any of the active BCMs stops responding. The BCM must communicate at least once to the internal µC in order to trigger this FAULT. The BCM UART CML can be cleared from the culprit BCM once the internal µC is able to communicate with it once again or can be cleared using PAGE (00h) CLEAR_FAULTS (03h) Command.

READ_VIN Command (88h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's HI side voltage in the following format:

$$V_{HI\_ACTUAL} = V_{HI\_REPORTED} \bullet 10^{-1}(V)$$

READ_IIN Command (89h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's HI side current in the following format:

$$I_{HI\_ACTUAL} = I_{HI\_REPORTED} \bullet 10^{-2}(A)$$

If PAGE data byte is equal (00h) command will return the sum of active BCM's HI side current.

READ_VOUT Command (8Bh)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's LO side voltage in the following format:

$$V_{LO\_ACTUAL} = V_{LO\_REPORTED} \bullet 10^{-1}(V)$$

READ_IOUT Command (8Ch)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's LO side current in the following format:

$$I_{LO\_ACTUAL} = I_{LO\_REPORTED} \bullet 10^{-2}(A)$$

If PAGE data byte is equal (00h) command will return the sum of active BCM's LO side current.

READ_TEMPERATURE_1 Command (8Dh)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's temperature in the following format:

$$T_{ACTUAL} = \pm T_{REPORTED}\ (°C)$$

If PAGE data byte is equal (00h) command will return the maximum temperature of active BCM's.

READ_POUT Command (96h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's LO side power in the following format:

$$P_{LO\_ACTUAL} = P_{LO\_REPORTED}\ (W)$$

If PAGE data byte is equal to (00h) command will return the sum of active BCM's LO side power.

MFR_VIN_MIN Command (A0h), MFR_VIN_MAX Command (A1h), MFR_VOUT_MIN Command (A4h), MFR_VOUT_MAX Command (A5h), MFR_IOUT_MAX Command (A6h), MFR_POUT_MAX Command (A7h)

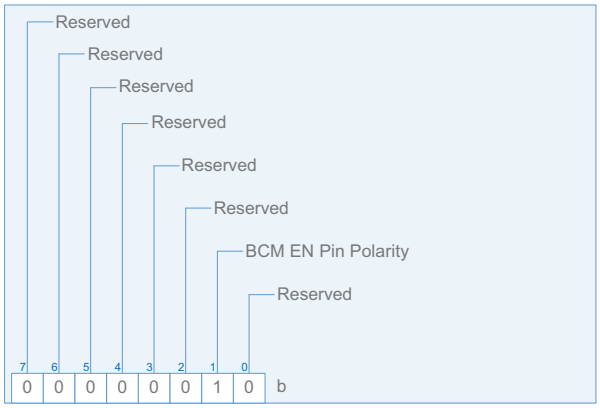
These values are set by the factory and indicate the device HI side/ LO side voltage and LO side current range and LO side power capacity.

The internal µC will report rated BCM HI side voltage minimum and maximum in Volts, LO side voltage minimum and maximum in Volts, LO side current maximum in Amperes and LO side power maximum in Watts.

If PAGE data byte is equal to (00h) then:

- MFR_VIN_MIN COMMAND (A0h) will return the highest MFR_VIN_MIN of all active BCMs
- MFR_VIN_MAX COMMAND (A1h) will return the lowest MFR_VIN_MAX of all active BCMs
- MFR_VOUT_MIN COMMAND (A4h) will return the highest MFR_VOUT_MIN of all active BCMs
- MFR_VOUT_MAX COMMAND (A5h) will return the lowest MFR_VOUT_MAX of all active BCMs
- MFR_IOUT_MAX COMMAND (A6h) will return the SUM of MFR_IOUT_MAX of all active BCMs
- MFR_POUT_MAX COMMAND (A7h) will return the SUM of MFR_POUT_MAX of all active BCMs

BCM_EN_POLARITY Command (D0h)



The value of this register is set in nonvolatile memory and can only be written when the BCMs are disabled.

When PAGE COMMAND (00h) data byte is equal to (01h – 04h), this command defines the polarity of the EN pin. If BCM_EN_POLARITY is set, the BCM will startup once V_{HI} is greater than the under voltage threshold.

The BCM EN PIN is internally pulled-up to 3.3V. If the BCM_EN_POLARITY is cleared, an external pull-down is then required. Applying V_{HI} greater than the under voltage threshold will not suffice to start the BCM.

READ_K_FACTOR Command (D1h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCMs K factor in the following format:

$$K\_FACTOR_{ACTUAL} = K\_FACTOR_{REPORTED} \bullet 2^{-16} (V/V)$$

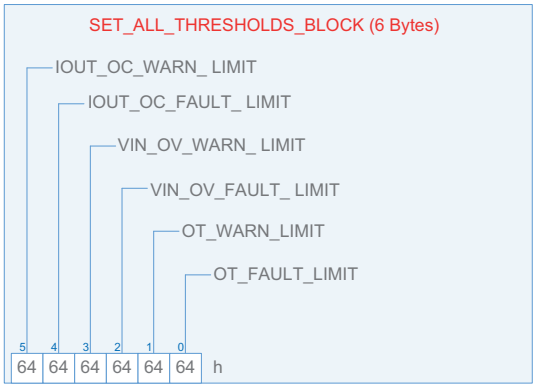
The K factor is defined in a BCM to represent the ratio of the transformer winding and hence is equal to V_{LO} / V_{HI}.

READ_BCM_ROUT Command (D4h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's LO side resistance in the following format:

$$BCM\_R_{LO\_ACTUAL} = BCM\_R_{LO\_REPORTED} \bullet 10^{-5} (\Omega)$$

SET_ALL_THRESHOLDS Command (D5h)



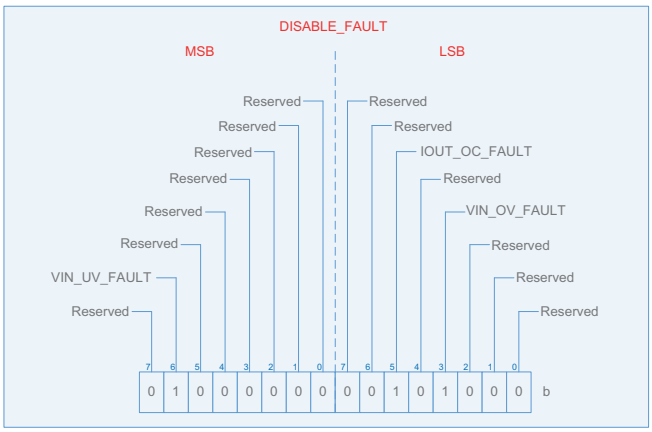
Values of this register block is set in nonvolatile memory and can only be written when the BCMs are disabled.

This command provides a convenient way to configure all the limits, or any combination of limits described previously using one command.

V_{HI} Overvoltage, Overcurrent and Overtemperature values are all set to 100% of the BCM datasheet supervisory limits by default and can only be set to a lower percentage.

To leave a particular threshold unchanged, set the corresponding threshold data byte to a value greater than (64h).

DISABLE_FAULT Command (D7h)



Unsupported bits are indicated above. A one indicates that the supervisory fault associated with the asserted bit is disabled.

The value of these registers is set in nonvolatile memory and can only be written when the BCMs are disabled.

This command allows the host to disable the supervisory faults and respective statuses. It does not disable the powertrain analog protections or warnings with respect to the set limits in the SET_ALL_THRESHOLDS Command.

The HI side undervoltage can only be disabled to a preset low limit as shown in the functional reporting range in the BCM data sheet.

The internal µC Implementation vs. PMBus™ Specification Rev 1.2

The internal µC is an I²C compliant, SMBus™ compatible device and PMBus command compliant device. This section denotes some deviation, perceived as differences from the PMBus Part I and Part II specification Rev 1.2.

1. The internal µC meets all Part I and II PMBus specification requirements with the following differences to the transport requirement.

Unmet DC parameter Implementation vs SMBus™ spec						
Symbol	Parameter	D44TL1A0		SMBus™ Rev 2.0		Units
		Min	Max	Min	Max	
V_{IL}[a]	Input Low Voltage	-	0.99	-	0.8	V
V_{IH}[a]	Input High Voltage	2.31	-	2.1	V_{VDD_IN}	V
I_{LEAK_PIN}[b]	Input Leakage per Pin	10	22	-	±5	µA

[a] V_{VDD_IN} = 3.3V
[b] V_{BUS} = 5V

2. The internal µC accepts 38 PMBus command codes. Implemented commands execute functions as described in the PMBus specification.

- Deviations from the PMBus specification:

  a. Section 15, fault related commands

  - The limits and Warnings unit implemented is percentage (%) a range from decimal (0-100) of the factory set limits.

3. The internal µC unsupported PMBus command code response as described in the Fault Management and Reporting:

- Deviations from the PMBus specification:

  a. PMBus section 10.2.5.3, exceptions

  - The busy bit of the STATUS_BYTE as implemented can be cleared (80h). In order to maintain compatibility with the specification (40h) can also be used.

- Manufacturer Implementation of the PMBus Spec

  a. PMBus section 10.5, setting the response to a detected fault condition

  - All powertrain responses are pre-set and cannot be changed. Refer to the BCM datasheet for details.

  b. PMBus section 10.6, reporting faults and warnings to the Host

  - SMBALERT# signal and Direct PMBus Device to Host Communication are not supported. However, the Digital Supervisor will set the corresponding fault status bits and will wait for the host to poll.

  c. PMBus section 10.7, clearing a shutdown due to a fault

  - There is no RESET pin or EN pin in the internal µC. Cycling power to the internal µC will not clear a BCM Shutdown. The BCM will clear itself once the fault condition is removed. Refer to the BCM datasheet for details.

  d. PMBus Section 10.8.1, corrupted data transmission faults:

  - Packet error checking is not supported.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the internal µC.

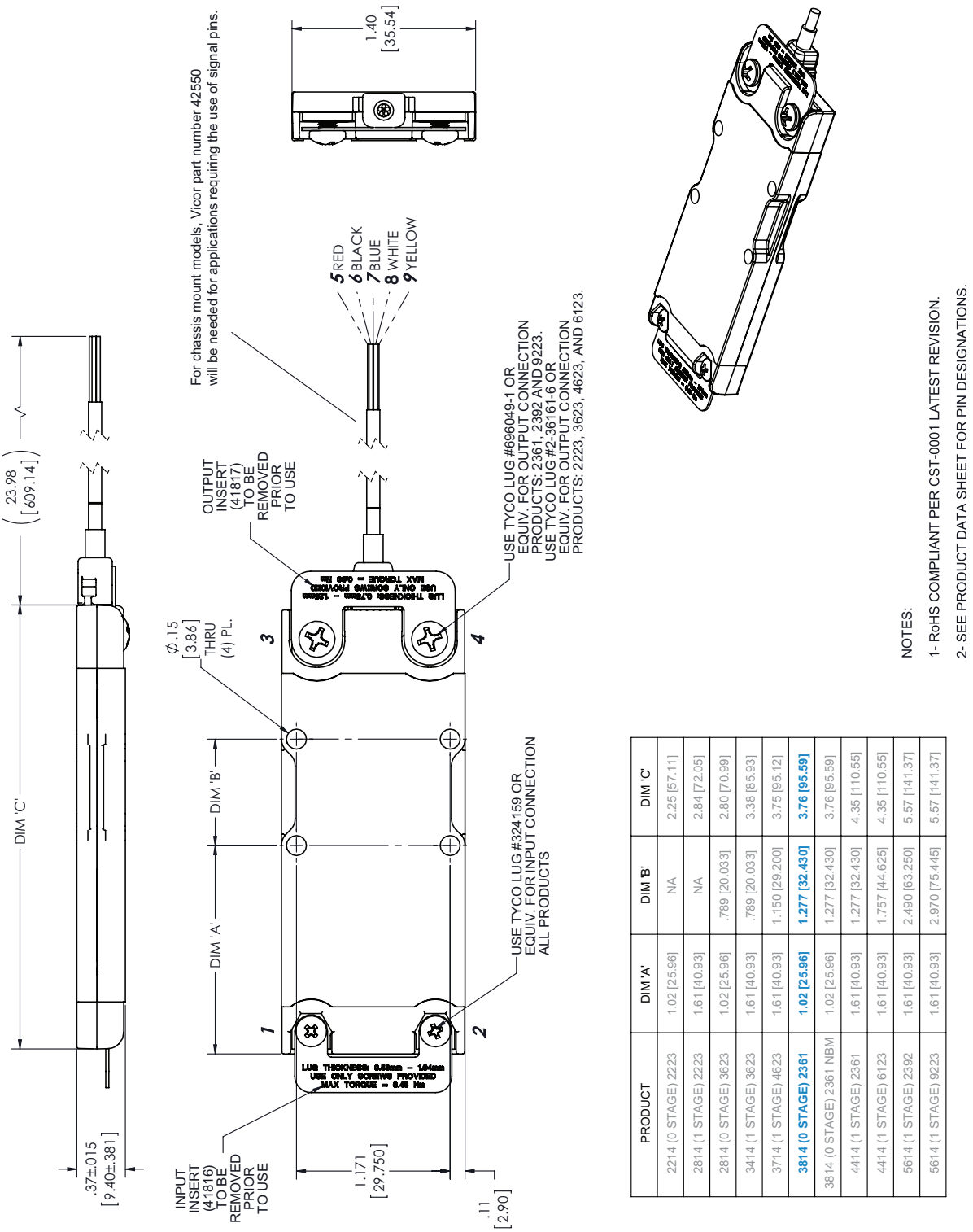
Section	Description	Response to Host		STATUS_BYTE	STATUS_CML		Notes
		NAK	FFh	CML	Other Fault	Unsupported Data	
10.8.1	Corrupted data						No response; PEC not supported
10.8.2	Sending too few bits			X	X		
10.8.3	Reading too few bits			X	X		
10.8.4	Host sends or reads too few bytes			X	X		
10.8.5	Host sends too many bytes	X		X		X	
10.8.6	Reading too many bytes		X	X	X		
10.8.7	Device busy	X	X				Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

Data Content Faults Implementation

This section describes data content fault as implemented in the internal µC.

Section	Description	Response to Host	STATUS_BYTE	STATUS_CML			Notes
		NAK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Improperly Set Read Bit In The Address Byte	X	X	X			
10.9.2	Unsupported Command Code	X	X		X		
10.9.3	Invalid or Unsupported Data		X			X	
10.9.4	Data Out of Range		X			X	
10.9.5	Reserved Bits						No response; not a fault

BCM in VIA Package Chassis (Lug) Mount Package Mechanical Drawing



PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'
2214 (0 STAGE) 2223	1.02 [25.96]	NA	2.25 [57.11]
2814 (1 STAGE) 2223	1.61 [40.93]	NA	2.84 [72.05]
2814 (0 STAGE) 3623	1.02 [25.96]	.789 [20.033]	2.80 [70.99]
3414 (1 STAGE) 3623	1.61 [40.93]	.789 [20.033]	3.38 [85.93]
3714 (1 STAGE) 4623	1.61 [40.93]	1.150 [29.200]	3.75 [95.12]
3814 (0 STAGE) 2361	**1.02 [25.96]**	**1.277 [32.430]**	**3.76 [95.59]**
3814 (0 STAGE) 2361 NBM	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]
4414 (1 STAGE) 2361	1.61 [40.93]	1.277 [32.430]	4.35 [110.55]
4414 (1 STAGE) 6123	1.61 [40.93]	1.757 [44.625]	4.35 [110.55]
5614 (1 STAGE) 2392	1.61 [40.93]	2.490 [63.250]	5.57 [141.37]
5614 (1 STAGE) 9223	1.61 [40.93]	2.970 [75.445]	5.57 [141.37]

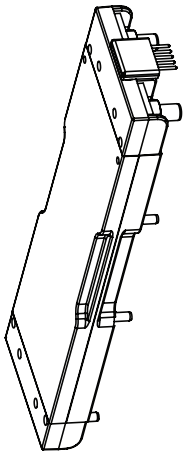
NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

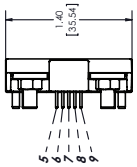
2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.

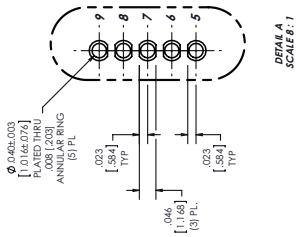
BCM in VIA Package PCB (Board) Mount Package Mechanical Drawing and Recommended Hole Pattern

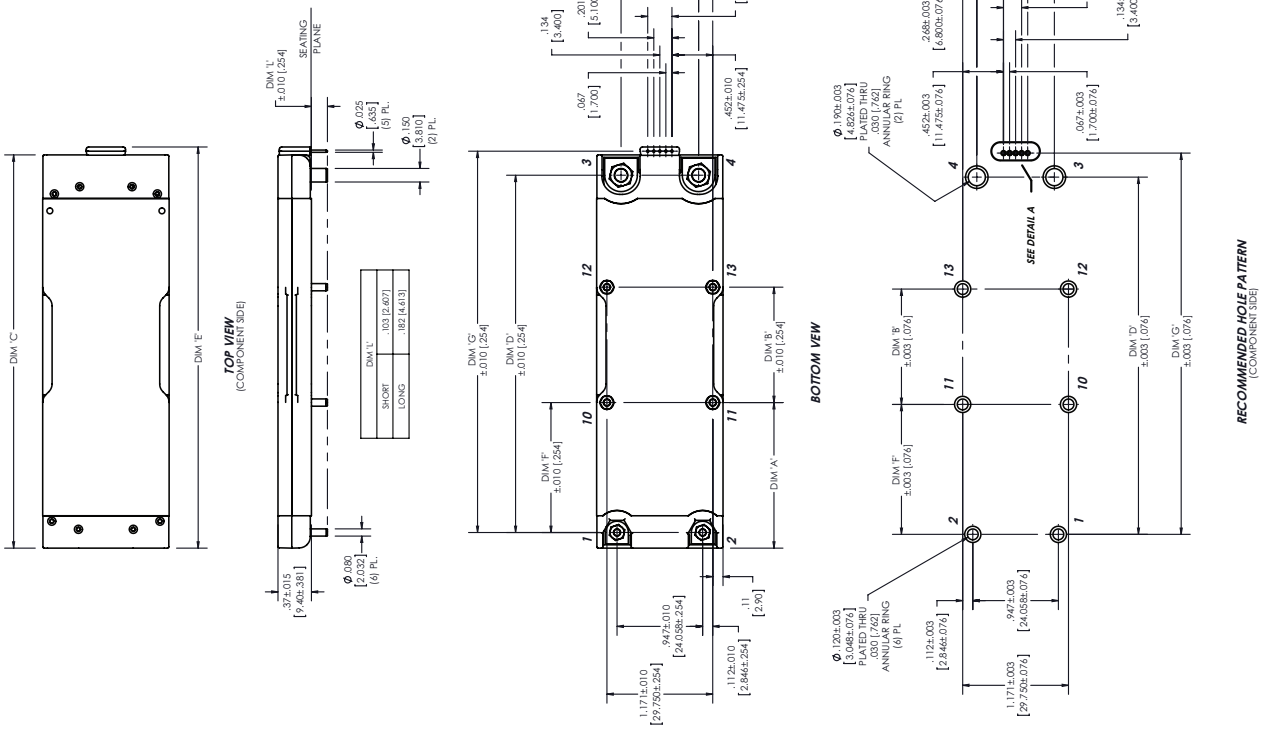
PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'E'	DIM 'F'	DIM 'G'
3814 (0 STAGE) 2361	**1.02 [25.96]**	**1.277 [32.430]**	**3.76 [95.59]**	**3.368 [85.554]**	**3.85 [97.80]**	**.850 [21.590]**	**3.632 [92.243]**
3814 (0 STAGE) 2361 NBM	1.02 [25.96]	1.277 [32.430]	3.76 [95.59]	3.368 [85.554]	3.85 [97.780]	.850 [21.590]	3.632 [92.243]
4414 (1 STAGE) 2361	1.61 [40.93]	1.277 [32.430]	4.36 [110.55]	3.957 [100.517]	4.44 [112.76]	1.439 [36.553]	4.221 [107.206]
5614 (1 STAGE) 2392	1.61 [40.93]	2.490 [63.250]	5.57 [141.37]	5.171 [131.337]	5.65 [143.58]	1.439 [36.553]	5.434 [138.026]



NOTES:
1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.
2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.







Revision History

Revision	Date	Description	Page Number(s)
1.0	03/3/16	Initial release	n/a
1.1	05/2/16	New Power Pin Nomenclature	All
1.2	06/17/16	Notes update	2, 3, 10
1.3	08/01/16	Charts format update	13, 14, 15
1.4	09/26/16	Value of R correction for READ_BCM_ROUT	23

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