

ZVS RESONANT CONVERTER FOR CONSUMER APPLICATION USING L6598 IC

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In this paper we study the details of the Multi-resonant Zero-current-switching converter which has smaller size and higher efficiency, and low noise operation. It will shown the design equations and demoboard results of a high-end TV power supply using ST L6598.

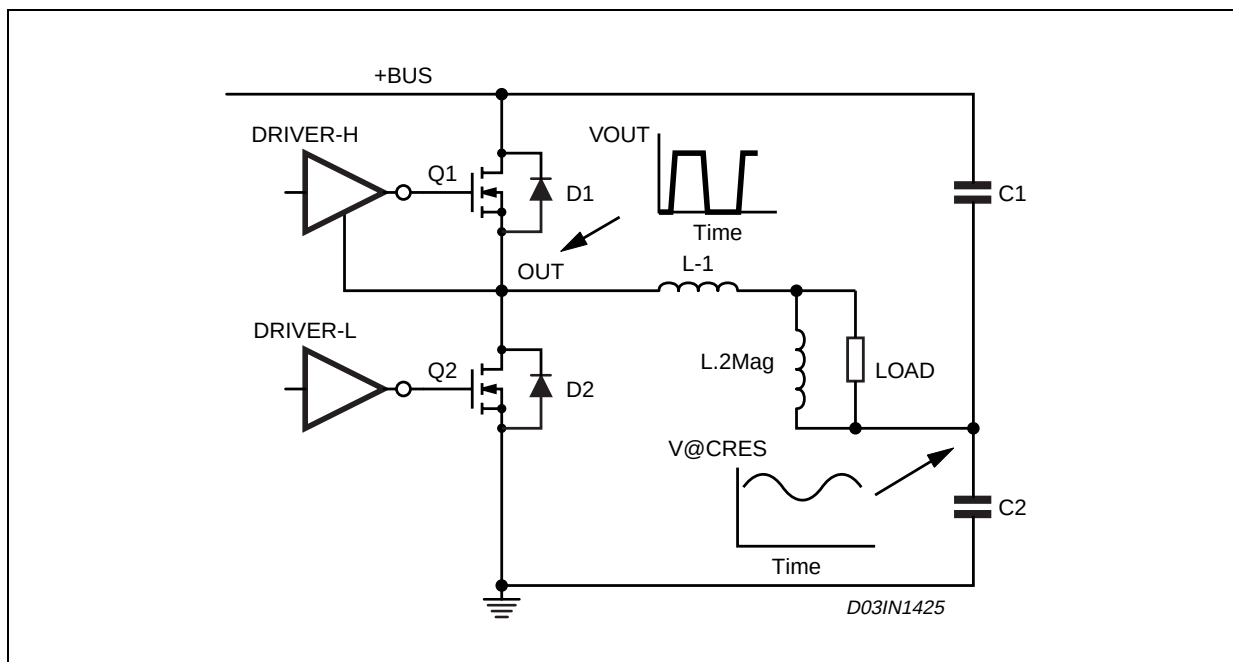
The small size, high efficiency, and low noise operation makes the half bridge resonant topology attractive for converters.

It will shown the design equations and demoboard test results of a high-end TV power supply using ST L6598.

1 CIRCUIT DESCRIPTION

The simplified schematic and operating waveforms are shown in Fig.1 and Fig.2.

Figure 1. Simplified Schematic



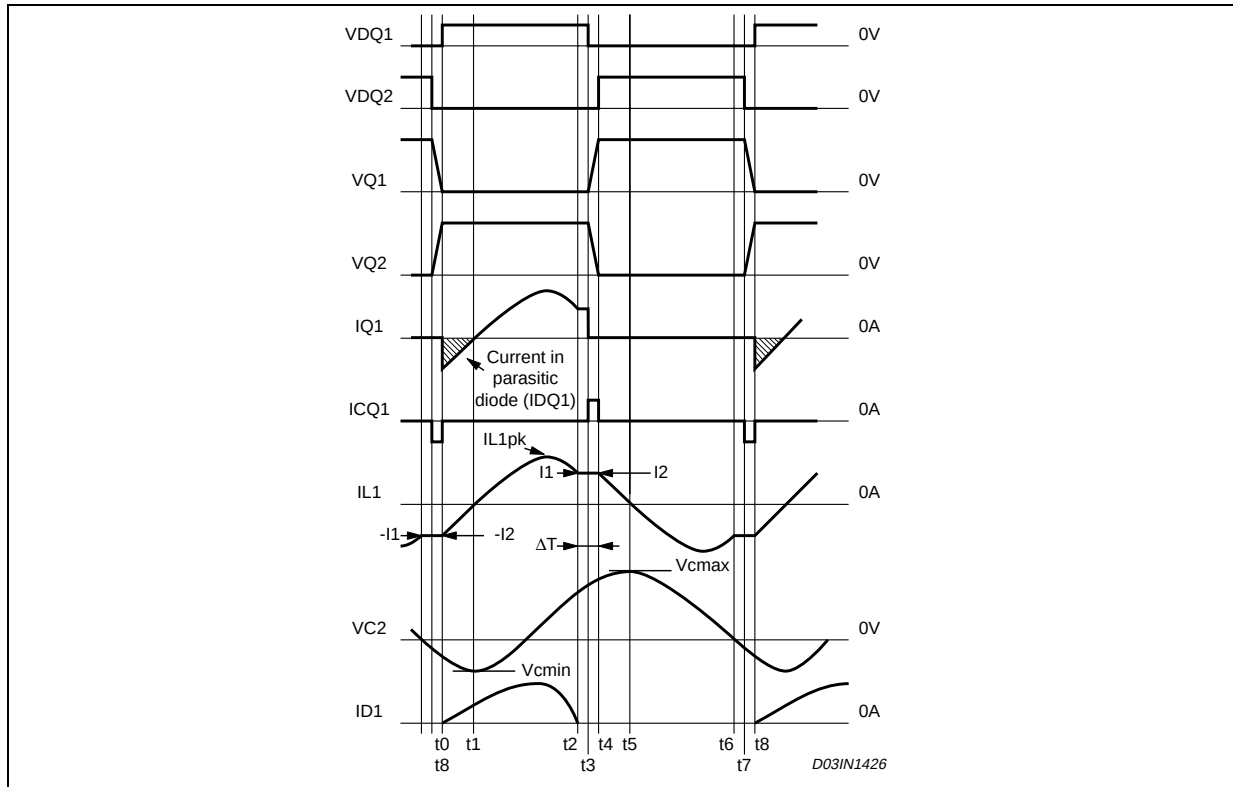
This half-bridge converter consists of switching devices Q_1 & Q_2 , resonant inductor L_1 , magnetizing inductor of transformer L_2 , resonant capacitors C_1 & C_2 , transformer T , rectifier diodes D_1 & D_2 , output capacitor C_{out} . C_{Q1} & C_{Q2} are the parasitic capacitors of the Q_1 & Q_2 . D_{Q1} & D_{Q2} are the parasitic reverse diodes of Q_1 & Q_2 .

Switching devices Q_1 & Q_2 repeat on and off alternately, and the on- and off-times are the same. 50% duty cycle.

This circuit has three operation.

1. The operation of a resonant circuit between L_1 and C_1+C_2 . Which supplies power to the load.
2. The operation of a resonant circuit between L_1+L_2 and C_1+C_2 . Which does not supply power with the load.
3. The operation of a resonant circuit between $C_{Q1} + C_{Q2}$, L_1+L_2 and C_1+C_2 . Which achieves the ZVS of the MOSFET.

Figure 2. Operating Waveforms



t0~t1:

In Q_1 reverse current flows through parasitic diode D_{Q1} . Q_2 is off.

The initial value of the resonant current between L_1 and C_1+C_2 at t_0 is $-I_2$, which coincide with the current in L_2 . The current in L_2 will increase at the rate of nV_{out}/L_2 ($n = N_1/N_2$, $N_2 = N_3$). At t_0 C_{Q1} is discharged. The voltage becomes zero. ZVS is achieved. The voltage of C_2 decreases further. C_2 is discharging.

t1~t2:

Q_1 is on and Q_2 is off.

The resonant current flows through Q_1 and in the opposite direction of $t_0\sim t_1$. The resonant current increases sinusoidally and reaches the maximum value then decreases till coincides with the current in L_2 at t_2 . The difference between resonant current and current in L_2 flows through the primary winding N_1 of the transformer. Power is supplied to the load.

t2~t3:

Q_1 is on and Q_2 is off.

The current I_1 in L_1 coincides with the current in L_2 at t_2 . No current flows through the secondary winding of the transformer. In this mode L_1+L_2 and C_1+C_2 resonate.

t3~t4:

Q_1 turns off at t3. Both Q_1 and Q_2 are off.

The charge stored in the parasitic capacitor C_{Q2} of Q_2 is discharged by means of the resonant current between L_1+L_2 and C_1+C_2 . Whereas C_{Q1} is charged.

t4~t5:

Q_1 is off. The resonant current flows through the parasitic diode D_{Q2} of Q_2 .

At t4 C_{Q2} is discharged. The voltage becomes zero. ZVS is achieved. The voltage of C_2 increases further.

t5~t6:

Q_1 is off and Q_2 is on.

The resonant current flows through Q_2 and in the opposite direction of t4~t5. The resonant current decreases sinusoidally and reaches the minimum value then increases till coincides with the current in L_2 at t6. The difference between resonant current and current in L_2 flows through the primary winding N1 of the transformer. Power is supplied to the load.

t6~t7:

Q_1 is off and Q_2 is on.

The current $-I_2$ in L_1 coincides with the current in L_2 at t6. No current flows through the secondary winding of the transformer. In this mode L_1+L_2 and C_1+C_2 resonate.

t7~t8:

Q_2 turns off. Q_1 and Q_2 are off.

The parasitic capacitor C_{Q2} of Q_2 is charged by means of the resonant current between L_1+L_2 and C_1+C_2 . Whereas C_{Q1} is discharged.

Here the circuit returns to the first mode and the cycle is repeated.

A main advantage of this resonant converter is that there are no turn-on switching losses exist in the FET because its inverse diode carries current and the voltage across the MOSFET is zero before the MOSFET conducts forward current.

There are still turn-off switching losses. But it can be erased by placing small snubber capacitors directly across the FET devices. And no discharge resistors are needed. This was because the capacitor is not discharged by turning the FET on but rather is discharged by turning-off the opposite FET.

Also the switching losses due to C_{oss} and C_{rss} is eliminated by the same reason mentioned before in the lossless snubbers. The energy stored in any capacitance directly across the device is returned to the DC source by virtue of the opposite FET turning off.

2 L6598 DEVICE DESCRIPTION

The L6598 is an integrated circuit realised in BCD OFF-LINE technology. Able to drive POWER MOS or IGBT, in half bridge topology, the L6598 is provided with all the features (such as VCO, SOFT-START, OP-AMP and ENABLES) needed to implement and control properly a resonant SMPS with a minimum components count. Even though the device is able to withstand high voltage (up to 600V), it can operate at low voltage starting from its operative supply.

Table 1. Device Pins Description

Pin N°	Name	Function
1	C _{SS}	Soft Start Timing Capacitor. The capacitor C _{SS} sets the soft start time, according to the relations: $T_{SS} = k_{SS}C_{SS}$ (typ. $k_{SS} = 0.15 \text{ s}/\mu\text{F}$). During t_{SS} the capacitor is charged by means of a current which depends on R _{fstart} value (i.e. on the difference between f _{start} and f _{min}). In this way T _{SS} is always set at $k_{SS}C_{SS}$ (i.e. T _{SS} depends only by C _{SS}). In steady state the voltage at pin 1 is 5V.
2	R _{fstart}	Maximum Oscillation Frequency Setting. The resistance connected between this pin and ground sets the f _{start} value, fixing the difference between f _{start} and f _{min} ($f_{start} > f_{min}$). The voltage at this pin is fixed at V _{REF} = 2V, and so R _{fstart} set the I _{fstart} current equal to V _{REF} /R _{fstart} . The minimum R _{fstart} value which can be connected to this pin is 25 kOhm.
3	C _f	Oscillator Frequency Setting. The capacitor C _f along with to R _{fstart} and R _{fmin} , sets f _{start} and f _{min} . In normal operation this pin shows a triangular wave.
4	R _{fmin}	Minimum Oscillation Frequency Setting. The resistance connected between this pin and ground sets the f _{min} value. The voltage at this pin is fixed at V _{REF} = 2V, and so R _{fmin} set the I _{fmin} current equal to V _{REF} /R _{fmin} . The minimum R _{fmin} value which can be connected to this pin is 25 kOhm.
5	OP _{out}	Out of the operational amplifier. To implement a feedback control loop this pin can be connected to the R _{fmin} pin by means an appropriate circuitry.
6	OP _{on-}	Inverting Input of the operational amplifier.
7	OP _{on+}	Non Inverting Input of the operational amplifier.
8	EN1	Enable 1. This pin (active high), forces the device in a latched shutdown state (like in the under voltage conditions). There are two ways to resume normal operation. The first is to reduce the supply voltage below the undervoltage threshold and then increase it again until the valid supply is recognized. The second is activating EN2 input. The enable 1 is especially designed for strong fault (e.g. in case of short circuit).
9	EN2	Enable 2. EN2 input (active high) restarts the start-up procedure (soft-start sequence).
10	GND	Ground
11	LVG	Low Side Driver Output. This pin must be connected to the low side power MOSFET gate of the half bridge. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
12	V _s	Supply Voltage. This pin, connected to the supply filter capacitor, is internally clamped (15.6V typical).
13	N.C.	Not Connected. It ensures the insulation between the high voltage section and the low voltage one.
14	OUT	High Side Driver Floating Reference. This pin must be connected close to the source of the high side power MOS or IGBT.
15	HVG	High Side Driver Output. This pin must be connected to the high side power MOSFET gate of the half bridge. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
16	V _{boot}	Bootstrapped Supply Voltage. Between this pin and V _s must be connected the bootstrap capacitor. A patented integrated circuitry replaces the high voltage external diode. This features is achieved by means of a high voltage DMOS, synchronously driven with the low side power MOSFET.

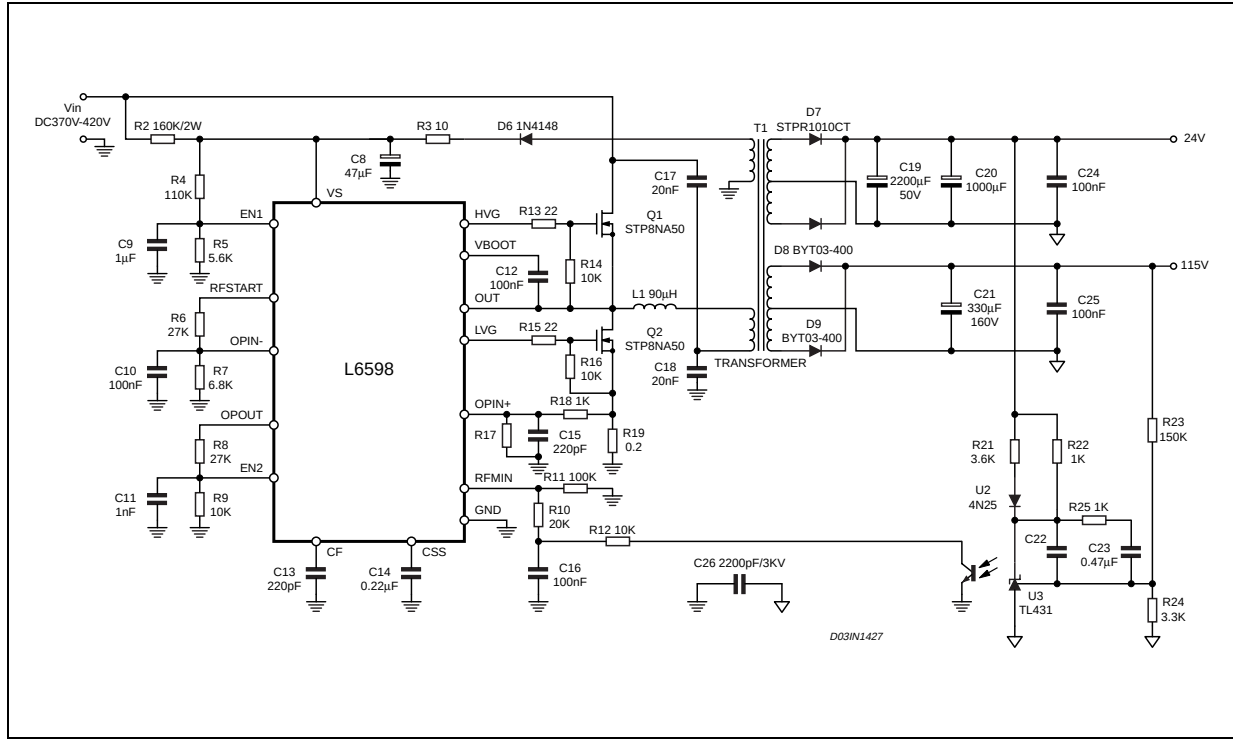
3 ANALYSIS AND DESIGN EQUATIONS

Following assumptions is for simplify the analysis.

- 1) All circuit components are ideal devices.
- 2) DT (Fig.2) is very short compared to the resonant time. $DT = 0$, and $I_1 = I_2$.

Fig.3 is the schematic of L6598 resonant converter demoboard.

Figure 3. 180W Half-Bridge resonant with the L6598: electrical schematic



The spec. of the power supply.

Input voltage: DC 370V ~ 420V (output of a PFC stage)

Output voltage: 110V/1.2A , 24V/2A

Output power : 180W

3.1 Resonant frequency and switching frequency

Before the design, we need to decide several operation frequencies of converter. That include the start switching frequency - F_{start} , minimum switching frequency - F_{min} and resonant frequency - F_r .

In this application, we choose:

$F_{start} = 250\text{KHz}$ (by design R_{fstart} of L6598)

$F_{min} = 68\text{KHz}$ (by design R_{fmin} of L6598)

$F_r = 84\text{KHz}$ (by design L_1 , C_{17} , C_{18})

To calculate R_{fstart} and R_{fmin} , using below equations:

$$R_{fmin} = \frac{1.41}{F_{min} C_f} \quad (1)$$

$$R_{fstart} = \frac{1.41}{(F_{start} - F_{min}) C_f} \quad (2)$$

Choose Cf = 220pF, then

$$R_{fmin} = \frac{1.41}{68 \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 94.2k\Omega \div 100k\Omega$$

$$R_{fstart} = \frac{1.41}{(250 - 68) \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 32.5k\Omega$$

Rfstart is 35.2Kohm , this is larger than the minimum value of Rfstart which is 25Kohm.

In this application, we use R6, R7 voltage divider to get a fixed voltage to Pin6 (OPin-) as the voltage of Pin2 (Rfstart) is fixed at Vref = 2V. At the same time Pin7(OPin+) connected to primary current sense resistor. Voltage of Pin7 (Vopin+) will increase while output power increase. The output of the operational amplifier will be high when Vopin+ tends to be higher than Vopin-. Then another voltage divider R8, R9 will send this high voltage to Pin9 (EN2). L6598 will stop the normal operation and restart as long as EN2 is high. Thus over-current-protection is achieved.

If set R6 = 27Kohm , R7 = 6.8Kohm, then the input voltage for Pin6 is 0.4V.

Now, Rfstart = R6+R7 = 33.8Kohm

Rfmin = R11 = 100Kohm

Recalculated Fstart & Fmin. Fmin is 64KHz, Fstart is 254KHz.

The design for resonant components will be finished in the followed step.

3.2 Design transformer and resonant components

First select core size.

$$A_p = \left(\frac{11.1 \cdot P_{in}}{k \cdot \Delta B \cdot F} \right)^{1.31} \quad (3)$$

For half-bridge converter, k = 0.165

With Pout = 180W, η = 94%, ΔB = 0.4T, Fmin = 64KHz,

Calculated Ap = 0.402 cm⁴

Choose core: EC39, with Ae = 1.32cm²

$$N_{pmin} = \frac{V_{in(min)} \cdot 10^4}{2 \cdot f_{smin} \cdot \Delta B \cdot A_e} \quad (4)$$

$$N_{pmin} = \frac{370 \cdot 10^4}{2 \cdot 68 \cdot 10^3 \cdot 0.4 \cdot 1.32} = 51.5$$

$$n = \frac{N_p}{N_{s1}} \geq \frac{\frac{V_{inmax}}{2}}{V_{o1} + V_{F1}} \quad (5)$$

$$n \geq \frac{\frac{420}{2}}{110 + 1} = 1.9$$

$$N_{s2} = \frac{(V_{o2} + V_{F2})N_{s1}}{V_{o1} + V_{F1}}$$

We choose $N_p = 52T$, $n = 2$

Then $N_{S110} = 26T$. This is 110V winding.

The turns of 24V winding is 6.

The turns of V_{cc} supply winding is 3.

Now design the resonant components.

Set normalize output voltage is $M = 0.95$

Set normalize output current is $J = 0.2$

$$Z_o = \frac{\left(\frac{V_{inmax}}{2}\right)^2 \cdot J \cdot M}{V_o \cdot I_o} \quad (6)$$

$$Z_o = \frac{\left(\frac{420}{2}\right)^2 \cdot 0.2 \cdot 0.95}{(110 \cdot 1.2) + (24 \cdot 2)} = 46.55$$

$$L_r = \frac{Z_o}{2\pi f_r} = \frac{56.55}{2\pi \cdot 84 \cdot 10^3} = 88.2\mu H \quad (7)$$

$$C_r = \frac{1}{2\pi f_r \cdot Z_o} = \frac{1}{2\pi \cdot 84 \cdot 10^3 \cdot 46.55} = 40.6nF \quad (8)$$

$C_r = C_{17} + C_{18}$,

Choose $C_{17} = C_{18} = 20nF$, then $C_r = 40nF$

Recalculate L_r under $F_r = 84KHz$. $L_r = L_1 = 90\mu H$

Choose primary inductance L_2 as 5 ~ 10 times the resonant inductance. $L_2 = 500\mu H$

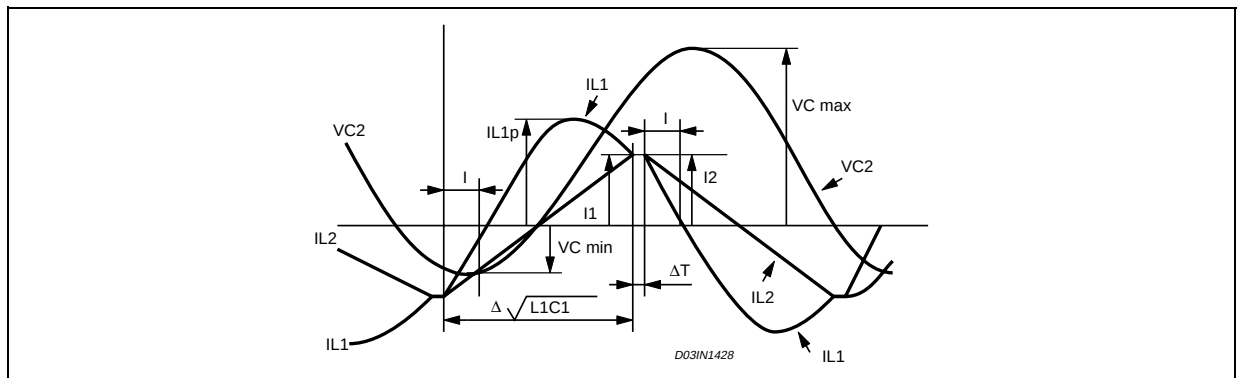
Now the resonant frequency of total circuit is

$$f_o = \frac{1}{2\pi \sqrt{(L_2 + L_1) \cdot C_r}} = 32.5kHz \quad (9)$$

3.3 conditions for resonance between L_2 and resonant circuit (L_1 , $C_{17} + C_{18}$)

When the resonant between L_2 and the resonant circuit starts, current I_{L2} varies from $-I_2$ to $+I_1$ during $t_2 - t_1$, and the voltage is nV_{out} and constant. The operating waveforms are shown in Fig. 4

Figure 4. operating waveforms



Therefore.

$$nV_{out} = L_2 \cdot \frac{I_1 + I_2}{\frac{T_r}{2}} \quad (10)$$

$$T_r = \frac{T_r}{2} = \pi \sqrt{L_1 C_r} \quad (11)$$

When assumed $I_1 = I_2$, then

$$I_1 = \frac{nV_{out} \cdot T_r}{2L_2} \quad (12)$$

Calculated value of I_1 is 1.32A.

3.4 Maximum voltage V_{cmax} and minimum voltage V_{cmin} of resonant capacitor

The voltage of the resonant capacitor varies in accordance with the charge and discharge current in both the resonant circuits between L_2 and $C_{17}+C_{18}$, and between L_1+L_2 and $C_{17}+C_{18}$.

The following equation shows the relation between the maximum value V_{cmax} and the minimum value V_{cmin} of the resonant capacitor voltage.

$$V_{c \max} = V_{c \min} + 2(V_{in} - nV_{out} - V_{c \min}) + \Delta V_c \quad (13)$$

nV_{out} : primary voltage of transformer

ΔV_c : charge in value of resonant capacitor voltage in the resonant circuit between L_1+L_2 and $C_{17}+C_{18}$

Where

$$V_{c \max} + V_{c \min} = V_{in} \quad (14)$$

The V_{cmax} and V_{cmin} are derived from the relation with the output current. And the output current I_{out} is:

$$I_{OUT} = \frac{n}{T_r + \Delta T} \int_0^{T_r} (i_{L_1} - i_{L_2}) dt \quad (15)$$

Where i_{L_1} and i_{L_2} are as follows:

$$i_{L_1} = (V_{in} - nV_{out} - V_{cmin}) \sqrt{\frac{C_r}{L_1}} \sin\left(\frac{t}{\sqrt{L_1 C_r}} - \theta\right) \quad (16)$$

$$i_{L_2} = \frac{I_1 + I_2}{T_r} t - I_2 \quad (17)$$

θ is the period of $t_0 \sim t_1$. While assume $\Delta T = 0$, and $I_1 = I_2$

$$I_{out} = \frac{2n\sqrt{L_1 Cr}}{T_r} \sqrt{(V_{in} - nV_{out} - V_{cmin})^2 \frac{Cr}{L_1} - I_1^2} \quad (18)$$

According to this equation, the minimum voltage V_{cmin} is obtained as follows:

$$V_{cmin} = V_{in} - nV_{out} - \sqrt{\frac{\left(I_{out} \cdot \frac{T_r}{2n\sqrt{L_1 \cdot Cr}}\right)^2 + I_1^2}{\left(\frac{Cr}{L_1}\right)}} \quad (19)$$

The V_{cmax} can be calculated according to equation (14). The maximum voltage applied to the resonant capacitor tends to increase as the output current increase.

Calculated V_{cmax} in this application is 310V at maximum output power.

3.5 Peak value I_{L1pk} of resonant current

Resonant current I_{L1} is calculated according to equation (16). The peak value of I_{L1} is

$$I_{L1pk} = (V_{in} - nV_{out} - V_{cmin}) \sqrt{\frac{Cr}{L_1}} \quad (20)$$

Calculated I_{L1pk} is 1.9A in this application.

3.6 Over current protection and over voltage protection

We set the over current protection point at $I_{L1pk} = 2.1A$. As the inverting input of operational amplifier is 0.4V, The calculated R_{sense} will be $0.4V/2.1A = 0.19\Omega$. Choose $0.2\Omega/1W$ resistor as R_{sense} (R20). Then the voltage on R20 will be 0.42V at expected OCP point.

By choosing the suitable voltage divider R18 and R17, we can get the 0.4V voltage to OPin+.

In this application we choose $R17 = 39K\Omega$, $R18 = 1K\Omega$.

Over voltage protection is achieved by sense the supply voltage of L6598 --Vs. R4 and R5 is a voltage divider which connected to Pin8 (EN1). When the voltage of Pin8 is higher than the threshold 0.6V, it forces the device in a latched shut down state.

By choose $R4 = 110K\Omega$ and $R5 = 5.6K\Omega$, the OVP is triggered at $V_s = 12.4V$. That is 10% higher than the normal operating voltage.

4 EVALUATION RESULT OF DEMOBOARD

4.1 Operating waveforms

See the operating waveform in Fig.5

The measured value : I_L is 1.4A, V_{cmax} is 300V, I_{L1pk} is 1.9A.

That is coincide with the calculated value.

Figure 5. Operating Waveform

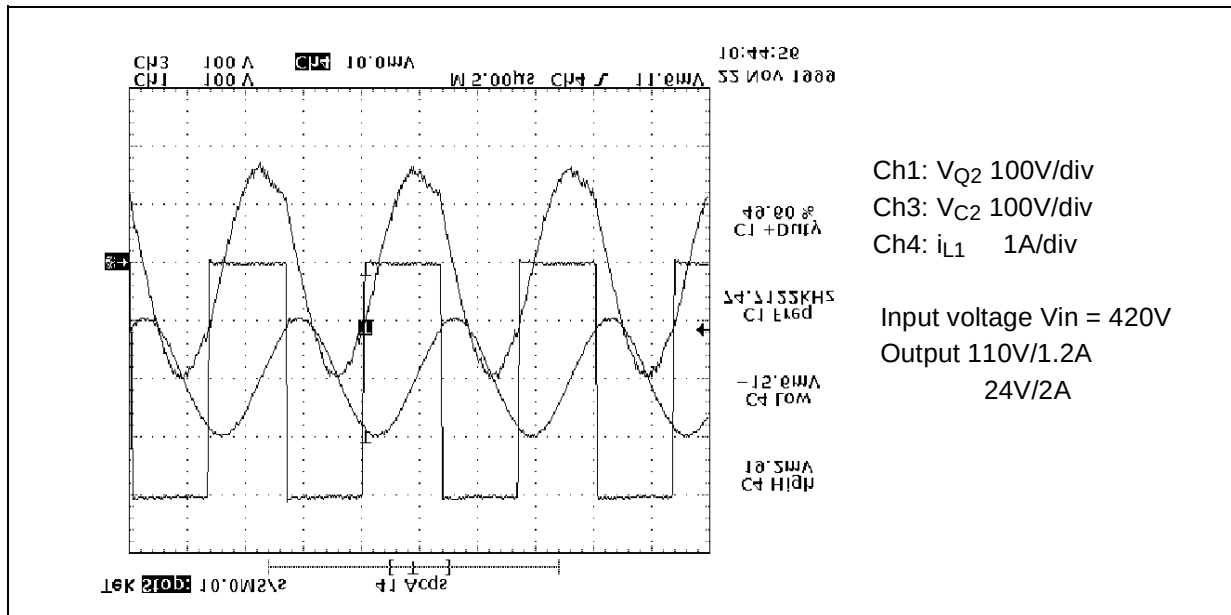
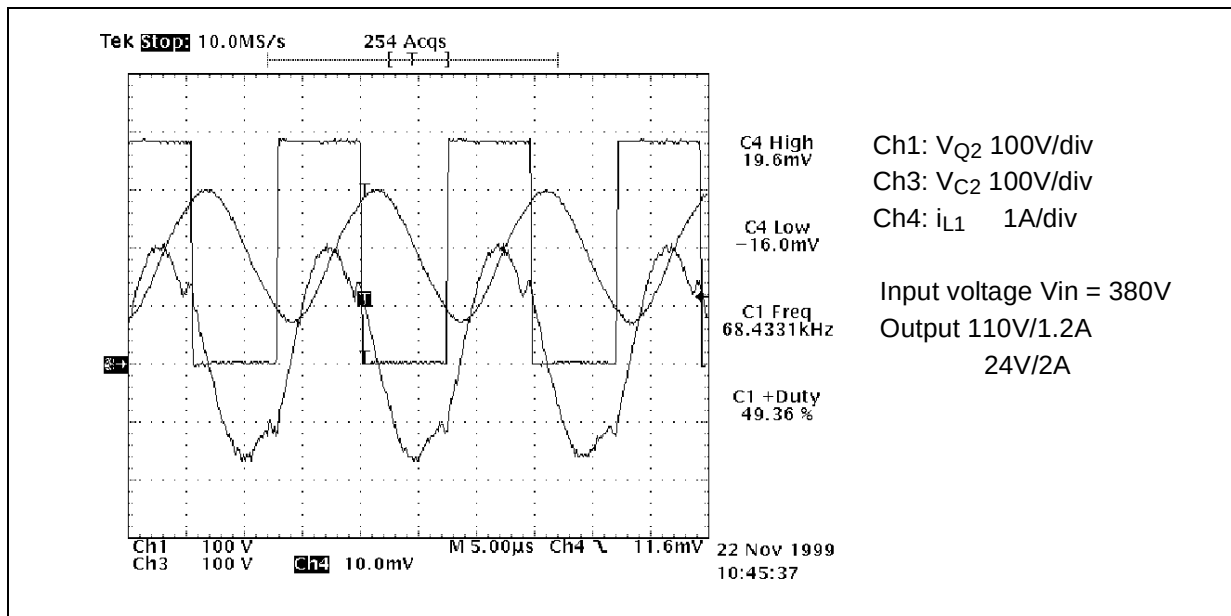


Figure 6.



4.2 Switching frequency characteristics

Figure 7. switching frequency vs input voltage

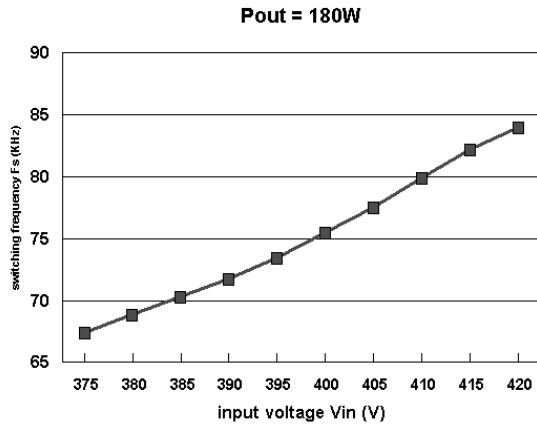
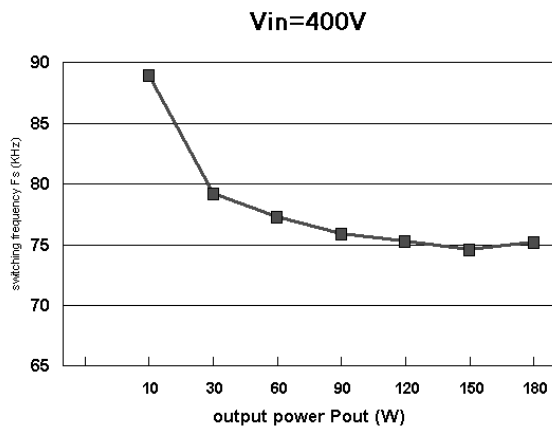


Figure 8. switching frequency vs output power



4.3 Efficiency characteristics

Figure 9. efficiency vs output power

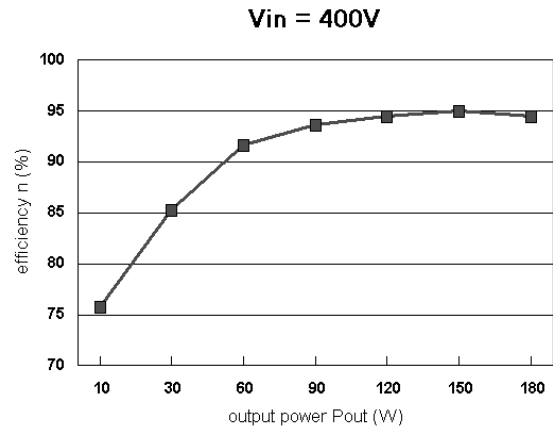
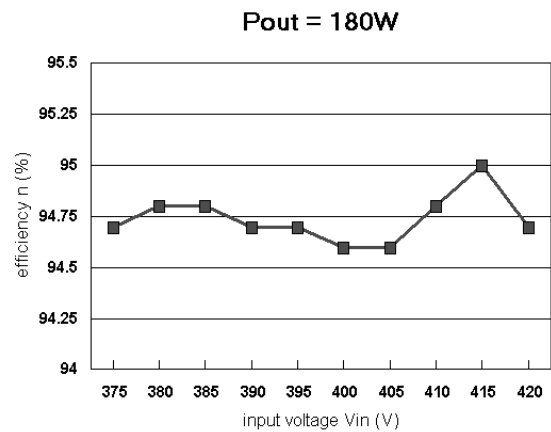


Figure 10. efficiency vs input voltage



The maximum efficiency is 95% at maximum output power of 180W.

4.4 OCP and OVP

The power supply will automatically pass in restart procedure when the output power exceed a certain value. In experiment, set output current 1.8A to 110V & 2A to 24V, the voltage of pin 9 (EN2 of L6598) will be higher than 1V and the IC restarts the start-up sequence. Thus the OCP achieves. The maximum output power is slightly depend on the input voltage. In this demo board the maximum output power is around 240W.

The over-current-protection will be active as well when 24V or 110V is under short circuit condition.

The operating frequency tends to increase as the output load decrease. The maximum switching frequency is limited by $(R10+R12)/R11$. Using equation (1) we can calculate the Fmax value. It is 278KHz. When the maximum frequency is reached and the load reduced further, the output voltage will no longer be regulated and tends to increase. So does the Vs voltage of L6598. Once Vs rise to 12.2V, the over-voltage-protection will be triggered.

In the demo board, the tested value is $V_s = 12.2V$ and $V_{o1} = 134V$, $V_{o2} = 29V$.

So to keep the output voltage regulated, a minimum output power is request. The test result can be find in the following table.

Table 2.

Input Voltage (DC)	370V	420V
Output minimum power	4W 110V/30mA 24V/30mA	9.5W 110V/80mA 24V/30mA
Switching frequency	70KHz	240KHz
Input power	7.3W	13W

The maximum switching frequency can be designed to a higher value to reduce the minimum output power by reducing the value of $(R10+R12)$. But the Fmax has a upper limitation given by L6598. It can not exceed 350KHz.

5 CONCLUSION

We could obtain high efficiency in this circuit. Because both ZVS, ZCS can be achieved of turn-on and ZVS can be achieved of turn-off.

The major drawback of this kind of converter is the line regulation is not good. So it is better to use the converter after a PFC circuit.

6 REFERENCE

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