Features

- **4Mbits x1 Non Volatile Memory Designed to Store Field Programmable Gate Arrays (FPGAs) Configurations**
- **In-System Programming (ISP) via Two-Wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT40KEL040 and ATF280E FPGAs**
- **Cascadable Read-back to Support Additional Configurations or Higher-density Arrays**
- **Low-power RadHard non volatile CMOS process**
- **Programmable Reset Polarity**
- **Low-power Dissipation**
  - **Active read: 18mW max**
  - **Standby mode: 3.6mW max**
- **High-reliability**
  - **Endurance: 50,000 Write Cycles (page mode)**
  - **Data Retention: 10 Years**
- **4Mbits On-chip Flash Array**
  - **512 bytes Page Write**
- **No Single Event Latch-up below a LET Threshold of 80MeV/mg/cm^2**
- **Tested up to a Total Dose of 60KRads (Si) (according to MIL STD 883 Method 1019)**
- **Operating Range:**
  - **Voltage: 3V to 3.6V**
  - **Temperature: -55 to +125°C**
- **Quality Grades:**
  - **QML-Q or V**
  - **ESCC**
- **Package: 305 Mils FP18**
- **Mass: 10 grams**

Space FPGA Configuration Memory

AT69170E

Advanced Information

1. Description

The AT69170E FPGA configuration memory (configurator) is an electrically erasable and re-programmable RadHard memory organized as 4Mx1bit. It is an easy-to-use and cost-effective configuration memory for space Field Programmable Grid Array (FPGA). It is manufactured with ATMEL 0.18µm low power non volatile CMOS RadHard process.

It is packaged in a 18-pin 305 Mils wide Flat Pack package. AT69170E uses a simple serial-access procedure to configure one or more FPGA devices. A two wire interface (TWI) is available for memory programming.

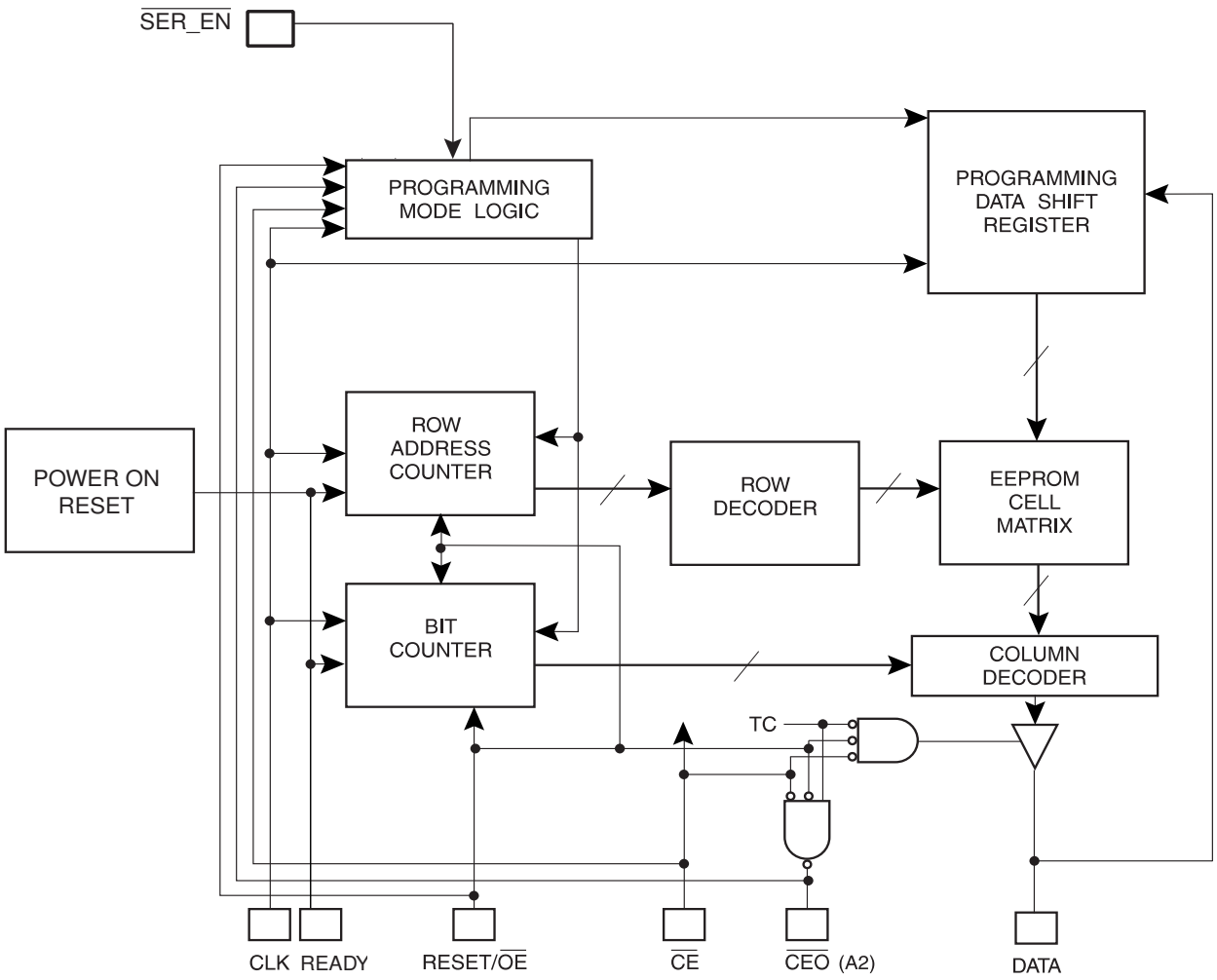
The user can select the polarity of the reset function by programming a dedicated test sequence. These devices also support a write-protection mechanism within its programming mode.

The factory blanks devices to all ‘1’ before shipping.

7752A–AERO–07/07

2. Block Diagram

Figure 2-1. AT69170E Block Diagram

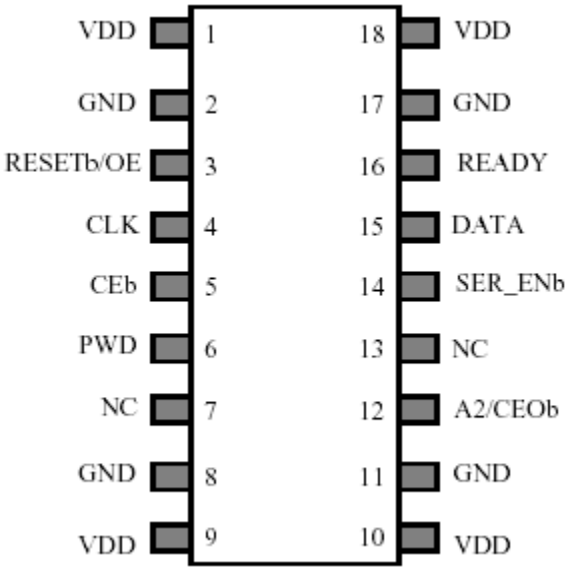


3. Pin Configuration

3.1 Package Description

The AT69170E is packaged in a 18-pins Flat Pack package.

Figure 3-1. AT69170E pin assignment in FP18 package



Note: 1. The package lid is connected to GND

3.2 Signal Description

Table 3-1. Signal Description - Overview

Pin Name	Function
$\overline{\text{RESET}}$/OE	Reset / Output Enable Input
$\overline{\text{CE}}$	Chip Enable Input
A2/$\overline{\text{CEO}}$	Device Select/ Chip Enable Output
CLK	Clock Input
DATA	Data Output
READY	Reset State Indicator Output
$\overline{\text{SER\_EN}}$	Serial Enable Input
PWD	Power Down Input
GND	Ground
V_{DD}	Power Supply

3.2.1 $\overline{\text{RESET}}$/OE

Reset / Output Enable input

The logic polarity of this input is programmable as either $\overline{\text{RESET}}$/OE or RESET/$\overline{\text{OE}}$. For ATMEL FPGA, RESET should be programmed active Low and OE active High. This document therefore describes the pin as $\overline{\text{RESET}}$/OE.

The $\overline{\text{RESET}}$/OE pin of the memory is by default RESET (active Low) and Output Enable (active High) when $\overline{\text{SER\_EN}}$ is High.

A Low level on $\overline{\text{RESET}}$/OE resets both the address and bit counters.

A High level on $\overline{\text{RESET}}$/OE (with $\overline{\text{CE}}$ Low) enables the data output driver.

3.2.2 $\overline{\text{SER\_EN}}$

Serial mode Enable (active Low).

Serial mode Enable is held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the Two-Wire Serial Programming Mode. For applications not using the serial mode, $\overline{\text{SER\_EN}}$ should be tied to V_{DD}.

3.2.3 $\overline{\text{CE}}$

Chip Enable input (active Low).

A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode.

Note that this pin will *not* enable/disable the device in the Two-Wire Serial Programming mode (when $\overline{\text{SER\_EN}}$ Low).

3.2.4 A2/$\overline{\text{CEO}}$

A2 Device selection input/Chip Enable Output (active Low).

A2 Device selection input is used to enable (or select) the device during programming (i.e. when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pull-down resistor.

Chip Enable Output (active Low). This output goes Low when the address counter of the memory has reached its maximum value. In a daisy chain of AT69170E EEPROM, the $\overline{\text{CEO}}$ pin of one device must be connected to the $\overline{\text{CE}}$ input of the next device in the chain. $\overline{\text{CEO}}$ will stay Low as long as $\overline{\text{CE}}$ is Low and OE is High. It will then follow $\overline{\text{CE}}$ until OE goes Low. Thereafter, $\overline{\text{CEO}}$ will stay high until the entire EEPROM is read again.

3.2.5 CLK

Clock input.

The clock input is used to increment the internal address and bit counter for reading and programming.

3.2.6 DATA

DATA input and output

The DATA I/O is a three-state output for FPGA configuration.

It is an open-collector bi-directional pin for programming.

3.2.7 READY

Open collector reset state indicator (output).

The READY line is driven Low during power-up reset. It is then released when power-up is complete. It is recommended to use a 4.7 kΩ pull-up resistor when this pin is used.

3.2.8 PWD

Power Down input (active high)

Driving High the PWD input pin of the memory reduces the memory power consumption down to less than 1mA. For normal operation of the memory, PWD pin shall be tied to a Low level.

3.2.9 VDD

Power supply input pin.

3.2.10 GND

Ground pin.

A 0.2 µF decoupling capacitor between VDD and GND is recommended.

4. Power-on mode

The AT69170E provides a READY output pin to indicate that the memory power-on sequence is ended and that it is ready for use. This pin is available as an open-collector indicator of the device's reset status. It is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.

It is recommended to pull-up this pin through a 4.7KOhms resistor.

5. Standby mode

The AT69170E configurator enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input. Power Consumption is reduced to less than 5mA of current at 3.3V.

6. Power down mode

In addition to the standby mode, the AT69170E implements a power down mode. In this mode, the AT69170E consumes less than 1mA of current at 3.3V.

The power down mode is entered driving High the PWD input pin of the memory. For normal operation of the memory, PWD pin shall be tied to a Low level.

7. Programming mode - TWI mode

The AT69170E is a serial EEPROM memory used to load programmable devices. AT69170E content is loaded and read thanks to a simple 2-wire serial interface (TWI). The programming mode is entered if $\overline{SER\_EN}$ is driven Low. In this mode the chip can be programmed by the Two-Wire serial interface (TWI).

The 2-wire interface (TWI) is based on a simple synchronous protocol where one wire (CLOCK) functions as a clock and shall be provided by the programmer and the second wire (DATA) is a bi-directional signal and is used to provide data and control information. The system must provide a small pull-up current for the DATA line.

Information is transmitted on the serial bus in frames made of:

- A Start Condition
- A Data field with Acknowledge bits
- A Stop Condition

Each frame begins with a Start Condition and is ended with a Stop Condition. The data field is made of an integer number of data bytes, each data byte consisting of 8 data bits followed by a 9th Acknowledge Bit. This Acknowledge Bit is provided by the recipient of the transmitted byte.

7.1 TWI Frame Description

While writing to the AT69170E, the programmer is responsible for issuing the instruction and data. The AT69170E acknowledges the transfer. While reading from the AT69170E, the programmer issues the instruction and acknowledges the data from the memory as necessary.

Data on the DATA pin may change only during the CLOCK Low time; whereas Start and Stop Conditions are identified as transitions during the CLOCK High time.

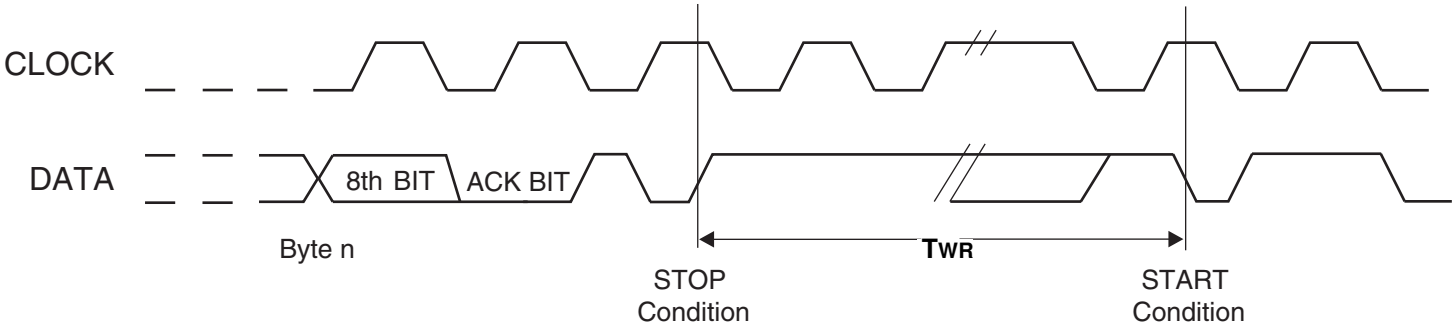
All bytes from accepted messages must be terminated by either an Acknowledge Bit or a Stop Condition.

7.1.1 Start and Stop Conditions

The Start Condition is indicated by a high-to-low transition of the DATA line when the CLOCK line is High. The Start Condition will return the device to the state where it is waiting for a Device Address.

The Stop Condition is generated by a low-to-high transition of the DATA line when the CLOCK line is High. The Stop Condition initiates an internally timed write signal whose maximum duration is T_{WR} (refer to the AC Characteristics tables for actual value). During this time, the Configurator must remain in programming mode (i.e., SER_EN is driven Low). DATA and CLOCK lines are ignored until the cycle is completed.

Figure 7-1. Start and Stop Conditions



7.1.2 Data Field Format

The data field consists of an integer number of bytes, each byte consisting of 8 bits of data, followed by a 9th Acknowledge Bit. This Acknowledge Bit is provided by the recipient of the transmitted data byte. Data on the DATA pin may change only during the CLOCK Low time.

The data field of the TWI frame is used to transmit addresses and data. Depending on the type of the byte transferred, bit ordering differs.

7.1.2.1 Device Address Byte

For the Device Address Byte, the **most significant bit** (MSB) of the data byte is the **first** bit transmitted on the DATA line. The least significant bit (LSB) is the last bit transmitted.

The Device address byte is defined as follow:

Table 7-1. Device Address Byte

Bit number	MSB - 7	6	5	4	3	2	1	LSB - 0
value	1	0	1	0	A2	1	1	R/$\overline{W}$
transfer order	1st	2nd	3rd	4th	5th	6th	7th	8th

The A2 bit is provided to allow selection of a memory in case multiple AT69170E share a common bus. When the A2 pin of the device is driven high(1), A2 bit shall be set logical ‘1’ in the command issued to the memory in order to select it. When A2 pin is driven low(1), A2 bit shall be set logical ‘0’ in the command.

The R/$\overline{W}$ bit is used to define the type of transfer. It shall be set logical ‘1’ for a read operation and logical ‘0’ for a write operation.

Note: 1. A2 pin on the Configurator must be forced to a logic “0” or “1” level. It is recommended that this pin is connected to GND or VDD using a 4.7 kΩ pull resistor.

7.1.2.2 EEPROM Address Bytes

The AT69170E EEPROM Address consists of three bytes. These bytes define the normal address space of the memory. Unused bits in an Address Byte must be set to “0”

For each byte of the EEPROM Address Bytes, the **most significant bit** (MSB) of the data byte is the **first** bit transmitted on the DATA line. The least significant bit (LSB) is the last bit transmitted.

Address Bytes are transmitted on the data line starting from the most significant byte and finishing with the least significant byte.

The EEPROM address being built of more than one byte, each byte of the address is acknowledged by the memory. Each Address Byte is followed by an Acknowledge Bit from the EEPROM.

Table 7-2. EEPROM Address

MSB							LSB	ACK	MSB							LSB	ACK	MSB							LSB	ACK
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	
0	0	0	0	0	A_{18}	A_{17}	A_{16}		A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8		A_7	A_6	A_5	A_4	A_3	A_2	0	0	
1st	2nd	3rd	4th	5th	6th	7th	8th	9th	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	1st	2nd	3rd	4th	5th	6th	7th	8th	9th

The EEPROM address shall be aligned on a multiple of 4 bytes (A1 =0 and A0=0) for all read/write operations.

Exceptions to this are

- Data Protection configuration
- RESET Polarity configuration
- Erase command

See the description of each special command for address specific definition

7.1.2.3 Data Bytes

For Data Bytes (both writing and reading), the first bit transmitted is the least significant bit.

Table 7-3. Data Byte

Bit number	MSB - 7	6	5	4	3	2	1	LSB - 0
value	x	x	x	x	x	x	x	x
transfer order	8th	7th	6th	5th	4th	3rd	2nd	1st

7.1.2.4 *Acknowledge Bit*

The Acknowledge Bit is asserted on the DATA line by the receiving device on a byte-by-byte basis.

The Acknowledge (ACK) bit is provided by the memory itself when the programmer is writing to the memory. It is provided by the programmer when the programmer is reading from the memory.

A data byte is accepted by the receiver by asserting a Low value on the DATA line, or it is refused by asserting a High value on the DATA line.

7.2 TWI Operations

7.2.1 Write Operation

Writing to the AT69170E is based on a 512 bytes **page write operation**.

The AT69170E implements 1024 pages of 512 bytes that can be written one after the other.

The AT69170E is based on a 4-byte Word architecture. This is the reason why the number of byte written must be a multiple of 4 (an integer number of Word). From 4 bytes up to 512 bytes can be written in a single write sequence.

Write operation through the TWI interface is entered by bringing $\overline{\text{SER\_EN}}$ Low.

The first data Word (4 data bytes) is written at the transmitted address. The least significant byte of the Word is transmitted first. The last byte of a Word driven on the DATA line is the most significant Byte.

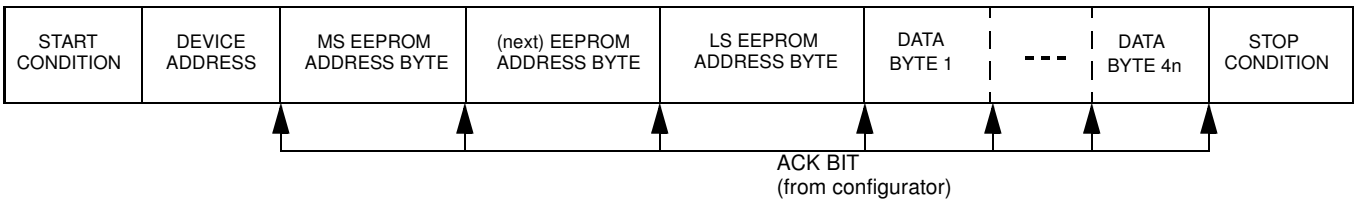
The address is incremented in the memory following the receipt of each Word. Only the lower bits of the address are incremented. Thus, after writing to the last byte address within the given page, the address will roll over to the first byte address of the same page. Writing can start at any aligned address (i.e.: A1=0 and A0=0) within a page.

Writing to the AT69170E memory consists of

- a Start Condition
- a Device Address Byte with R/W = 0
  - an Acknowledge Bit from the Configurator
- MS Byte of the EEPROM Address
  - an Acknowledge Bit from the Configurator
- (Next) Byte of the EEPROM Address
  - an Acknowledge Bit from the Configurator
- LS Byte of EEPROM Address double word aligned
  - an Acknowledge Bit from the Configurator
- 4n Data Bytes (sent to the Configurator)
  - each byte followed by an Acknowledge Bit from the Configurator
- a Stop Condition

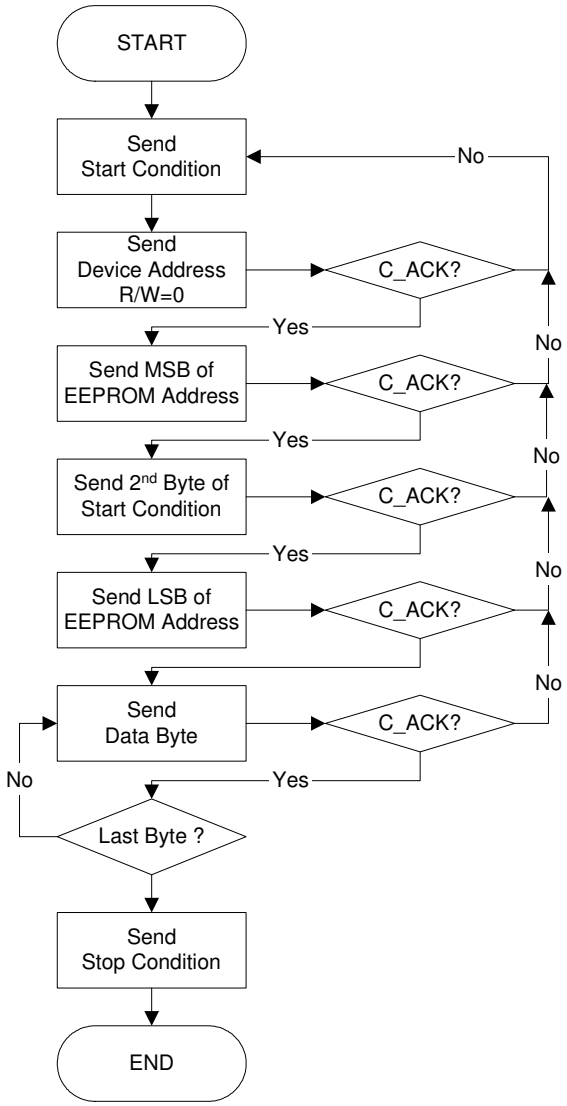
Here is an overview of the write instruction frame.

Figure 7-2. Write Instruction Frame



Here is a summary of the process a programmer shall use to program one page in the memory.

Figure 7-3. Page Programming Summary - TWI Write



C_ACK : Configurator send Acknowledge

7.2.1.1 Write polling

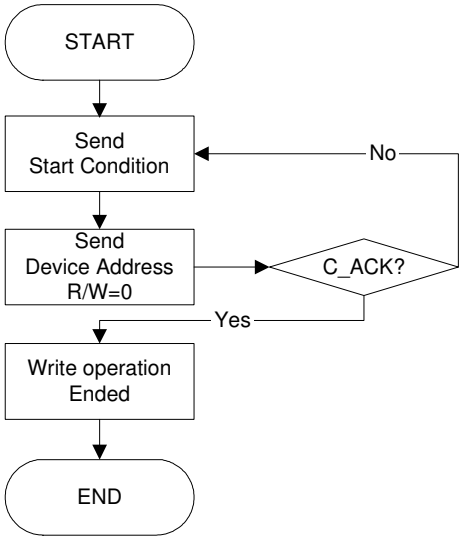
On receipt of the Stop Condition, the Configurator enters an internally-timed write cycle. While the Configurator is busy with this write cycle, it will not acknowledge any transfers.

The programmer can start the next page write by sending the Start Condition followed by the Device Address. As long as the internal write cycle is not ended, the AT69170E does not acknowledge the Device byte. Then the programmer should abandon the transfer without asserting a Stop Condition.

The programmer can then repeatedly initiate a write instruction as above, until an acknowledge is received. When the Acknowledge Bit is received, the write instruction should continue by sending the first EEPROM Address Byte to the Configurator.

An alternative to write polling would be to wait a period of t_{WR} before sending the next page of data or exiting the programming mode. All signals must be maintained during the entire write cycle.

Figure 7-4. Write Polling Summary - TWI Polling



C_ACK : Configurator send Acknowledge

7.2.2 Read Operation

Read instructions are initiated similarly to write instructions, but the R/W bit in the Device Address is set logical one. There are three variants of the read instruction: current address read, random read.

For all reads, it is important to understand that the internal Data Byte address counter maintains the last address accessed during the previous read or write operation, incremented by one. This address remains valid between operations as long as the chip power is maintained and the device remains in 2-wire access mode (i.e., SER_EN is driven Low). If the last operation was a read at address n, then the current address would be n + 1. If the final operation was a write at address n, then the current address would again be n + 1 with one exception. If address n was the last byte address in the page, the incremented address n + 1 would “roll over” to the first byte address on the next page.

7.2.2.1 Current address read

The current address read is the command used to read the memory starting from the address currently latched in the internal address counter. There is no need to transmit any address in the command sent by the programmer.

After the programmer receives a Data Byte, it shall respond with either an Acknowledge Bit or a Stop condition. As long as the Configurator receives an Acknowledge Bit, it will continue to increment the Data Byte address and serially clock out sequential Data Bytes until the memory address limit is reached. The Sequential Read instruction is terminated when the programmer

does not respond with an Acknowledge Bit, but instead generates a Stop Condition following the receipt of a Data Byte.

A Current Address Read instruction consists of

- a Start Condition
- a Device Address with R/W = 1
  - an Acknowledge Bit from the Configurator
- Data Bytes from the Configurator
  - an Acknowledge Bit from the programmer
- Data Byte from the Configurator
- a Stop Condition from the programmer.

Figure 7-5. Read From Current Address Frame format

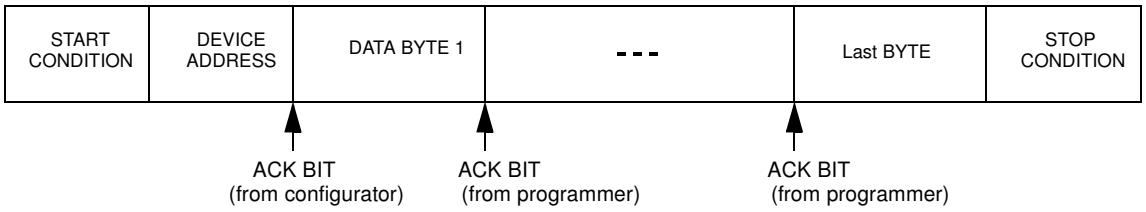
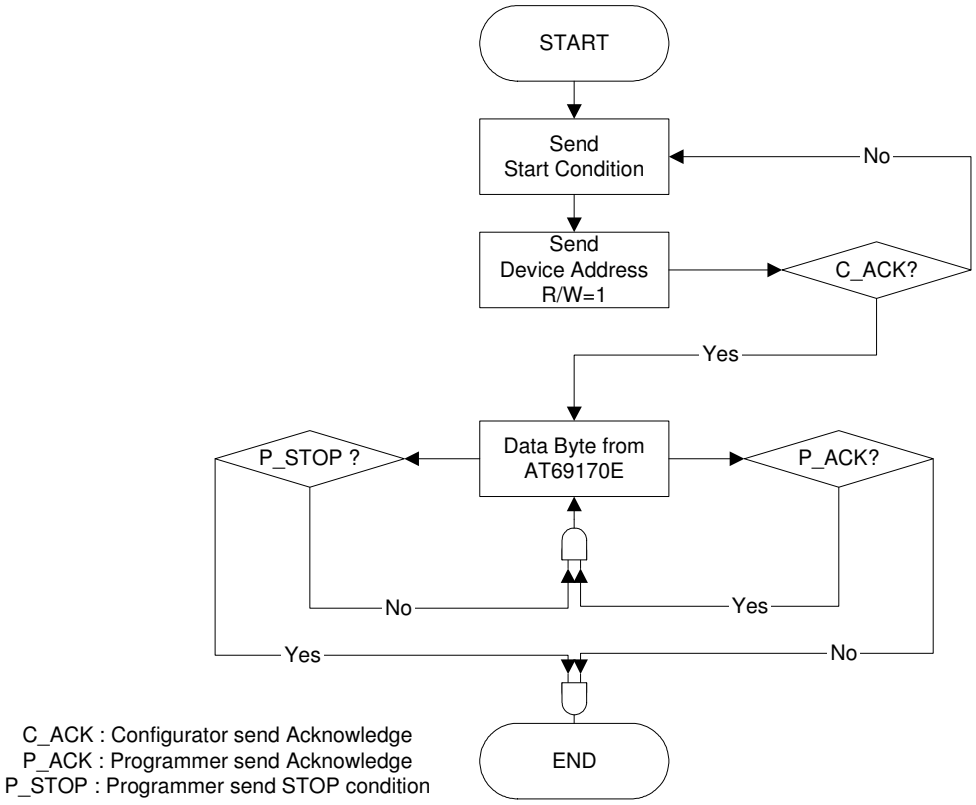


Figure 7-6. Read From Current Address Summary - TWI Current Read



7.2.2.2 Random read

The random read is the command used to read the memory starting from the address given in the command send by the programmer. The address provided by the programmer in the command must be aligned (A1=0 and A0=0).

After the programmer receives a Data Byte, it shall respond with either an Acknowledge Bit or a Stop condition. As long as the Configurator receives an Acknowledge Bit, it will continue to increment the Data Byte address and serially clock out sequential Data Bytes until the memory address limit is reached. The Sequential Read instruction is terminated when the programmer does not respond with an Acknowledge Bit, but instead generates a Stop Condition following the receipt of a Data Byte.

A Random Address Read instruction consists of

- a Start Condition
- a Device Address with R/W = 0
  - an Acknowledge Bit from the Configurator
- MS Byte of the EEPROM Address
  - an Acknowledge Bit from the Configurator
- (Next) Byte of the EEPROM Address
  - an Acknowledge Bit from the Configurator
- LS Byte of EEPROM Address double word aligned
  - an Acknowledge bit from the Configurator
- a Start Condition
- a Device Address with R/W = 1
  - an Acknowledge Bit from the Configurator
- Data Bytes
  - an Acknowledge bit from the Configurator
- a Data Byte from the Configurator
- a Stop Condition from the programmer.

Figure 7-7. Random Read frame

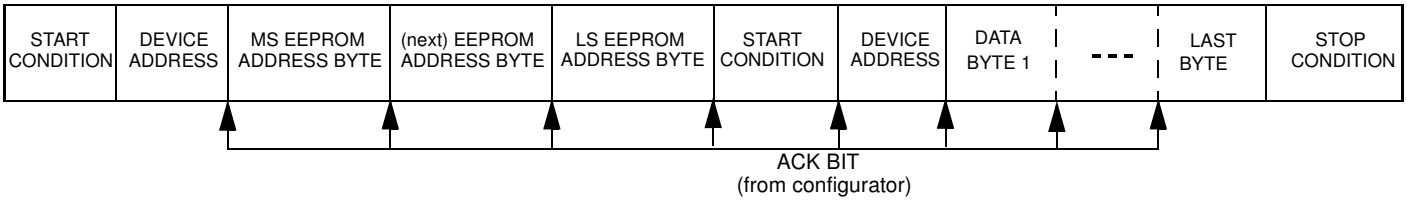
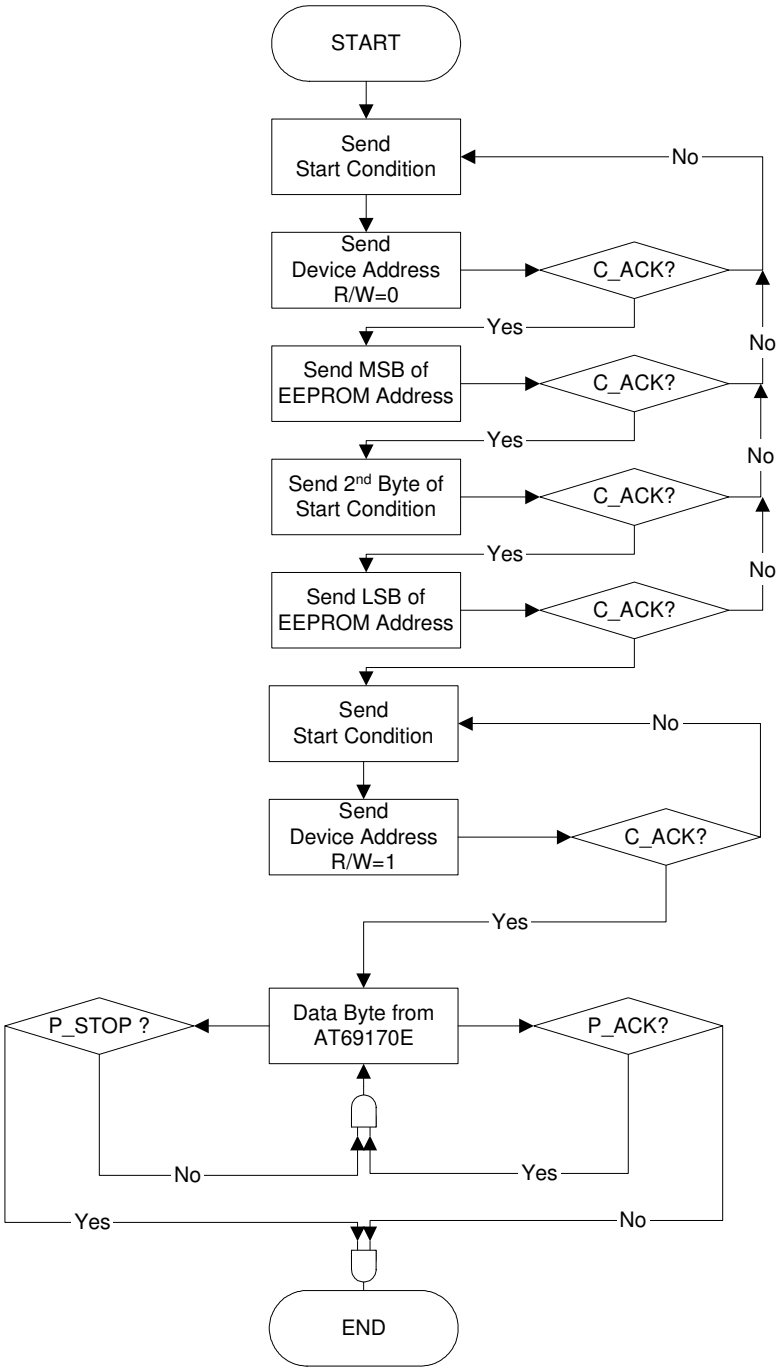


Figure 7-8. Random Read Summary - TWI Random Read



C_ACK : Configurator send Acknowledge
P_ACK : Programmer send Acknowledge
P_STOP : Programmer send STOP condition

7.3 Special Functions

The special functions available on the AT69170E are

- Data Protection
- RESET/OE Polarity
- Full Chip Erase

Access to the special functions is based on use of not aligned addresses (A1 and A0 different from 0) in the command sent by the programmer to the AT69170E.

7.3.1 Exit Special Function

In order to indicate to the memory that the special function is ended, the following sequence shall be performed at the end of each special function.

- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA
- write 0x00000000 at address 0x55555

7.3.2 Data Protection

The AT69170E has a “Write Protection” feature that disables data write capability to the memory. When the lock is activated, data loaded to the memory is not written in the memory and previous data is preserved.

There is no physical write protect pins for AT69170E. The write protection feature is determined by the state of an embedded fuses. Read and write of the protection is done through the 2-wire bus (Clock and Data) when the memory is in the programming mode ($\overline{\text{SER\_EN}}$ is driven Low).

7.3.2.1 Enabling Write Protection

To enable the write protection, the following sequence shall be applied:

- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA
- write 0x000000A0 at address 0x55555
-

7.3.2.2 Disbaling Write Protection

To disable the write protection, the following sequence shall be applied:

- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA
- write 0x00000080 at address 0x55555
- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA
- write 0x00000020 at address 0x55555

7.3.2.3 Reading Write Protection Configuration

To read the state of the write protection, the following sequence shall be applied:

- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA

- write 0x000000F2 at address 0x55555
- read data from address 0x000000001
  - If the most significant byte of the read data is “0x00” then memory can be written.
  - if the most significant byte of the read data is “0xFF” then memory is write protected.

7.3.3 RESET/OE Polarity

The AT69170E configurator allows the user to program the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This is required to allow the devices to properly configure various FPGA families. The default configuration is $\overline{RESET}$/OE:

- RESET active Low
- OE active High

After the RESET polarity has been modified, the Configurator must be powered down and back up again before attempting to verify functionality or use the newly programmed RESET function.

7.3.3.1 $\overline{RESET}$/OE

Configuration of the polarity as OE active high and RESET active low ($\overline{RESET}$/OE) is obtained applying the following sequence:

- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA
- write 0x000000FF at address 0x55555

7.3.3.2 RESET/$\overline{OE}$

To set the polarity option active high on RESET and active low on OE ($\overline{RESET}$/OE), the following sequence shall be applied:

- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA
- write 0x0000FFFF at address 0x55555

To read the state of the ($\overline{RESET}$/OE) Polarity, the following sequence shall be applied:

- write 0xAAAAAAAA at address 0x55555
- write 0x555555555 at address 0x2AAAA
- write 0x000000F2 at address 0x55555
- read data from address 0x000000001
  - If bit 23 of the read data is “0” then the polarity is *$\overline{RESET}$/OE*
  - If bit 23 of the read data is “1” then the polarity is *RESET/$\overline{OE}$*

7.3.4 Chip Erase

The AT69170E configurator allows to erase the entire AT69170E memory in one special command. In order to erase the chip, the following sequence shall be applied:

- write 0x555555 at address 0x2AAAA
- write 0xAAAAAA at address 0x55555
- write 0x555555 at address 0x000B0

8. FPGA Configuration mode

8.1 Configuration mode overview

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT69170E Serial Configuration EEPROM has been designed for compatibility with the Master Serial mode.

The control signals for the AT69170E ($\overline{CE}$, $\overline{RESET}$/OE and CLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the AT69170E without requiring an external intelligent controller.

The EEPROM $\overline{RESET}$/OE and $\overline{CE}$ pins control the tri-state buffer on the DATA output pin and enable the address counter. When $\overline{RESET}$/OE is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The $\overline{CE}$ pin also controls the output of the AT69170 series configurator. If $\overline{CE}$ is held High after the $\overline{RESET}$/OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When $\overline{OE}$ is subsequently driven Low, the counter and the DATA output pin are enabled. When $\overline{RESET}$/OE is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of $\overline{CE}$.

When the configurator has driven out all of its data and $\overline{CEO}$ is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the AT69170E address counter is automatically reset.

8.2 FPGA Configuration Operation

Connections between an FPGA device and the AT69170E Serial EEPROM are define as follow.

- $\overline{\text{SER\_EN}}$ pin is connected to VDD to allow configuration.
- $\overline{\text{RESET}}$/OE is connected to the FPGA configuration start indicator. It is used to put the memory in its default state and initiate the configuration.
- $\overline{\text{CE}}$ pins input is connected to the memory chip select of the FPGA.
- The FPGA master clock output drives the CLK input of the AT69170E series configurator.
- The DATA output of the AT69170E series configurator drives the input data port of the FPGA devices.
- The $\overline{\text{CEO}}$ output of the AT69170E drives the $\overline{\text{CE}}$ input of the next configurator in a cascaded chain of EEPROMs.

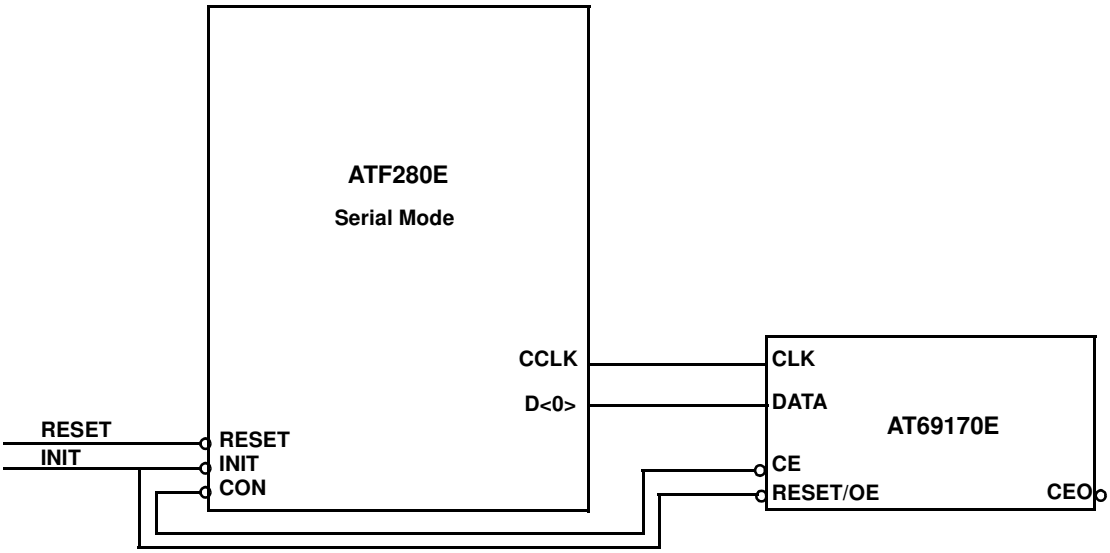
8.2.1 Typical Configuration with ATF280E FPGA

The ATF280E provides two signals, RESET and INIT, that can be used to initiate the configuration. One of this pin shall be connected to the AT69170E $\overline{\text{RESET}}$/OE pin. The ATF280E CON pin is tied to the Configurator chip enable (CE) to allow selection of the device.

The ATF280E FPGA drives the CCLK clock on the AT69170E so that the memory provides one data bit on D0 per CCLK rising edge. Each CCLK increments the AT69170E internal address counter, and serial data is presented to the FPGA.

Once the bitstream is complete, CON is released by the FPGA, indicating the device is completely ready for user operation.

Figure 8-1. AT280E FPGA configuration mode



8.2.2 Cascading Serial EEPROMs

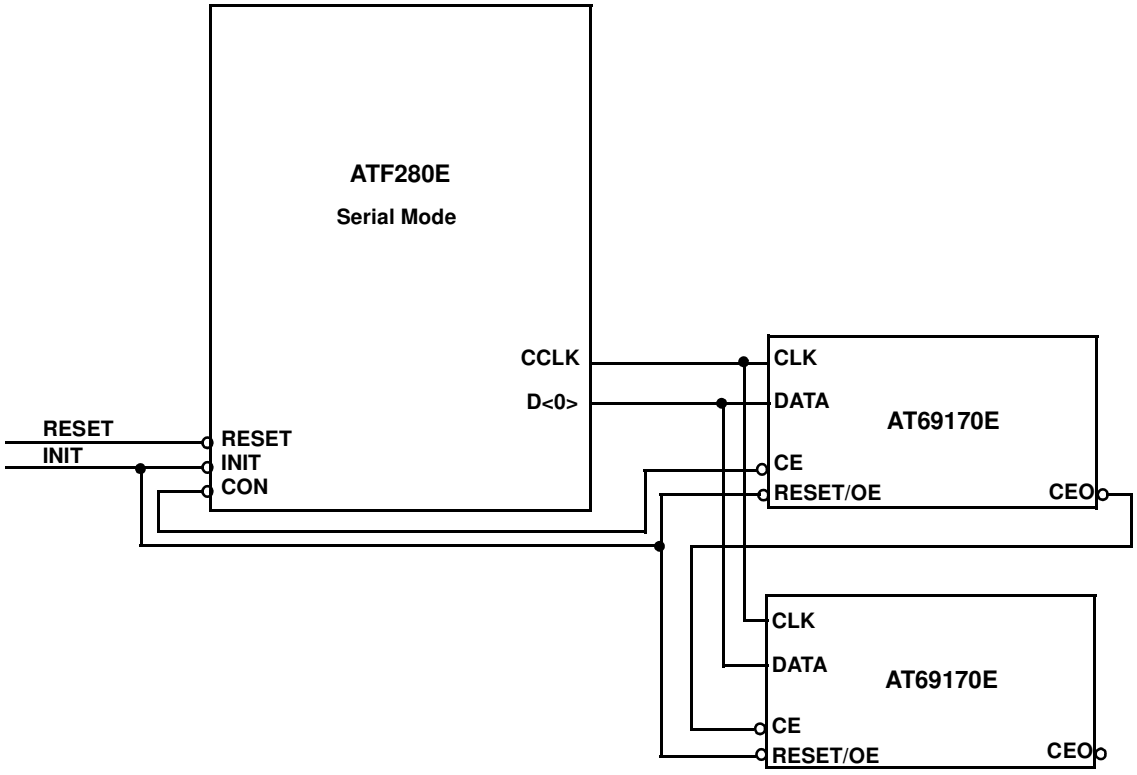
For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, it is possible to cascade AT69170E. This provides additional memory to fit FPGA bit-stream size.

Once the last bit from the first configurator is read, the memory asserts its $\overline{CEO}$ output Low and disables its DATA line driver. The second configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the $\overline{RESET}$/OE on each configurator is driven to its active (Low) level.

If the address counters does not requires to be reset upon completion, then the $\overline{RESET}$/OE input can be tied to its inactive (High) level.

Figure 8-2. AT69170E Cascade



9. Electrical Characteristics

9.1 Operating Conditions

	AT69170E
Operating Temperature (Case)	-55 to +125°C
Vcc Power Supply	3V to 3.6V

9.2 Absolute Maximum Ratings*

Supply Voltage (Vcc)..... -0.5V to 4.6V

Storage Temperature.....-65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground.....-0.5V to +4.6V

All Output Voltages
with Respect to Ground.....-0.5V to V_{DD} + 0.5V

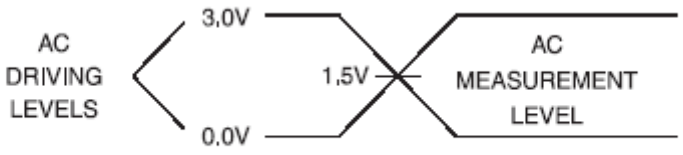
ESD.....> 2000V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.3 DC Characteristics

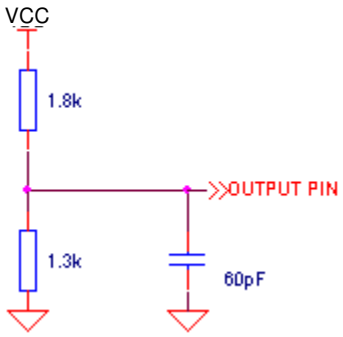
Symbol	Parameter	Condition	Min.	Max	Units
I_{IL} , I_{IH}	Low Level Input Current	V_{IN} = 0V to 3.6V Vcc max	-2	2	µA
I_{OZL} , I_{OZH}	Output Leakage Current	$V_{I/O}$ = 0V to 3.6V Vcc max	-2	2	µA
I_{CCSB1}	Standby Current CMOS	$\overline{CE}$ >= V_{DD} - 0.3V		1	mA
I_{CCSB}	Standby Current TTL	$\overline{CE}$ >= VIH		2	mA
I_{CCOPR}	Read Operating Current	f = 15 MHz; I_{OUT} = 0 mA		5	mA
I_{CCOPW}	Write Operating Current	f = 1/Twr		70	mA
V_{IL}	Input Low Voltage		GND - 0.3	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	Vcc - 0.4		V

9.3.1 Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

9.3.2 Output Test Load



9.3.3 Pin Capacitance (f=1MHz, 25°C)

Symbol	Typ	Max	Units	Conditions
C_{IN}	7	10	pF	V_{IN} = 0V
C_{OUT}	7	10	pF	V_{OUT} = 0V

Note: 1. This parameter is guaranteed but not tested.

9.4 AC Characteristics & Waveforms

9.4.1 TWI characteristics & waveform

Figure 9-1. AT69170E serial data transfer - TWI

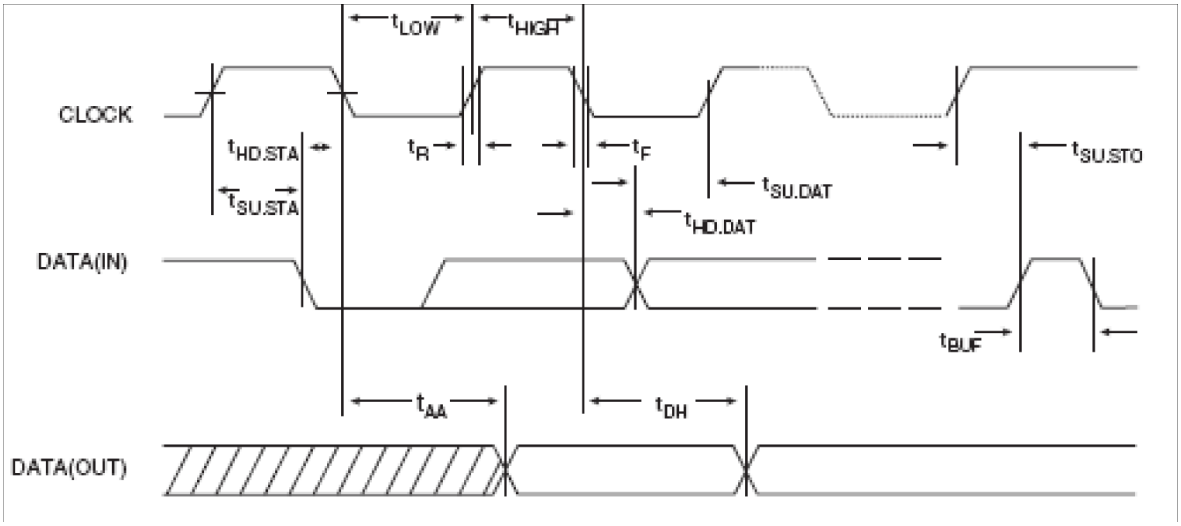


Table 9-1. AT69170E serial data transfer timings - TWI

Symbol	Description	AT69170E		Units
		Min	Max	
Fclock	Clock Frequency - CLOCK		400	KHz
Tclk	Clock Period	2.5		µs
Tlow	Clock Low Pulse Width	1.2		µs
Thigh	Clock High Pulse Width	1.2		µs
Taa	Clock Low to Data Out Valid		0.9	µs
Tbuf	Time the bus must be free before a new transmission can start	1.2		µs
Thd-sta	Start Hold Time from CLOCK	0.6		µs
Tsu-sta	Start Setup Time from CLOCK	0.6		µs
Thd-dat	Data In Hold Time	0.1		µs
Tsu-dat	Data In Setup Time	0.1		µs
Tr	Inputs Rise Time		0.3	µs
Tf	Inputs Fall Time		0.3	µs
Tsu-sto	Stop Setup Time	0.6		µs
Tdh	Data Out Hold Time	0		µs
Twr	Write Cycle Time		8000	Tlck

9.4.2 FPGA Configuration characteristics & waveform - Memory Dump

Figure 9-2. FPGA Configuration with AT69170E - Memory Dump

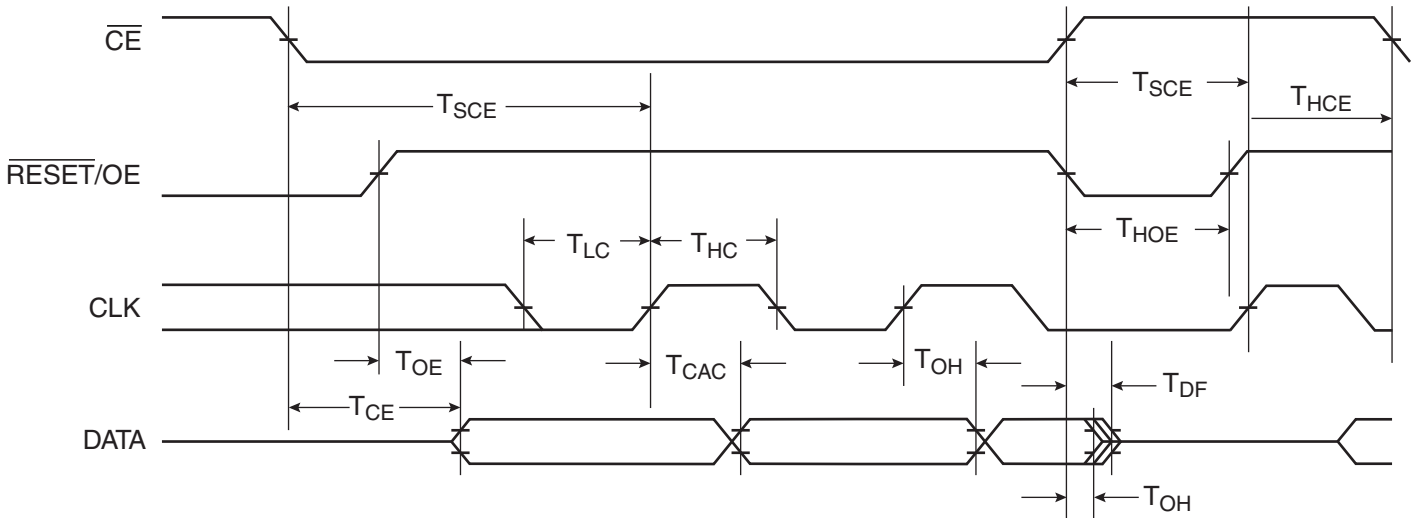


Figure 9-3. FPGA Configuration - AT69170E cascade mode

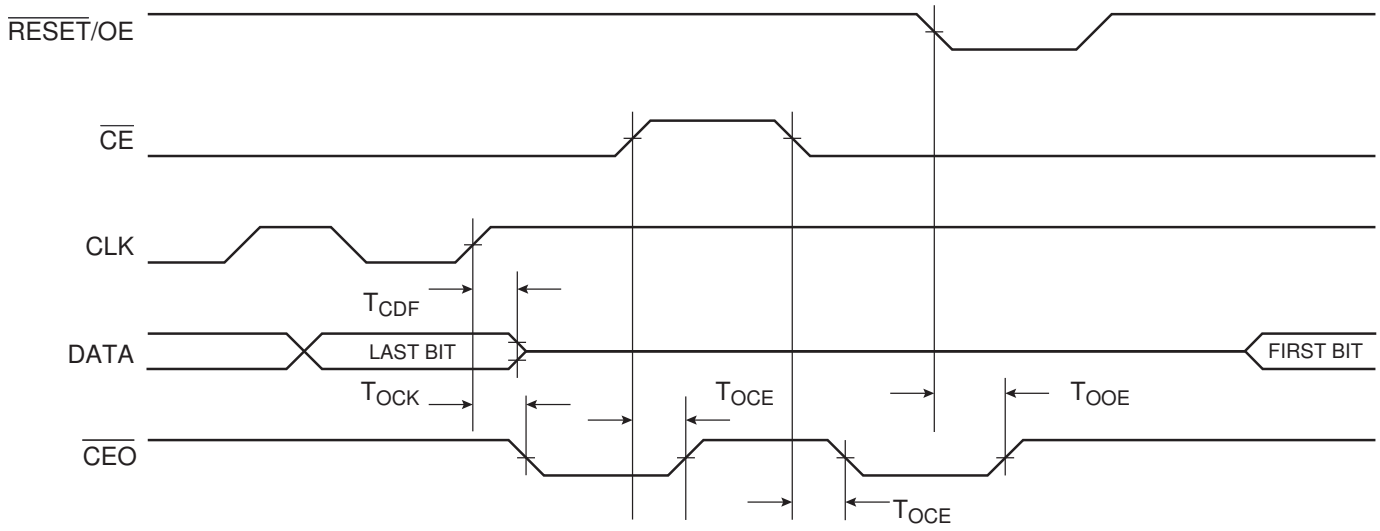
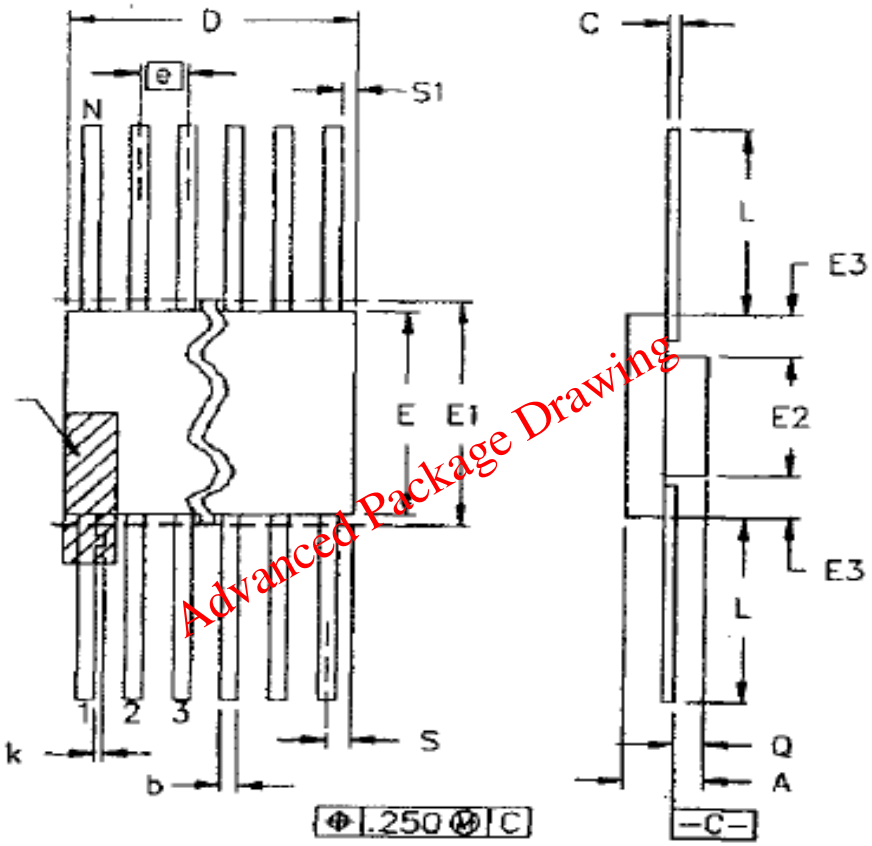


Table 9-2. FPGA Configuration timings

Symbol	Description	AT69170E		Units
		Min	Max	
T_{OE}	Data Output Delay from OE		35	ns
T_{CE}	Data Output Delay from $\overline{CE}$		40	ns
T_{CAC}	Data Output Delay from CLK		40	ns
T_{OH}	Data Hold from $\overline{CE}$, OE, or CLK	0		ns
T_{DF}	Data Float Output Delay from $\overline{CE}$ or OE		30	ns
Tcdf	Data Float Output Delay from CLK		30	ns

Symbol	Description	AT69170E		Units
		Min	Max	
Tock	$\overline{CEO}$ Output Delay from CLK		35	ns
Toce	$\overline{CEO}$ Output Delay from $\overline{CE}$		25	ns
Tooe	$\overline{CEO}$ Output Delay from $\overline{RESET}$/OE		25	ns
T_{LC}	CLK Low Time	20		ns
T_{HC}	CLK High Time	20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	20		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		ns
T_{HOE}	RESET pulse width that guarantees the counter is reset	60		ns
F_{MAX}	Maximum Clock Frequency		15	MHz

10. Packaging Information



11. Ordering Information

Ordering Code	Package	Flow
AT69170E-Dx-E	FP18 (Dx)	Engineering Samples
AT69170E-Dx-MQ		QMLQ
AT69170E-Dx-SV		QMLV
AT69170E-Dx-ESCC		ESCC

Note: 1. Contact factory for availability

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