DDR VDDQ and VTT Termination Voltage Regulator TJ3212

FEATURES

- Two linear regulators
  - Maximum 2A current from VDDQ
  - Source and sink up to 2A VTT current
- 1.7V to 2.8V adjustable VDDQ output voltage
- 0.85V to 1.4V VTT output voltage (tracking at 50% of VDDQ)
- Buffered VREF output
- 500mV typical VDDQ dropout voltage at 2A
- Excellent load and line regulation, low noise
- Meets JEDEC DDR-I and DDR-II memory power spec
- Linear regulator design requires no inductors and has low external component count
- Integrated power MOSFETs
- Dual purpose ADJ/Shutdown pin
- Enable VTT pin for sleep or suspend to RAM function
- Built-in over-current limit and thermal shutdown for VDDQ and VTT
- Fast transient response
- Low quiescent current

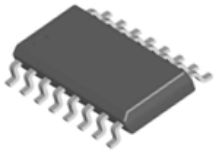
TDFN-8 PKG



SOP-8 PKG



SOP-16 PKG



ORDERING INFORMATION

Device	Package
TJ3212Q	TDFN-8
TJ3212DP	SOP-8
TJ3212D	SOP-16

APPLICATION

- DDR memory and active termination buses
- Desktop computers, servers
- Residential and enterprise gateways
- DSL modems
- Routers and switches
- DVD recorders, LCD TV and STB
- 3D AGP cards

DESCRIPSION

The TJ3212 is a dual-output low noise linear regulator designed to meet SSTL-2 and SSTL-3 specifications for DDR-SDRAM VDDQ supply and termination voltage VTT supply. With integrated power MOSFETs the TJ3212 can source up to 2A of VDDQ continuous current, and source or sink up to 2A VTT continuous current. The typical dropout voltage for VDDQ is 500mV at 2A load current.

The TJ3212 provides excellent full load regulation and fast response to transient load changes. It also has built-in over-current limits and thermal shutdown at 170°C.

The TJ3212 supports Suspend-To-RAM (STR) and ACPI compliance with Shutdown Mode which tri-states VTT to minimize quiescent system current.

The TJ3212 is available in a space saving TDFN-8 and SOIC-8 surface mount packages. Low thermal resistance allows them to withstand high power dissipation at 85°C ambient. The TJ3212 can operate over the industrial ambient temperature range of –40°C to 85°C.

Ordering Information

Package	Order No.	Description	Supplied As	Status
TDFN-8	TJ3212Q		Reel	Contact us
SOP-8	TJ3212DP		Reel	Contact us
SOP-16	TJ3212D		Tube	Contact us

Absolute Maximum Ratings

CHARACTERISTIC		SYMBOL	RATINGS	UNIT
V_{IN} to GND			[GND - 0.3] to +6.0	V
Pin Voltage	V_{DDQ}, V_{TT} to GND		[GND - 0.3] to +6.0	V
	ADJSD to GND		[GND - 0.3] to +6.0	V
Output Current	V_{DDQ} / V_{TT}, continuous (Note 1)		2.0 / ± 2.0	A
	V_{DDQ} / V_{TT}, peak		2.8 / ± 2.8	A
	V_{DDQ} Source + V_{TT} Source		3	A
Operating Ambient Temperature		T_A	–40 to 85	°C
Operating Junction Temperature		T_J	–40 to 170	°C
Storage Temperature		T_{STG}	–40 to 150	°C
Thermal Resistance (Note 2) TDFN-8 SOP-8 SOP-16		R_{JA}	 55 120 90	°C / W
Continuous Power Dissipation (Note 2) T_A = 25°C / 85°C TDFN-8 SOP-8 SOP-16		$PD_{(Cont.)}$	 2.6 / 1.5 1.2 / 0.7 1.6 / 0.9	W
Lead Temperature (Soldering, 10sec)		T_{SOL}	300	°C
ESD Protection (HBM)			2000	V

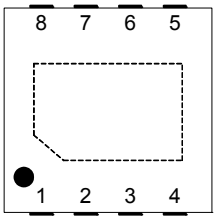
Operating Ratings

CHARACTERISTIC	SYMBOL	RATINGS	UNIT
Ambient Operating Temperature Range	T_{OPR}	–40 to 85	°C
V_{DDQ} Regulator			
Supply Voltage, V_{IN}		3.0 to 3.6	V
Load Current, Continuous		0 to 2	A
Load Current, Peak (1 sec)		2.5	A
C_{DDQ}		220	uF
V_{TT} Regulator			
Supply Voltage, V_{IN}		3.0 to 3.6	V
Load Current, Continuous		0 to ±2.0	A
Load Current, Peak (1 sec)		±2.50	A
C_{TT}		220	uF

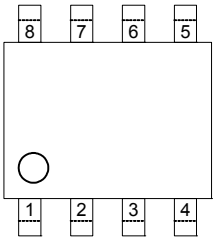
Operating Ratings (Continued)

CHARACTERISTIC	SYMBOL	RATINGS	UNIT
V_{IN} Supply Voltage Range		3.0 to 3.6	V
V_{DDQ} Source + V_{TT} Source			
Load Current, Continuous		2.5	A
Load Current, Peak (1 sec)		3.5	A
Junction Operating Temperature Range	T_{JOPR}	–40 to +150	°C

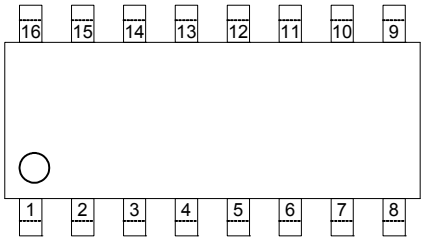
PIN CONFIGURATION



TDFN-8



SOP-8

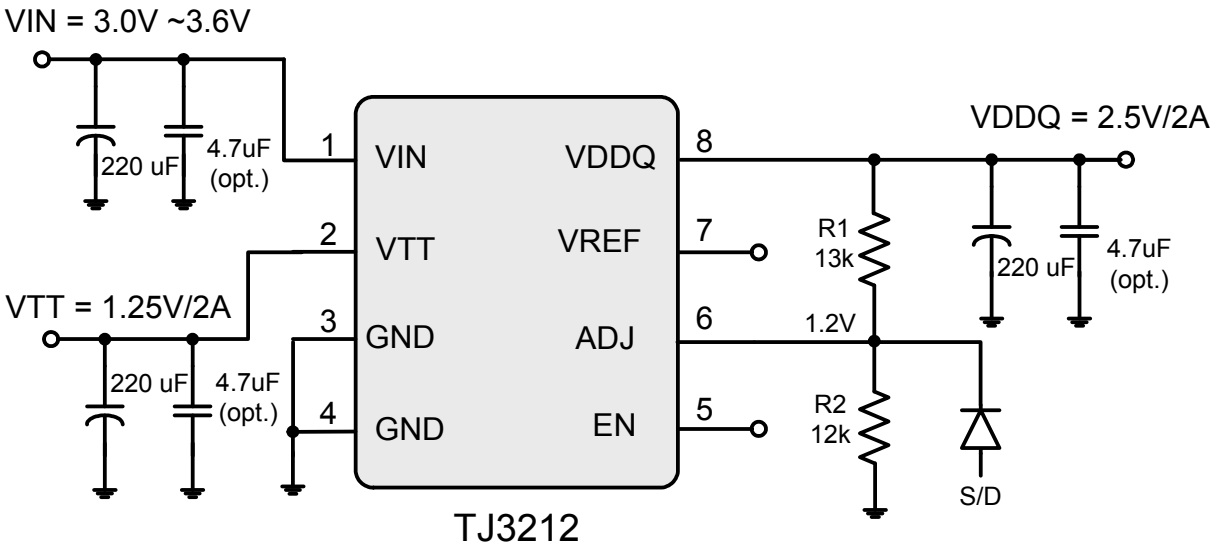


SOP-16

PIN DESCRIPTION

Pin No.	TDFN-8 / SOP-8 PKG		SOP-16 PKG	
	Name	Function	Name	Function
1	VIN	Input Supply	VIN	Input Supply
2	VTT	Output Voltage for Connection to Termination Resistors	VIN	Input Supply
3	GND	Ground	VIN	Input Supply
4	GND	Ground	N.C	Not internally connected.
5	EN	Chip Enable	N.C	Not internally connected.
6	ADJ	VDDQ Adjust	VTT	Output Voltage for Connection to Termination Resistors
7	VREF	Reference Voltage	GND	Ground
8	VDDQ	VDDQ Regulator Output Voltage	GND	Ground
9	-	-	EN	Chip Enable
10	-	-	SENSE	Feedback for Regulating VTT
11	-	-	VREF	Reference Voltage
12	-	-	VDDQ	VDDQ Regulator Output Voltage
13	-	-	VDDQ	VDDQ Regulator Output Voltage
14	-	-	ADJ	VDDQ Adjust
15	-	-	GND	Ground
16	-	-	VIN	Input Supply

TYPICAL APPLICATION



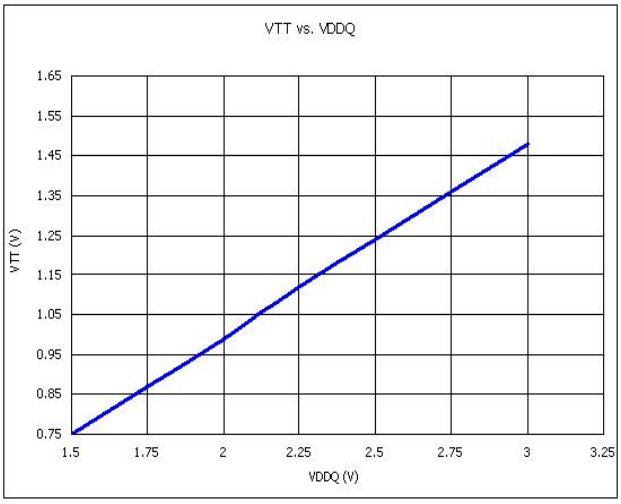
ELECTRICAL CHARACTERISTICS

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{IN}		3.0		3.6	V
Quiescent Current	I_Q	I_{DDQ} = 0, I_{TT} =0		2		mA
ADJSD Voltage	V_{ADJSD}	(3)	1.225	1.250	1.275	V
Shutdown Current	I_{SHDN}	V_{ADJSD} = 3.3V (shutdown)		0.1		mA
ADJSD Logic High	SHDN_H	(2)	2.7			V
ADJSD Logic Low	SHDN_L	(3)			1.5	V
Under-voltage Lockout	UVLO	Hysteresis = 100mV (3)	2.40	2.70	2.90	V
Thermal SHDN Threshold	T_{OVER}	(3)	150	170		°C
Thermal SHDN Hysteresis	T_{HYS}			50		°C
V_{DDQ}, V_{TT} TEMPCO	TEMPCO	I_{OUT} = 1A (3)		100		ppm/°C
VDDQ Regulator						
VDDQ Output Voltage	$V_{DDQ\ EDF}$	I_{DDQ} = 100mA	2.450	2.500	2.550	V
VDDQ Load Regulation	$V_{DDQ\ LOAD}$	10mA ≤ I_{DDQ} ≤ 2A (4)		10	25	mV
VDDQ Line Regulator	$V_{DDQ\ LINE}$	3.0V ≤ V_{IN} ≤ 3.6V, I_{DDQ} = 0.1A		5	25	mV
VDDQ Dropout Voltage	V_{DROP}	I_{DDQ} = 2A (5)		500		mV
ADJSD Bias Current	I_{ADJ}	(3)		0.8	3	uA
VDDQ Current Limit	$I_{DDQ\ LIM}$		2.0	2.5		A
VTT Regulator						
VTT Output Voltage	$V_{TT\ DEF}$	I_{TT} = 100mA	1.225	1.250	1.275	V
VTT Load Regulation	$V_{TT\ LOAD}$	Source, 10mA ≤ I_{TT} ≤ 2A (4) Sink, -2A ≤ I_{TT} ≤ 10mA (4)	 -30	10 -10	30	mV mV
VTT Line Regulator	$V_{TT\ LINE}$	3.0V ≤ V_{IN} ≤ 3.6V, I_{TT} = 0.1A		5	15	mV
ITT Current Limit	$I_{TT\ LIM}$	Source / Sink (4)	± 2.0	± 2.5		A
VTT Shutdown Leakage Current	$I_{VTT\ OFF}$	V_{EN_VTT} = 0.4V (shutdown)			10	uA
Reference Voltage	V_{REF}	C_{REF} = 0.1uF, I_{REF} = 100uA	1.225	1.250	1.275	V

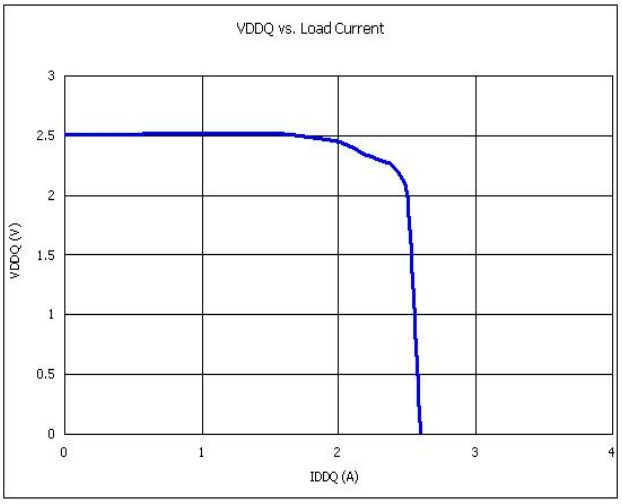
Note 1. VIN = 3.3V, VDDQ = 2.50V, VTT = 1.25V (default values), CDDQ=CTT=47 F, TA = 25°C unless otherwise specified.
Note 2. The ADJSD Logic High value is normally satisfied for full input voltage range by using a low leakage current (below 1 A). Schottky diode at ADJSD control pin.
Note 3. Guaranteed by design.
Note 4. Load and line regulation are measured at constant junction temperature by using pulse testing with a low duty cycle. For high current tests, correlation method can be used. Changes in output voltage due to heating effects must be taken into account separately. Load and line regulation values are guaranteed by design up to the maximum power dissipation.
Note 5. Dropout voltage is the input to output voltage differential at which output voltage has dropped 100mV from the nominal value obtained at 3.3V input. It depends on load current and junction temperature. Guaranteed by design.

TYPICAL OPERATING CHARACTERISTICS

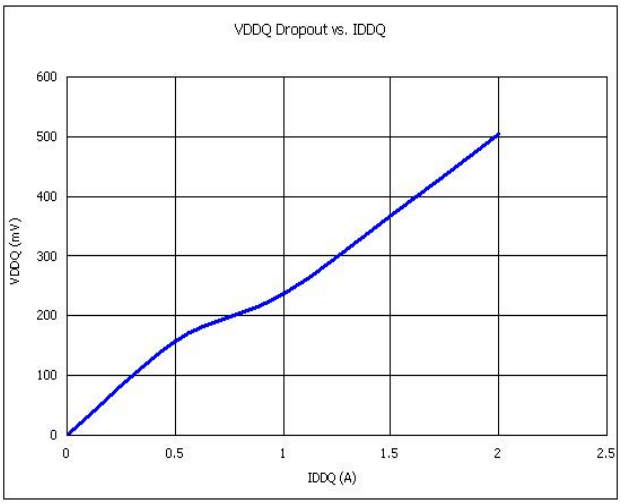
VTT vs. VDDQ



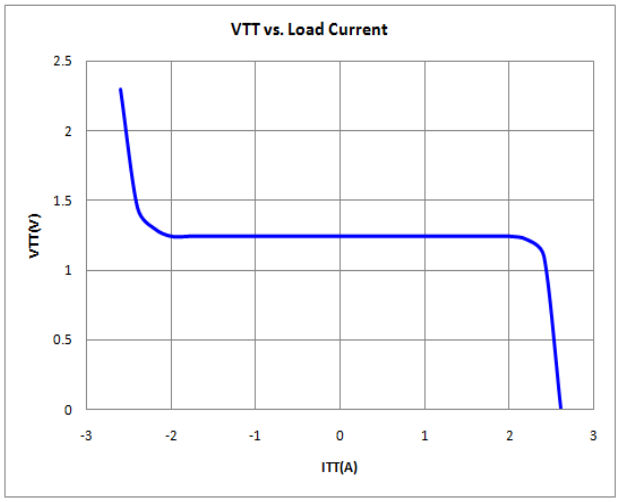
VDDQ vs. IDDQ



VDDQ Dropout vs. IDDQ

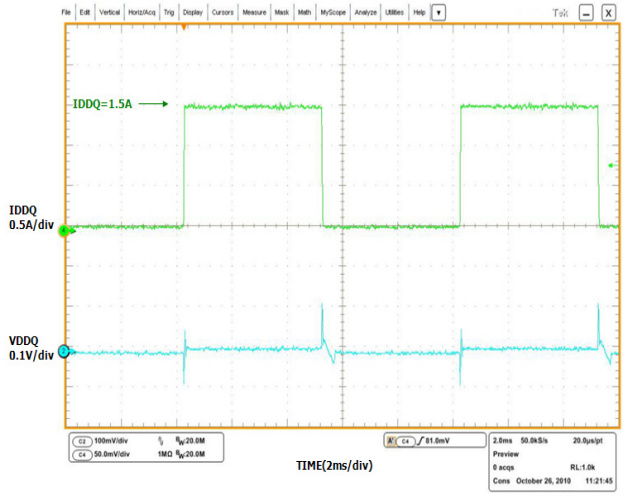


VTT vs. Load Current

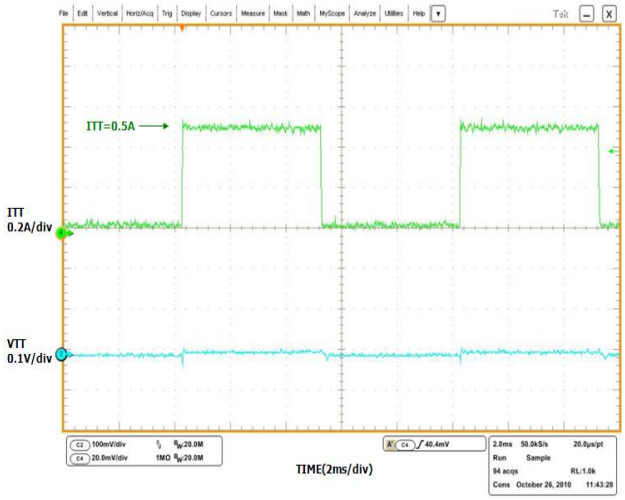


TYPICAL OPERATING CHARACTERISTICS (Continued)

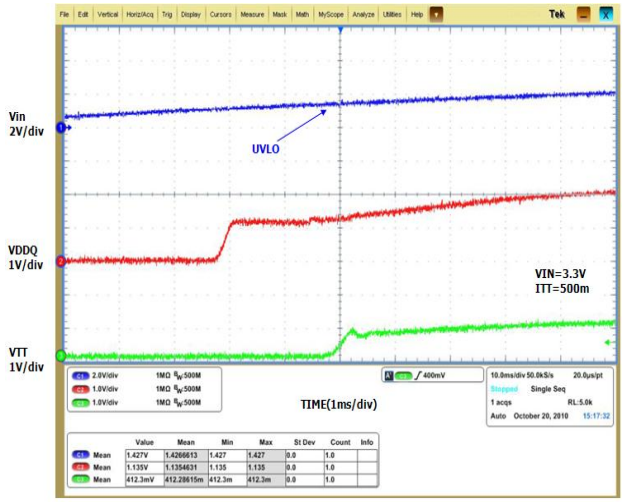
VDDQ Transient Response



VTT Transient Response



Softstart into full load



APPLICATION INFORMATION

Powering DDR Memory

Double-Data-Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAMs transmit data at both the rising and falling edges of the memory bus clock.

DDR's use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power-supply rejection, while reducing power dissipation. To achieve this performance improvement, DDR requires more complex power management architecture than previous RAM technology.

Unlike the conventional DRAM technology, DDR SDRAM uses differential inputs and a reference voltage for all interface signals. This increases the data bus bandwidth, and lowers the system power consumption. Power consumption is reduced by lower operating voltage, a lower signal voltage swing associated with Stub Series Terminated Logic (SSTL_2), and by the use of a termination voltage, V_{TT}. SSTL_2 is an industry standard defined in JEDEC document JESD8-9. SSTL_2 maintains high-speed data bus signal integrity by reducing transmission reflections. JEDEC further defines the DDR SDRAM specification in JESD79C.

DDR memory requires three tightly regulated voltages: V_{DDQ}, V_{TT}, and V_{REF} (see Figure 1). In a typical SSTL_2 receiver, the higher current V_{DDQ} supply voltage is normally 2.5V with a tolerance of ±200mV. The active bus termination voltage, V_{TT}, is half of V_{DDQ}. V_{REF} is a reference voltage that tracks half of V_{DDQ} ±1%, and is compared with the V_{TT} terminated signal at the receiver. V_{TT} must be within ± 40mV of V_{REF}.

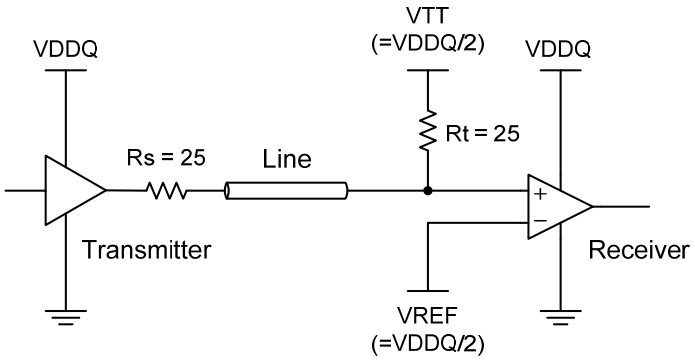


Figure 1. Typical DDR terminations, Class II

The V_{TT} power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2mA to achieve the 405mV minimum over V_{TT} needed at the receiver:

$$I_{termination} = \frac{405mV}{R_t(25\Omega)} = 16.2mA$$

A typical 64Mbyte SSTL-2 memory system, with 128 terminated lines, has a worst-case maximum V_{TT} supply current up to ± 2.07A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ± 200mA.

The V_{DDQ} power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 0.5A to 1A, with peaks up to 2A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for V_{TT} to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

TJ3212 Regulator

The TJ3212 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single package. V_{DDQ} regulator can supply up to 2A current, and the two quadrant V_{TT} termination regulator has current sink and source capability to ± 2A. The V_{DDQ} linear regulator uses a PMOS pass element for a very low dropout voltage, typically 500mV at a 2A output. The output voltage of V_{DDQ} can be set by an external voltage divider. The use of regulators for both the upper and lower side of the V_{DDQ} output allows a fast transient response to any change of the load, from high current to low current or inversely. The second output, V_{TT}, is regulated at V_{DDQ} / 2 by an internal resistor divider. Same as V_{DDQ}, V_{TT} has the same fast transient response to load change in both directions. The V_{TT} regulator can source, as well as sink, up to 2A current. The TJ3212 is designed for optimal operation from a nominal 3.3V DC bus, but can work with V_{IN} up to 5V. When operating at higher V_{IN} voltages, attention must be given to the increased package power dissipation and proportionally increased heat generation. Limited by the package thermal resistance, the maximum output current of the device at higher V_{IN} cannot exceed the limit imposed by the maximum power dissipation value.
V_{REF} is typically routed to inputs with high impedance, such as a comparator, with little current draw. An adequate V_{REF} can be created with a simple voltage divider of precision, matched resistors from V_{DDQ} to ground. A small ceramic bypass capacitor can also be added for improved noise performance.

Input and Output Capacitors

The TJ3212 requires that at least a 220uF electrolytic capacitor be located near the V_{IN} pin for stability and to maintain the input bus voltage during load transients. An additional 4.7uF ceramic capacitor between the V_{IN} and GND, located as close as possible to those pins, is recommended to ensure stability.
At a minimum, a 220uF electrolytic capacitor is recommended for the V_{DDQ} output. An additional 4.7uF ceramic capacitor between the V_{DDQ} and GND, located very close to those pins, is recommended.
At a minimum, a 220uF electrolytic capacitor is recommended for the V_{TT} output. This capacitor should have low ESR to achieve best output transient response. SP or OSCON capacitors provide low ESR at high frequency, and thus are a good choice. In addition, place a 4.7uF ceramic capacitor between the V_{TT} pin and GND, located very close to those pins. The total ESR must be low enough to keep the transient within the V_{TT} window of 40mV during the transition for source to sink. An average current step of ± 0.5A requires:

$$ESR < \frac{40mV}{1A} = 40m\Omega$$

Both outputs will remain stable and in regulation even during light or no load conditions. The general recommendation for circuit stability for the TJ3212 requires the following:

1) $C_{IN} = C_{DDQ} = C_{TT}$ = 220uF / 4.7uF for the full temperature range of –40 to +85°C.
2) $C_{IN} = C_{DDQ} = C_{TT}$ = 100uF / 2.2uF for the temperature range of –25 to +85°C.

Adjusting VDDQ Output Voltage

The TJ3212 internal bandgap reference is set at 1.25V. The V_{DDQ} voltage is adjustable by using a resistor divider, R1 and R2:

$$V_{DDQ} = V_{ADJ} \times \frac{R1 + R2}{R2}$$

where V_{ADJ} = 1.25V. The recommended divider value is R1 = R2 = 10k for DDR-1 application, and R1 = 4.42k, R2 = 10k for DDR-2 application (V_{DDQ} = 1.8V, V_{TT} = 0.9V).

Shutdown

ADJSD also serves as a shutdown pin. When this is pulled high (SHDN_H), both the V_{DDQ} and the V_{TT} outputs tri-state and could sink/source less than 10uA. During shutdown, the quiescent current is reduced to less than 0.5mA, independent of output load.

It is recommended that a low leakage Schottky diode be placed between the ADJSD Pin and an external shutdown signal to prevent interference with the ADJ pin's normal operation. When the diode anode is pulled low, or left open, the TJ3212 is again enabled.

For Shutdown operation, observe the following:

V_{DDQ}	Under ADJSD shutdown condition, V_{DDQ} should go to tri-state.
	Under EN_VTT shutdown condition, V_{DDQ} should keep state (2.5V).
V_{TT}	Under ADJSD or EN_VTT shutdown condition, V_{TT} should go to tri-state and should sink or source less than 10uA.
V_{REF}	Under ADJSD shutdown condition, V_{REF} should go to zero.
	Under EN_VTT shutdown condition, V_{REF} should keep state (1.2V or VDDQ/2).

Current Limit and Over-temperature Protection

The TJ3212 features internal current limiting with thermal protection. During normal operation, V_{DDQ} limits the output current to approximately 2A and V_{TT} limits the output current to approximately ± 2A. When V_{TT} is current limiting into a hard short circuit, the output current folds back to a lower level (~1A) until the over-current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the junction temperature of the device exceeds 170°C(typical), the thermal protection circuitry triggers and tri-states both V_{DDQ} and V_{TT} outputs. Once the junction temperature has cooled to below about 120°C the TJ3212 returns to normal operation.

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (PD) primarily consists of two paths in the series. The first path is the junction to the case (θ_{JC}) which is defined by the package style and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any condition can be estimated by the following thermal equation:

$$T_J = T_A + P_D \times (\theta_{JC}) + P_D \times (\theta_{CA})$$
$$= T_A + P_D \times (\theta_{CA})$$