SCOPE: CMOS, TTL-COMPATIBLE ANALOG MULTIPLEXER

Device Type	Generic Number
01	DG528A(x)/883B
02	DG529A(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
K	GDIP1-T18 or CDIP2-T18	18 LEAD CERDIP	J18
Z	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V^-

V^+ 44V
GND 25V
Digital Inputs, V_S, V_D .....(-V) -2V to (V^+)+2V
or 20mA, whichever occurs first
Current, Any terminal except S or D 30mA
Continuous Current, S or D 20mA
Peak Current (Pulsed at 1ms, 10% duty cycle max) 50mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation 1/..... T_A=+70°C
18 lead CERDIP(derate 10.5mW/°C above +70°C) 842mW
20 lead LCC (derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 18 lead CERDIP..... 45°C/W
Case Outline 20 lead LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 18 lead CERDIP..... 95°C/W
Case Outline 20 lead LCC ..... 110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T_A) ..... -55°C to +125°C

NOTE 1: All leads are soldered or wolded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C __ V+=+15V, V-=-15V,___ RS=2.4V, GND=WR=0V, V_{AH}=2.4V, V_{AL}=0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SWITCH		NOTE 2					
Analog-Signal Range	V_{ANALOG}	V_S=±15V NOTE 3	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S =-200µA, V_D=±10V, V_{AL}=0.8V, V_{AH}=2.4V, Sequence each switch ON	1,3 2	All		400 500	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_S =10mA, V_D=-10V, V_{EN}=0V	1 2	All	-1 -50	1 50	nA
Source OFF Leakage Current	$I_{S(OFF)}$	V_S =-10mA, V_D=10V, V_{EN}=0V	1 2	All	-1 -50	1 50	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S =±10mA, V_D=±10V, V_{EN}=0V	1 2 2	All 01 02	-10 -200 -100	10 200 -100	nA
Drain ON Leakage Current	$I_{D(ON)}$	V_D=V_S=±10V, V_{AL}=0.8V, V_{AH}=2.4V, V_{EN}=2.4V, NOTE 3, 4	1 2 2	All 01 02	-10 -200 -100	10 200 100	nA
INPUT							
Input Current/Voltage High	I_{AH}	V_{IN}= 2.4V V_{IN}=15V	1,3 2 1,3 2	All All	-1 -30 -1	1 1 30	µA
Input Current/Voltage Low	I_{AL}	V_{EN}=0V, 2.4V; V_A=0V, V_A=WR=RS=0V	1,3 2	All	-1 -30	1	µA
SUPPLY							
Positive Supply Current	I+	V_{EN}=V_A=0V	1	All		2.5	mA
Negative Supply Current	I-	V_{EN}=V_A=0V	1	All	-1.5		mA
DYNAMIC							
Transition Time	t_{RANS}	Figure 1	9 10,11	All		1.0 1.5	µs
Enable and Write Turn ON Time	t_{ON} __ (EN,WR)	See Figures 2 and 3	9 10,11	All		1.5 2.0	µs
Enable and Write Turn OFF Time	t_{OFF} __ (EN, RS)	See Figures 2 and 3	9 10,11	All		1.5 2.0	µs

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V+=+15V, V-=-15V, RS=2.4V, GND=WR=0V, V_{AH}=2.4V, V_{AL}=0.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
MINIMUM INPUT TIMING							
$\overline{WR}$ Pulse Width	t_{WW}	Figure 7	9,10,11	All	300		ns
AX, EN Data valid to $\overline{WR}$	t_{DW}	(Stabilization Time) Figure 7	9,10,11	All	180		ns
AX, EN Data valid after $\overline{WR}$	t_{WD}	(Hold Time) Figure 7	9,10,11	All	30		ns
$\overline{RS}$ Pulse Width	$t_{\overline{RS}}$	Figure 7; V_S=5V NOTE 5	9,10,11	All	500		ns

NOTE 2: Guaranteed by design.
NOTE 3: Sequence each switch on.
NOTE 4: ID(ON) is leakage drom driver into on switch
NOTE 5: Reset pulse period must be at least 50µs during and after power-on.

TRUTH TABLE

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	DG528A ON SWITCH
X	X	X	X	↑	1	*
X	X	X	X	X	0	**
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8
	A1	**A0**	**EN**	$\overline{WR}$	$\overline{RS}$	**DG529A ON SWITCH**
	X	X	X	↑	1	*
	X	X	X	0	1	**
	X	X	0	0	1	None
	0	0	1	0	1	1
	0	1	1	0	1	2
	1	0	1	0	1	3
	1	1	1	0	1	4

TERMINAL CONNECTION

TERMINAL NUMBER	01 DG528A	01 DG528A	02 DG529A	02 DG529A
	J18	L20	J18	L20
1	$\overline{WR}$	NC	$\overline{WR}$	NC
2	A0	$\overline{WR}$	A0	$\overline{WR}$
3	EN	A0	EN	A0
4	V-	EN	V-	EN
5	S1	VSS	S1A	VSS
6	S2	S1	S2A	S1A
7	S3	S2	S3A	S2A
8	S4	S3	S4A	S3A
9	D	S4	DA	S4A
10	S8	D	DB	DA
11	S7	NC	S4B	NC
12	S6	S8	S3B	DB
13	S5	S7	S2B	S4B
14	V+	S6	S1B	S3B
15	GND	S5	V+	S2B
16	A2	VDD	GND	S1B
17	A1	GND	A1	VDD
18	$\overline{RS}$	A2	$\overline{RS}$	GND
19		A1		A1
20		$\overline{RS}$		$\overline{RS}$

NOTE: Logic "1": V_{AH}≥2.4V * LATCHING: Maintains previous switch conditions
Logic "0": V_{AL}≥0.8V **RESET: None (latches cleared)

ORDERING INFORMATION:	
DG528AK/883B 18 CDIP	DG529AK/883B 18 CDIP
DG528AZ/883B 20 LCC	DG529AZ/883B 20 LCC

FIGURE 1: TRANSITION TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 3: Enable t_{ON}/t_{OFF} Test Time Circuit: See Commercial Data Sheet
FIGURE 4: Write Turn-On Time Test Circuit: See Commerical Data Sheet
FIGURE 5: Write Turn-Off Time Test Circuit: See Commerical Data Sheet
FIGURE 7: Typical Timing Diagrams: See Commerical Data Sheet

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:
1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:
1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:
a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested shall be guaranteed to the limits of Table 1.