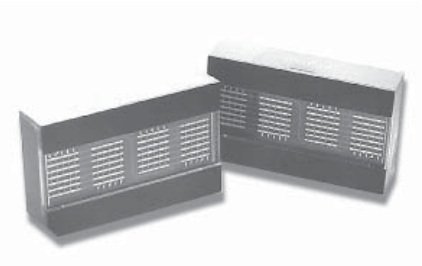
HDLx-3416 Series

Four Character 6.9 mm (0.27 inch)
Smart 5 x 7 Alphanumeric Displays

Data Sheet



Description

These are 5 x 7 dot matrix displays with four 0.27" tall characters, driven by an on-board CMOS IC. The IC stores and decodes 7 bit ASCII data and displays it with an easy to read 5x7 font. Multi-plexing circuitry and drivers are included in the IC to allow the display to interface simply with bus-based microprocessor systems.

The address and data inputs of the display can be directly connected to the microprocessor address and data buses.

These displays are related to the HDLX-2416 family, and thus share the same enhancements over the HPDL-2416 segmented displays. These features include support for the full 128 character US ASCII character set, 8 level dimming control, external hardware dimming capability, and digit blanking.

An extended function disable exists for those designers who desire compatibility with competitive displays. This function disables the dimming and digit blanking controls.

Features

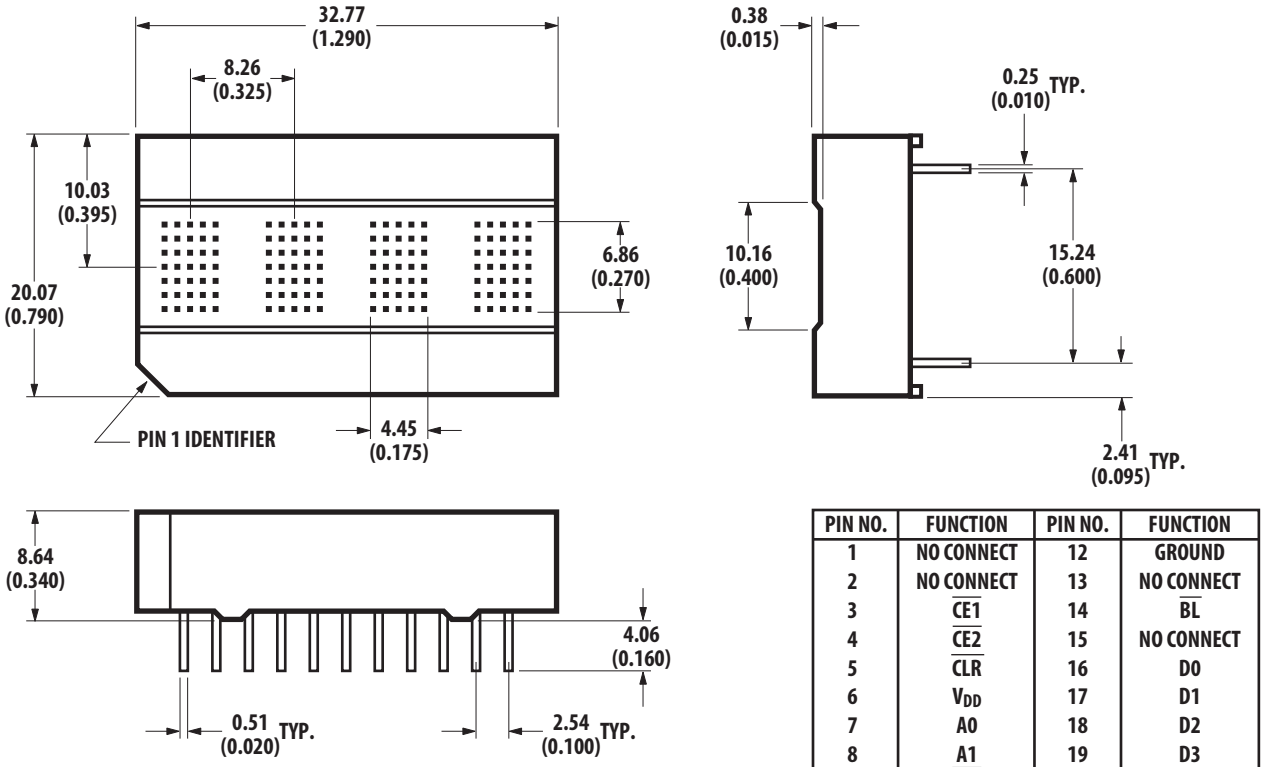
- Smart alphanumeric display
  Built-in RAM, ASCII decoder, and LED drive circuitry
- Software controlled dimming and blanking
- 128 ASCII character set
- End-stackable
- Categorized for luminous intensity
  – Yellow and Green categories for color
  – Use of like categories yields a uniform display
- Wide operating temperature range -40°C to +85°C
- Wave solderable
- Wide viewing angle (50° typical)

Devices:

High Efficiency Red	Orange	Yellow	Green
HDLO-3416	HDLA-3416	HDLY-3416	HDLG-3416

ESD WARNING: *Standard CMOS handling precautions should be observed to avoid static discharge.*

Package Dimensions



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	NO CONNECT	12	GROUND
2	NO CONNECT	13	NO CONNECT
3	$\overline{CE1}$	14	$\overline{BL}$
4	$\overline{CE2}$	15	NO CONNECT
5	$\overline{CLR}$	16	D0
6	V_{DD}	17	D1
7	A0	18	D2
8	A1	19	D3
9	$\overline{WR}$	20	D4
10	$\overline{CU}$	21	D5
11	CUE	22	D6

Notes:
1. Unless otherwise specified, the tolerance on all dimensions is ± 0.254 mm (0.010).
2. All dimensions are in millimeters (inches).

Absolute Maximum Ratings

Supply Voltage, V_{DD} to Ground[1]	-0.5 V to 7.0 V
Input Voltage, Any Pin to Ground	-0.5 V to V_{DD} + 0.5 V
Free Air Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_S	-40°C to +85°C
CMOS IC Junction Temperature, T_J (IC)	+150°C
Relative Humidity (non-condensing) at 65°C	85%
Soldering Temperature [1.59 mm (0.063 in.) Below Body]	
Solder Dipping	260°C for 5 secs
Wave Soldering	250°C for 3 secs
ESD Protection, R = 1.5 kΩ, C = 100 pF	V_Z = 1 kV (each pin)

Note:
1. Maximum Voltage is with no LEDs illuminated.

Character Set

ASCII CODE			D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0																
0	0	1	1																
0	1	0	2															
0	1	1	3																
1	0	0	4																
1	0	1	5																
1	1	0	6																
1	1	1	7																

NOTES: 1 = HIGH LEVEL
0 = LOW LEVEL

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	4.5	5.0	5.5	V

Electrical/Optical Characteristics over Operating Temperature Range

4.5 < V_{DD} < 5.5 V (unless otherwise specified)

All Devices

			25°C[1]				
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Max.**	**Units**	**Test Conditions**
I_{DD} Blank	I_{DD} (blnk)		1.0		4.0	mA	All Digits Blanked
Input Current	I_I	-40			10	µA	V_{IN} = 0 V to V_{DD} V_{DD} = 5.0 V
Input Voltage High	V_{IH}	2.0			V_{DD}	V	
Input Voltage Low	V_{IL}	GND			0.8	V	
I_{DD} 4 Digits 20 Dots/ Character[2,3]	I_{DD} (#)		110	130	160	mA	"#" ON in All Four Locations
I_{DD} Cursor All Dots ON @ 50%	I_{DD} (CU)		92	110	135	mA	Cursor ON in All Four Locations

Notes:
1. V_{DD} = 5.0 V
2. Average I_{DD} measured at full brightness. Peak I_{DD} = 28/15 x Average I_{DD} (#).
3. I_{DD} (#) max. = 130 mA, 150°C IC junction temperature and V_{DD} = 5.5 V.

Optical Characteristics at 25°C[1]

V_{DD} = 5.0 V at Full Brightness

High Efficiency Red HDLO-3416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per Digit, Character Average	I_V	1.2	3.5	mcd	"*" Illuminated in All Four Digits. 19 Dots ON per Digit.
Peak Wavelength	λ_{PEAK}		635	nm	
Dominant Wavelength[2]	λ_D		626	nm	

Orange HDLA-3416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per Digit, Character Average	I_V	1.2	3.5	mcd	"*" Illuminated in All Four Digits 19 Dots ON per Digit.
Peak Wavelength	λ_{PEAK}		600	nm	
Dominant Wavelength[2]	λ_D		602	nm	

Yellow HDLY-3416

Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per Digit, Character Average	I_V	1.2	3.7	mcd	"*" Illuminated in All Four Digits 19 Dots ON per Digit.
Peak Wavelength	λ_{PEAK}		583	nm	
Dominant Wavelength[2]	λ_D		585	nm	

Green HDLG-3416

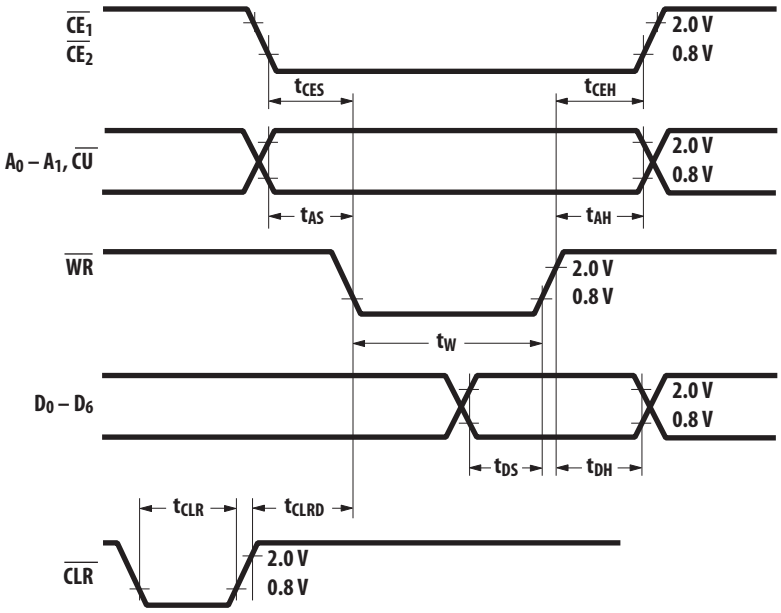
Parameter	Symbol	Min.	Typ.	Units	Test Conditions
Average Luminous Intensity per Digit, Character Average	I_V	1.2	5.6	mcd	"*" Illuminated in All Four Digits 19 Dots ON per Digit.
Peak Wavelength	λ_{PEAK}		568	nm	
Dominant Wavelength[2]	λ_D		574	nm	

Notes:
1. Refers to the initial case temperature of the device immediately prior to the light measurement.
2. Dominant wavelength, λ_D, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.

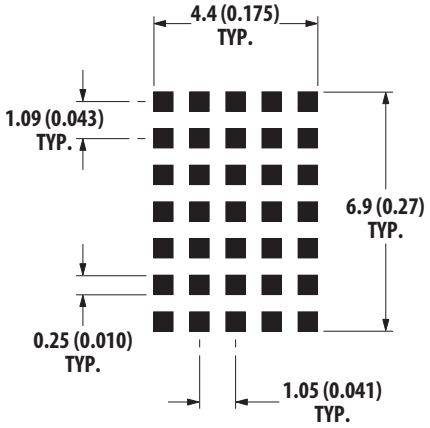
AC Timing Characteristics over Operating Temperature Range at V_{DD} = 4.5 V

Parameter	Symbol	Min	Units
Address Setup	t_{AS}	10	ns
Address Hold	t_{AH}	40	ns
Data Setup	t_{DS}	50	ns
Data Hold	t_{DH}	40	ns
Chip Enable Setup	t_{CES}	0	ns
Chip Enable Hold	t_{CEH}	0	ns
Write Time	t_W	75	ns
Clear	t_{CLR}	10	µs
Clear Disable	t_{CLRD}	1	µs

Timing Diagram



Enlarged Character Font



Notes:
1. Unless otherwise specified, the tolerance on all dimensions is ± 0.254 mm (0.010").
2. Dimensions are in millimeters (inches).

Electrical Description

Pin Function	Description
Chip Enable ($\overline{CE_1}$ and $\overline{CE_2}$, Pins 3 and 4)	$\overline{CE_1}$ and $\overline{CE_2}$ must be a logic 0 to write to the display.
Clear ($\overline{CLR}$, Pin 5)	When $\overline{CLR}$ is a logic 0 the ASCII RAM is reset to 20hex (space) and the Control Register/Attribute RAM is reset to 00hex.
Cursor Enable (CUE Pin 11)	CUE determines whether the IC displays the ASCII or the Cursor memory. (1 = Cursor, 0 = ASCII.)
Cursor Select ($\overline{CU}$, Pin 10)	$\overline{CU}$ determines whether data is stored in the ASCII RAM or the Attribute RAM/Control Register. (1 = ASCII, 0 = Attribute RAM/ Control Register.)
Write ($\overline{WR}$, Pin 9)	$\overline{WR}$ must be a logic 0 to store data in the display.
Address Inputs (A_1 and A_0, Pins 7 and 8)	A_0-A_1 selects a specific location in the display memory. Address 00 accesses the far right display location. Address 11 accesses the far left location.
Data Inputs (D_0-D_6, Pins 16 – 22)	D_0-D_6 are used to specify the input data for the display.
V_{DD} (Pin 6)	V_{DD} is the positive power supply input.
GND (Pin 12)	GND is the display ground.
Blanking Input ($\overline{BL}$, Pin 14)	$\overline{BL}$ is used to flash the display, blank the display or to dim the display.

Display Internal Block Diagram

Figure 1 shows the HDLX-3416 display internal block diagram. The CMOS IC consists of a 4 x 7 Character RAM, a 2 x 4 Attribute RAM, a 5 bit Control Register, a 128 character ASCII decoder and the refresh circuitry necessary to synchronize the decoding and driving of four 5 x 7 dot matrix displays.

Four 7 bit ASCII words are stored in the Character RAM. The IC reads the ASCII data and decodes it via the 128 character ASCII decoder. The ASCII decoder includes the 64 character set of the HPDL-2416, 32 lower case ASCII symbols, and 32 foreign language symbols.

A 5 bit word is stored in the Control Register. Three fields within the Control Register provide an 8 level brightness control, master blank, and extended functions disable.

For each display digit location, two bits are stored in the Attribute RAM. One bit is used to enable a cursor character at each digit location. A second bit is used to individually disable the blanking features at each digit location.

The display is blanked and dimmed through an internal blanking input on the row drivers. Logic within the IC allows the user to dim the display either through the $\overline{BL}$ input or through the brightness control in the control register. Similarly the display can be blanked through the $\overline{BL}$ input, the Master Blank in the Control Register, or the Digit Blank Disable in the Attribute RAM.

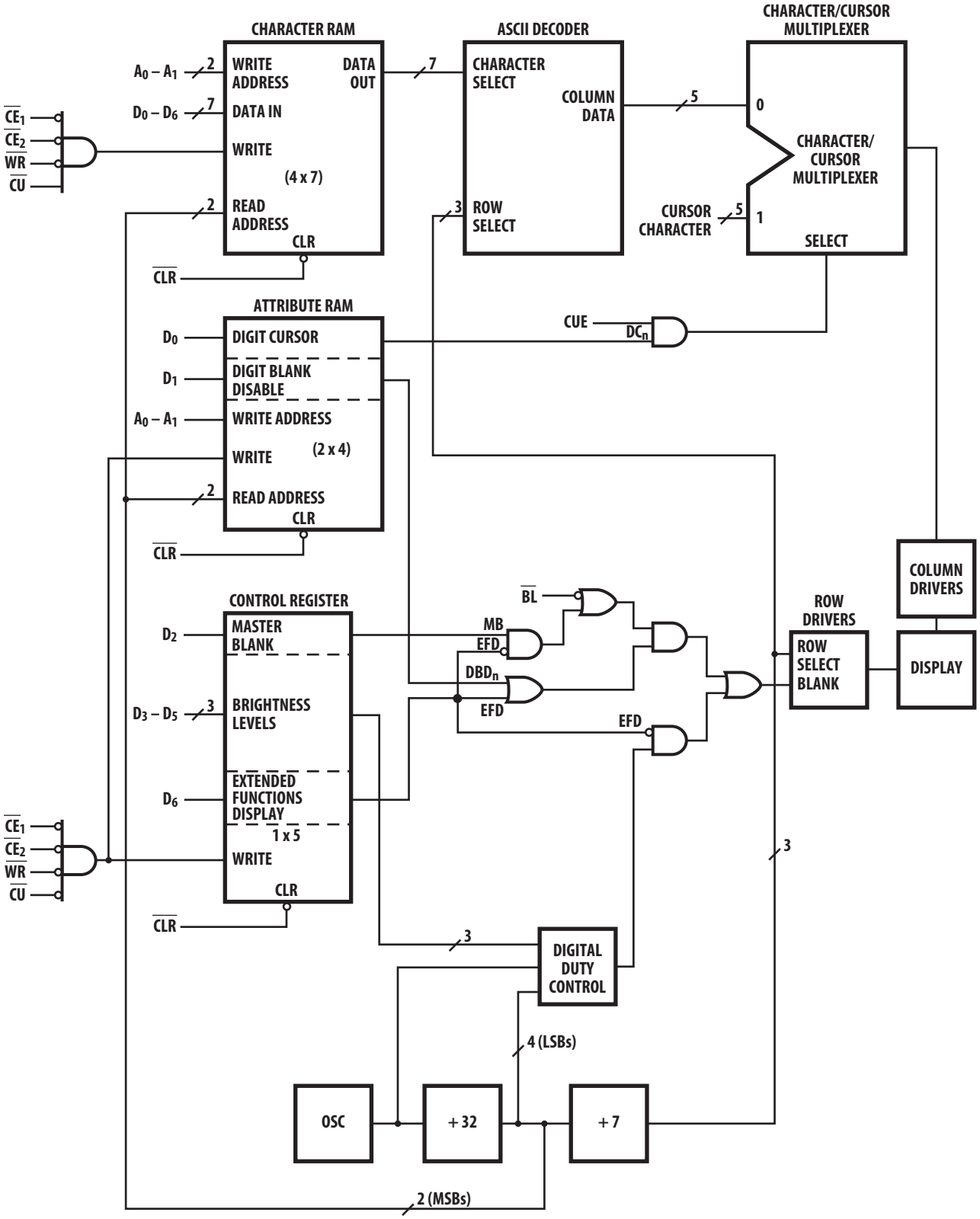


Figure 1. Internal block diagram.

Display Clear

Data stored in the Character RAM, Control Register, and Attribute RAM will be cleared if the clear ($\overline{CLR}$) is held low for a minimum of 10 µs. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$). After the display is cleared, the ASCII code for a space (20hex) is loaded into all character RAM locations and 00hex is loaded into all Attribute RAM/Control Register memory locations.

Data Entry

Figure 2 shows a truth table for the HDLX-3416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to logic 0 and the cursor select ($\overline{CU}$) to logic 1 will enable ASCII data loading. When cursor select ($\overline{CU}$) is set to logic 0, data will be loaded into the Control Register and Attribute RAM. Address inputs A_0-A_1 are used to select the digit location in the display. Data inputs D_0-D_6 are used to load information into the display. Data will be latched into the display on the rising edge of the $\overline{WR}$ signal. D_0-D_6, A_0-A_1, $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CU}$ must be held stable during the write cycle to ensure that correct data is stored into the display. Data can be loaded into the display in any order. Note that when A_0 and A_1 are logic 0, data is stored in the right most display location.

Cursor

When cursor enable (CUE) is a logic 1, a cursor will be displayed in all digit locations where a logic 1 has been stored in the Digit Cursor memory in the Attribute RAM. The cursor consists of all 35 dots ON at half brightness. A flashing cursor can be displayed by pulsing CUE. When CUE is a logic 0, the ASCII data stored in the Character RAM will be displayed regardless of the Digit Cursor bits.

Blanking

Blanking of the display is controlled through the $\overline{BL}$ input, the Control Register, and Attribute RAM. The user can achieve a variety of functions by using these controls in different combinations, such as full hardware display blank, software blank, blanking of individual characters, and synchronized flashing of individual characters or entire display (by strobing the blank input). All of these blanking modes affect only the output drivers, maintaining the contents and write capability of the internal RAMs and Control Register, so that normal loading of RAMs and Control Register can take place even with the display blanked.

CUE	$\overline{BL}$	$\overline{CLR}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	$\overline{CU}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Function
0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	Display ASCII
1	1	1														Display Stored Cursor
X	X	0														Reset RAMs
X	0	1														Blank Display but do not reset RAMs and Control Register
X	X	1	0	0	0	0	0	0	Extended Functions Disable	Intensity Control			Master Blank	Digit Blank Disable 0	Digit Cursor 0	Write to Attribute RAM and Control Register
						0	0	1	0 = Enable D_1-D_5	000 = 100% 001 = 60% 010 = 40% 011 = 27% 100 = 17% 101 = 10% 110 = 7% 111 = 3%			0 = Display ON	Digit Blank Disable 1	Digit Cursor 1	DBDn = 0, Allows Digit n to be blanked
						0	1	0	1 = Disable D_1-D_5				1 = Display Blanked	Digit Blank Disable 2	Digit Cursor 2	DBDn = 1 Prevents Digit n from being blanked. DCn = 0 Removes cursor from Digit n
						0	1	1	D_0 Always Enabled					Digit Blank Disable 3	Digit Cursor 3	DCn = 1 Stores cursor at Digit n
X	X	1	0	0	0	1	0	0	Digit 0 ASCII Data (Right Most Character)							Write to Character RAM
						1	0	1	Digit 1 ASCII Data							
						1	1	0	Digit 2 ASCII Data							
						1	1	1	Digit 3 ASCII Data (Left Most Character)							
X	X	1	1	X	X	X	X	X	X	X	X	X	X	X	X	No Change
			X	1	X											
			X	X	1											

0 = Logic 0; 1 = Logic 1; X = Do Not Care

Figure 2. Display truth table.

Figure 3 shows how the Extended Function Disable (bit D_6 of the Control Register), Master Blank (bit D_2 of the Control Register), Digit Blank Disable (bit D_1 of the Attribute RAM), and BL input can be used to blank the display.

When the Extended Function Disable is a logic 1, the display can be blanked only with the $\overline{BL}$ input. When the Extended Function Disable is a logic 0, the display can be blanked through the $\overline{BL}$ input, the Master Blank, and the Digit Blank Disable. The entire display will be blanked if either the BL input is logic 0 or the Master Blank is logic 1, providing all Digit Blank Disable bits are logic 0. Those digits with Digit Blank Disable bits a logic 1 will ignore both blank signals and remain ON. The Digit Blank Disable bits allow individual characters to be blanked or flashed in synchronization with the $\overline{BL}$ input.

Dimming

Dimming of the display is controlled through either the $\overline{BL}$ input or the Control Register. A pulse width modulated signal can be applied to the $\overline{BL}$ input to dim the display. A three bit word in the Control Register generates an internal pulse width modulated signal to dim the display. The internal dimming feature is enabled only if the Extended Function Disable is a logic 0.

Bits 3–5 in the Control Register provide internal brightness control. These bits are inter-preted as a three bit binary code, with code (000) corresponding to the maximum brightness and code (111) to the minimum brightness. In addition to varying the display brightness, bits 3–5 also vary the average value of I_{DD}. I_{DD} can be specified at any brightness level as shown in Table 1.

EFD	MB	DBDn	$\overline{BL}$	
0	0	0	0	– Display Blanked by BL
0	0	X	1	– Display ON
0	X	1	0	– Display Blanked by BL. Individual Characters "ON" based on "1" being stored in DBDn
0	1	0	X	– Display Blanked by MB
0	1	1	1	– Display Blanked by MB. Individual characters "ON" based on "1" being stored in DBDn
1	X	X	0	– Display Blanked by BL
1	X	X	1	– Display ON

Figure 3. Display blanking truth table.

Table 1. Current Requirements at Different Brightness Levels

Symbol	D_5	D_4	D_3	Brightness	25°C Typ.	25°C Max.	Max. over Temp.	Units
I_{DD}(#)	0	0	0	100%	110	130	160	mA
	0	0	1	60%	66	79	98	mA
	0	1	0	40%	45	53	66	mA
	0	1	1	27%	30	37	46	mA
	1	0	0	17%	20	24	31	mA
	1	0	1	10%	12	15	20	mA
	1	1	0	7%	9	11	15	mA
	1	1	1	3%	4	6	9	mA

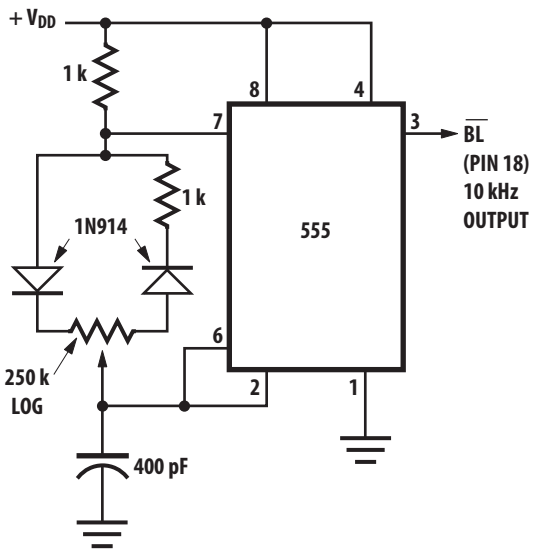


Figure 4. Intensity modulation control using an astable multivibrator (reprinted with permission from Electronics magazine, Sept. 19, 1974, V NU Business pub. Inc.).

Figure 4 shows a circuit designed to dim the display from 98% to 2% by pulse width modulating the $\overline{BL}$ input. A logarithmic or a linear potentiometer may be used to adjust the display intensity. However, a logarithmic potentiometer matches the response of the human eye and therefore provides better resolution at low intensities. The circuit frequency should be designed to operate at 10 kHz or higher. Lower frequencies may cause the display to flicker.

Extended Function Disable

Extended Function Disable (bit D_6 of the Control Register) disables the extended blanking and dimming functions in the HDLX-3416. If the Extended Function Disable is a logic 1, the internal brightness control, Master Blank, and Digit Blank Disable bits are ignored. However, the $\overline{BL}$ input and Cursor control are still active.

Mechanical and Electrical Considerations

The HDLX-3416 is a 22 pin DIP package that can be stacked horizontally and vertically to create arrays of any size. The display is designed to operate continuously from -40°C to +85°C for all possible input conditions.

The HDLX-3416 is assembled by die attaching and wire bonding 140 LEDs and a CMOS IC to a high temperature printed circuit board. A polycarbonate lens is placed over the PC board creating an air gap environment for the LED wire bonds. Backfill epoxy environmentally seals the display package. This package construction makes the display highly tolerant to temperature cycling and allows wave soldering.

The inputs to the CMOS IC are protected against static discharge and input current latchup. However, for best results standard CMOS handling precautions should be used. Prior to use, the HDLX-3416 should be stored in anti-static tubes or conductive material. During assembly a grounded conductive work area should be used, and assembly personnel should wear conductive wrist straps. Lab coats made of synthetic material should be avoided since they are prone to static charge build-up.

Input current latchup is caused when the CMOS inputs are subjected either to a voltage below ground (Vin < ground) or to a voltage higher than V_{DD} (Vin > V_{DD}) and when a high current is forced into the input. To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{DD}. Voltages should not be applied to the inputs until V_{DD} has been applied to the display.Transient input voltages should be eliminated.

Soldering and Post Solder Cleaning Instructions for the HDLX-3416

The HDLX-3416 may be hand soldered or wave soldered with SN63 solder. When hand soldering it is recommended that an electronically temperature controlled and securely grounded soldering iron be used. For best results, the iron tip temperature should be set at 315°C (600°F). For wave soldering, a rosin-based RMA flux can be used. The solder wave temperature should be set at 245°C ± 5°C (473°F ± 9°F), and dwell in the wave should be set between 1½ to 3 seconds for optimum soldering. The preheat temperature should not exceed 110°C (230°F) as measured on the solder side of the PC board.

For further information on soldering and post solder cleaning, see Application Note 1027, Soldering LED Components.

Contrast Enhancement

The objective of contrast enhancement is to provide good readability in the end user's ambient lighting conditions. The concept is to employ both luminance and chrominance contrast techniques. These enhance readability by having the OFF-dots blend into the display background and the ON-dots vividly stand out against the same background. For additional information on contrast enhancement, see Application Note 1015.

Intensity Bin Limits

	Intensity Range (mcd)	
Bin	**Min.**	**Max.**
A	1.20	1.77
B	1.45	2.47
C	2.02	3.46
D	2.83	4.85
E	3.97	6.79
F	5.55	9.50
G	7.78	13.30

Note:
Test conditions as specified in Optical Characteristic table.

Color Bin Limits

		Color Range (nm)	
Color	**Bin**	**Min.**	**Max.**
Green	1	576.0	580.0
	2	573.0	577.0
	3	570.0	574.0
	4	567.0	571.5
Yellow	3	581.5	585.0
	4	584.0	587.5
	5	586.5	590.0
	6	589.0	592.5

Note:
Test conditions as specified in Optical Characteristic table.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-3642EN - June 20, 2012