

Transcend 44-Pin IDE Flash Module

128MB ~ 4GB

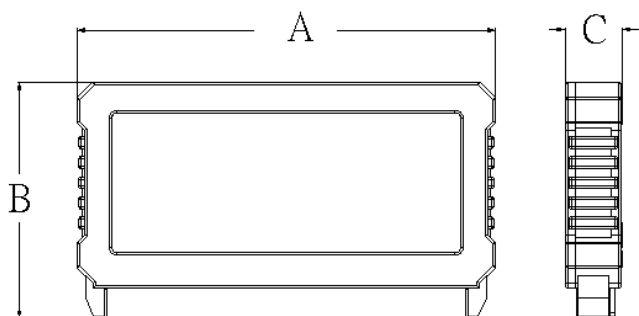
Description

With an IDE interface and strong data retention ability, 44-Pin IDE Flash Modules are ideal for use in the harsh environments where Industrial PCs, Set-Top Boxes, etc. are used.

Features

- RoHS compliant products
- Storage Capacity: 128MB ~ 4GB
- Operating Voltage: 3.3V $\pm$ 5% or 5V $\pm$ 10%
- Operating Temperature: 0°C ~ 70°C
- Endurance: 2,000,000 Program/Erase cycles
- MTBF: 1,000,000 hours
- Durability of Connector: 10,000 times
- Fully compatible with devices and OS that support the IDE standard (pitch = 2.00 mm)
- Built-in ECC function assures high reliability of data transfer
- Supports up to Ultra DMA Mode 4
- Supports PIO Mode 6

Placement



Dimensions

Side	Millimeters	Inches
A	52.00 $\pm$ 0.40	2.047 $\pm$ 0.016
B	29.50 $\pm$ 0.50	1.162 $\pm$ 0.020
C	7.20 $\pm$ 0.20	0.284 $\pm$ 0.008

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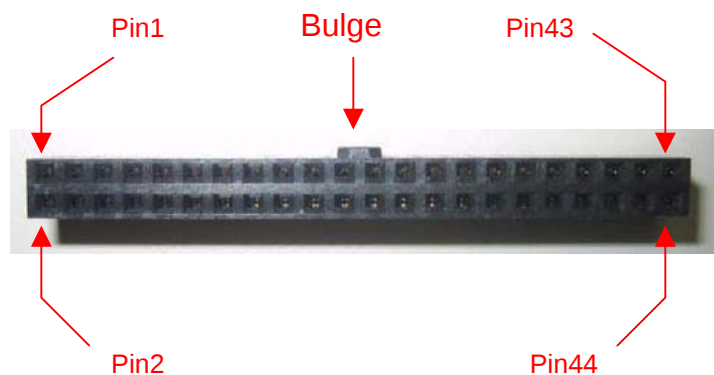
Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
01	RESET	12	HD12	23	IOWB	34	PDIAGB
02	GND	13	HD2	24	GND	35	HA0
03	HD7	14	HD13	25	IORB	36	HA2
04	HD8	15	HD1	26	GND	37	CE1B
05	HD6	16	HD14	27	NC	38	CE2B
06	HD9	17	HD0	28	NC	39	DASPB
07	HD5	18	HD15	29	NC	40	GND
08	HD10	19	GND	30	GND	41	VCC
09	HD4	20	VCC	31	IREQ	42	VCC
10	HD11	21	NC	32	IOIS16B	43	GND
11	HD3	22	GND	33	HA1	44	NC

Pin Definition

Symbol	Function
HD0 ~ HD15	Data Bus (Bi-directional)
HA0 ~ HA2	Address Bus (Input)
RESET	Device Reset (Input)
IORB	Device I/O Read (Input)
IOWB	Device I/O Write (Input)
IOIS16B	Transfer Type 8/16 bit (Output)
CE1B, CE2B	Chip Select (Input)
PDIAGB	Pass Diagnostic (Bi-directional)
DASPB	Disk Active/Slave Present (Bi-directional)
IREQ	Interrupt Request (Output)
NC	No Connection
GND	Ground
VCC	Vcc Power Input

Pin Layout

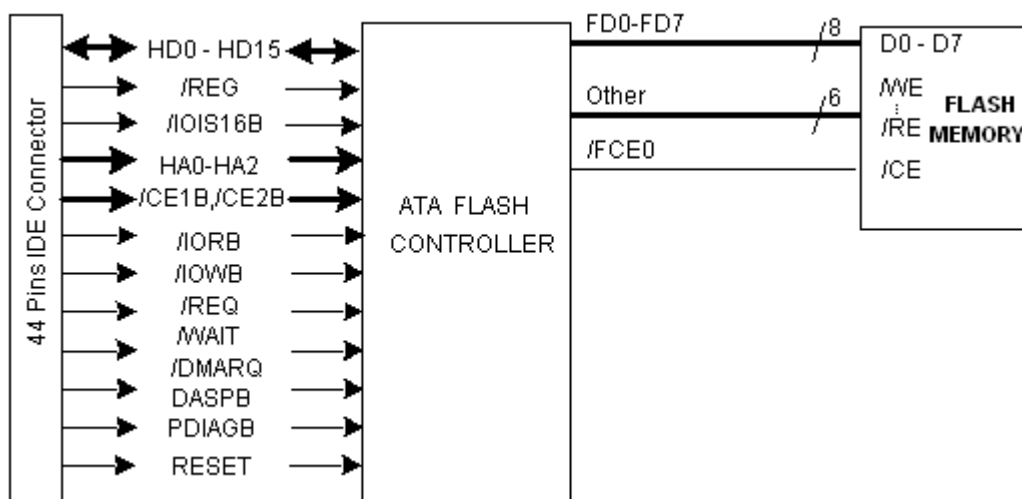


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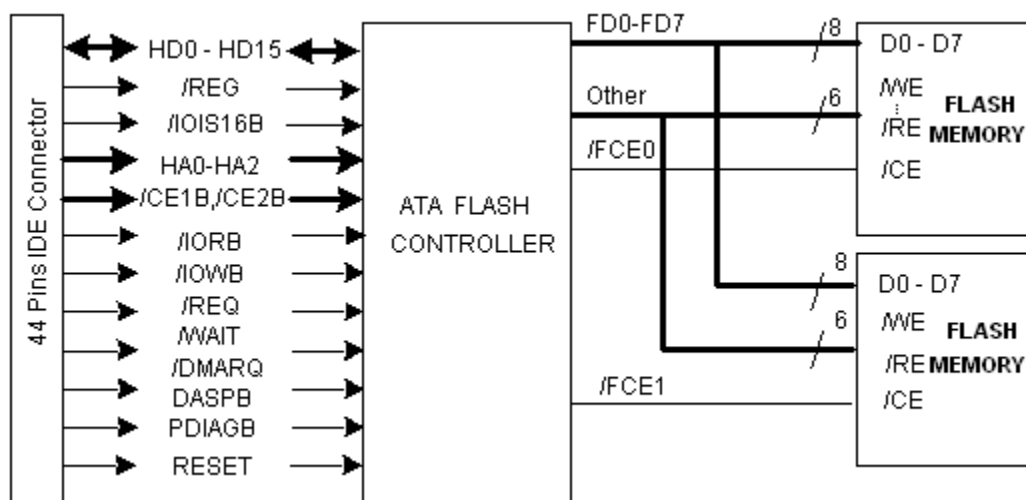
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Block Diagram

With 1 pcs of Flash Memory:



With 2 pcs of Flash Memory:



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Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD-VSS	DC Power Supply	-0.6	+6	V
Ta	Operating Temperature	0	+70	°C
Tst	Storage Temperature	-40	+85	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
VDD	Power supply	3.0	5.5	V
VIN	Input voltage	0	VDD+0.3	V
Ta	Operating Temperature	0	+70	°C

DC Characteristics (Ta=0 °C to +70 °C, Vcc = 3.3V ±10%)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	VIH	--	2	--	--	V
	VIL	--	--	--	0.2 x Vcc	V
Output Voltage	VOH	IOH = 4,8mA	Vcc – 0.8	--	--	V
	VOL	IOL = 4,8mA	--	--	0.4	V
Input leakage current	ILK	VIH = VDD / VIL = GND	-1	--	1	uA
Sleep current	ISP	--	--	0.5	1	mA

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■ True IDE Mode

The card can be configured in a True IDE. This card is configured in this mode only when the -OE input signal is asserted GND by the host. In this True IDE mode Attribute Registers are not accessible from the host. Only I/O operations to the task file and data register are allowed. The default operation of the data register is 16-bit mode. The card permits 8-bit accessed if the user issued a Set Feature Command to put the device in 8-bit mode.

(1) True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-OWR	D8 to D15	D0 to D7
Invalid mode	L	L	x	x	x	High-Z	High-Z
Standby mode	H	H	x	x	x	High-Z	High-Z
Data register access	H	L	0	L	H	odd byte	even byte
Alternate status access	L	H	6H	L	H	High-Z	status out
Other task file access	H	L	1-7H	L	H	High-Z	data

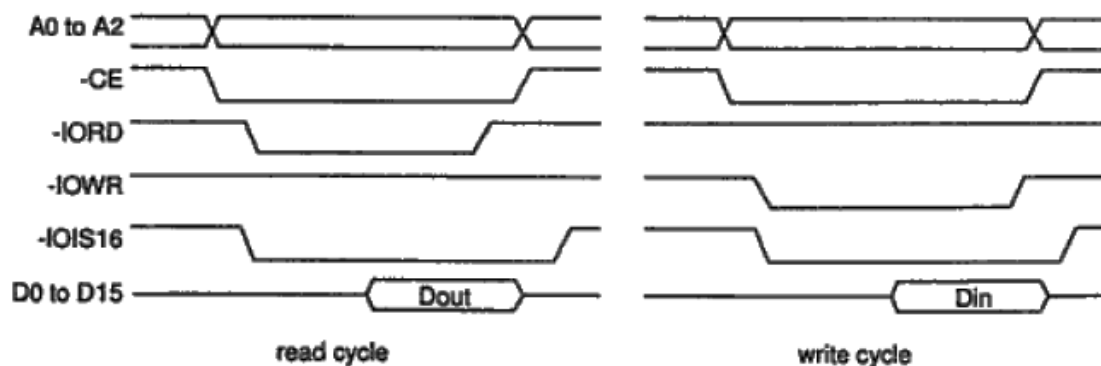
Note: x: L or H

(2) True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-OWR	D8 to D15	D0 to D7
Invalid mode	L	L	x	x	x	don't care	don't care
Standby mode	H	H	x	x	x	don't care	don't care
Data register access	H	L	0	H	L	odd byte	even byte
Control register access	L	H	6H	H	L	don't care	control in
Other task file access	H	L	1-7H	H	L	don't care	data

Note: x: L or H

(3) True IDE Mode I/O Access Timing Example



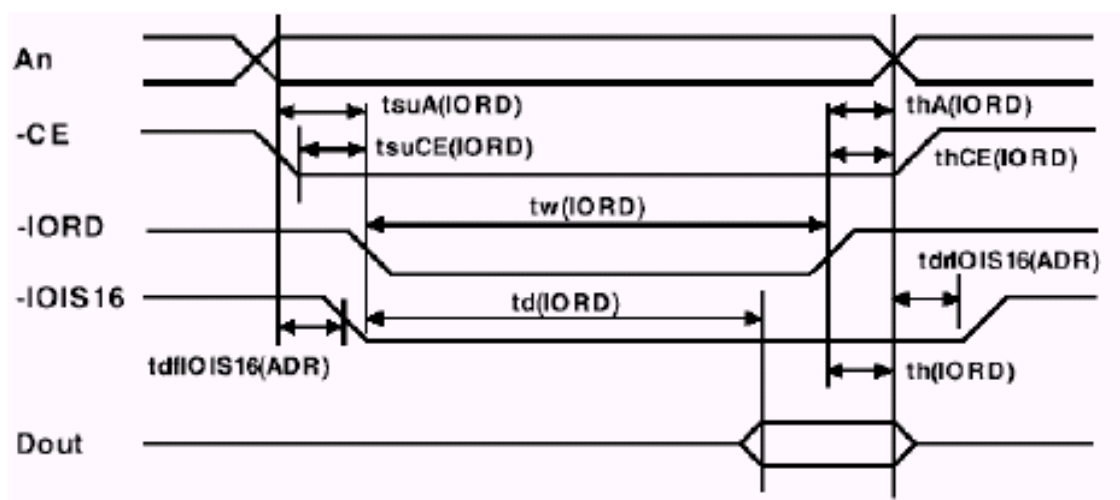
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True IDE Mode Access Read AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data delay after IORD	td(IORD)	—	—	50	ns
Data hold following IORD	th(IORD)	5	—	—	ns
IORD width time	tw(IORD)	70	—	—	ns
Address setup before IORD	tsuA(IORD)	15	—	—	ns
Address hold following IORD	thA(IORD)	10	—	—	ns
CE setup before IORD	tsuCE(IORD)	5	—	—	ns
CE hold following IORD	thCE(IORD)	10	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tsfIOIS16(ADR)	—	—	35	ns

True IDE Mode Access Read Timing



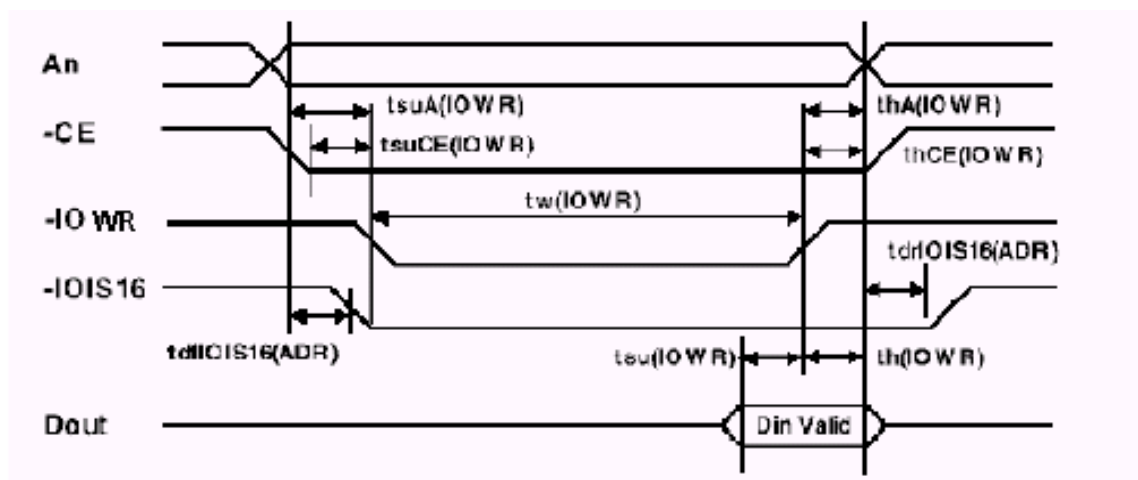
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True IDE Mode Access Write AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data setup before IOWR	tsu(IOWR)	20	—	—	ns
Data hold following IOWR	th(IOWR)	10	—	—	ns
IOWR width time	tw(IOWR)	50	—	—	ns
Address setup before IOWR	tsuA(IOWR)	15	—	—	ns
Address hold following IOWR	thA(IOWR)	10	—	—	ns
CE setup before IOWR	tsuCE(IOWR)	5	—	—	ns
CE hold following IOWR	thCE(IOWR)	10	—	—	ns
IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
IOIS16 delay rising from address	tsfIOIS16(ADR)	—	—	35	ns

True IDE Mode Access Write Timing



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■ IDE Mode Access Read/Write AC Characteristics

CFA Rev 2.0 and ATA/ATAPI-5 Defined True IDE Mode I/O Timing Specification (*1)

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Data setup before IOWR (min)	tsu(IOWR)	60	45	30	30	20	ns
Data hold following IOWR (min)	th(IOWR)	30	20	15	10	10	ns
Data delay after IORD (max)	td(IORD)	115	90	80	60	50	ns
Data hold following IORD (min)	th(IORD)	5	5	5	5	5	ns
IOWR/IORD width time (min)	tw(IOWR/IORD)	165	125	100	80	70	ns
Address setup before IOWR/IORD (min)	tsuA(IOWR/IORD)	70	50	30	30	25	ns
Address hold following IOWR/IORD (min)	thA(IOWR/IORD)	20	15	10	10	10	ns
CE setup before IOWR/IORD (min)	tsuCE(IOWR/IORD)	70	50	30	30	25	ns
CE hold following IOWR/IORD (min)	thCE(IOWR/IORD)	20	15	10	10	10	ns
IOIS16 delay falling from address (max)	tdflIOIS16(ADR)	90	50	40	n/a (*3)	n/a (*3)	ns
IOIS16 delay rising from address (max)	tsflIOIS16(ADR)	60	45	30	n/a (*3)	n/a (*3)	ns

Supported True IDE Mode I/O Timing Specification (*2)

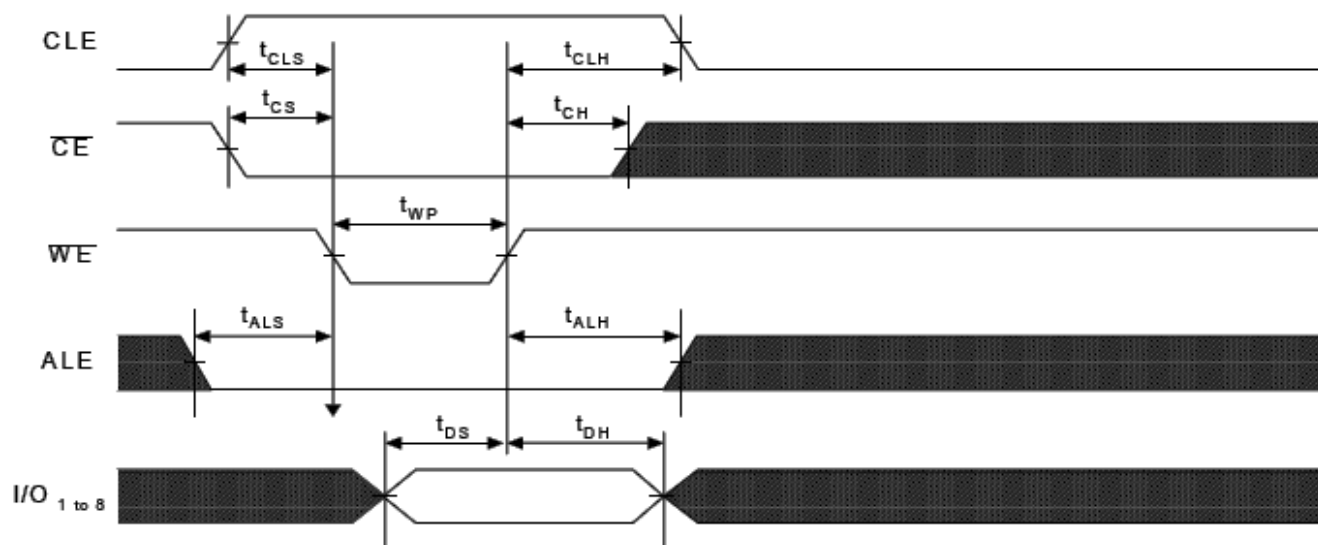
Parameter	Symbol	Controller Supported	Unit
Data setup before IOWR (min)	tsu(IOWR)	20	ns
Data hold following IOWR (min)	Th(IOWR)	10	ns
Data delay after IORD (max)	Td(IORD)	50	ns
Data hold following IORD (min)	Th(IORD)	5	ns
IOWR/ IORD width time (min)	tw(IOWR/ IORD)	70	ns
Address setup before IOWR/IORD (min)	tsuA(IOWR/IORD)	15	ns
Address hold following IOWR/IORD (min)	thA(IOWR/IORD)	10	ns
CE setup before IOWR/IORD (min)	TsuCE(IOWR/IORD)	5	ns
CE hold following IOWR/IORD (min)	thCE(IOWR/IORD)	10	ns
IOIS16 delay falling from address (max)	tdflIOIS16(ADR)	35	ns
IOIS16 delay rising from address (max)	tsflIOIS16(ADR)	35	ns

Note: This timing apply only to modes 0, 1 and 2. For modes 3 and 4, the "IOIS16" signal is not valid.

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FLASH Interface Command write Timing :



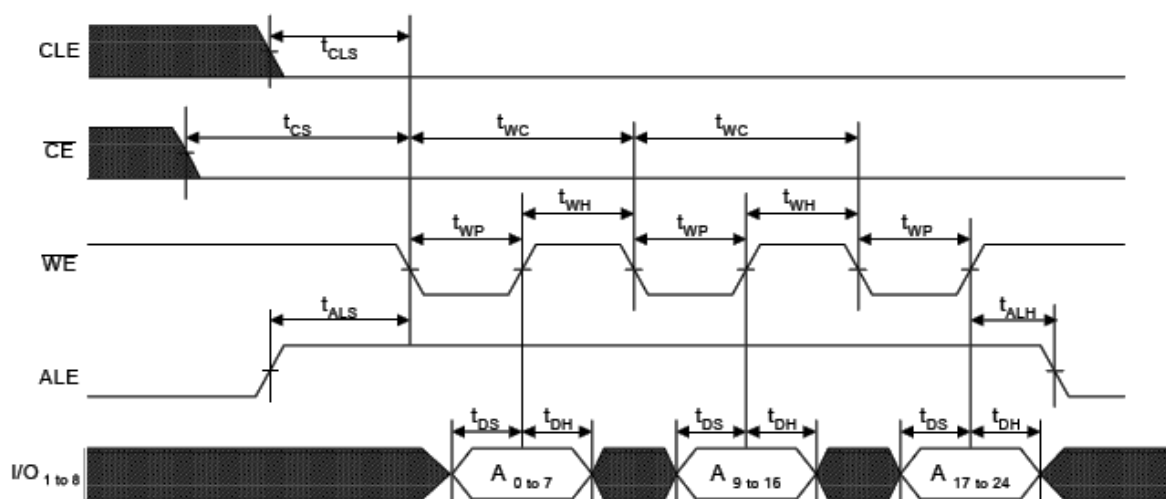
AC Timing Characteristics -Flash side ($T_{OPR} = 0^{\circ}\text{C}$ to 70°C , $T_{OPRI} = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.0\text{V}$ to 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
CLE Output Setup Time	t_{CLS}	0	0		ns
CLE Output Hold Time	t_{CLH}	10	34		ns
CE Output Setup Time	t_{CS}	0	>34		ns
CE Output Hold Time	t_{CH}	10	>34		ns
WE Output Pulse Width	t_{WP}	25	34		ns
ALE Output Setup Time	t_{ALS}	0	>34		ns
ALE Output Hold Time	t_{ALH}	10	>34		ns
Data Output Setup Time	t_{DS}	20	25		ns
Data Output Hold Time	t_{DH}	10	40		ns

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FLASH Interface Address Write Timing :



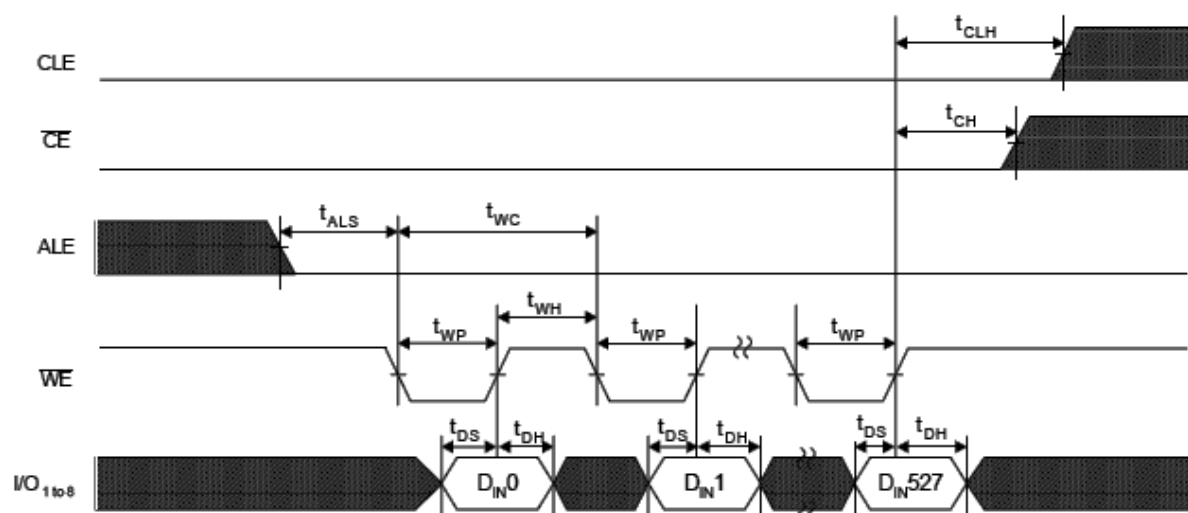
AC Timing Characteristics -Flash side ($T_{OPR} = 0^{\circ}\text{C}$ to 70°C , $T_{OPR1} = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.0\text{V}$ to 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
CLE Output Setup Time	t_{CLS}	0	>34		ns
CLE Output Hold Time	t_{CLH}	10	>34		ns
CE Output Setup Time	t_{CS}	0	>34		ns
CE Output Hold Time	t_{CH}	10	>34		ns
WE Output Pulse Width	t_{WP}	25	34		ns
WE Output High Hold Time	t_{WH}	15	34		ns
ALE Output Setup Time	t_{ALS}	0	0		ns
ALE Output Hold Time	t_{ALH}	10	34		ns
Data Output Setup Time	t_{DS}	20	25		ns
Data Output Hold Time	t_{DH}	10	40		ns
Flash Write Cycle Time	t_{WC}	50	68		ns

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FLASH Interface DATA Write Timing :



AC Timing Characteristics -Flash side ($T_{OPR} = 0^{\circ}\text{C}$ to 70°C , $T_{OPR1} = -40^{\circ}\text{C}$ to

85°C , $V_{CC} = 3.0\text{V}$ to 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
CLE Output Hold Time	t_{CLH}	10	>34		ns
CE Output Hold Time	t_{CH}	10	>34		ns
WE Output Pulse Width	t_{WP}	25	34		ns
WE Output High Hold Time	t_{WH}	15	34		ns
ALE Output Setup Time	t_{ALS}	0	>34		ns
Data Output Setup Time	t_{DS}	20	40		ns
Data Output Hold Time	t_{DH}	10	20		ns
Flash Write Cycle Time	t_{WC}	50	68		ns

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■ True IDE Mode I/O map

-CE2	-CE1	A2	A1	A0	-IORD=L	-IOWR=L
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector count register	Sector count register
1	0	0	1	1	Sector number register	Sector number register
1	0	1	0	0	Cylinder low register	Cylinder low register
1	0	1	0	1	Cylinder high register	Cylinder high register
1	0	1	1	0	Drive head register	Drive head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt. status register	Device control register
0	1	1	1	1	Drive address register	Reserved

(1) Data register: This register is a 16-bit register that has read/write ability, and it is used for transferring 1 sector data between the card and the host. This register can be accessed in word mode and byte mode. This register overlaps the Error or Feature register.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

(2) Error register: This register is a read only register, and it is used for analyzing the error content at the card accessing. This register is valid when the BSY bit in Status register and Alternate Status register are set to "0"(Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	"0"	IDNF	"0"	ABRT	"0"	AMNF

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bit	Name	Function
7	BBK(Bad Block detected)	This bit is set when a Bad Block is detected in requester ID field.
6	UNC(Data ECC error)	This bit is set when Uncorrectable error is occurred at reading the card.
4	IDNF(ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT(ABoRTed command)	This bit is set if the command has been aborted because of the card status condition.(Not ready, Write fault, Invalid command, etc.)
0	AMNF(Address Mark Not Found)	This bit is set in case of a general error.

(3) Feature register: This register is write only register, and provides information regarding features of the drive which the host wishes to utilize.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature byte							

(4) Sector count register:

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value of this register is zero, a count of 256 sectors is specified. In plural sector transfer, if not successfully completed, the register contains the number of sectors, which need to be transferred in order to complete, the request.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector count byte							

(5) Sector number register: This register contains the starting sector number, which is started by following sector transfer command.

Bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector number byte							

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(6) Cylinder low register: This register contains the low 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder low byte							

(7) Cylinder high register: This register contains the high 8-bit of the starting cylinder address, which is started by following sector transfer command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder high byte							

(8) Drive head register: This register is used for selecting the Drive number and Head number for the following command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Obsolete	LBA	Obsolete	DRV		Head number bit[3:0]		

bit	Name	Function
7	Obsolete bit	This bit is set to "1" normally.
6	LBA	LBA is a flag to select either Cylinder/Head/Sector(CHS) or Logical Block Address (LBA) mode. When LBA = 0, CHS mode is selected. When LBA = 1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00 : Sector Number Register D7-D0. LBA15-LBA08 : Cylinder Low Register D7-D0. LBA23-LBA16 : Cylinder High Register D7-D0. LBA27-LBA24 : Drive / Head Register bits HS3-HS0.
5	Obsolete bit	This bit is set to "1" normally.
4	DRV(DRiVe select)	This bit is used for selecting the Master Drive or Slave Drive in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3	Head number	These bits are used for selecting the Head number for the following command. Bit 3 is MSB.

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(9) Status register: This register is read only register, and it indicates the card status of command execution. When this register is read in configured I/O card mode (INDEX=1,2,3) and level interrupt mode, -IREQ is negated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY(BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRDY(Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read or write or seek requests. If this bit is set to "0", the card prohibits these requests.
5	DWF(Drive Write Fault)	This bit is set if this card indicates the write fault status.
4	DSC(Drive Seek Complete)	This bit is set when the drive seek complete.
3	DRQ(Data ReQuest)	This bit is set when the information can be transferred between the host and Data register. This bit is cleared when the card receives the other command.
2	CORR(CORReCted data)	This bit is set when a correctable data error has been occurred and the data has been corrected.
1	IDX(InDeX)	This bit is always set to "0".
0	ERR(ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register or Error register. This bit is cleared by the next command.

(10) Alternate status register: This register is the same as Status register in physically, so the bit assignment refers to previous item of Status register. But this register is different from Status register that -IREQ is not negated when data read.

(11) Command register: This register is write only register, and it is used for writing the command at executing the drive operation. The command code written in the command register, after the parameter is written in the Task File during the card is Ready state.

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(12) Device control register: This register is write only register, and it is used for controlling the card interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	x	x	x	1	SRST	nIEN	0

Bit	Name	Function
7 to 4	X	don't care
3	1	This bit is set to "1".
2	SRST(Software ReSeT)	This bit is set to "1" in order to force the card to perform Task File Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to "0".
1	nIEN(Interrupt Enable)	This bit is used for enabling -IREQ. When this bit is set to "0", -IREQ is enabled. When this bit is set to "1", -IREQ is disabled.
0	0	This bit is set to "0".

(13) Drive Address register: This register is read only register, and it is used for confirming the drive status. This register is provides for compatibility with the AT disk drive interface. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on bit7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
X	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

Bit	Name	Function
7	X	This bit is unknown. It remains tri-state, when host read.
6	nWTG(WriTing Gate)	This bit is set 0.
5 to 2	nHS3-0(Head Select3-0)	These bits is the negative value of Head Select bits(bit 3 to 0)in Drive/Head register.
1	nDS1(Idrive Select1)	This bit is 0, when drive 1 is selected.
0	nDS0(Idrive Select0)	This bit is 0, when drive 0 is selected.

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ATA Command Set

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LSB
1	Check power mode	E5H or 98H	—	—	—	—	Y	—	—
2	Execute drive diagnostic	90H	—	—	—	—	Y	—	—
3	Erase sector(s)	C0H	—	Y	Y	Y	Y	Y	Y
4	Format track	50H	—	Y	—	Y	Y	Y	Y
5	Identify Drive	ECH	—	—	—	—	Y	—	—
6	Idle	E3H or 97H	—	Y	—	—	Y	—	—
7	Idle immediate	E1H or 95H	—	—	—	—	Y	—	—
8	Initialize drive parameters	91H	—	Y	—	—	Y	Y	—
9	Read buffer	E4H	—	—	—	—	Y	—	—
10	Read multiple	C4H	—	Y	Y	Y	Y	Y	Y
11	Read long sector	22H, 23H	—	—	Y	Y	Y	Y	Y
12	Read sector(s)	20H, 21H	—	Y	Y	Y	Y	Y	Y
13	Read verify sector(s)	40H, 41H	—	Y	Y	Y	Y	Y	Y
14	Recalibrate	1XH	—	—	—	—	Y	—	—
15	Request sense	03H	—	—	—	—	Y	—	—
16	Seek	7XH	—	—	Y	Y	Y	Y	Y
17	Set features	EFH	Y	—	—	—	Y	—	—
18	Set multiple mode	C6H	—	Y	—	—	Y	—	—
19	Set sleep mode	E6H or 99H	—	—	—	—	Y	—	—
20	Stand by	E2H or 96H	—	—	—	—	Y	—	—
21	Stand by immediate	E0H or 94H	—	—	—	—	Y	—	—
22	Translate sector	87H	—	Y	Y	Y	Y	Y	Y
23	Wear level	F5H	—	—	—	—	Y	Y	—
24	Write buffer	E8H	—	—	—	—	Y	—	—
25	Write long sector	32H or 33H	—	—	Y	Y	Y	Y	Y
26	Write multiple	C5H	—	Y	Y	Y	Y	Y	Y
27	Write multiple w/o erase	CDH	—	Y	Y	Y	Y	Y	Y
28	Write sector	30H or 31H	—	Y	Y	Y	Y	Y	Y
29	Write sector w/o erase	38H	—	Y	Y	Y	Y	Y	Y
30	Write verify	3CH	—	Y	Y	Y	Y	Y	Y

Note : FR : Feature Register

SC : Sector Count register (00H to FFH)

SN : Sector Number register (01H to 20H)

CY : Cylinder Low/High register

DR : Drive bit of Drive/Head register

HD : Head No.(0 to 3) of Drive/Head register

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■ PIO data in command protocol

This class includes:

- CFA TRANSLATE SECTOR
- IDENTIFY DEVICE
- IDENTIFY PACKET DEVICE
- READ BUFFER
- READ MULTIPLE
- READ SECTOR(S)
- SMART READ DATA

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. Figure 12 describes the protocol of a PIO data in command. This description does not include all possible error conditions.

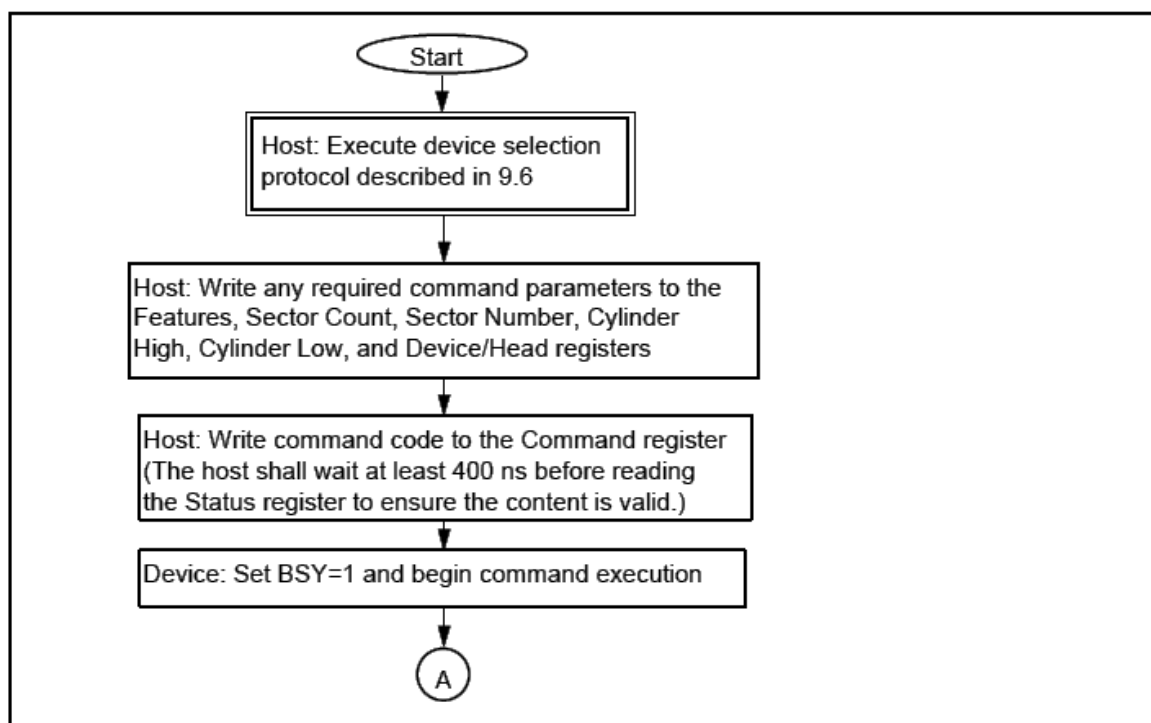


Figure 12 – PIO data in command protocol*(continued)*

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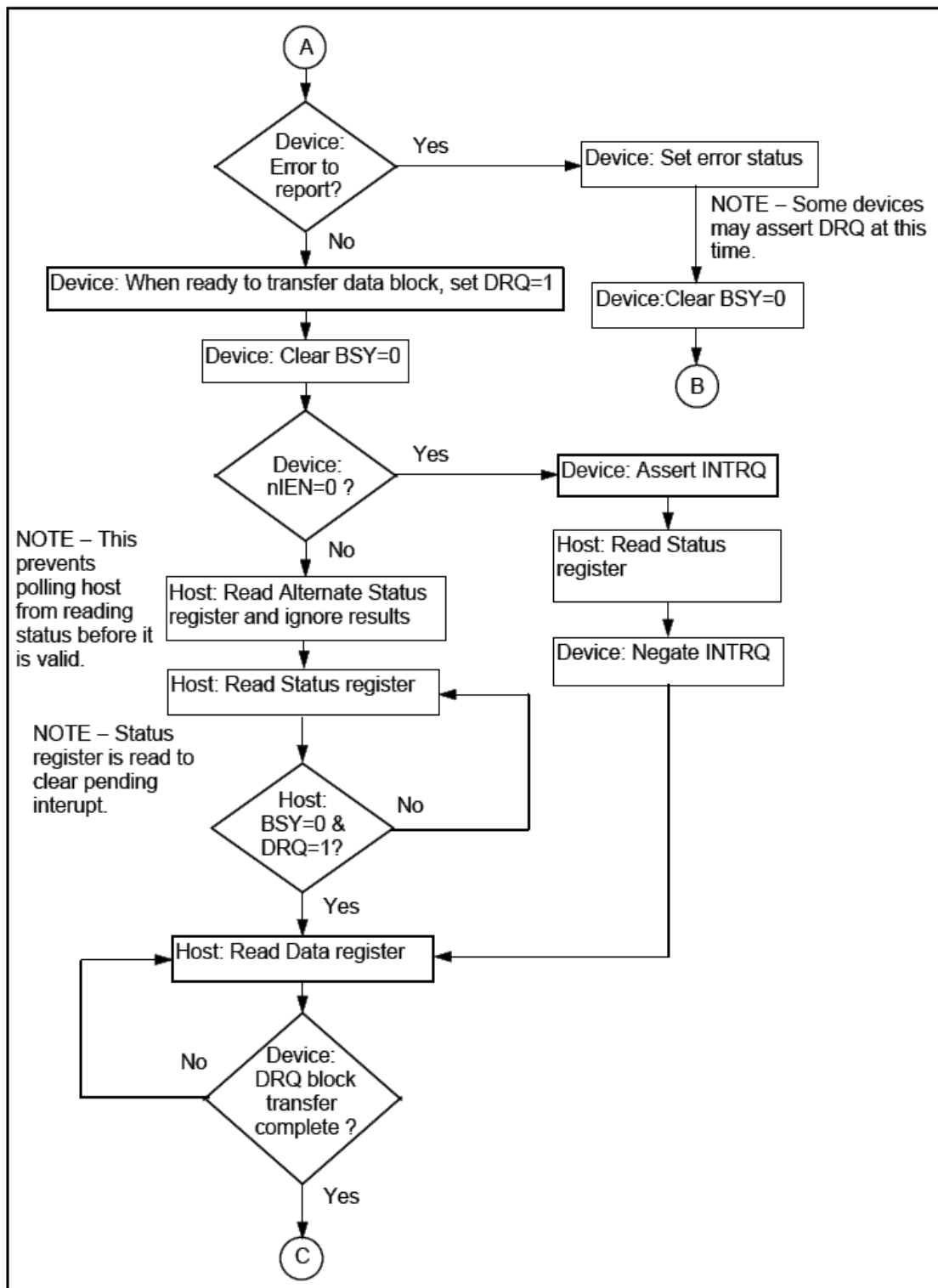


Figure 12 – PIO data in command protocol(continued)

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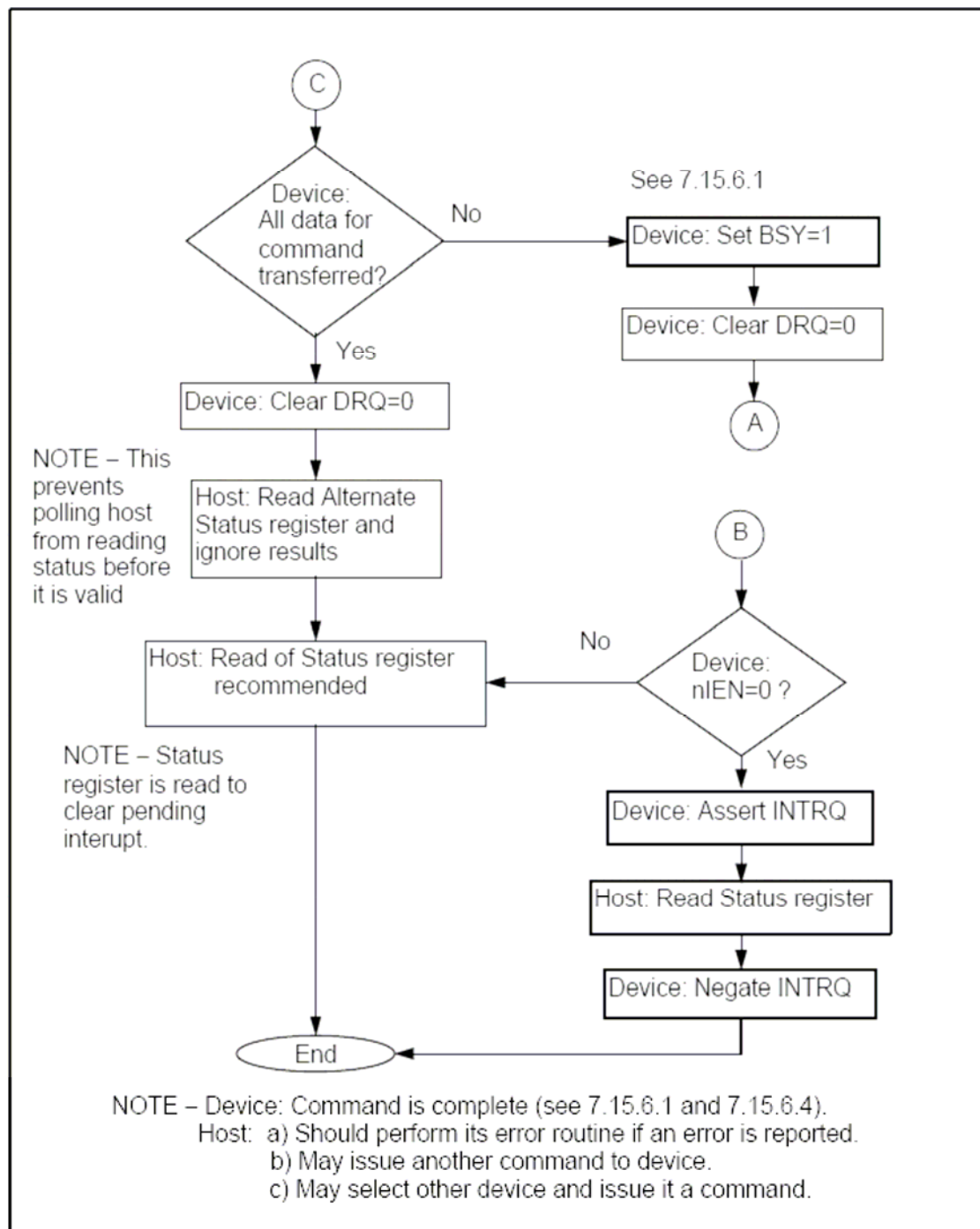


Figure 12 – PIO data in command protocol(*concluded*)

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■ PIO data out command protocol

This class includes:

- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA WRITE SECTORS WITHOUT ERASE
- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- WRITE BUFFER
- WRITE MULTIPLE
- WRITE SECTOR(S)

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 13 describes the protocol of a PIO data out command. This description does not include all possible error conditions.

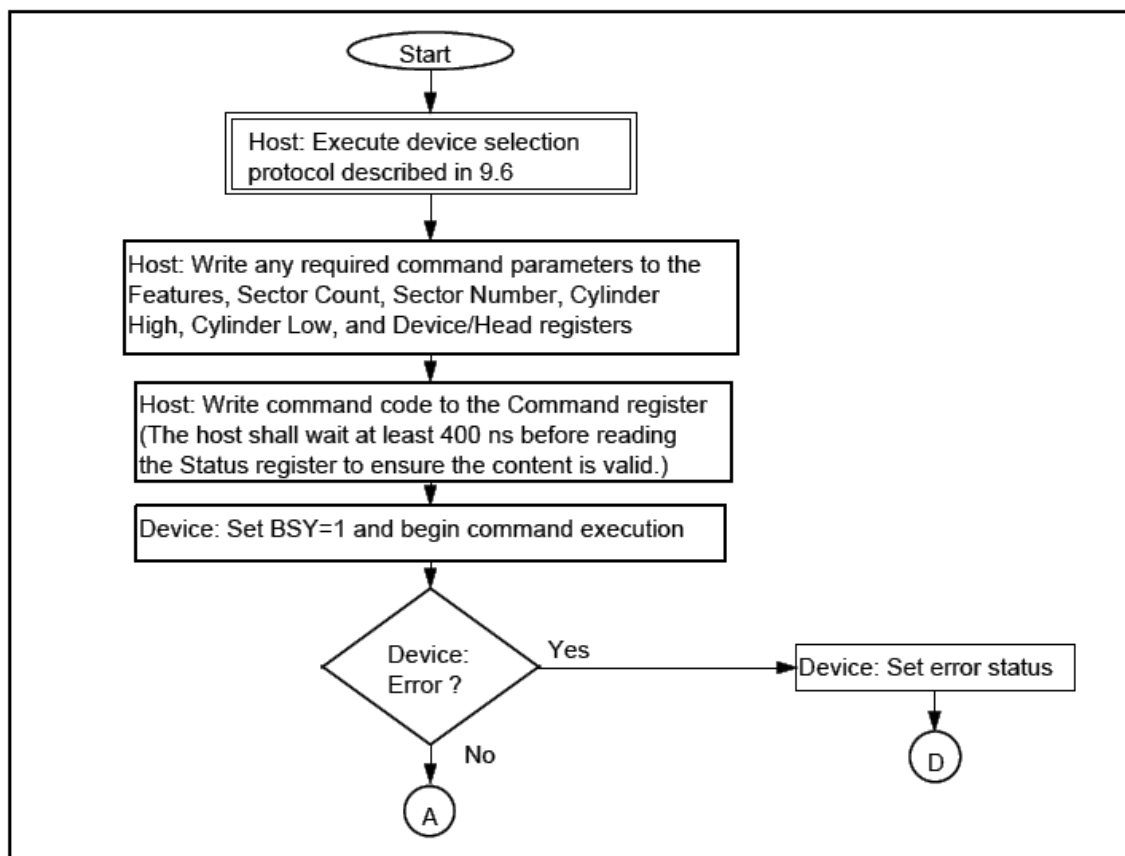


Figure 13 – PIO data out command protocol(continued)

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■ PIO data out command protocol

This class includes:

- CFA WRITE MULTIPLE WITHOUT ERASE
- CFA WRITE SECTORS WITHOUT ERASE
- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- WRITE BUFFER
- WRITE MULTIPLE
- WRITE SECTOR(S)

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 13 describes the protocol of a PIO data out command. This description does not include all possible error conditions.

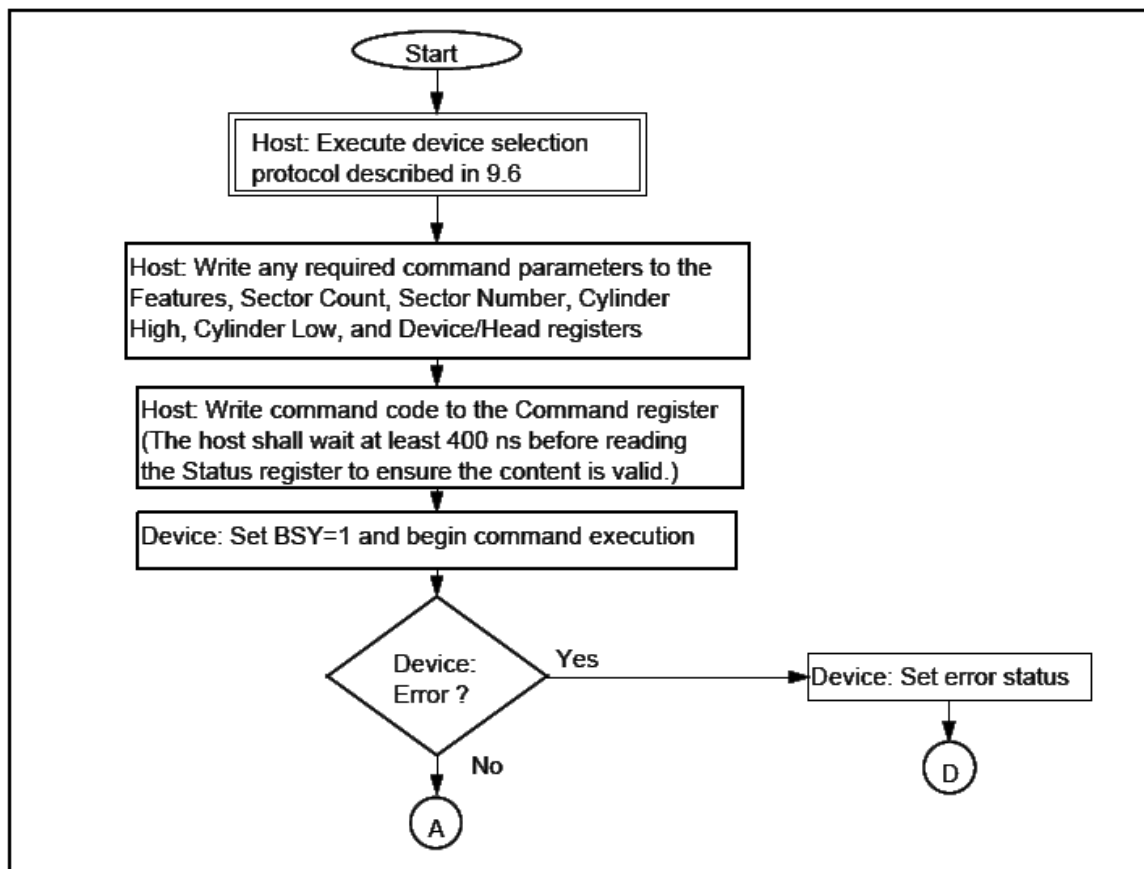


Figure 13 – PIO data out command protocol(continued)

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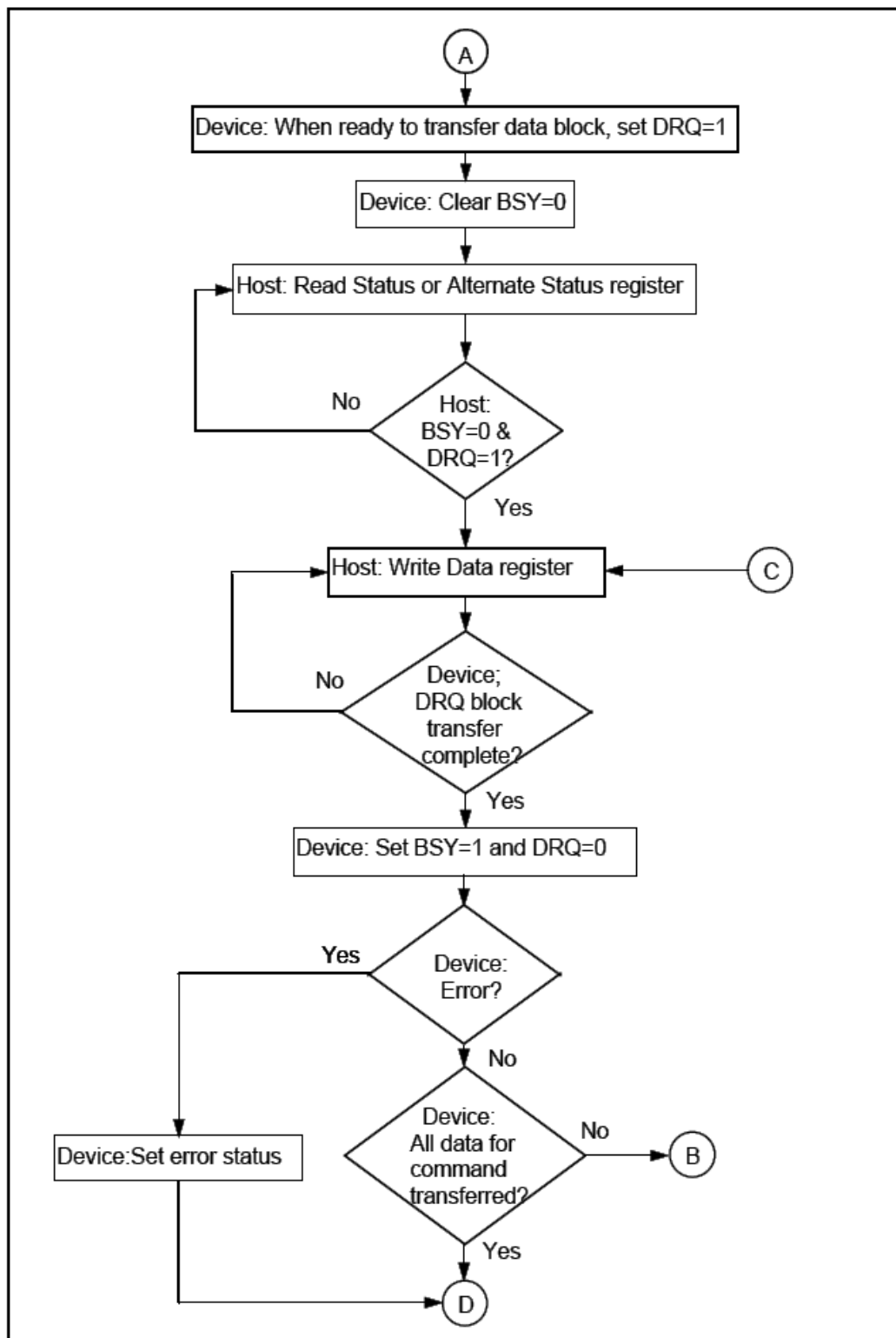


Figure 13 – PIO data out command protocol(continued)

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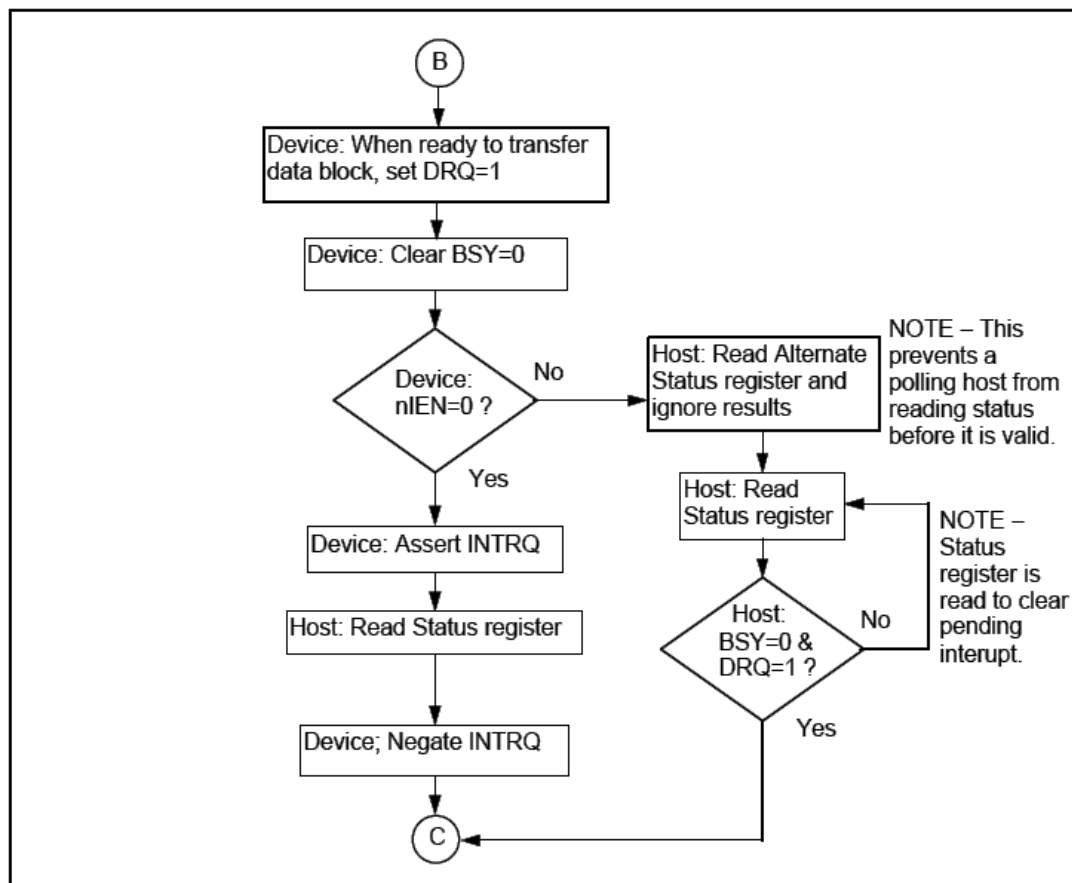


Figure 13 – PIO data out command protocol(continued)

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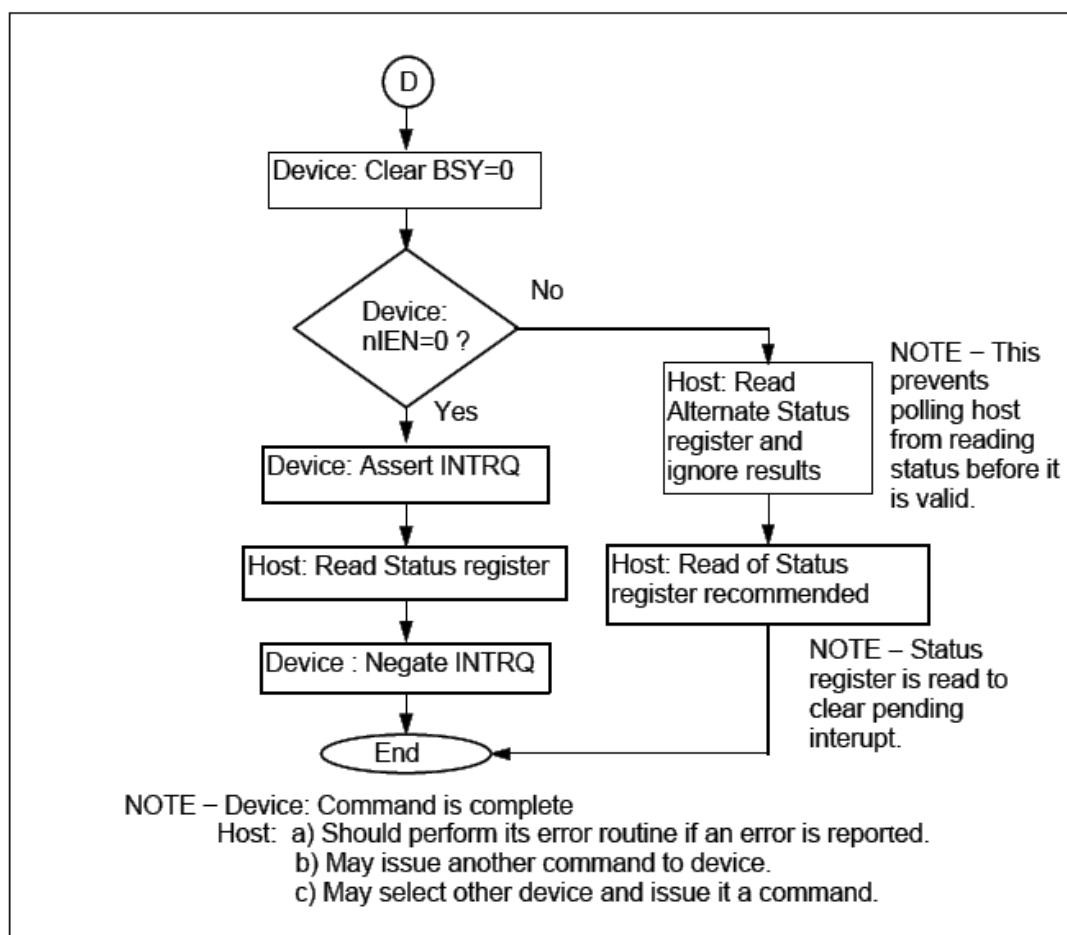


Figure 13 – PIO data out command protocol*(concluded)*

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■ PIO data transfers

Figure 21 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO mode 3 or 4 shall power up in a PIO mode 0, 1, or 2.

For PIO modes 3 and above, the minimum value of t_0 is specified by word 68 in the IDENTIFY DEVICE parameter list. Table 30 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO mode 3 or 4 are the current mode of operation.

NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO mode 3 and enable IORDY as the default.

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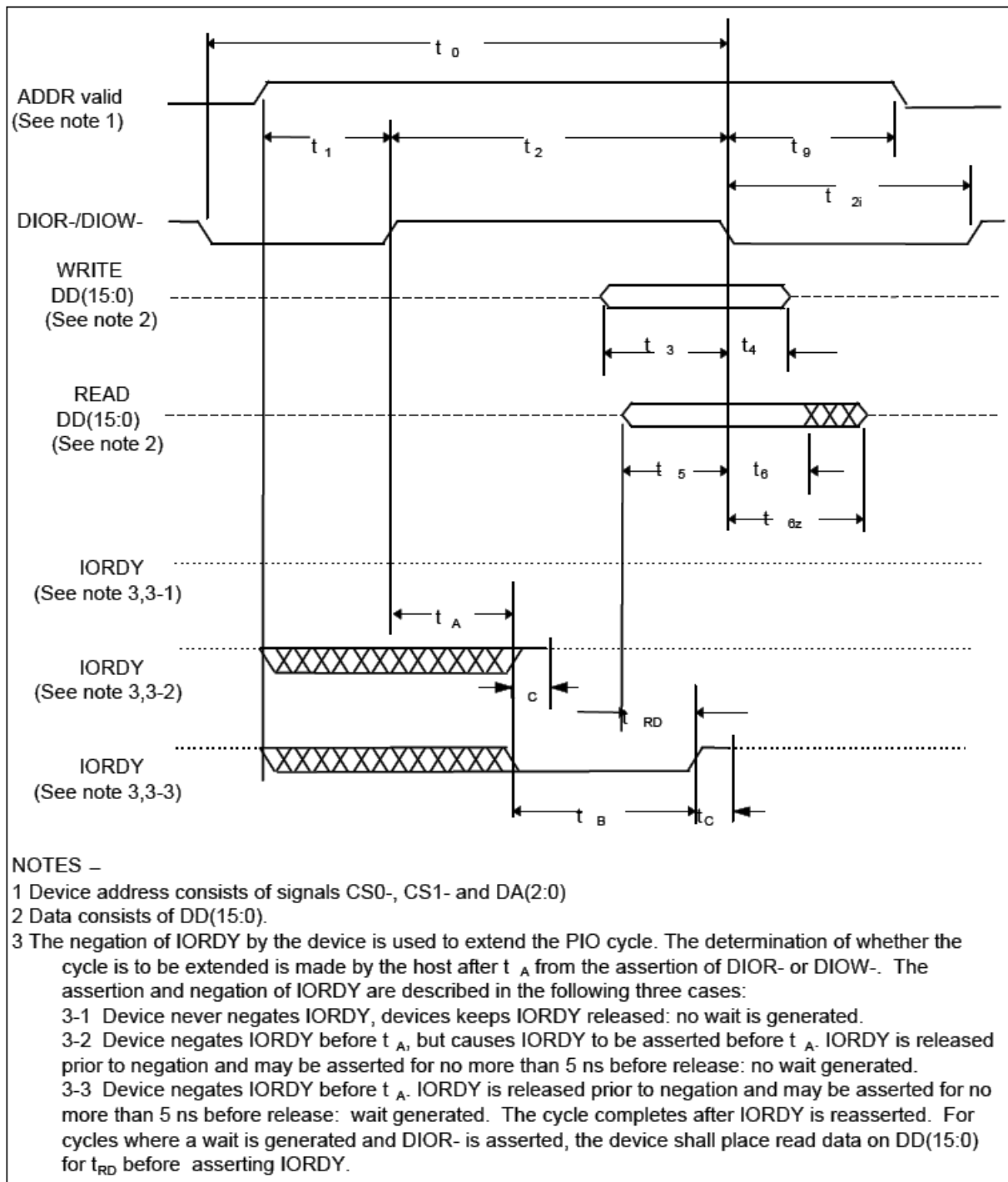


Figure 21 – PIO data transfer to/from device

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Table 30 – PIO data transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t ₀	Cycle time	(min)	600	383	240	180	120	1
t ₁	Address valid to DIOR-/DIOW-setup	(min)	70	50	30	30	25	
t ₂	DIOR-/DIOW- 16-bit	(min)	165	125	100	80	70	1
t _{2i}	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t ₃	DIOW- data setup	(min)	60	45	30	30	20	
t ₄	DIOW- data hold	(min)	30	20	15	10	10	
t ₅	DIOR- data setup	(min)	50	35	20	20	20	
t ₆	DIOR- data hold	(min)	5	5	5	5	5	
t _{6Z}	DIOR- data tristate	(max)	30	30	30	30	30	2
t ₉	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
t _{RD}	Read Data Valid to IORDY active (if IORDY initially low after t _A)	(min)	0	0	0	0	0	
t _A	IORDY Setup time		35	35	35	35	35	3
t _B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	
t _C	IORDY assertion to release	(max)	5	5	5	5	5	
NOTES – 1 t₀ is the minimum total cycle time, t₂ is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t₀, t₂, and t_{2i} shall be met. The minimum total cycle time requirements is greater than the sum of t₂ and t_{2i}. This means a host implementation may lengthen either or both t₂ or t_{2i} to ensure that t₀ is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation. 2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state). 3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t₅ shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t₅ is not applicable.								

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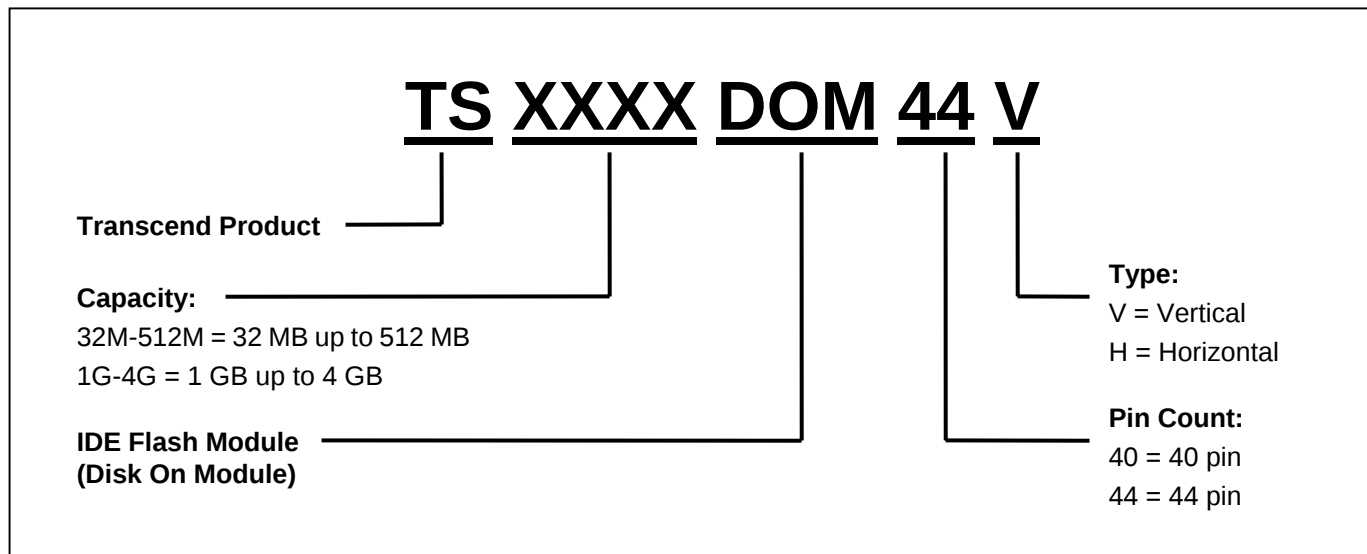
Capacity Specifications:

Transcend P/N	Capacity	Cylinder	Head	Sector
TS128MDOM44V	128MB	978	8	32
TS256MDOM44V	256MB	978	16	32
TS512MDOM44V	512MB	993	16	63
TS1GDOM44V	1GB	1985	16	63
TS2GDOM44V	2GB	3954	16	63
TS4GDOM44V	4GB	7889	16	63

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Ordering Information



The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice.

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