

MC74HC4851A, MC74HC4852A

Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

Automotive Customized

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

Features

- Injection Current Cross-Coupling Less than 1 mV/mA (See Figure 10)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- In Compliance With the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: 154 FETs or 36 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

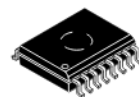


ON Semiconductor®

www.onsemi.com



SOIC-16
D SUFFIX
CASE 751B



SOIC-16 WIDE
DW SUFFIX
CASE 751G

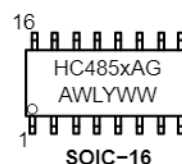


TSSOP-16
DT SUFFIX
CASE 948F

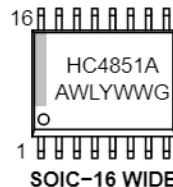


QFN16
MN SUFFIX
CASE 485AW

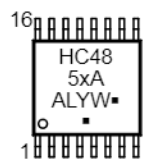
MARKING DIAGRAMS



SOIC-16



SOIC-16 WIDE



TSSOP-16



QFN16

x = 1 or 2
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

MC74HC4851A, MC74HC4852A

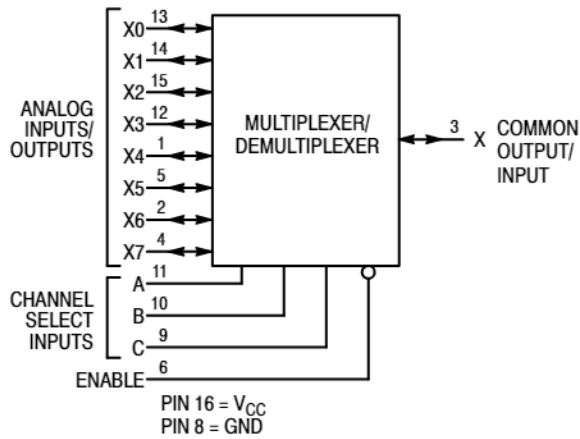


Figure 1. MC74HC4851A Logic Diagram
Single-Pole, 8-Position Plus Common Off

FUNCTION TABLE - MC74HC4851A

Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

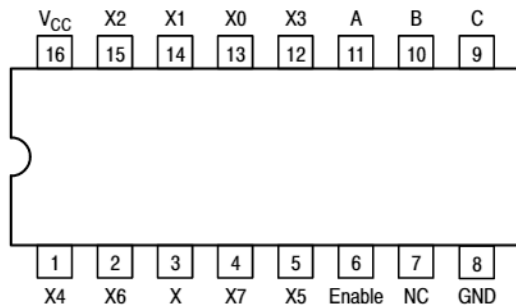


Figure 2. MC74HC4851A 16-Lead Pinout (Top View)

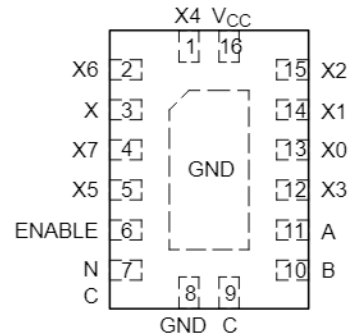


Figure 3. MC74HC4851A QFN Pinout

FUNCTION TABLE - MC74HC4852A

Control Inputs				
Enable	Select			
	B	A	ON Channels	
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

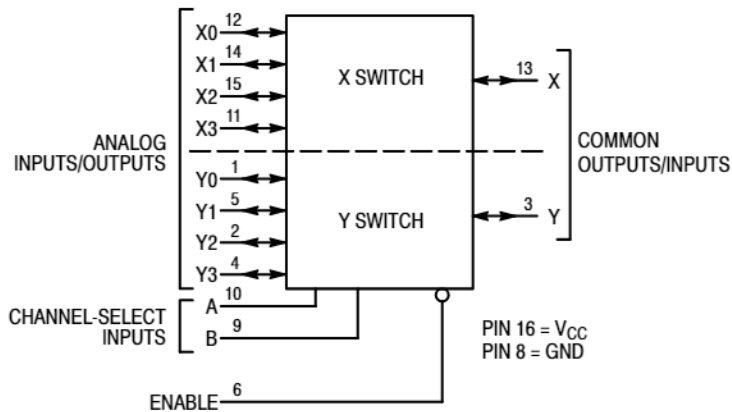


Figure 4. MC74HC4852A Logic Diagram
Double-Pole, 4-Position Plus Common Off

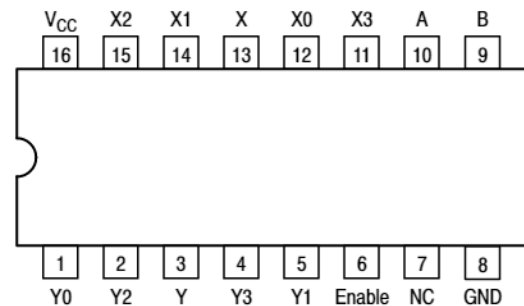


Figure 5. MC74HC4852A 16-Lead Pinout (Top View)

MC74HC4851A, MC74HC4852A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Any Pin) (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C

TSSOP Package: -6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in}	DC Input Voltage (Any Pin) (Referenced to GND)	GND	V _{CC}	V	
V _{IO} *	Static or Dynamic Voltage Across Switch	0.0	1.2	V	
T _A	Operating Temperature Range, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

*For voltage drops across switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = GND$, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{on} = \text{Per Spec}$	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
I_{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)} = V_{CC} \text{ or } GND$ $V_{in(analog)} = GND$	6.0	2	20	40	μA

MC74HC4851A, MC74HC4852A

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
R _{ON}	Maximum "ON" Resistance	V _{in} = V _{IL} or V _{IH} ; V _{IS} = V _{CC} to GND (Note 1); I _S ≤ 2.0 mA (Note 2)	2.0	1700	1750	1800	Ω
			3.0	1100	1200	1300	
			4.5	550	650	750	
			6.0	400	500	600	
ΔR _{ON}	Delta "ON" Resistance	V _{in} = V _{IL} or V _{IH} ; V _{IS} = V _{CC} /2 (Note 1); I _S ≤ 2.0 mA (Note 2)	2.0	300	400	500	Ω
			3.0	160	200	240	
			4.5	80	100	120	
			6.0	60	80	100	
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel Common Channel	V _{in} = V _{CC} or GND	6.0	±0.1 ±0.1	±0.1 ±0.1	±0.1 ±0.1	μA
I _{on}	Maximum On-Channel Leakage Channel-to-Channel	V _{in} = V _{CC} or GND	6.0	±0.1	±0.1	±0.1	μA

1. V_{IS} is the input voltage of an analog I/O pin.

2. I_S is the current flowing in or out of analog I/O pin.

AC CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC}	-55 to 25°C	≤85°C	≤125°C	Unit
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Analog Input to Analog Output	2.0	160	180	200	ns
		3.0	80	90	100	
		4.5	40	45	50	
		6.0	30	35	40	
t _{PHL} , t _{PHZ,PZH} , t _{PLH} , t _{PLZ,PZL}	Maximum Propagation Delay, Enable or Channel-Select to Analog Output	2.0	260	280	300	ns
		3.0	160	180	200	
		4.5	80	90	100	
		6.0	78	80	80	
C _{in}	Maximum Input Capacitance (All Switches Off) (All Switches Off)	Digital Pins	10	10	10	pF
		Any Single Analog Pin	35	35	35	
		Common Analog Pin	40	40	40	
C _{PD}	Power Dissipation Capacitance	Typical	5.0	20		pF

INJECTION CURRENT COUPLING SPECIFICATIONS (V_{CC} = 5V, T_A = -55°C to +125°C)

Symbol	Parameter	Condition	Typ	Max	Unit
V _{Δout}	Maximum Shift of Output Voltage of Enabled Analog Channel	I _{in} * ≤ 1 mA, R _S ≤ 3.9 kΩ	0.1	1.0	mV
		I _{in} * ≤ 10 mA, R _S ≤ 3.9 kΩ	1.0	5.0	
		I _{in} * ≤ 1 mA, R _S ≤ 20 kΩ	0.5	2.0	
		I _{in} * ≤ 10 mA, R _S ≤ 20 kΩ	5.0	20	

* I_{in} = Total current injected into all disabled channels.

MC74HC4851A, MC74HC4852A

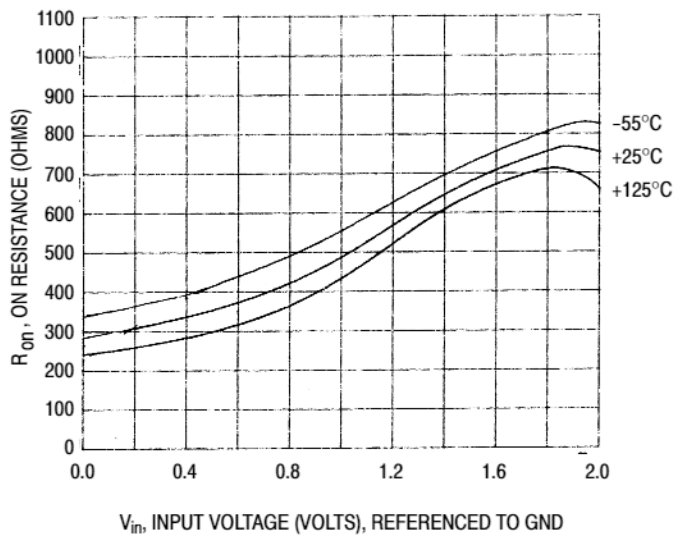


Figure 6. Typical On Resistance $V_{CC} = 2V$

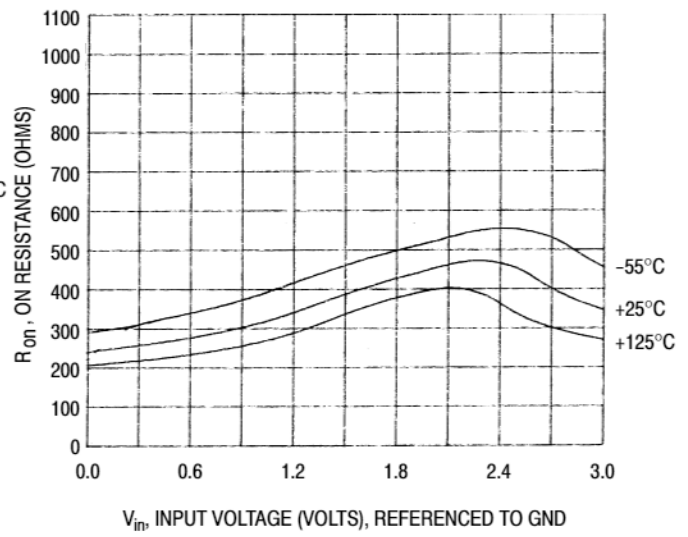


Figure 7. Typical On Resistance $V_{CC} = 3V$

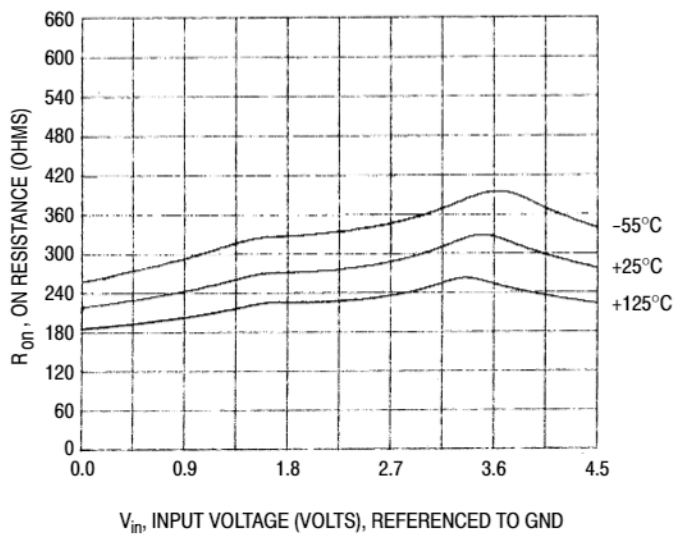


Figure 8. Typical On Resistance $V_{CC} = 4.5V$

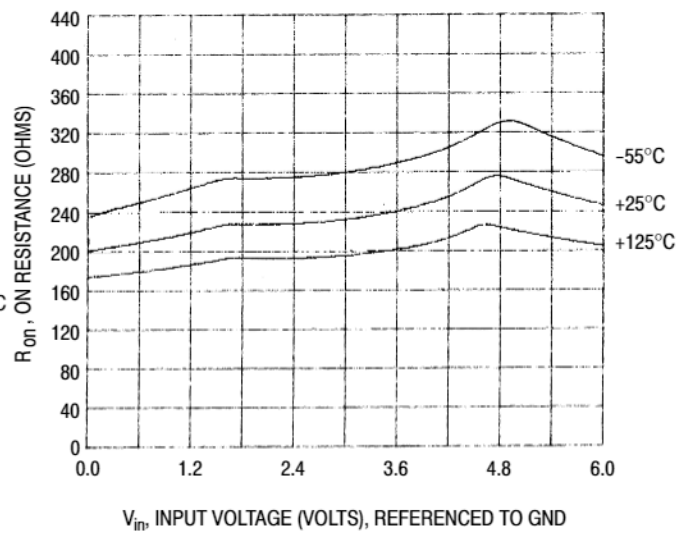


Figure 9. Typical On Resistance $V_{CC} = 6V$

MC74HC4851A, MC74HC4852A

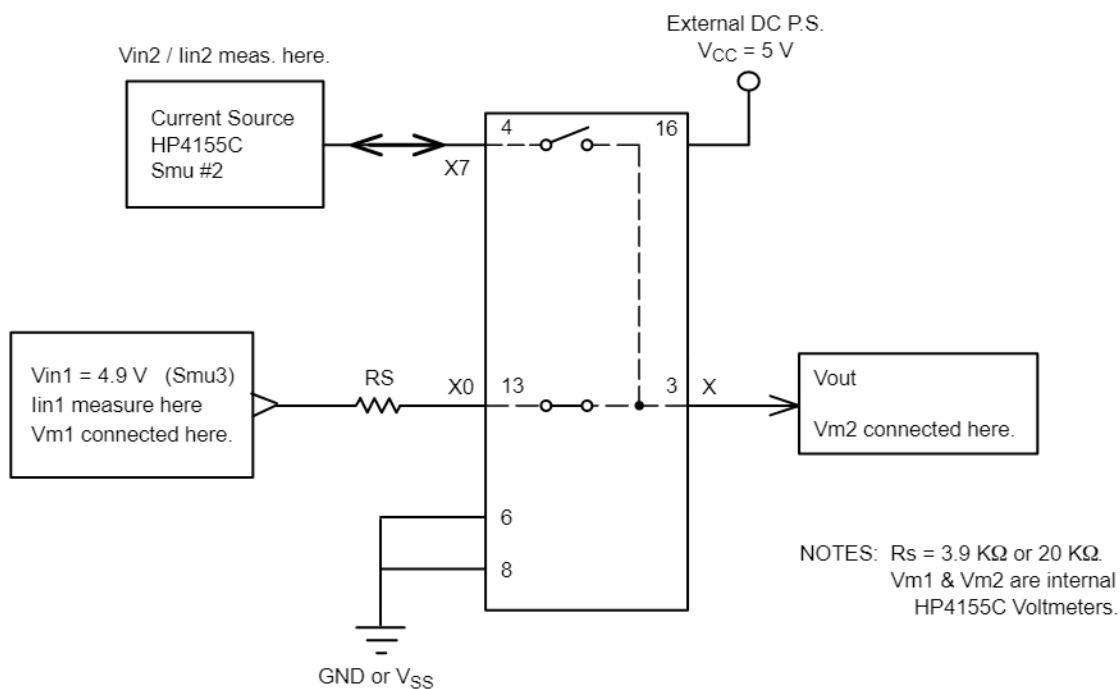


Figure 10. Injection Current Coupling Specification

MC74HC4851A, MC74HC4852A

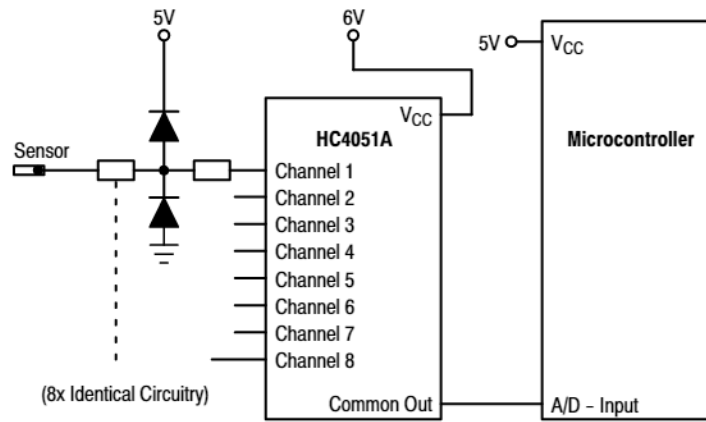


Figure 11. Actual Technology

Requires 32 passive components and one extra 6V regulator to suppress injection current into a standard HC4051 multiplexer

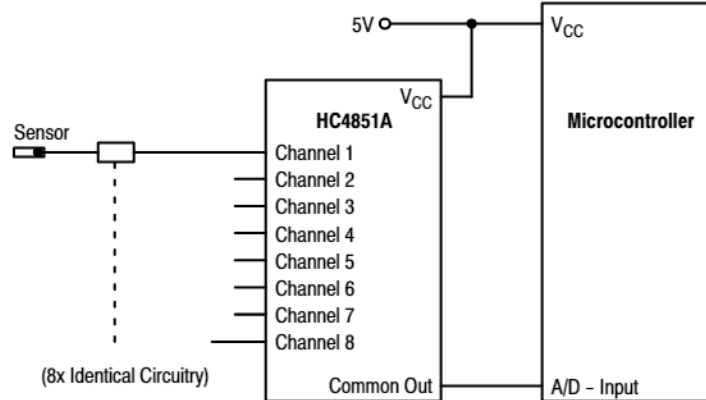


Figure 12. MC74HC4851A Solution

Solution by applying the HC4851A multiplexer

MC74HC4851A, MC74HC4852A

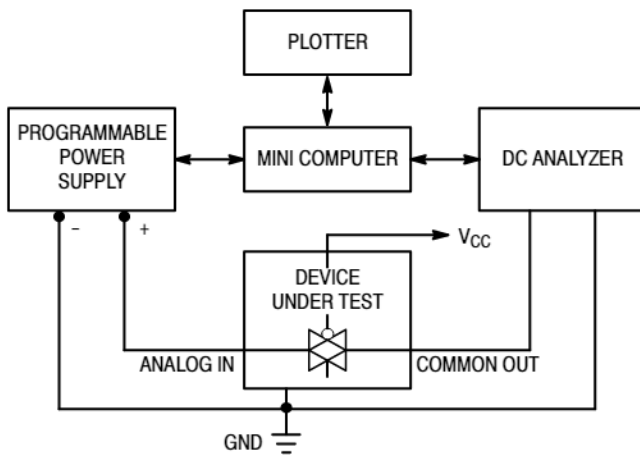


Figure 13. On Resistance Test Set-Up

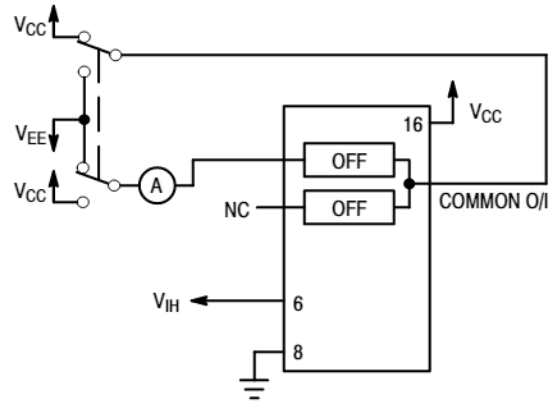


Figure 14. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

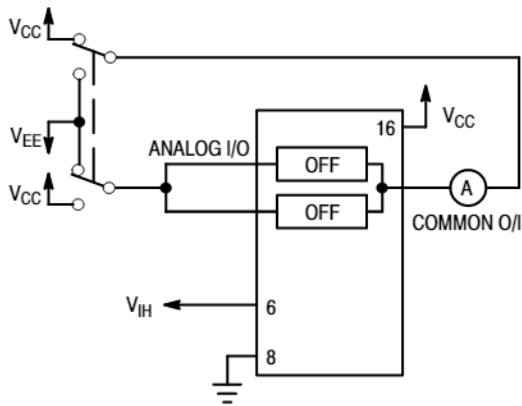


Figure 15. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

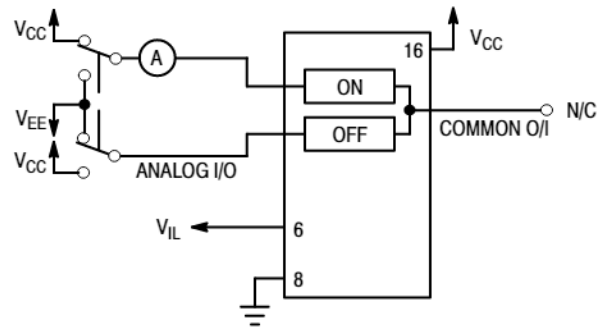


Figure 16. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

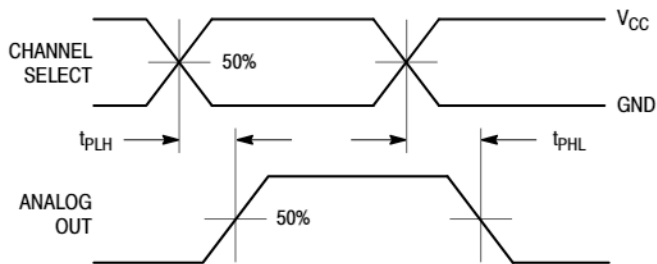
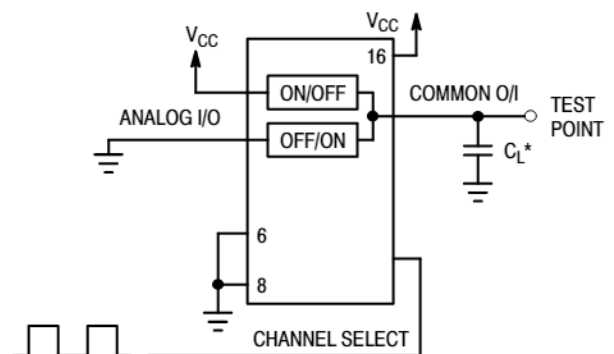


Figure 17. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 18. Propagation Delay, Test Set-Up Channel Select to Analog Out

MC74HC4851A, MC74HC4852A

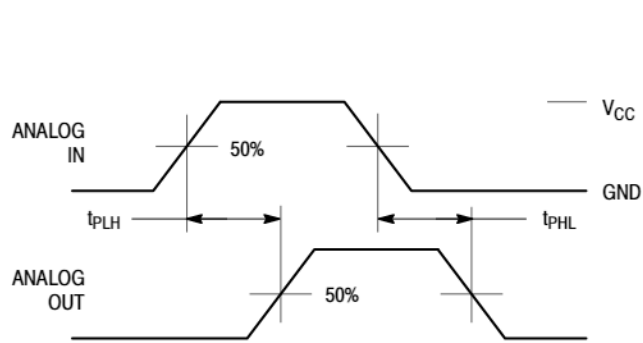
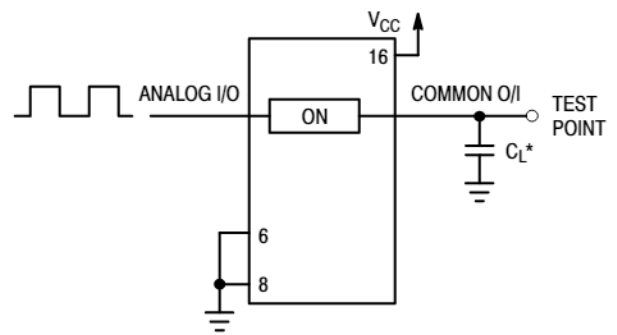


Figure 19. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 20. Propagation Delay, Test Set-Up Analog In to Analog Out

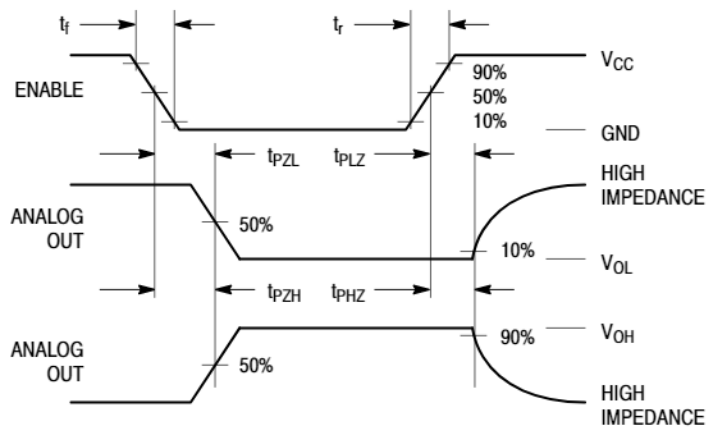


Figure 21. Propagation Delays, Enable to Analog Out

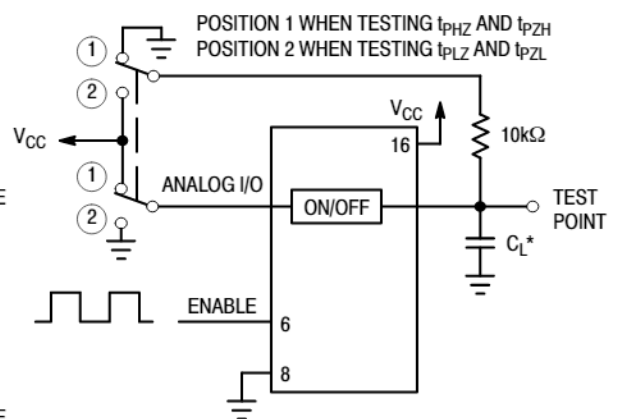


Figure 22. Propagation Delay, Test Set-Up Enable to Analog Out

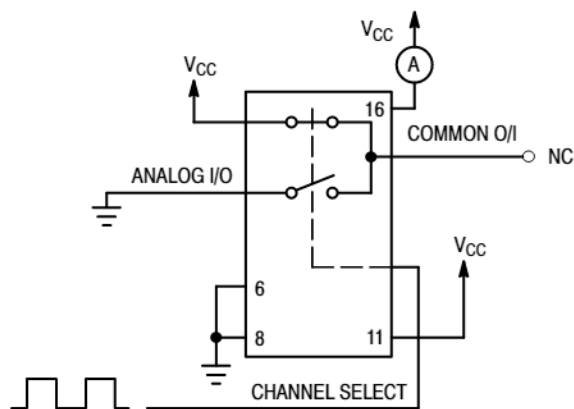


Figure 23. Power Dissipation Capacitance, Test Set-Up

MC74HC4851A, MC74HC4852A

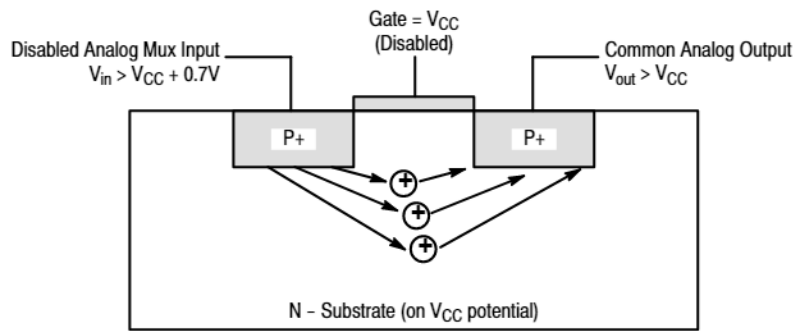


Figure 24. Diagram of Bipolar Coupling Mechanism
Appears if V_{in} exceeds V_{CC} , driving injection current into the substrate

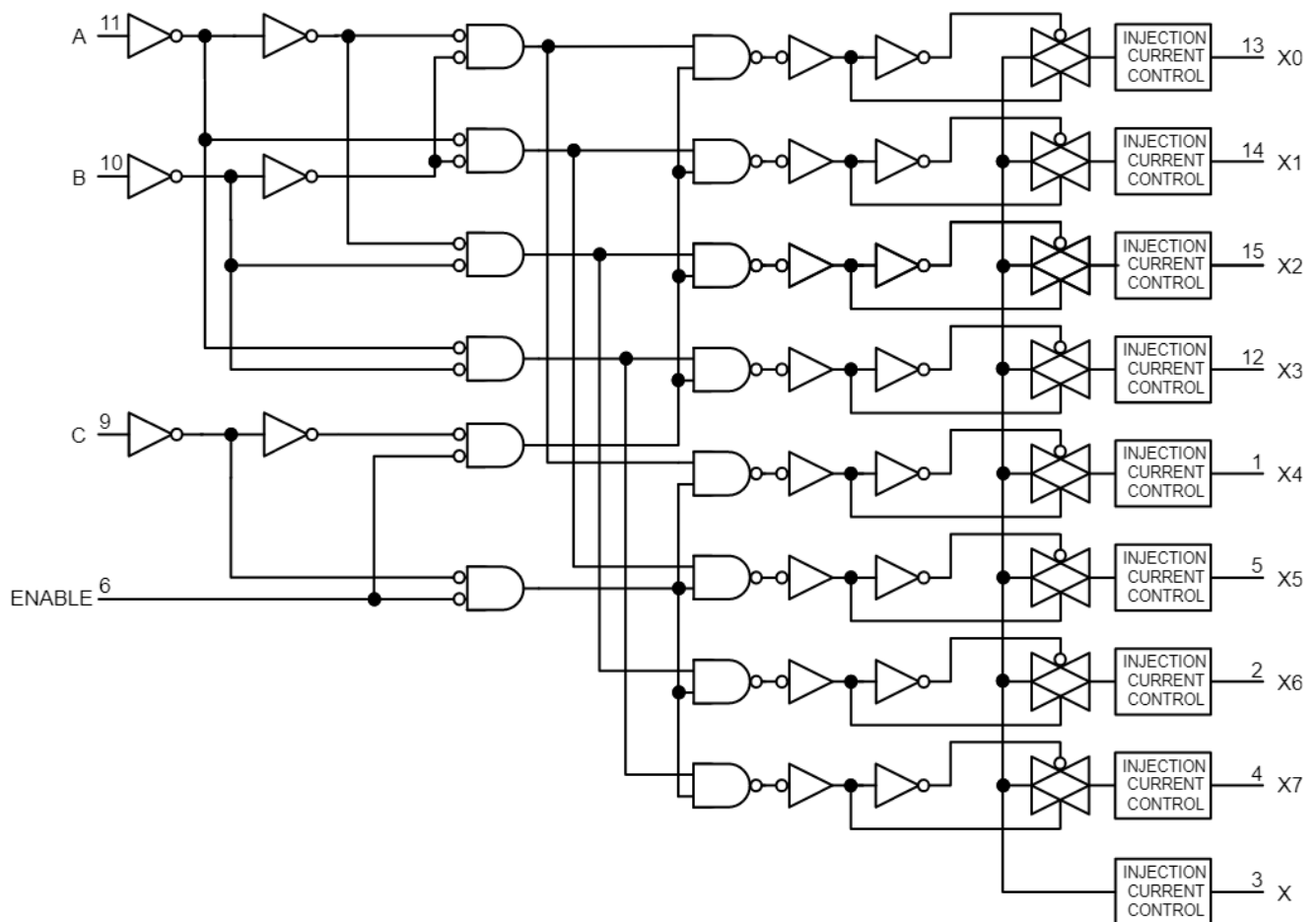


Figure 25. Function Diagram, HC4851A

MC74HC4851A, MC74HC4852A

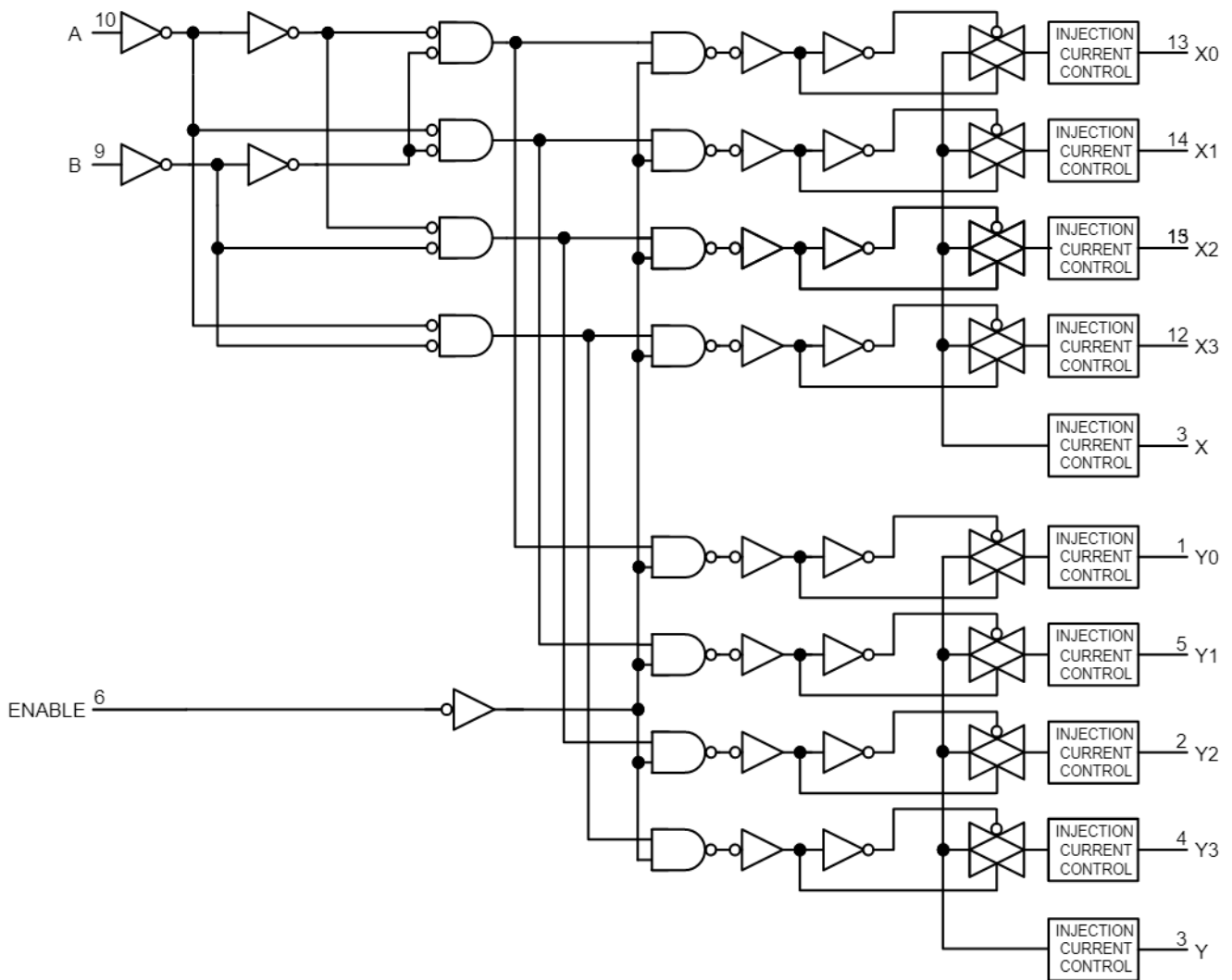


Figure 26. Function Diagram, HC4852A

MC74HC4851A, MC74HC4852A

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC4851ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4851ADR2G		2500 Units / Tape & Reel
NLVHC4851ADR2G*		2500 Units / Tape & Reel
MC74HC4851ADTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLVHC4851ADTR2G*		
MC74HC4851ADWR2G	SOIC-16 WIDE (Pb-Free)	1000 Units / Tape & Reel
NLVHC4851ADWR2G*		
NLV74HC4851AMNTWG*	QFN16 (Pb-Free)	3000 Units / Tape & Reel

MC74HC4852ADG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74HC4852ADR2G		2500 Units / Tape & Reel
NLV74HC4852ADR2G*		2500 Units / Tape & Reel
MC74HC4852ADTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLVHC4852ADTR2G*		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

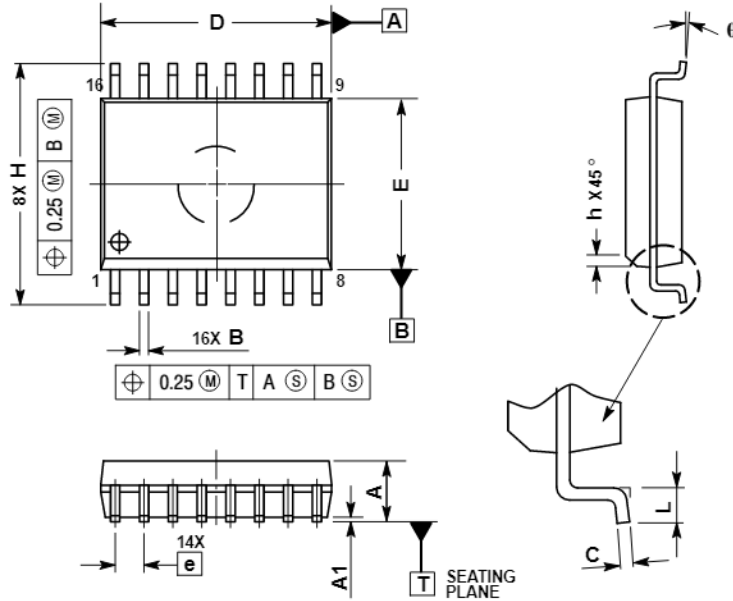
Technical drawing of a 16x0.36mm PCB layout. The drawing shows a top-down view of a rectangular board with dimensions 16x0.36mm. The layout is symmetrical about a vertical center line. The overall width is 16mm, and the overall height is 0.36mm. The layout consists of two main sections, each containing a vertical column of eight rectangular components. The components are arranged in a staggered pattern. The distance between the two columns is 7.06mm. The distance between the components in each column is 0.65mm. The components are labeled with dimensions: 16X 0.36, 7.06, 0.65 PITCH, and 1.26. The drawing is labeled "DIMENSIONS: MILLIMETERS".

13

MC74HC4851A, MC74HC4852A

PACKAGE DIMENSIONS

SOIC-16 WB
DW SUFFIX
CASE 751G-03
ISSUE D

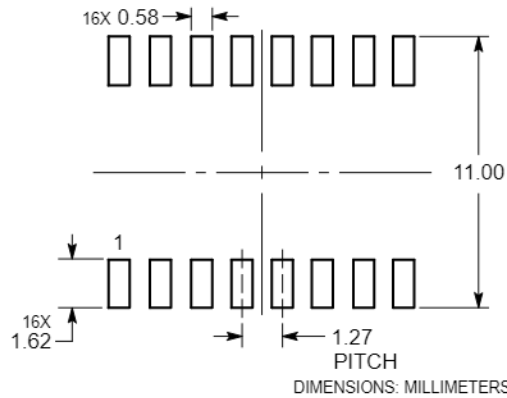


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

SOLDERING FOOTPRINT*



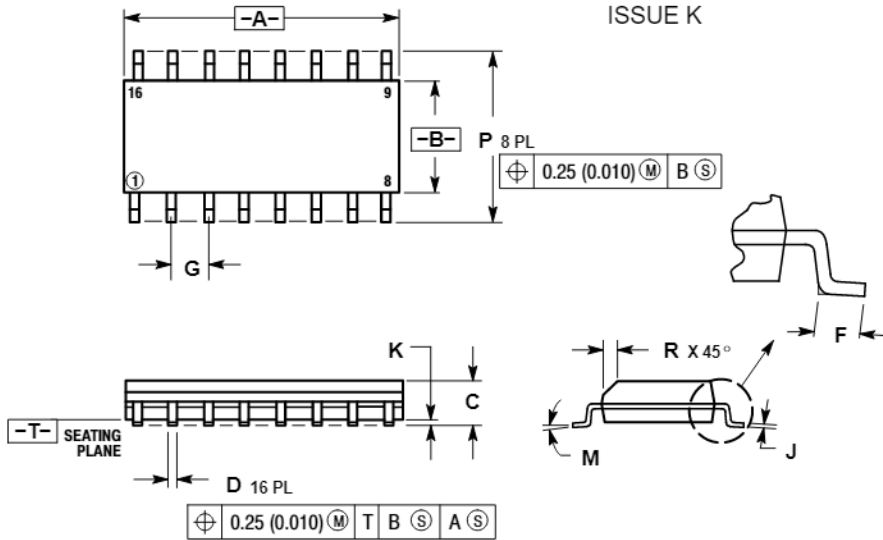
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC4851A, MC74HC4852A

PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE K

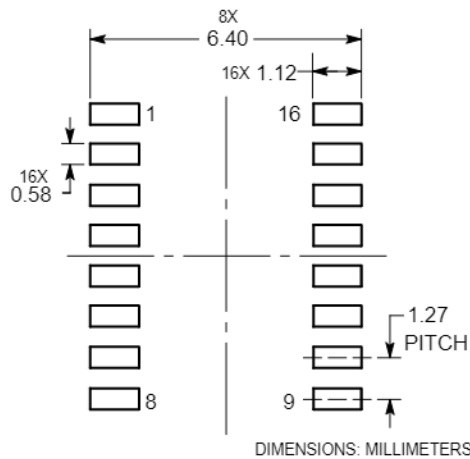


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27 BSC		0.050 BSC	
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.229	0.244
K	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

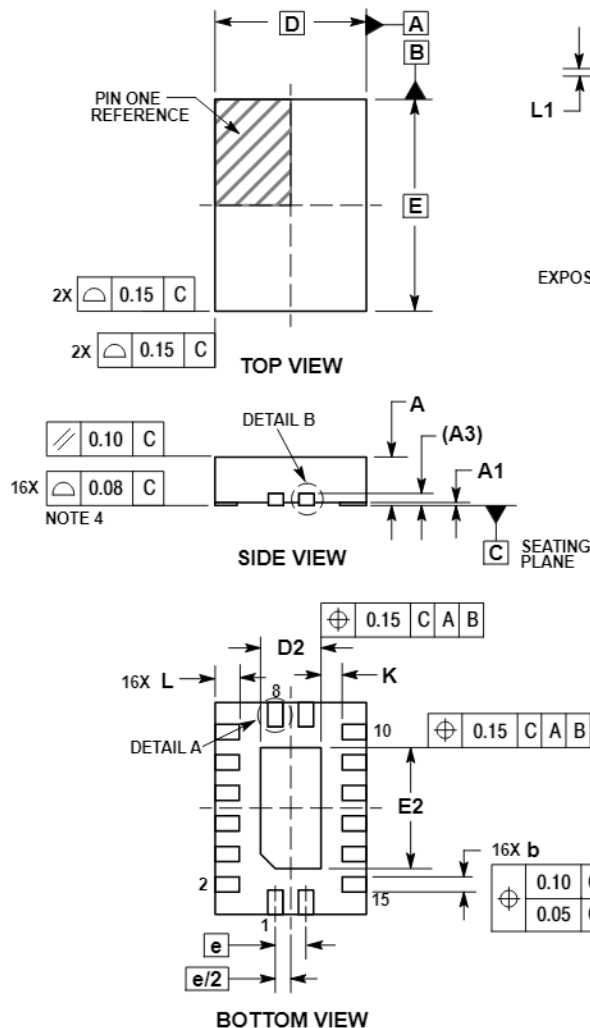


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HC4851A, MC74HC4852A

PACKAGE DIMENSIONS

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

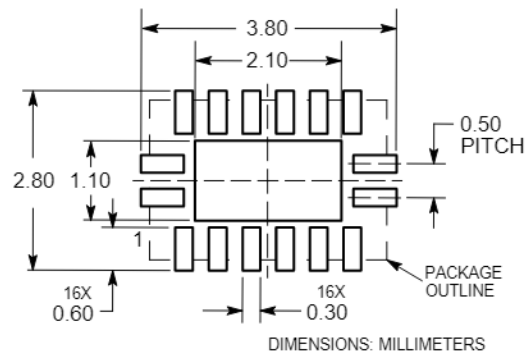


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.50	BSC
D2	0.85	1.15
E	3.50	BSC
E2	1.85	2.15
e	0.50	BSC
K	0.20	---
L	0.35	0.45
L1	---	0.15

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

MC74HC4851A/D