CYNSE70064A Network Search Engine

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1.0 Features

- **64K 34-bit entries in a single device**
- **32K entries in 68-bit mode, 16K entries in 136-bit mode, 8K entries in 272-bit mode**
- **83 million transactions per second in 68- and 136-bit configurations**
- **41.5 million transactions in 34- and 272-bit configurations**
- **Searches any subfield in a single cycle**
- **Synchronous pipelined operation**
- **Up to 31 search engines can be cascaded**
- **When cascaded, the database entries can range up to 1984K 34-bit entries**
- **Multiple width tables in a single database bank**
- **Glueless interface to industry-standard SRAMs and/or SSRAMs**
- **Simple hardware instruction interface**
- **IEEE 1149.1 test access port**
- **1.8V core voltage supply**
- **2.5/3.3V I/O voltage supply**
- **272-pin BGA package**.

2.0 Functional Overview

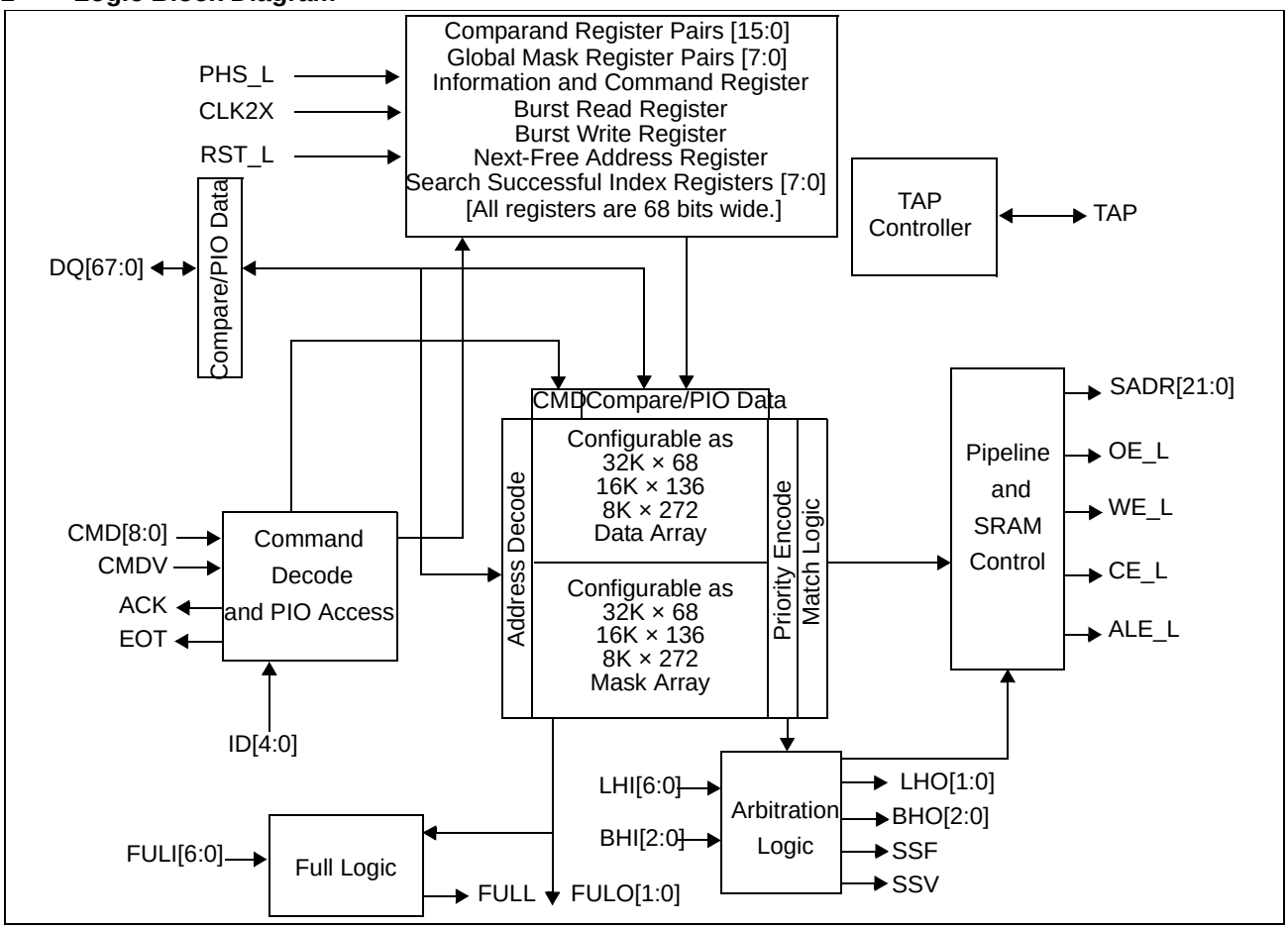
Cypress Semiconductor Corporation's (Cypress's) CYNSE70064A network search engine (NSE) incorporates patent-pending Associative Processing Technology™ (APT) and is designed to be a high-performance, pipelined, synchronous, 32K-entry NSE. The CYNSE70064A database entry size can be 68 bits, 136 bits, or 272 bits. In the 68-bit entry mode, the size of the database is 32K entries. In the 136-bit mode, the size of the database is 16K entries, and in the 272-bit mode, the size of the database is 8K entries. The CYNSE70064A is configurable to support multiple databases with different entry sizes. The 34-bit entry table can be implemented using the global mask registers (GMRs) building-database size of 64K entries with a single device.

The NSE can sustain 83 million transactions per second when the database is programmed or configured as 68 or 136 bits. When the database is programmed to have an entry size of 34 or 272 bits, the NSE will perform at 41.5 million transactions per second. The CYNSE70064A device can be used to accelerate network protocols such as longest-prefix match (CIDR), ARP, MPLS, and other layer 2, 3, and 4 protocols.

This high-speed, high-capacity NSE can be deployed in a variety of networking and communications applications. The performance and features of the CYNSE70064A make it attractive in applications such as Enterprise LAN switches and routers and broadband switching and/or routing equipment supporting multiple data rates at OC-48 and beyond. The NSE is designed to be scalable in order to support network database sizes to 1984K entries specifically for environments that require large network policy databases.

3.0 Product Summary

3.1 Logic Block Diagram



4.0 Functional Description

The following subsections contain command (CMD) and DQ bus (command and databus), database entry, arbitration logic, pipeline and SRAM control, and full logic descriptions.

4.1 CMD Bus and DQ Bus

CMD[8:0] carries the CMD and its associated parameter. DQ[67:0] is used for data transfer to and from the database entries, which comprise a data and a mask field that are organized as data and mask arrays. The DQ bus carries the Search data (of the data and mask arrays and internal registers) during the Search command as well as the address and data during Read and/or Write operations. The DQ bus can also carry the address information for the flow-through accesses to the external SRAMs and/or SSRAMs.

4.2 Database Entry (Data Array and Mask Array)

Each database entry comprises a data and a mask field. The resultant value of the entry is “1,” “0,” or “X (don’t care),” depending on the value in the data and mask bits. The on-chip priority encoder selects the first matching entry in the database that is nearest to location 0.

4.3 Arbitration Logic

When multiple search engines are cascaded to create large databases, the data being searched is presented to all search engines simultaneously in the cascaded system. If multiple matches occur within the cascaded devices, arbitration logic on the search engines will enable the winning device (with a matching entry that is closest to address 0 of the cascaded database) to drive the SRAM bus.

4.4 Pipeline and SRAM Control

Pipeline latency is added to give enough time to a cascaded system's arbitration logic to determine the device that will drive the index of the matching entry on the SRAM bus. Pipeline logic adds latency to both the SRAM access cycles and the SSF and SSV signals to align them to the host ASIC receiving the associated data.

4.5 Full Logic

Bit[0] in each of the 68-bit entries has a special purpose for the Learn command (0 = empty, 1 = full). When all the data entries have bit[0] = 1, the database asserts the FULL flag, indicating that all the search engines in the depth-cascaded array are full.

5.0 Signal Descriptions

Table 5-1 lists and describes all CYNSE70064A signals.

Table 5-1. CYNSE70064A Signal Description

Symbol	Type[1]	Description
Clocks and Reset		
CLK2X	I	***Master Clock***. CYNSE70064A samples all the data and control pins on the positive edge of CLK2X. All signals are driven out of the device on the rising edge of CLK2X (when PHS_L is LOW).
PHS_L	I	***Phase***. This signal runs at half the frequency of CLK2X and generates an internal CLK[2] from CLK2X. See Section 6.0, "Clocks" on page 13.
RST_L	I	***Reset***. Driving RST_L LOW initializes the device to a known state.
CMD and DQ Bus		
CMD[8:0]	I	***CMD Bus***. [1:0] specifies the command and [8:2] contains the CMD parameters. The descriptions of individual commands explains the details of the parameters. The encoding of commands based on the [1:0] field are: 00: PIO Read 01: PIO Write 10: Search 11: Learn.
CMDV	I	***CMD Valid***. This signal qualifies the CMD bus: 0: No command 1: Command.
DQ[67:0]	I/O	***Address/Data Bus***. This signal carries the Read and Write address and data during register, data, and mask array operations. It carries the compare data during Search operations. It also carries the SRAM address during SRAM PIO accesses.
ACK[3]	T	***Read Acknowledge***. This signal indicates that valid data is available on the DQ bus during register, data, and mask array Read operations, or that the data is available on the SRAM data bus during SRAM Read operations.
EOT[3]	T	***End of Transfer***. This signal indicates the end of burst transfer to the data or mask array during Read or Write burst operations.
SSF	T	***Search Successful Flag***. When asserted, this signal indicates that the device is the global winner in a Search operation.
SSV	T	***Search Successful Flag Valid***. When asserted, this signal qualifies the SSF signal.
SRAM Interface		
SADR[21:0]	T	***SRAM Address***. This bus contains address lines to access off-chip SRAMs that contain associative data. See *Table 12-1* for the details of the generated SRAM address. In a database of multiple CYNSE70064As, each corresponding bit of SADR from all cascaded devices must be connected.
CE_L	T	***SRAM Chip Enable***. This is the chip-enable control for external SRAMs. In a database of multiple CYNSE70064As, CE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.

Notes:

1. I = Input only, I/O = Input or Output, O = Output only, T = three-state output.
2. CLK" is an internal clock signal. Any reference to "CLK cycles" means one cycle of CLK.
3. ACK and EOT require a weak external pull-down such as 47KΩ or 100KΩ.

Table 5-1. CYNSE70064A Signal Description (continued)

Symbol	Type[1]	Description
WE_L	T	***SRAM Write Enable***. This is the Write-enable control for external SRAMs. In a database of multiple CYNSE70064As, WE_L of all cascaded devices must be connected together. This signal is then driven by only one of the devices.
OE_L	T	***SRAM Output Enable***. This is the output-enable control for external SRAMs. Only the last device drives this signal (with the LRAM bit set).
ALE_L	T	***Address Latch Enable***. When this signal is LOW, the addresses are valid on the SRAM address bus. In a database of multiple CYNSE70064As, the ALE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.
Cascade Interface		
LHI[6:0]	I	***Local Hit In***. These pins depth-cascade the device to form a larger table. One signal of this bus is connected to the LHO[1] or LHO[0] of each of the upstream devices in a block. All unused LHI pins are connected to a logic 0. (For more information, see Section 11.0, “Depth-Cascading” on page 97.)
LHO[1:0]	O	***Local Hit Out***. LHO[1] and LHO[0] are the same logical signal. Either the LHO[1] or the LHO[0] is connected to one input of the LHI bus of up to four downstream devices in a block of up to eight. (For more information see Section 11.0, “Depth-Cascading” on page 97.)
BHI[2:0]	I	***Block Hit In***. Inputs from the previous block BHO[2:0] are tied to BHI[2:0] of the current device. In a four-block system, the last block can contain only seven devices because the identification code 11111 is used for broadcast access.
BHO[2:0]	O	***Block Hit Out***. These outputs from the last device in a block are connected to the BHI[2:0] inputs of the devices in the downstream blocks.
FULI[6:0]	I	***Full In***. Each signal in this bus is connected to FULO[0] or FULO[1] of an upstream device to generate the FULL flag for the depth-cascaded block.
FULO[1:0]	O	***Full Out***. FULO[1] and FULO[0] are the same logical signal. One of these two signals must be connected to the FULI of up to four downstream devices in a depth-cascaded table. Bit [0] in the data array indicates whether the entry is full (1) or empty (0).This signal is asserted if all bits in the data array are ones. (Refer to Section 11.0, “Depth-Cascading” on page 97, for information on how to generate the FULL flag.)
FULL	O	***Full Flag***. When asserted, this signal indicates that the table of multiple depth-cascaded devices is full.
Device Identification		
ID[4:0]	I	***Device Identification***. The binary-encoded device identification for a depth-cascaded system starts at 00000 and goes up to 11110. 11111 is reserved for a special broadcast address that selects all cascaded search engines in the system. On a broadcast Read-only, the device with the LDEV bit set to 1 responds.
Supplies		
V_{DD}	n/a	***Chip Core Supply***. 1.8V.
V_{DDQ}	n/a	***Chip I/O supply***. 2.5V or 3.3V.
Test Access Port		
TDI	I	Test access port’s test data in.
TCK	I	Test access port’s test clock.
TDO	T	Test access port’s test data out.
TMS	I	Test access port’s Test Mode Select.
TRST_L	I	Test access port’s Reset.

6.0 Clocks

CYNSE70064A receives the CLK2X and PHS_L signals. It uses the PHS_L signal to divide CLK2X and generate an internal CLK, as shown in *Figure 6-1*. The CYNSE70064A uses CLK2X and CLK for internal operations.

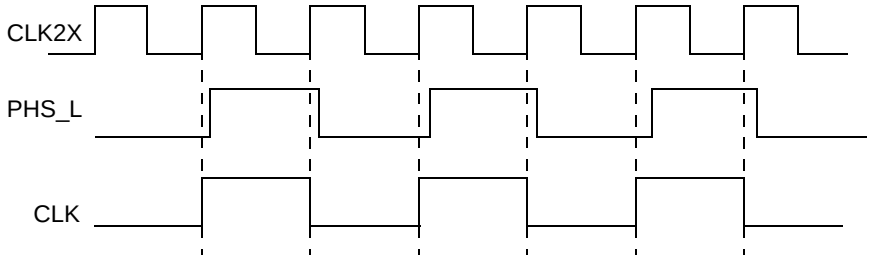


Figure 6-1. CYNSE70064A Clocks (CLK2X and PHS_L)

7.0 Registers

All registers in the CYNSE70064A are 68 bits wide. The CYNSE70064A contains 16 pairs of comparand storage registers, eight pairs of GMRs, eight search successful index registers and one each of CMD, information, burst Read, burst Write, and next-free address registers. *Table 7-1* provides an overview of all the CYNSE70064A registers. The registers are ordered in ascending address order. Each register group is then described in the following subsections.

Table 7-1. Register Overview

Address	Abbreviation	Type	Name
0–31	COMP0–31	R	Sixteen pairs of comparand registers that store comparands from the DQ bus for learning later.
32–47	MASKS	RW	Eight global mask register pairs.
48–55	SSR0–7	R	Eight search successful index registers.
56	COMMAND	RW	Command register.
57	INFO	R	Information register.
58	RBURREG	RW	Burst Read register.
59	WBURREG	RW	Burst Write register.
60	NFA	R	Next-free address register.
61–63	–	–	Reserved.

7.1 Comparand Registers

The device contains 32 68-bit comparand registers (16 pairs) dynamically selected in every Search operation to store the comparand presented on the DQ bus. The Learn command will later use these registers when executed. The CYNSE70064A stores the Search command's cycle A comparand in the even-numbered register and the cycle B comparand in the odd-numbered register, as shown in *Figure 7-1*.

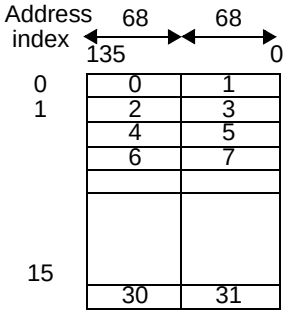


Figure 7-1. Comparand-Register Selection During Search and Learn Instructions

7.2 Mask Registers

The device contains 16 68-bit global mask registers (eight pairs) dynamically selected in every Search operation to select the Search subfield. The addressing of these registers is explained in *Figure 7-2*. The three-bit GMR Index supplied on the command (CMD) bus can apply eight pairs of global masks during the Search and Write operations, as shown below. ***Note***. In 68-bit Search and Write operations, the host ASIC must program both the even and odd mask registers with the same values.

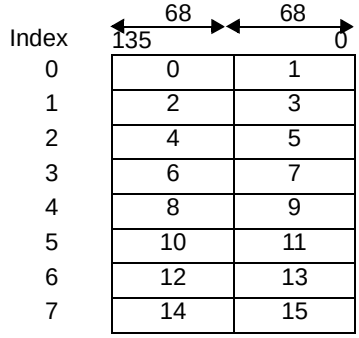


Figure 7-2. Addressing the Global Masks Register Array

Each mask bit in the GMRs is used during Search and Write operations. In Search operations, setting the mask bit to 1 enables compares; setting the mask bit to 0 disables compares (forced match) at the corresponding bit position. In Write operations to the data or mask array, setting the mask bit to 1 enables Writes; setting the mask bit to 0 disables Writes at the corresponding bit position.

7.3 Search Successful Registers (SSR[0:7])

The device contains eight search successful registers (SSRs) to hold the index of the location where a successful Search occurred. The format of each register is described in *Table 7-2*. The Search command specifies which SSR stores the index of a specific Search command in cycle B of the Search instruction. Subsequently, the host ASIC can use this register to access that data array, mask array, or external SRAM using the index as part of the indirect access address (see *Table 10-4* and *Table 10-7*). The device with a valid bit set performs a Read or Write operation. All other devices suppress the operation.

Table 7-2. Search Successful Register Description

Field	Range	Initial Value	Description
INDEX	[14:0]	X	***Index***. This is the address of the 68-bit entry where a successful Search occurs. The device updates this field only when the Search is successful. If a hit occurs in a 136-bit entry-size quadrant, the LSB is 0. If a hit occurs in a 272-bit entry-size quadrant, the two LSBs are 00. This index updates if the device is either a local or global winner in a Search operation.
–	[30:15]	0	***Reserved***.
VALID	[31]	0	***Valid***. During Search operation in a depth-cascaded configuration, the device that is a global winner in a match sets this bit to 1. This bit updates only when the device is a global winner in a Search operation.
–	[67:32]	0	***Reserved***.

7.4 Command Register

Table 7-3 describes the command register fields.

Table 7-3. Command Register Description

Field	Range	Initial Value	Description
SRST	[0]	0	***Software Reset***. If 1, this bit resets the device with the same effect as a hardware reset. Internally, it generates a reset pulse lasting for eight CLK cycles. This bit automatically resets to a 0 after the reset has completed.
DEVE	[1]	0	***Device Enable***. If 0, it keeps the SRAM bus (SADR, WE_L, CE_L, OE_L, and ALE_L), SSF, and SSV signals in three-state condition and forces the cascade interface output signals LHO[1:0] and BHO[2:0] to 0. It also keeps the DQ bus in input mode. The purpose of this bit is to make sure that there are no bus contentions when the devices power up in the system.

Table 7-3. Command Register Description (continued)

Field	Range	Initial Value	Description
TLSZ	[3:2]	01	***Table Size***. The host ASIC must program this field to configure the chips into a table of a certain size. This field affects the pipeline latency of the Search and Learn operations as well as the Read and Write accesses to the SRAM (SADR[21:0], CE_L, OE_L, WE_L, ALE_L, SSV, SSF, and ACK). Once programmed, the Search latency stays constant. Latency in number of CLK cycles 00: One device 4 01: Up to eight devices 5 10: Up to 31 devices 6 11: Reserved.
HLAT	[6:4]	000	***Latency of Hit Signals***. This field further adds latency to the SSF and SSV signals during Search, and ACK signal during SRAM Read access by the following number of CLK cycles. 000: 0 100: 4 001: 1 101: 5 010: 2 110: 6 011: 3 111: 7
LDEV	[7]	0	***Last Device in the Cascade***. When set, this is the last device in the depth-cascaded table and is the default driver for the SSF and SSV signals. In the event of a Search failure, the device with this bit set drives the hit signals as follows: SSF = 0, SSV = 1. During nonSearch cycles, the device with this bit set drives the signals as follows: SSF = 0, SSV = 0.
LRAM	[8]	0	***Last Device on the SRAM Bus***. When set, this device is the last device on the SRAM bus in the depth-cascaded table and is the default driver for the SADR, CE_L, WE_L, and ALE_L signals. In cycles where no CYNSE70064A device in a depth-cascaded table drives these signals, this devices drives the signals as follows: SADR = 22'h3FFFFF, CE_L = 1, WE_L = 1, and ALE_L = 1. OE_L is always driven by the device for which this bit is set.
CFG	[16:9]	00000000	***Database Configuration***. The device is divided internally into four partitions of 8K × 68, each of which can be configured as 8K × 68, 4K × 136, or 2K × 272, as follows. 00: 8K × 68 01: 4K × 136 10: 2K × 272 11: Reserved Bits [10:9] apply to configuring the first partition in the address space. Bits [12:11] apply to configuring the second partition in the address space. Bits [14:13] apply to configuring the third partition in the address space. Bits [16:15] apply to configuring the fourth partition in the address space.
	[67:17]	0	***Reserved***.

7.5 Information Register

Table 7-4 describes the information register fields.

Table 7-4. Information Register Description

Field	Range	Initial Value	Description
Revision	[3:0]	000[4]	***Revision Number***. This is the current device revision number. Numbers start at one and increment by one for each revision of the device.
Implementation	[6:4]	000 or 001	This is the CYNSE70064A implementation number.
Reserved	[7]	0	***Reserved***.
Device ID	[11:8]	0001 or 0010	This is the device identification number.
Device ID	[12]	0 or 1	***Reserved***.
Device ID	[15:13]	000	These are the three MSBs of the device identification number.
MFID	[31:16]	1101_1100_0111_1111	***Manufacturer ID***. This field is the same as the manufacturer identification number and continuation bits in the TAP controller.
Reserved	[67:32]		***Reserved***.

Note:
4. This field may change in future versions.

7.6 Read Burst Address Register

Table 7-5 shows the Read burst address register (RBURREG) fields which must be programmed before a burst Read.

Table 7-5. Read Burst Register Description

Field	Range	Initial Value	Description
ADR	[14:0]	0	***Address***. This is the starting address of the data or mask array during a burst Read operation. It automatically increments by one for each successive Read of the data or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:15]		***Reserved***.
BLEN	[27:19]	0	***Length of Burst Access***. The device provides the capability to read from 4–511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[67:28]		***Reserved***.

7.7 Write Burst Address Register Description

Table 7-6 describes the Write burst address register (WBURREG) fields which must be programmed before a burst Write.

Table 7-6. Write Burst Register Description

Field	Range	Initial Value	Description
ADR	[14:0]	0	***Address***. This is the starting address of the data or mask array during a burst Write operation. It automatically increments by one for each successive Write of the data or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:15]		***Reserved***.
BLEN	[27:19]	0	***Length of Burst Access***. The device provides the capability to Write from 4–511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[67:28]		***Reserved***.

7.8 NFA Register

Bit [0] of each 68-bit data entry is specially designated for use in the operation of the Learn command. For 68-bit-configured quadrants, this bit indicates whether a location is full (bit set to 1) or empty (bit set to 0). Every Write and/or Learn command loads the address of the first 68-bit location that contains a 0 in the entry's bit[0]. This is stored in the NFA register (see *Table 7-7*). If all the bits[0] in a device are set to 1, the CYNSE70064A asserts FULO[1:0] to 1.

For 136-bit-configured quadrants, the LSB of the NFA register is always set to 0. The host ASIC must set both bit[0] and bit[68] in a 136-bit word to either 0 or 1 to indicate full or empty status. Both bit[0] and bit[68] must be set to either 0 or 1, (that is, the 10 or 01 settings are invalid).

Table 7-7. NFA Register

Address	67–15	14–0
60	Reserved	Index

8.0 NSE Architecture and Operation Overview

The CYNSE70064A consists of 32K × 68-bit storage cells referred to as data bits. There is a mask cell corresponding to each data cell. *Figure 8-1* shows the three organizations of the device based on the value of the CFG bits in the command register.

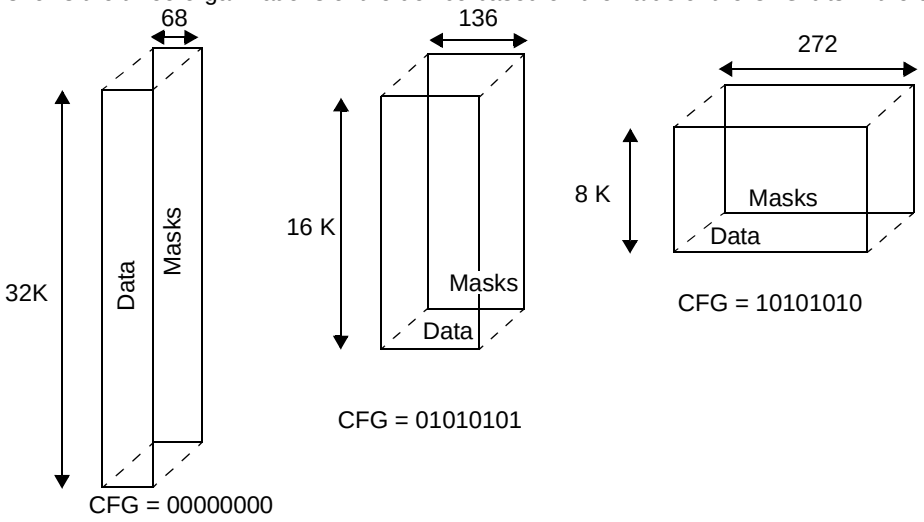


Figure 8-1. CYNSE70064A Database WIDTH Configuration

During a Search operation, the Search data bit (S), data array bit (D), mask array bit (M) and the global mask bit (G) are used in the following manner to generate a match at that bit position (see *Table 8-1*). The entry with a match on every bit position results in a successful Search during a Search operation.

Table 8-1. Bit Position Match

G	M	D	S	Match
0	X	X	X	1
1	0	X	X	1
1	1	0	0	1
1	1	1	0	0
1	1	0	1	0
1	1	1	1	1

In order for a successful Search within a device to make the device the local winner in the Search operation, all 68-bit positions must generate a match for a 68-bit entry in 68-bit configured quadrants, or all 136-bit positions must generate a match for two consecutive even and odd 68-bit entries in quadrants configured as 136 bits, or all 272-bit positions must generate a match for four consecutive entries aligned to four entry-page boundaries of 68-bit entries in quadrants configured as 272 bits.

An arbitration mechanism using a cascade bus determines the global winning device among the local winning devices in a Search cycle. The global winning device drives the SRAM bus, SSV, and the SSF signals. In case of a Search failure, the device(s) with the LDEV and LRAM bits set drives the SRAM bus, SSF, and SSV signals.

The CYNSE70064A device can be configured to contain tables of different widths, even within the same chip. *Figure 8-2* shows a sample configuration of different widths.

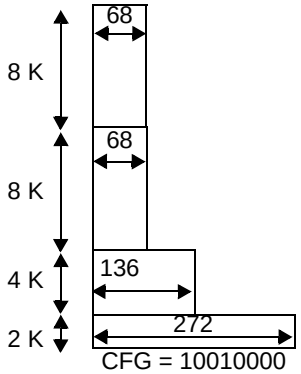


Figure 8-2. Multiwidth Database Configurations Example

9.0 Data and Mask Addressing

Figure 9-1 shows CYNSE70064A data and mask array addressing.

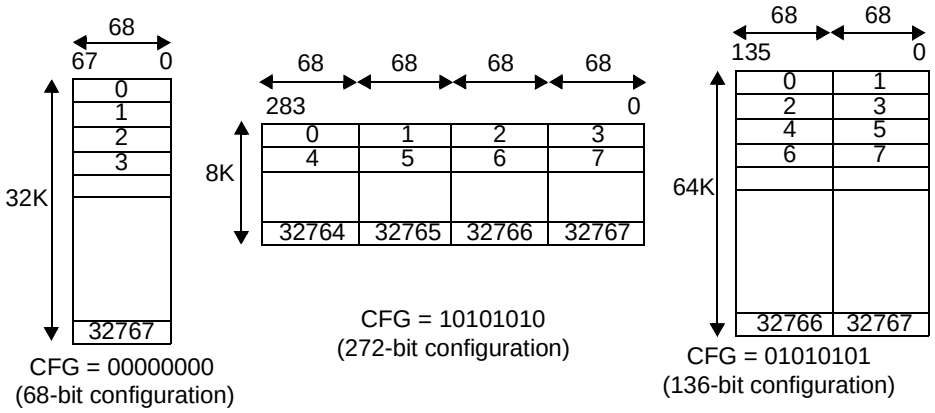


Figure 9-1. Addressing of the CYNSE70064A Data and Mask Arrays

10.0 Commands

A master device such as an ASIC controller issues commands to the CYNSE70064A device using the command valid (CMDV) signal and the CMD bus. The following subsections describe the operation of the commands.

10.1 Command Codes

The CYNSE70064A implements four basic commands, shown in *Table 10-1*. The command code must be presented to CMD[1:0] while keeping the CMDV signal HIGH for two CLK2X cycles (designated as cycles A and B). The controller ASIC must align the instructions using the PHS_L signal. The CMD[8:2] field passes the parameters of the command in cycles A and B.

Table 10-1. Command Codes

Command Code	Command	Description
00	Read	Reads one of the following: data array, mask array, device registers, or external SRAM.
01	Write	Writes one of the following: data array, mask array, device registers, or external SRAM.
10	Search	Searches the data array for a desired pattern using the specified register from the GMR array and local mask associated with each data cell.
11	Learn	The device has internal storage for up to 16 comparands that it can learn. The device controller can insert these entries at the next-free address (as specified by the NFA register) using the Learn instruction.

10.2 Commands and Command Parameters

Table 10-2 lists the CMD bus fields that contain the CYNSE70064A command parameters and their respective cycles. Each command is described separately in the subsections that follow.

Table 10-2. Command Parameters

CMD	CYC	8	7	6	5	4	3	2	1	0
Read	A	SADR[21]	SADR[20]	x	0	0	0	0 = Single 1 = Burst	0	0
	B	0	0	0	0	0	0	0 = Single 1 = Burst	0	0
Write	A	SADR[21]	SADR[20]	x	GMR Index [2:0]			0 = Single 1 = Burst	0	1
	B	0	0	0	GMR Index [2:0]			0 = Single 1 = Burst	0	1

Table 10-2. Command Parameters (continued)

CMD	CYC	8	7	6	5	4	3	2	1	0
Search	A	SADR[21]	SADR[20]	x	GMR Index 2:0]			68-bit or 136-bit: 0 272-bit: 1 in first cycle 0 in second cycle	1	0
	B	SSRI[2:0]			Comparand Register Index				1	0
Learn[5]	A	SADR[21]	SADR[20]	x	Comparand Register Index				1	1
	B	0	0	Mode 0: 68-bit 1: 136-bit	Comparand Register Index				1	1

10.3 Read Command

The Read can be a single Read of a data array, a mask array, an SRAM, or a register location (CMD[2] = 0). It can be a burst Read of the data (CMD[2] = 1) or mask array locations using an internal auto-incrementing address register (RBURADR). A description of each type is provided in *Table 10-3*. A single-location Read operation lasts six cycles, as shown in *Figure 10-1*. The burst Read adds two cycles for each successive Read. The SADR[21:20] bits supplied in the Read instruction cycle A drives SADR[21:20] signals during the Read of an SRAM location.

Table 10-3. Read Command Parameters

CMD Parameter CMD[2]	Read Command	Description
0	Single Read	Reads a single location of the data array, mask array, external SRAM, or device registers. All access information is applied on the DQ bus.
1	Burst Read	Reads a block of locations from the data array, or mask array as a burst. The internal register (RBURADR) specifies the starting address and the length of the data transfer from the data or mask array, and it auto-increments the address for each access. All other access information is applied on the DQ bus. ***Note***. The device registers and external SRAM can only be read in single-Read mode.

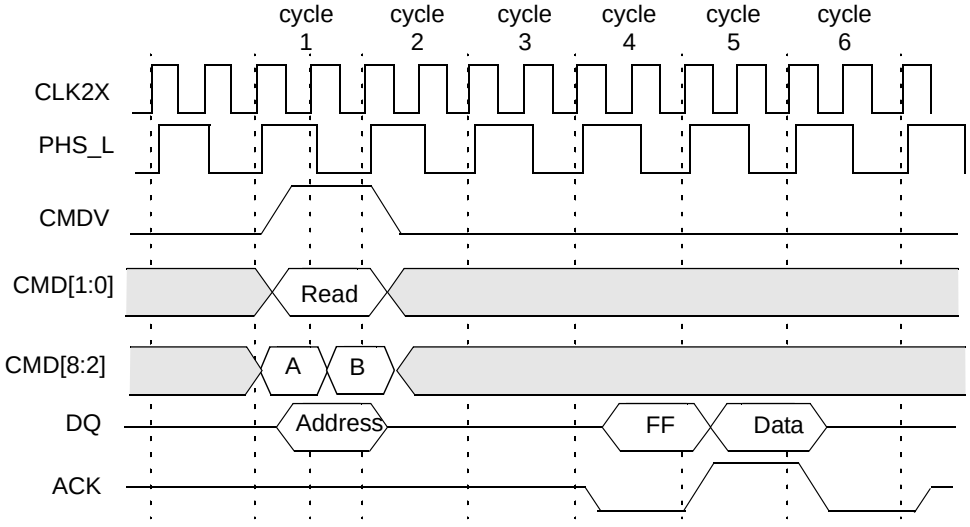


Figure 10-1. Single-Location Read Cycle Timing

The single Read operation takes six clock cycles, in the following sequence.

- **Cycle 1**: The host ASIC applies the Read instruction on the CMD[1:0] (CMD[2] = 0) using CMDV = 1 and the DQ bus supplies the address, as shown in *Table 10-4* and *Table 10-5*. The host ASIC selects the CYNSE70064A for which ID[4:0] matches the DQ[25:21] lines. If the DQ[25:21] = 11111, the host ASIC selects the CYNSE70064A with the LDEV bit set. The host ASIC also supplies SADR[21:20] on CMD[8:7] in cycle A of the Read instruction if the Read is directed to the external SRAM.
- **Cycle 2**: The host ASIC floats DQ[67:0] to three-state condition.

Note:
5. The 272-bit-configured devices or 272-bit-configured quadrants within devices do not support the Learn instruction.

- **Cycle 3**: The host ASIC keeps DQ[67:0] in three-state condition.
- **Cycle 4**: The selected device starts to drive the DQ[67:0] bus, and drives the ACK signal from Z to LOW.
- **Cycle 5**: The selected device drives the Read data from the addressed location on the DQ[67:0] bus, and drives the ACK signal HIGH.
- **Cycle 6**: The selected device floats the DQ[67:0] to three-state condition and drives the ACK signal LOW.

At the termination of cycle 6, the selected device releases the ACK line to three-state condition. The Read instruction is complete, and a new operation can begin. Note that the latency of the SRAM Read will be different than the one described above (see Subsection 12.2, “SRAM PIO Access” on page 101). *Table 10-4* lists and describes the format of the Read address for a data array, mask array, or SRAM.

Table 10-4. Read Address Format for Data Array, Mask Array, or SRAM

DQ[67:30]	DQ[29]	DQ[28:26]	DQ[25:21]	DQ[20:19]	DQ[18:15]	DQ[14:0]
Reserved	0: Direct 1: Indirect	SSRI (applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is 0, this field carries the address of the data array location. If DQ[29] is 1, the SSRI specified on DQ[28:26] is used to generate the address of the data array location: {SSR[14:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSRI (applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is 0, this field carries the address of the mask array location. If DQ[29] is 1, the SSRI specified on DQ[28:26] is used to generate the address of the mask array location: {SSR[14:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSRI (applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is 0, this field carries the address of the SRAM location. If DQ[29] is 1, the SSRI specified on DQ[28:26] is used to generate the address of the SRAM location: {SSR[14:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}[6]

Table 10-5 describes the Read address format for the internal registers. *Figure 10-2* illustrates the timing diagram for the burst Read of the data or mask array.

Table 10-5. Read Address Format for Internal Registers

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	ID	11: Register	Reserved	Register Address

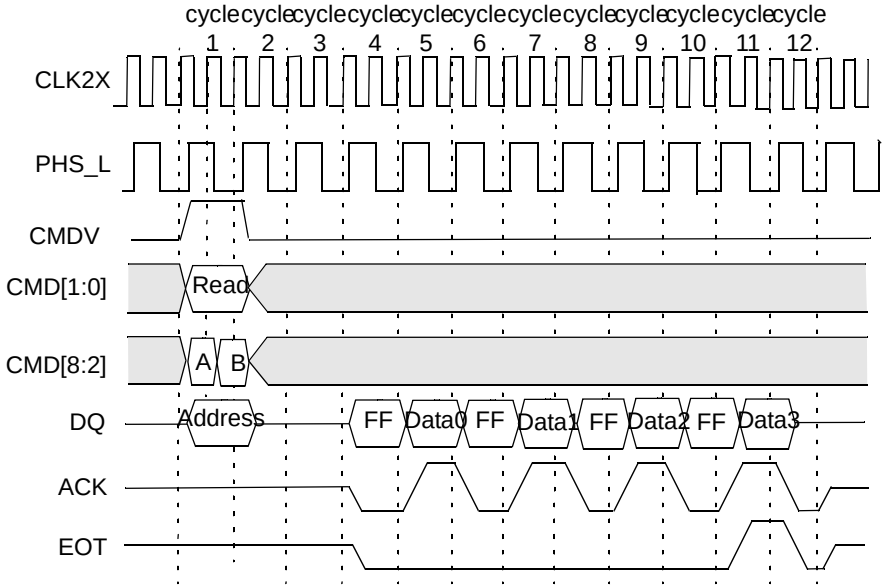


Figure 10-2. Burst Read of the Data and Mask Arrays (BLEN = 4)

The Read operation lasts 4 + 2n CLK cycles (where n is the number of accesses in the burst specified by the BLEN field of the RBURREG) in the sequence shown below. This operation assumes that the host ASIC has programmed the RBURREG with the starting address (ADR) and the length of the transfer (BLEN) before initiating the burst Read command.

Note:

6. “ | ” stands for logical OR operation. “{}” stands for concatenation operator.

- **Cycle 1**: The host ASIC applies the Read instruction on CMD[1:0] (CMD[2] = 1) using CMDV = 1 and the address supplied on the DQ bus, as shown in *Table 10-6*. The host ASIC selects the CYNSE70064A where ID[4:0] matches the DQ[25:21] lines. If the DQ[25:21] = 11111, the host ASIC selects the CYNSE70064A with the LDEV bit set.
- **Cycle 2**: The host ASIC floats DQ[67:0] to the three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in the three-state condition.
- **Cycle 4**: The selected device starts to drive the DQ[67:0] bus and drives ACK and EOT from Z to LOW.
- **Cycle 5**: The selected device drives the Read data from the addressed location on the DQ[67:0] bus, and drives the ACK signal HIGH.

Cycles 4 and 5 repeat for each additional access until all the accesses specified in the burst length (BLEN) field of RBURREG are complete. On the last transfer, the CYNSE70064A drives the EOT signal HIGH.

- **Cycle (4 + 2n)**: The selected device drives the DQ[67:0] to the three-state condition, and drives the ACK and EOT signals LOW.

At the termination of cycle (4 + 2n), the selected device floats the ACK line to the three-state condition. The burst Read instruction is complete, and a new operation can begin. *Table 10-6* describes the Read address format for data and mask arrays for burst Read operations.

Table 10-6. Read Address Format for Data and Mask Arrays

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:15]	DQ[14:0]
Reserved	ID	00: Data Array	Reserved	***Do not care***. These 15 bits come from the internal register (RBURADR) which increments for each access.
Reserved	ID	01: Mask Array	Reserved	***Do not care***. These 15 bits come from the internal register (RBURADR) which increments for each access.

10.4 Write Command

The Write can be a single Write of a data array, mask array, register, or external SRAM location (CMD[2] = 0). It can be a burst Write (CMD[2] = 1) using an internal auto-incrementing address register (WBURADR) of the data or mask array locations. A single-location Write is a 3-cycle operation, as shown in *Figure 10-3*. The burst Write adds one extra cycle for each successive location Write.

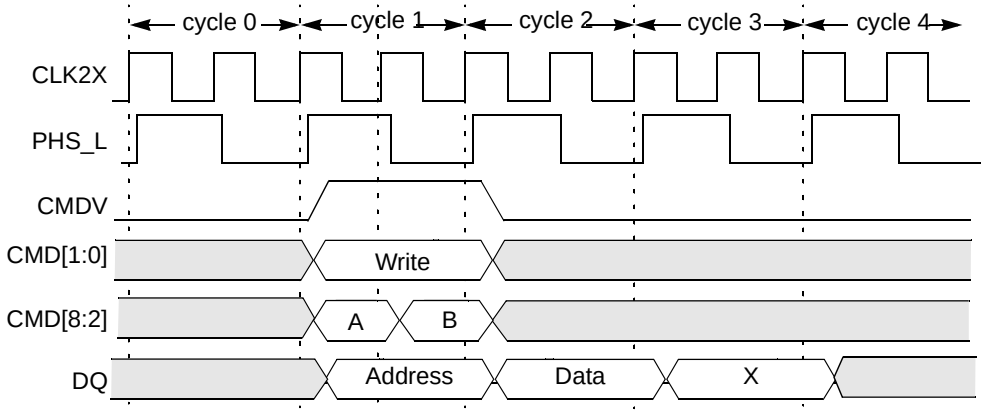


Figure 10-3. Single Write Cycle Timing

The following is the Write operation sequence, and *Table 10-7* shows the Write address format for the data array, the mask array, or single-Write SRAM. *Table 10-8* shows the Write address format for the internal registers.

- **Cycle 1A:** The host ASIC applies the Write instruction to the CMD[1:0] (CMD[2] = 0), using CMDV = 1 and the address supplied on the DQ bus. The host ASIC also supplies the GMR Index to mask the Write to the data or mask array location on CMD[5:3]. For SRAM Writes, the host ASIC must supply the SADR[21:20] on CMD[8:7].
- **Cycle 1B:**The host ASIC continues to apply the Write instruction to the CMD[1:0] (CMD[2] = 0), using CMDV = 1 and the address supplied on the DQ bus. The host ASIC continues to supply the GMR Index to mask the Write to the data or mask array locations in CMD[5:3].The host ASIC selects the device where ID[4:0] matches the DQ[25:21] lines, or it selects all the devices when DQ[25:21] = 11111.
- **Cycle 2:** The host ASIC drives the DQ[67:0] with the data to be written to the data array, mask array, or register location of the selected device.
- **Cycle 3:** Idle cycle.

At the termination of cycle 3, another operation can begin.

Note. The latency of the SRAM Write will be different than the one described above (see Subsection 12.2, “SRAM PIO Access” on page 101).

Table 10-7. Write Address Format for Data Array, Mask Array, or SRAM (Single Write)

DQ [67:30]	DQ[29]	DQ[28:26]	DQ [25:21]	DQ[20:19]	DQ [18:15]	DQ[14:0]
Reserved	0: Direct 1: Indirect	SSR (applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is 0, this field carries the address of the data array location. If DQ[29] is 1, the SSR specified on DQ[28:26] is used to generate the address of data array location: {SSR[14:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSR (applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is 0, this field carries the address of the mask array location. If DQ[29] is 1, the SSR specified on DQ[28:26] is used to generate the address of the mask array location: {SSR[14:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]
Reserved	0: Direct 1: Indirect	SSR (applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is 0, this field carries the address of the SRAM location. If DQ[29] is 1, the SSR specified on DQ[28:26] is used to generate the address of SRAM location: {SSR[14:2], SSR[1] | DQ[1], SSR[0] | DQ[0]}.[6]

Table 10-8. Write Address Format for Internal Registers

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	ID	11: Register	Reserved	Register address

Figure 10-4 shows the timing diagram of a burst Write operation of the data or mask array.

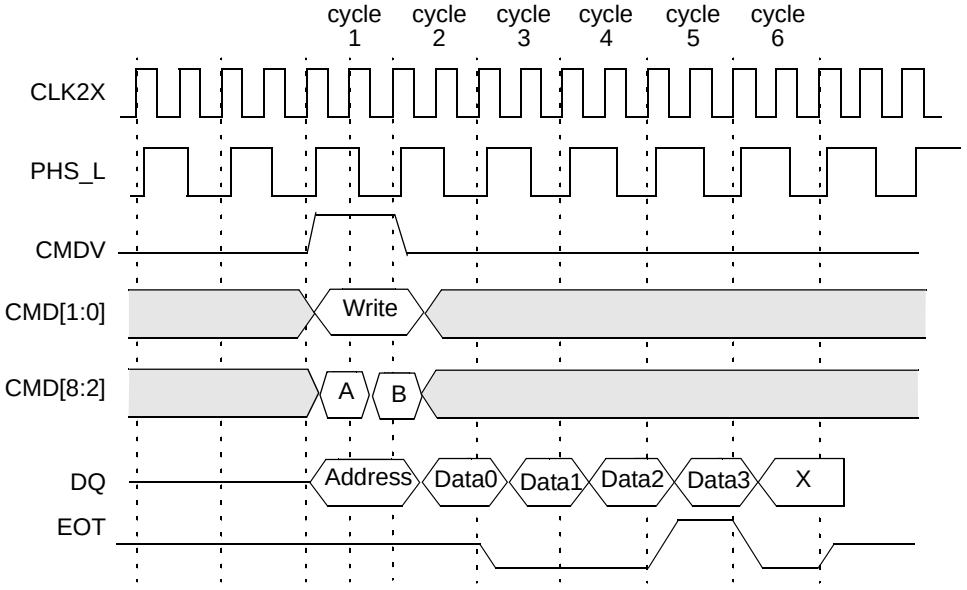


Figure 10-4. Burst Write of the Data and Mask Arrays (BLEN = 4)

The burst Write operation lasts for (n + 2) CLK cycles. n signifies the number of accesses in the burst as specified in the BLEN field of the WBURREG register. The following is the block Write operation sequence. This operation assumes that the host ASIC has programmed the WBURREG with the starting address (ADR) and the length of transfer (BLEN) before initiating a burst Write command.

- **Cycle 1A**: The host ASIC applies the Write instruction to the CMD[1:0] (CMD[2] = 1), using CMDV = 1 and the address supplied on the DQ bus, as shown in *Table 10-9*. The host ASIC also supplies the GMR Index to mask the Write to the data or mask array locations in CMD[5:3].
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on the CMD[1:0] (CMD[2] = 1), using CMDV = 1 and the address supplied on the DQ bus. The host ASIC continues to supply the GMR Index to mask the Write to the data or mask array locations in CMD[5:3]. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. It selects all the devices when DQ[25:21] = 11111.

- **Cycle 2**: The host ASIC drives the DQ[67:0] with the data to be written to the data or mask array location of the selected device. The CYNSE70064A writes the data from the DQ[67:0] bus only to the subfield that has the corresponding mask bit set to 1 in the GMR specified by the index CMD[5:3] supplied in cycle 1.
- **Cycles 3 to n + 1**: The host ASIC drives the DQ[67:0] with the data to be written to the next data or mask array location (addressed by the auto-increment ADR field of the WBURREG register) of the selected device.

The CYNSE70064A writes the data on the DQ[67:0] bus only to the subfield that has the corresponding mask bit set to 1 in the GMR specified by the index CMD[5:3] supplied in cycle 1. The CYNSE70064A drives the EOT signal LOW from cycle 3 to cycle n; the CYNSE70064A drives the EOT signal HIGH in cycle n + 1 (n is specified in the BLEN field of the WBURREG).

- **Cycle n + 2**: TheCYNSE70064A drives the EOT signal LOW.

At the termination of cycle n + 2, the CYNSE70064A floats the EOT signal to a three-state operation, and a new instruction can begin.

Table 10-9. Write Address Format for Data and Mask Array (Burst Write)

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:15]	DQ[14:0]
Reserved	ID	00: Data array	Reserved	***Do not care***. These 15 bits come from the internal register (WBURADR), which increments with each access.
Reserved	ID	01: Mask array	Reserved	***Do not care***. These 15 bits come from the internal register (WBURADR), which increments with each access.

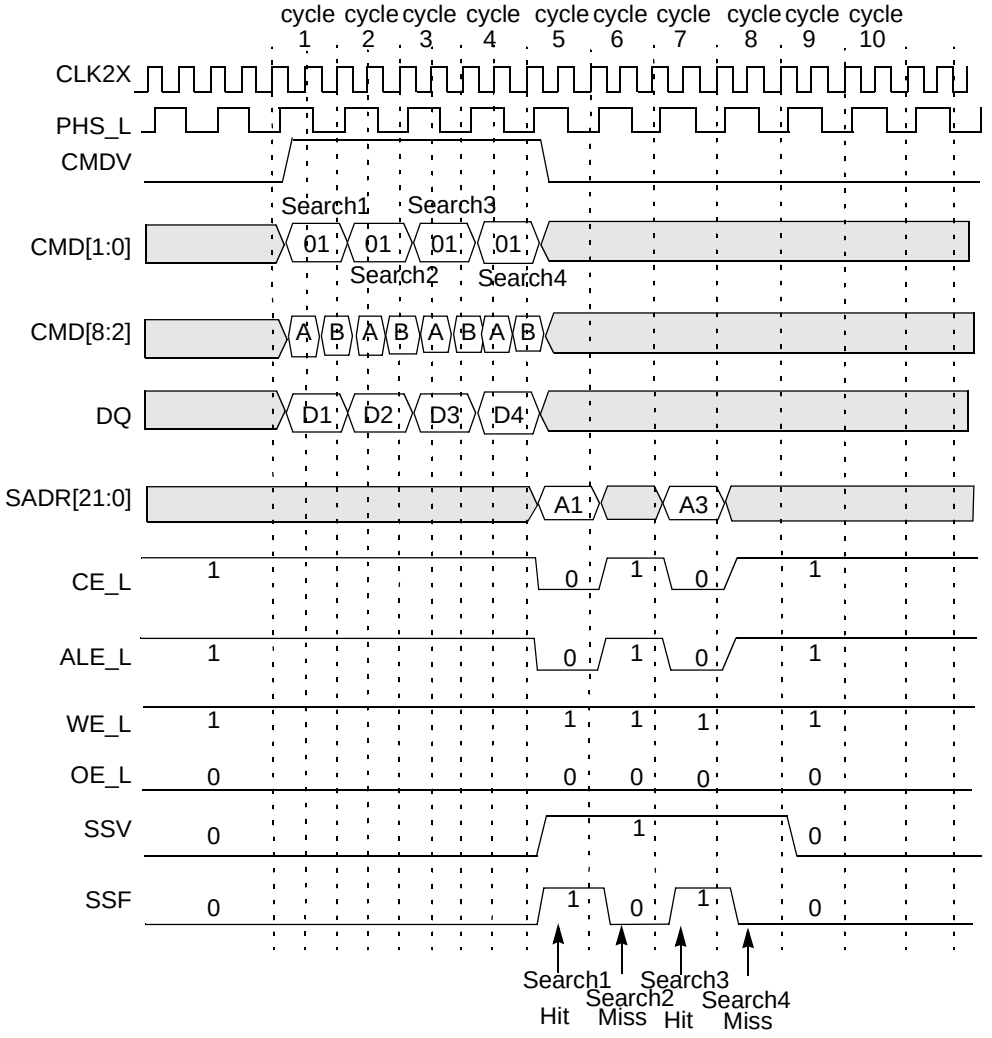
10.5 Search Command

This subsection describes the following:

- 68-bit Search on tables configured as ×68 using one device
- 68-bit Search on tables configured as ×68 using up to eight devices
- 68-bit Search on tables configured as ×68 using up to 31 devices
- 136-bit Search on tables configured as ×136 using one device
- 136-bit Search on tables configured as ×136 using up to eight devices
- 136-bit Search on tables configured as ×136 using up to 31 devices
- 272-bit Search on tables configured as ×272 using one device
- 272-bit Search on tables configured as ×272 using up to eight devices
- 272-bit Search on tables configured as ×272 using up to 31 devices
- Mixed-size searches on tables configured with different widths using an CYNSE70064A.

10.6 68-bit Search on Tables Configured as ×68 using a Single CYNSE70064A Device

Figure 10-5 shows the timing diagram for a Search command in the 68-bit-configured table (CFG = 00000000) consisting of a single device for one set of parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. The hardware diagram for this Search subsystem is shown in *Figure 10-6*.



CFG = 00000000, HLAT = 000, TLSZ = 00, LRAM = 1, LDEV = 1.

Figure 10-5. Timing Diagram for 68-bit Search in x68 Table (One Device)

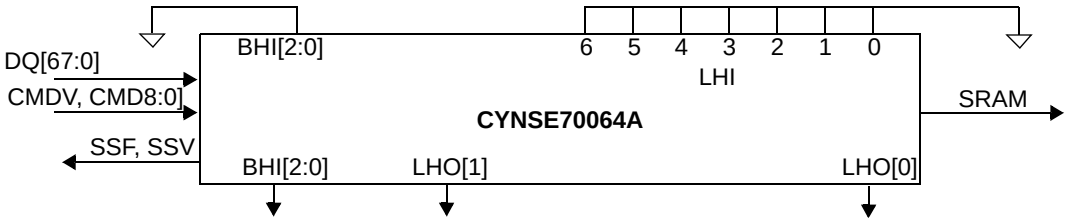


Figure 10-6. Hardware Diagram for 68-bit Search in x68 Table (One Device)

The following is the sequence of operation for a single 68-bit Search command (also refer to Command and Command Parameters, Subsection 10.2 on page 18).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and to apply Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for information on SSR[0:7]). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note. For 68-bit searches, the host ASIC must supply the same 68-bit data on DQ[67:0] during both cycles A and B. The even and odd pair of GMRs selected for the compare must be programmed with the same value.

The logical 68-bit Search operation is shown in *Figure 10-7*. The entire table consisting of 68-bit entries is compared to a 68-bit word K (presented on the DQ bus in both cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs selected by the GMR Index in the command's cycle A. The 68-bit word K (presented on the DQ bus in both cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command's cycle B. In a ×68 configuration, only the even comparand register can be subsequently used by the Learn command. The word K (presented on the DQ bus in both cycles A and B of the command) is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (See "SRAM Addressing" on page 100.).

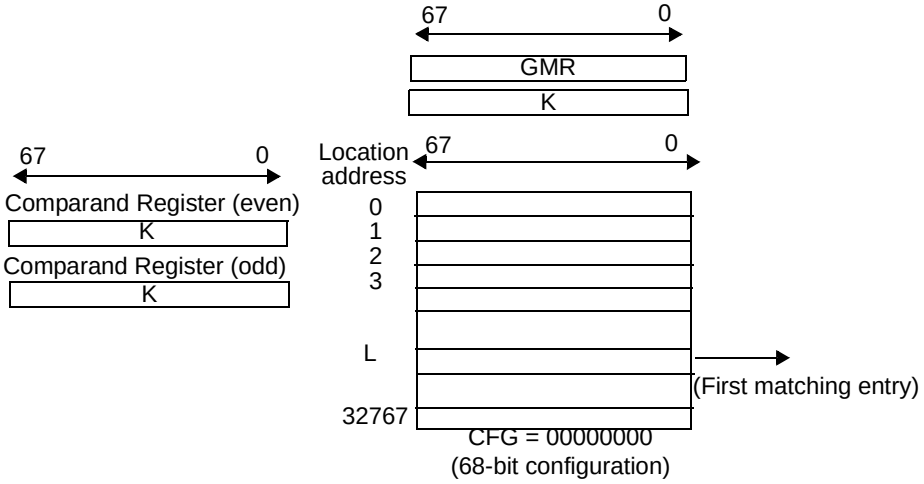


Figure 10-7. ×68 Table with One Device

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 68-bit searches in ×68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit Search command cycle (two CLK2X cycles) is shown in *Table 10-10*.

Table 10-10. The Latency of Search from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K × 68 bits	4
1–8 (TLSZ = 01)	256K × 68 bits	5
1–31 (TLSZ = 10)	992K × 68 bits	6

The latency of a Search from command to SRAM access cycle is 4 for a single device in the table and TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 10-11*.

Table 10-11. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.7 68-bit Search on Tables Configured as ×68 Using up to Eight CYNSE70064A Devices

The hardware diagram of the Search subsystem of eight devices is shown in *Figure 10-8*. The following are the parameters programmed into the eight devices.

- First seven devices (devices 0–6): CFG = 00000000, TLSZ = 01, HLAT = 010, LRAM = 0, and LDEV = 0.
- Eighth device (device 7): CFG = 00000000, TLSZ = 01, HLAT = 010, LRAM = 1, and LDEV = 1.

Note. All eight devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table (device number 7 in this case) must be programmed with LRAM = 1 and LDEV = 1. All other upstream devices (devices 0 through 6 in this case) must be programmed with LRAM = 0 and LDEV = 0.

Figure 10-9 shows the timing diagram for a Search command in the 68-bit-configured table of eight devices for device number 0. *Figure 10-10* shows the timing diagram for a Search command in the 68-bit-configured table of eight devices for device number 1. *Figure 10-11* shows the timing diagram for a Search command in the 68-bit-configured table of eight devices for device number 7 (the last device in this specific table). For these timing diagrams four 68-bit searches are performed sequentially. Hit/Miss assumptions were made as shown below in *Table 10-12*.

Table 10-12. Hit/Miss Assumption

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Miss
Device 1	Miss	Hit	Hit	Miss
Devices 2–6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

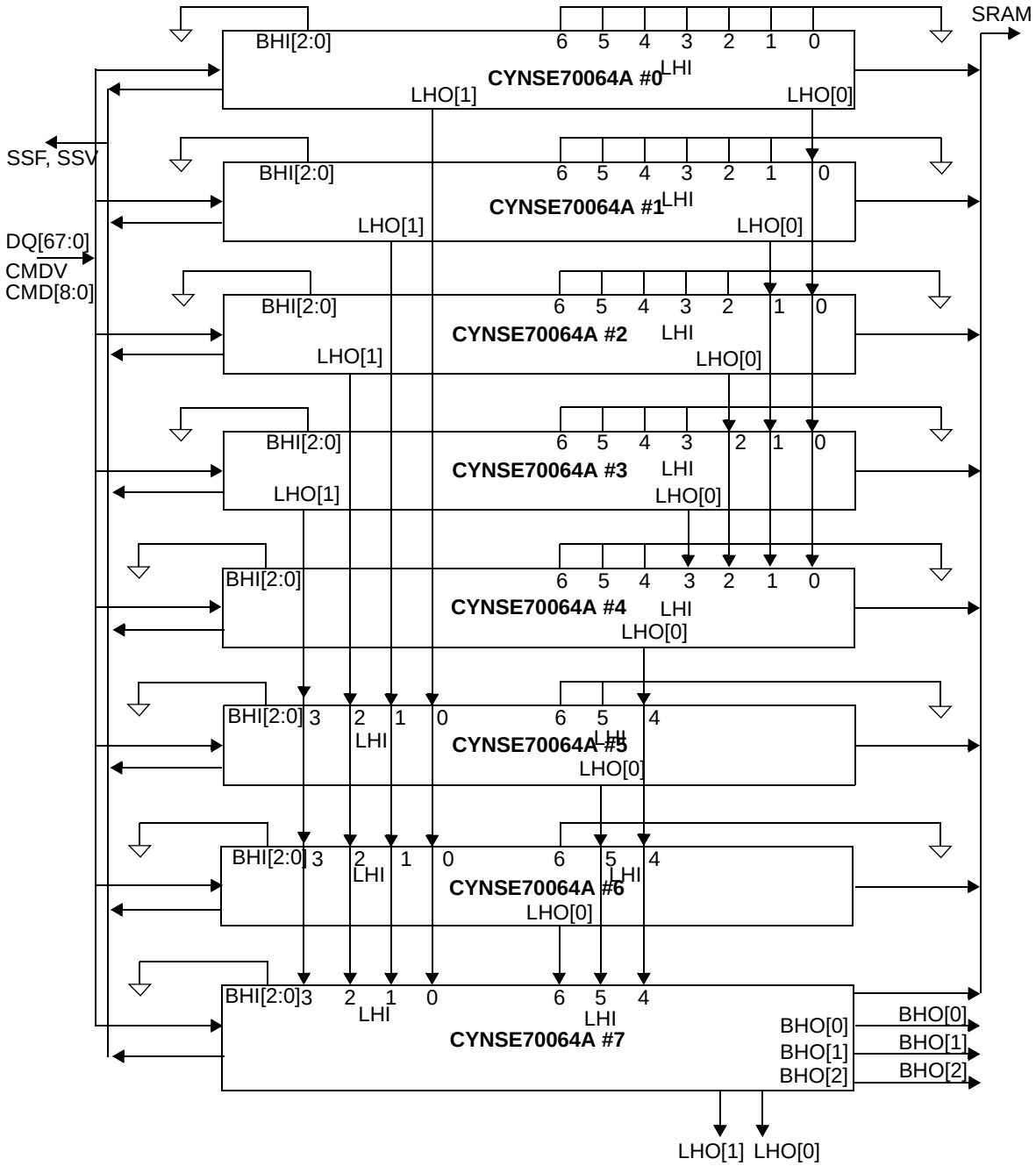
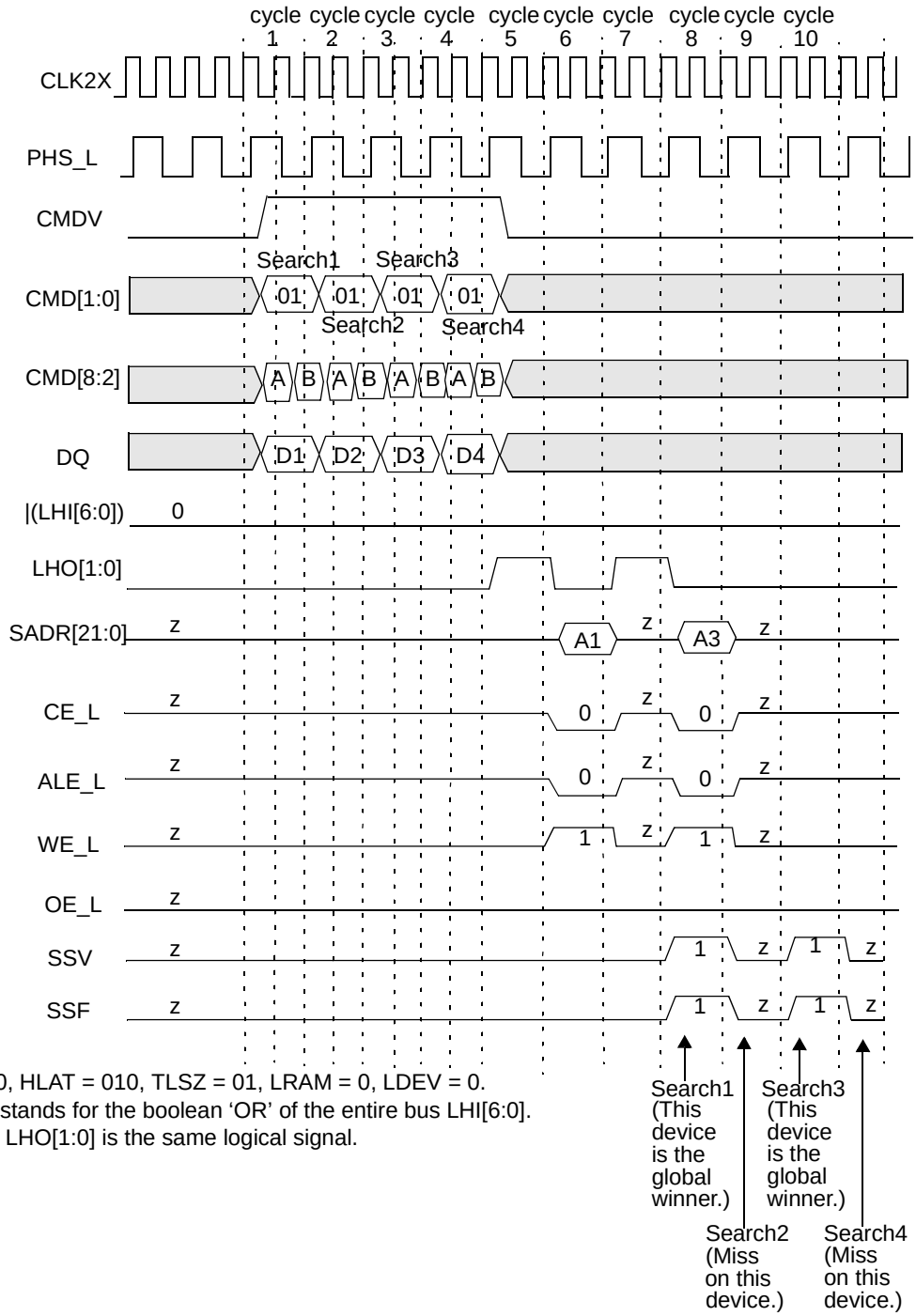
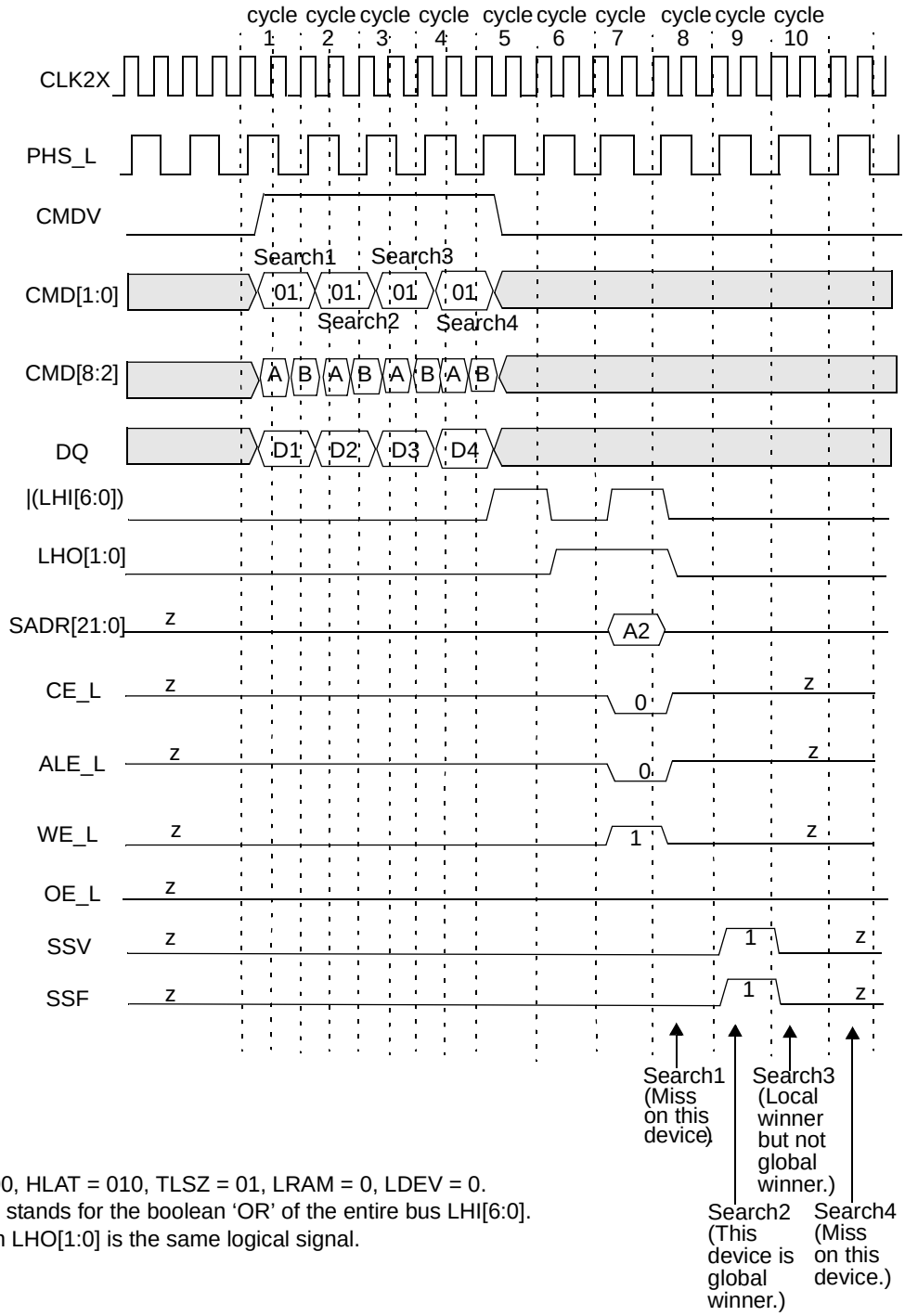


Figure 10-8. Hardware Diagram for a Table With Eight Devices



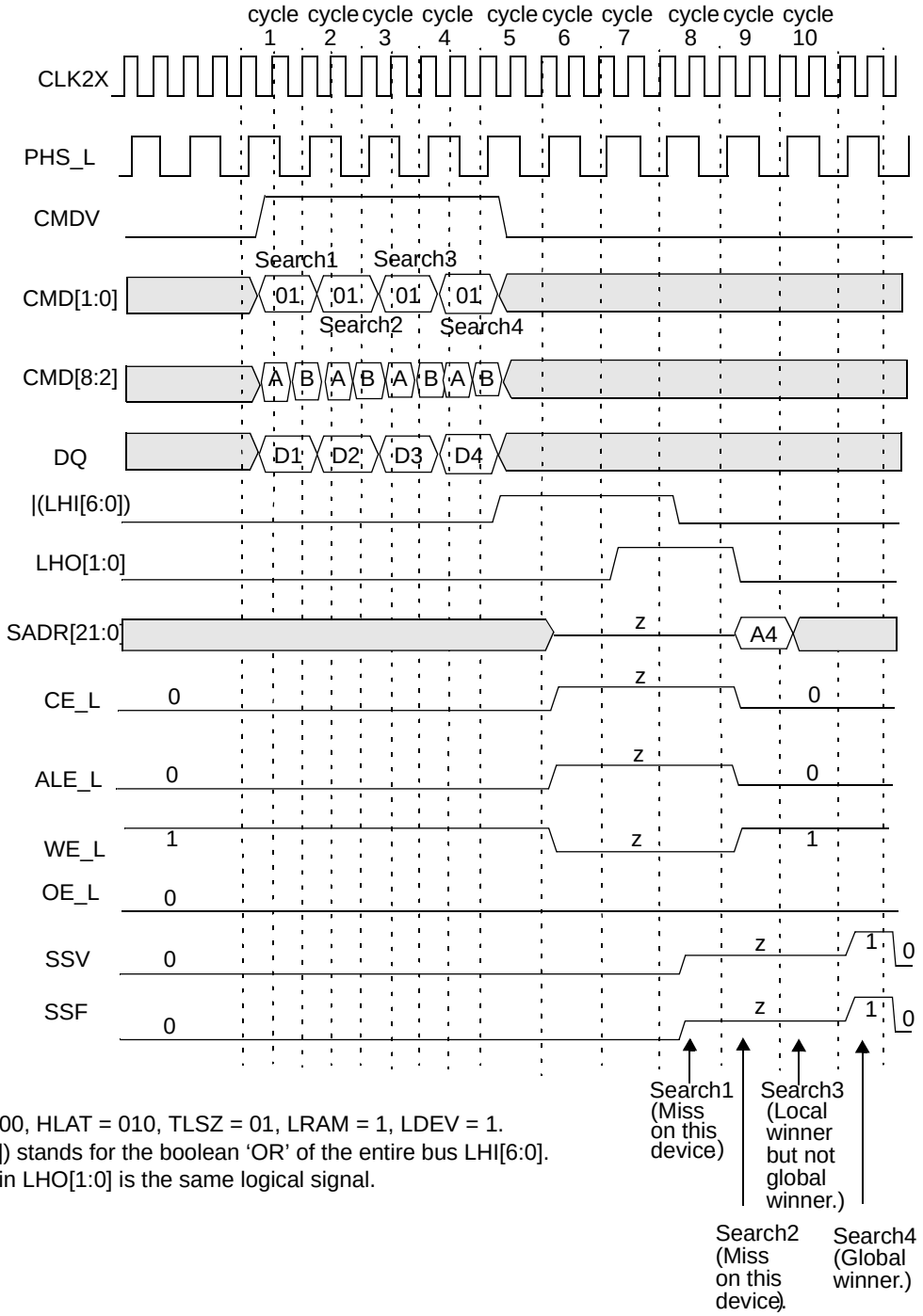
CFG = 00000000, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-9. Timing Diagram for 68-bit Search Device Number 0



CFG = 00000000, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-10. Timing Diagram for 68-bit Search Device Number 1



CFG = 00000000, HLAT = 010, TLSZ = 01, LRAM = 1, LDEV = 1.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-11. Timing Diagram for 68-bit Search Device Number 7 (Last Device)

The following is the sequence of operation for a single 68-bit Search command (also refer to "Command and Command Parameters," Subsection 10.2 on page 18).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) to CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and to apply Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 14 for a description of SSR[0:7]). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note. For 68-bit searches, the host ASIC must supply the same 68-bit data on DQ[67:0] during both cycles A and B, and the even and odd pairs of GMRs selected for the comparison must be programmed with the same value.

The logical 68-bit Search operation is shown in *Figure 10-12*. The entire table with eight devices of 68-bit entries is compared to a 68-bit word K (presented on the DQ bus in both cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected by the GMR Index in the command's cycle A. The 68-bit word K (presented on the DQ bus in both cycles A and B of the command) is also stored in both even and odd comparand register pairs (selected by the Comparand Register Index in command cycle B) in each of the eight devices. In the ×68 configuration, only the even comparand register can subsequently be used by the Learn command in one of the devices (only the first non-full device). The word K (presented on the DQ bus in both cycles A and B of the command) is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 100). The global winning device will drive the bus in a specific cycle. On a global miss cycle the device with LRAM = 1 (default driving device for the SRAM bus) and LDEV = 1 (default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

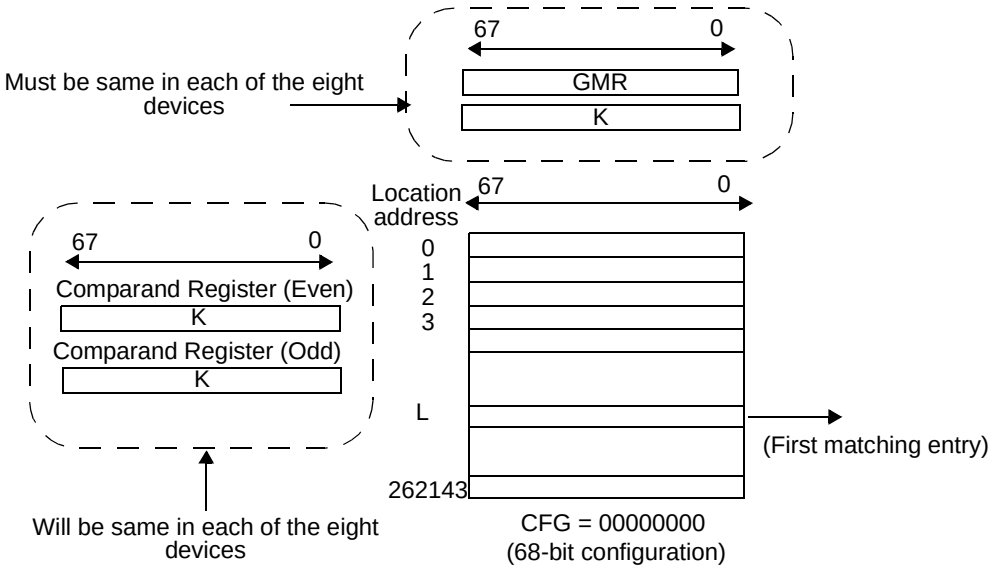


Figure 10-12. x68 Table with Eight Devices

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 68-bit searches in ×68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit Search command cycle (two CLK2X cycles) is shown in *Table 10-13*.

Table 10-13. The Latency of Search from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K × 68 bits	4
1–8 (TLSZ = 01)	256K × 68 bits	5
1–31 (TLSZ = 10)	992K × 68 bits	6

The latency of the Search from command to SRAM access cycle is 5 for up to eight devices in the table (TLSZ = 01). SSV and SSF also shift further to the right for different values of HLAT, as specified in *Table 10-14*.

Table 10-14. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.8 68-bit Search on Tables Configured as ×68 Using up to 31 CYNSE70064A Devices

The hardware diagram of the Search subsystem of 31 devices is shown in *Figure 10-13*. Each of the four blocks in the diagram represents eight CYNSE70064A devices (except the last, which has seven devices). The diagram for a block of eight devices is shown in *Figure 10-14*. The following are the parameters programmed into the 31 devices.

- First thirty devices (devices 0–29): CFG = 00000000, TLSZ = 10, HLAT = 001, LRAM = 0, and LDEV = 0.
- Thirty-first device (device 30): CFG = 00000000, TLSZ = 10, HLAT = 001, LRAM = 1, and LDEV = 1.

Note. All 31 devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (device number 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the Hit/Miss assumptions defined in *Table 10-15*. For the purpose of illustrating the timings, it is further assumed that the there is only one device with a matching entry in each of the blocks. *Figure 10-15* shows the timing diagram for a Search command in the 68-bit-configured table of 31 devices for each of the eight devices in block 0. *Figure 10-16* shows a timing diagram for a Search command in the 68-bit-configured table of 31 devices for the all the devices in block number 1 (above the winning device in that block). *Figure 10-17* shows the timing diagram for the globally winning device (defined as the final winner within its own and all blocks) in block number 1. *Figure 10-18* shows the timing diagram for all the devices below the globally winning device in block number 1. *Figure 10-19*, *Figure 10-20*, and *Figure 10-21* show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device, respectively, for block number 2. *Figure 10-22*, *Figure 10-23*, *Figure 10-24*, and *Figure 10-25* show the timing diagrams of the devices above globally winning device, the globally winning device, and the devices below the globally winning device except the last device (device 30), respectively, for block number 3.

The 68-bit Search operation is pipelined and executes as follows. Four cycles from the Search command, each of the devices knows the outcome internal to it for that operation. In the fifth cycle after the Search command, the devices in a block arbitrate for a winner amongst them (a “block” being defined as less than or equal to eight devices resolving the winner within them using the LHI[6:0] and LHO[1:0] signalling mechanism). In the sixth cycle after the Search command, the blocks (of devices) resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for a Search operation.

Table 10-15. Hit/Miss Assumptions

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

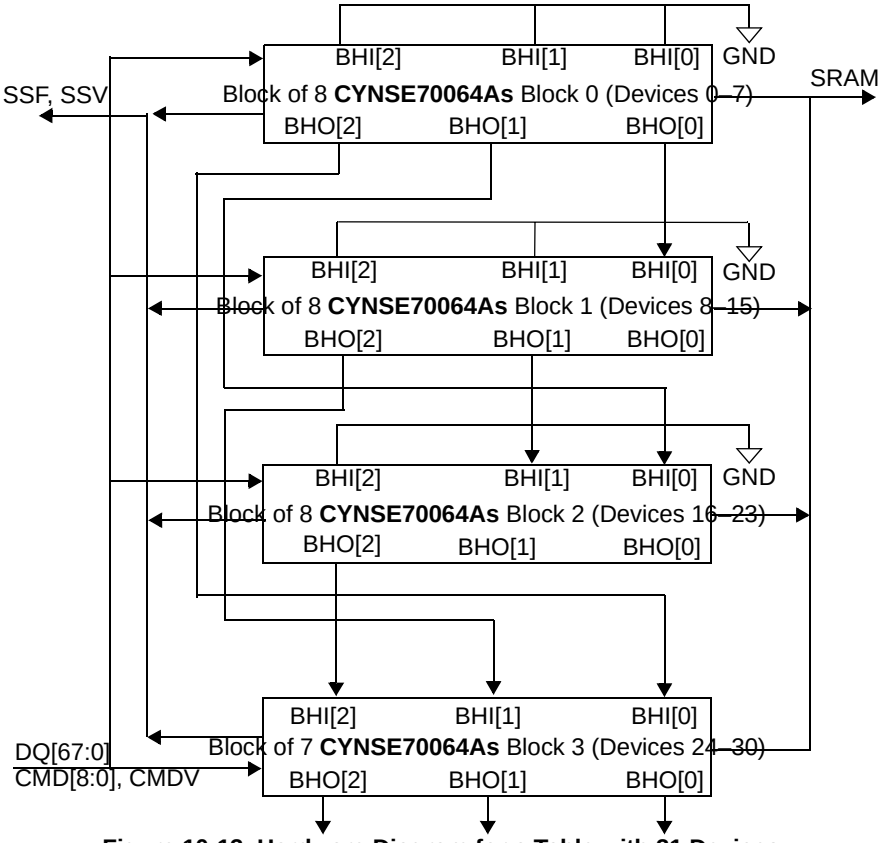


Figure 10-13. Hardware Diagram for a Table with 31 Devices

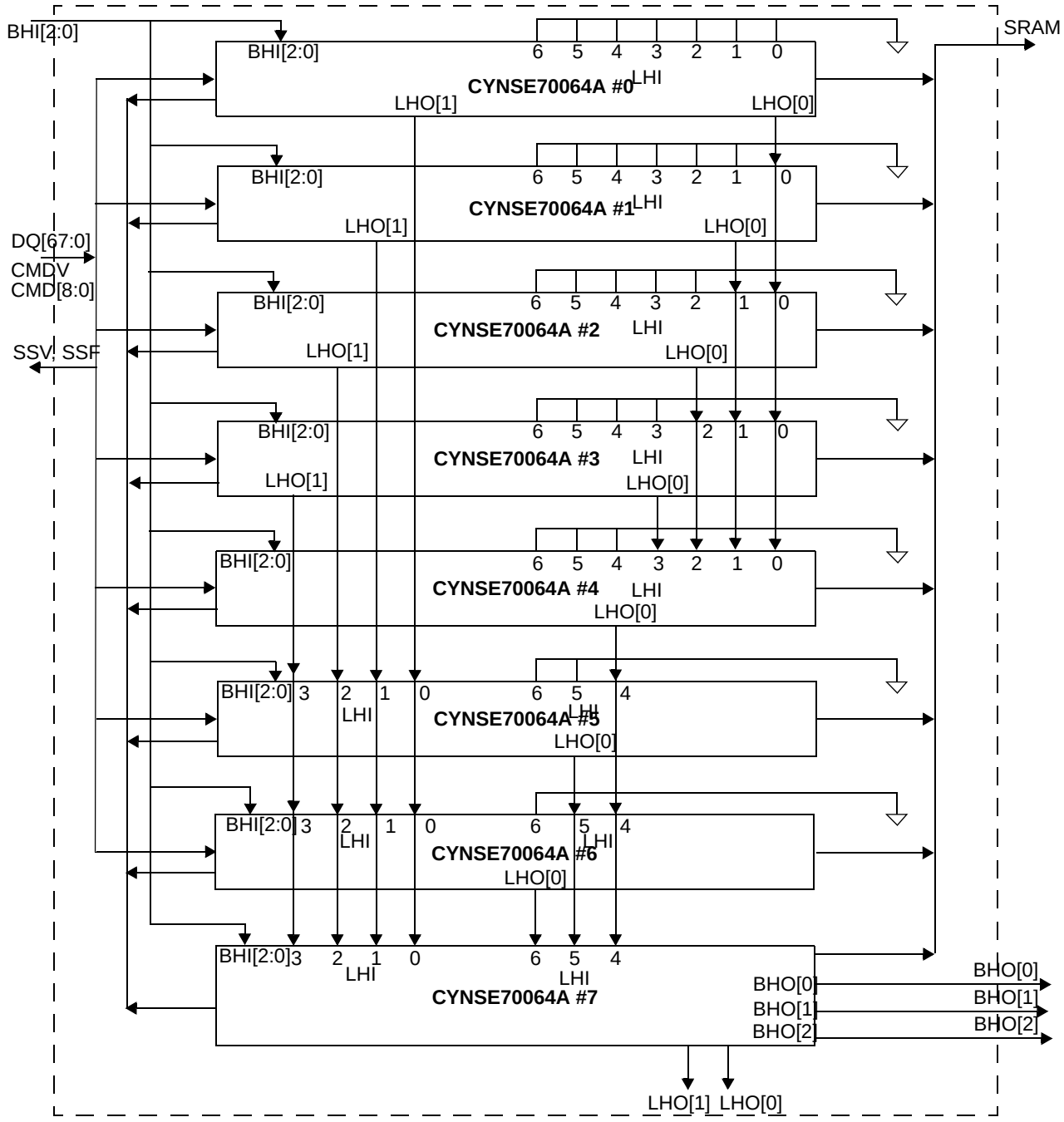
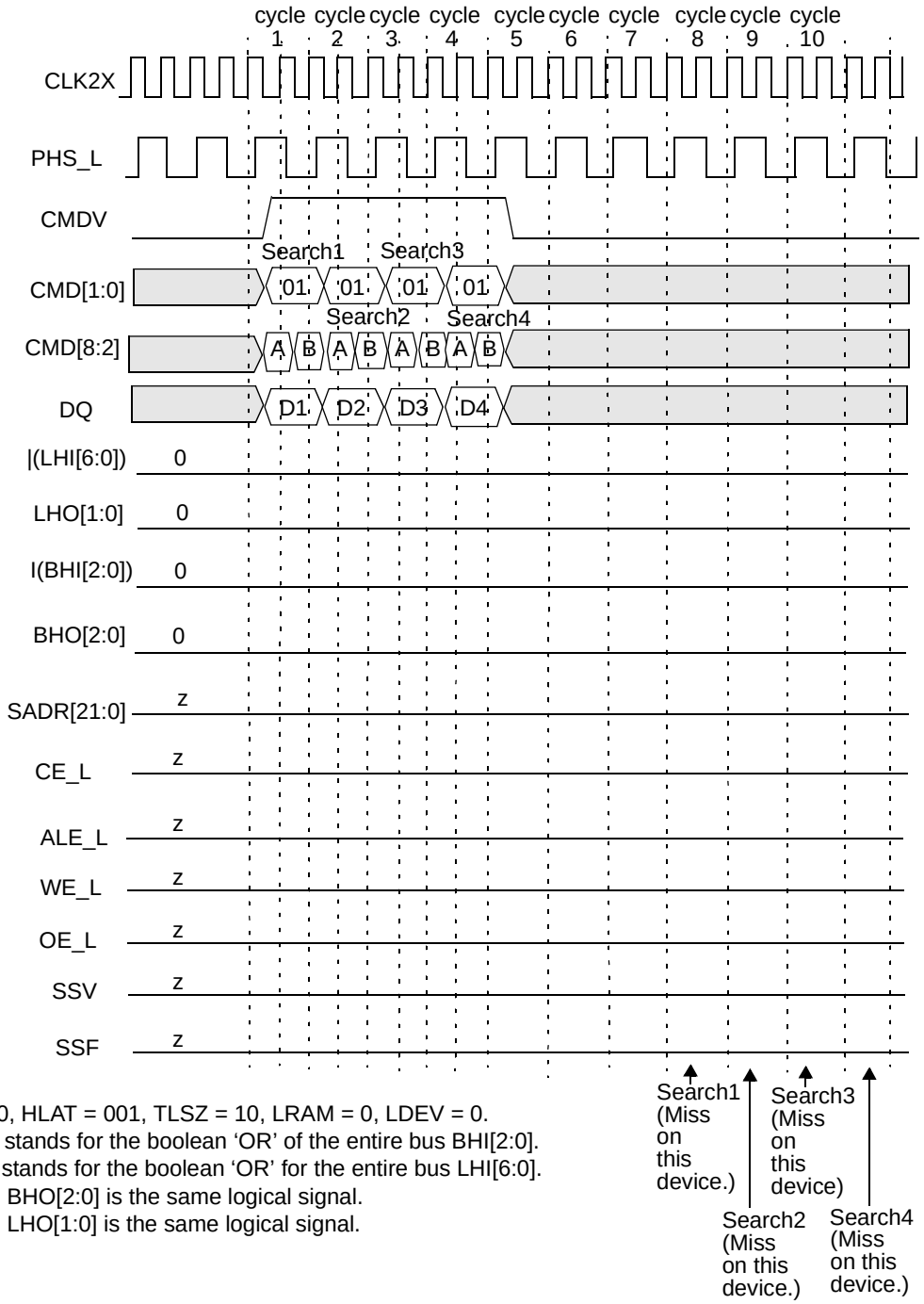
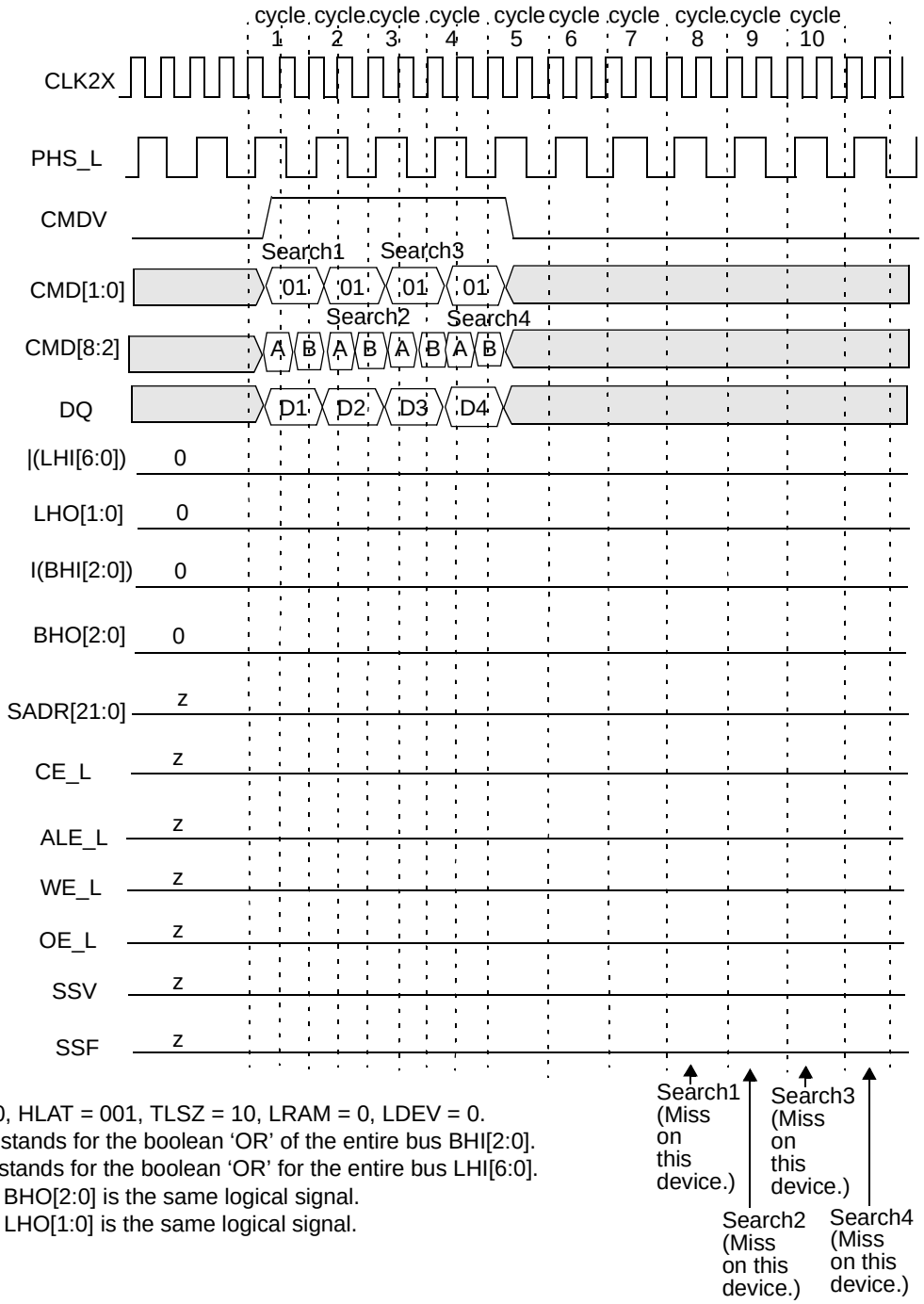


Figure 10-14. Hardware Diagram for a Block of up to Eight Devices



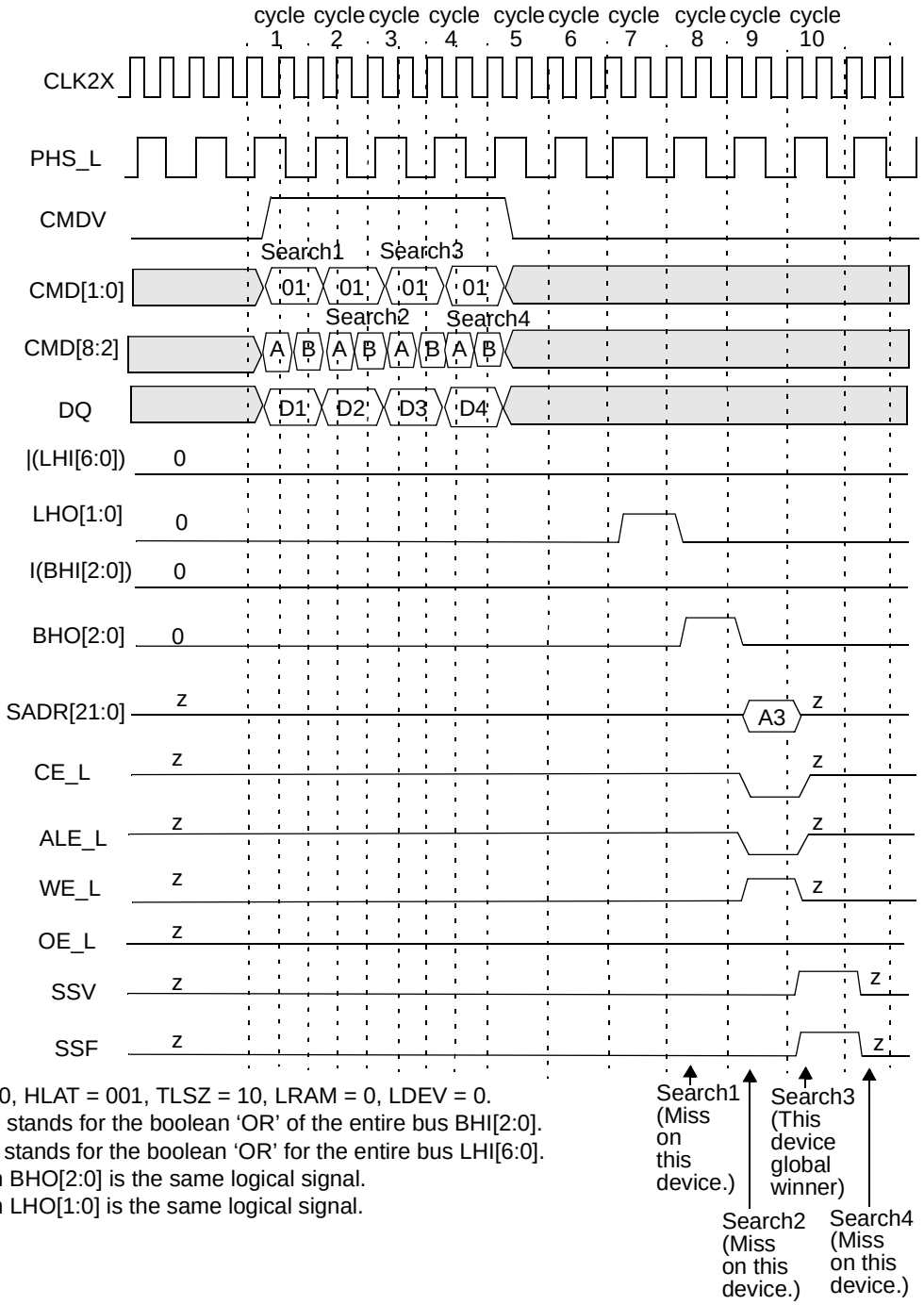
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-15. Timing Diagram for Each Device In Block Number 0 (Miss on Each Device)



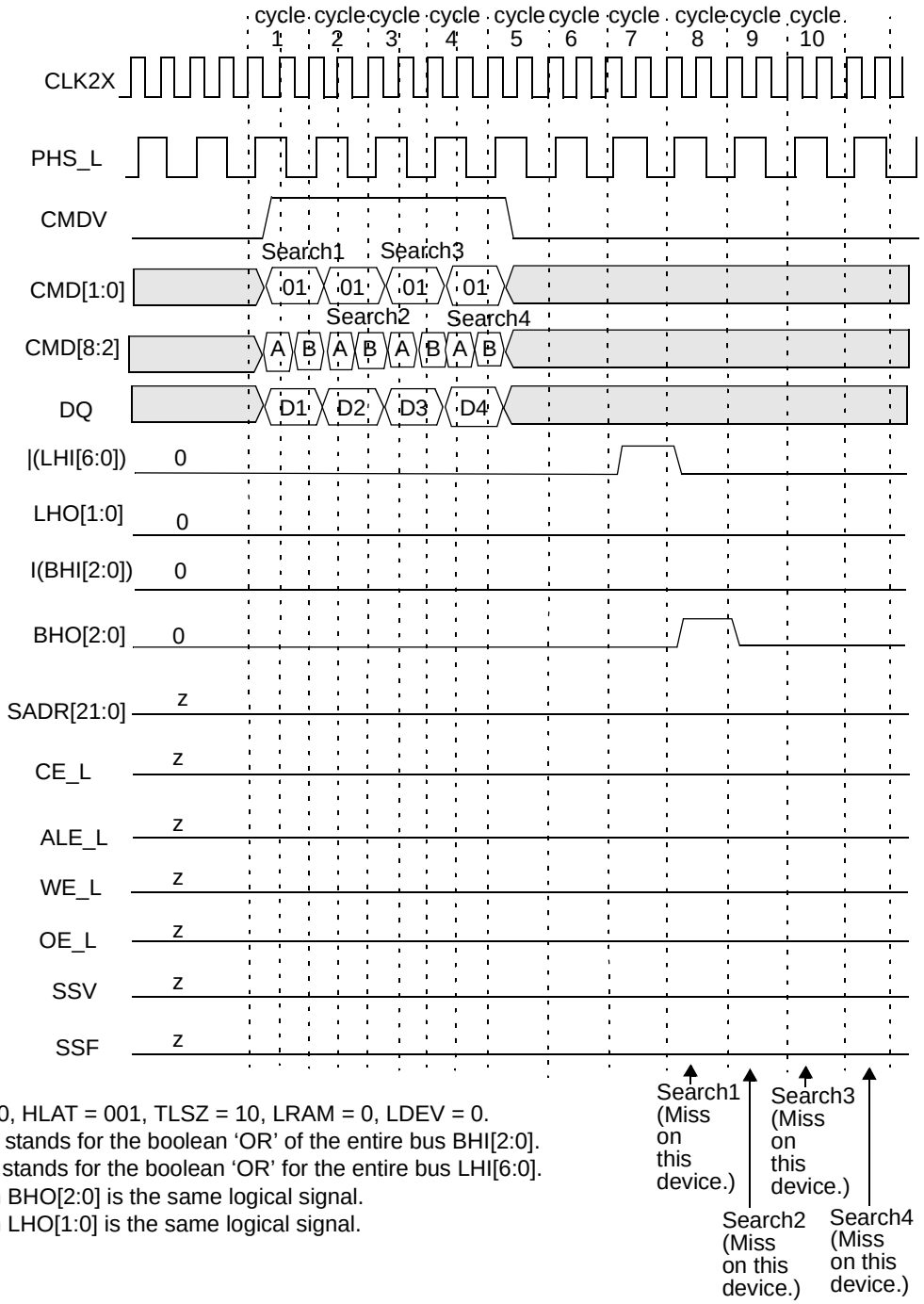
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0)] stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-16. Timing Diagram for Each Device Above the Winning Device in Block Number 1



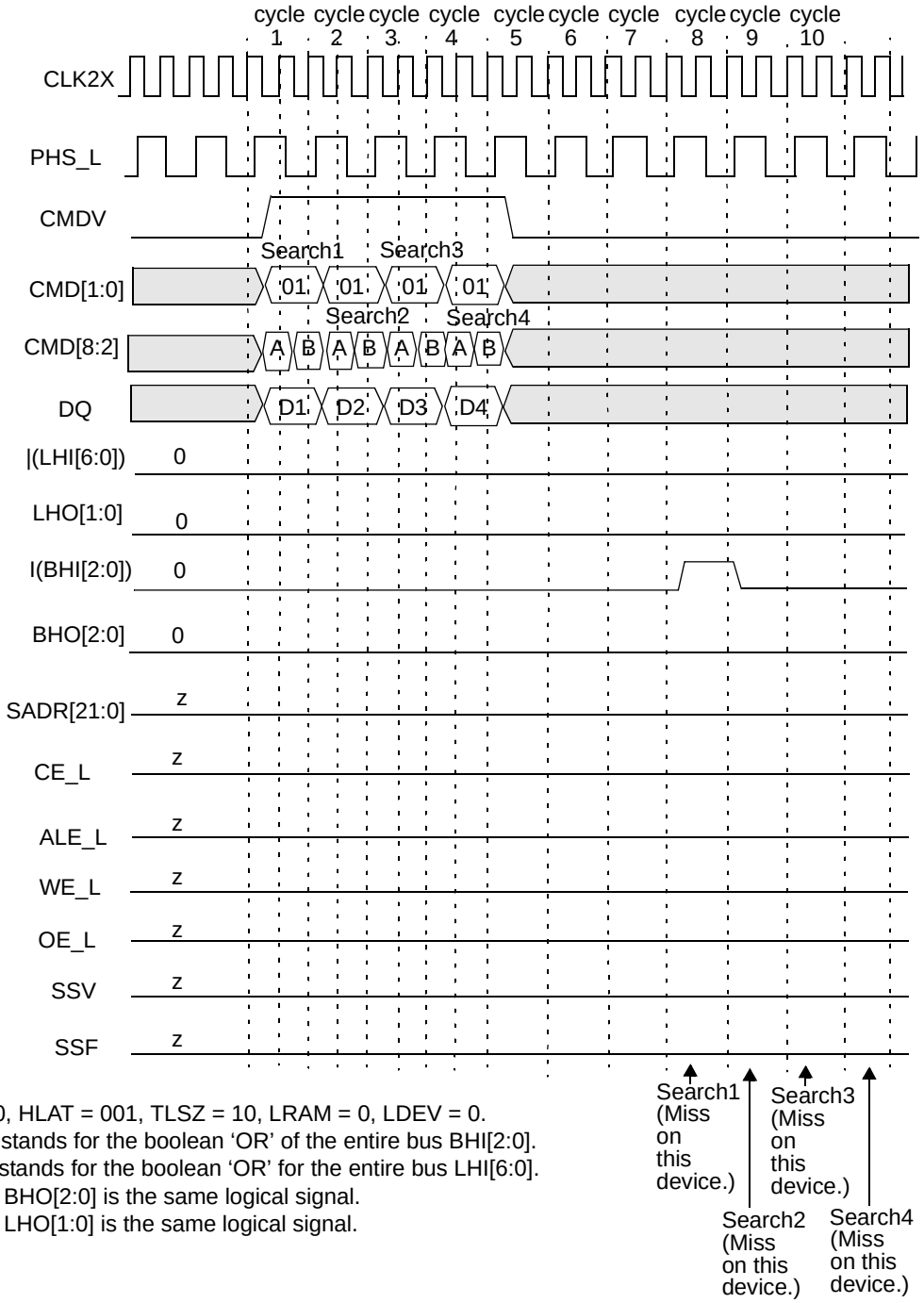
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-17. Timing Diagram for Globally Winning Device in Block Number 1



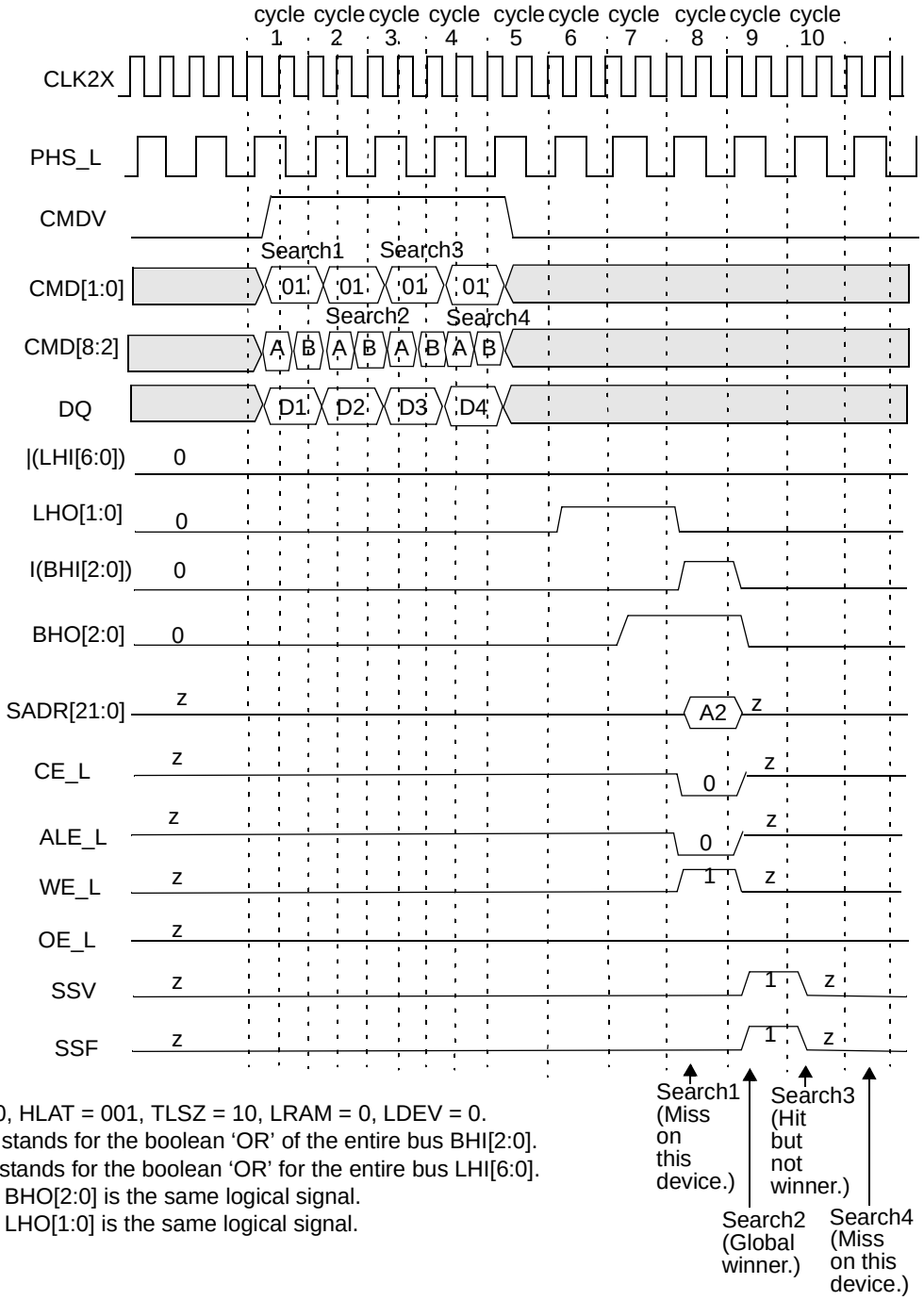
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-18. Timing Diagram for Devices Below the Winning Device in Block Number 1



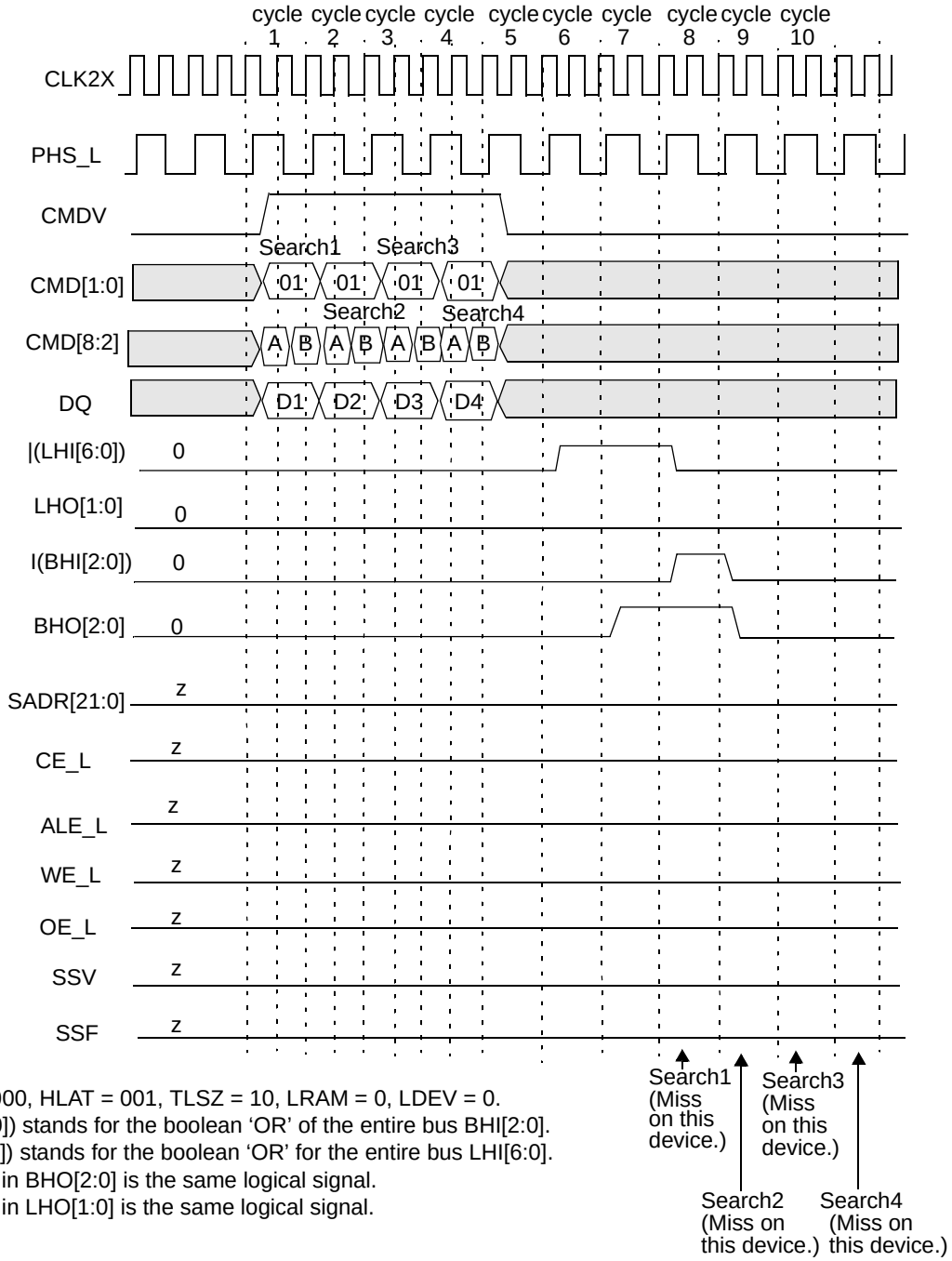
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-19. Timing Diagram for Devices Above the Winning Device in Block Number 2



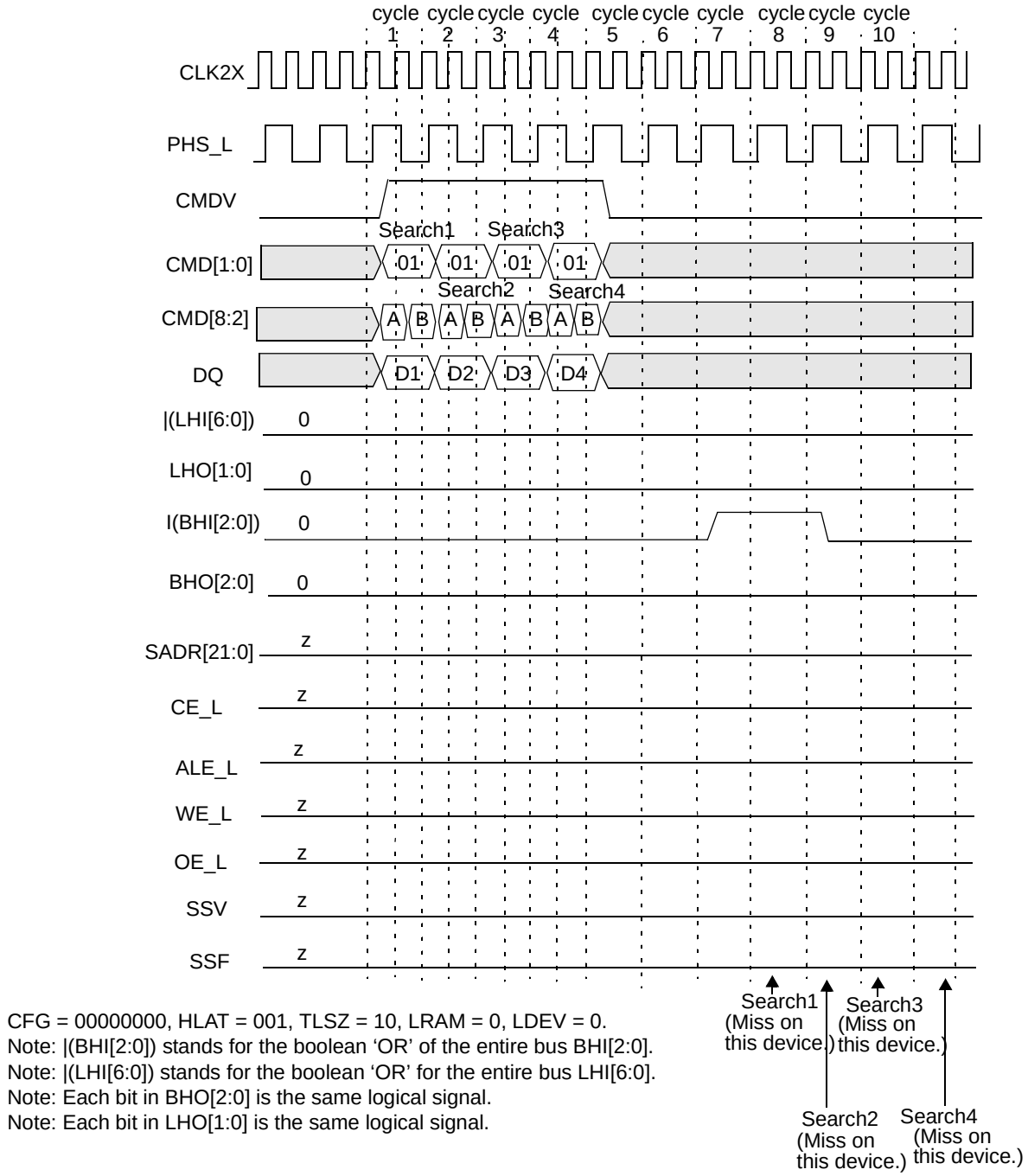
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-20. Timing Diagram for Globally Winning Device in Block Number 2



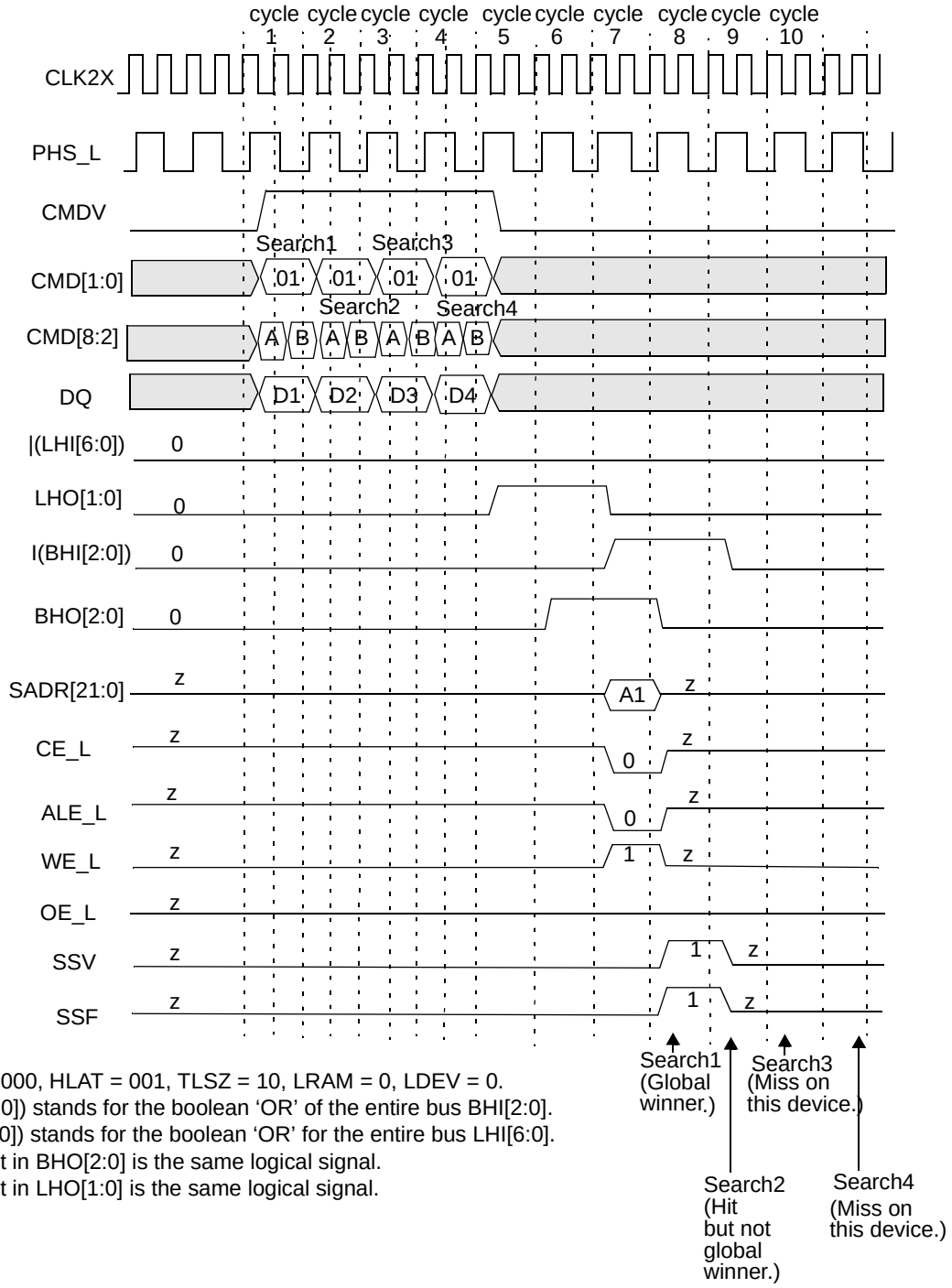
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-21. Timing Diagram for Devices Below the Winning Device in Block Number 2



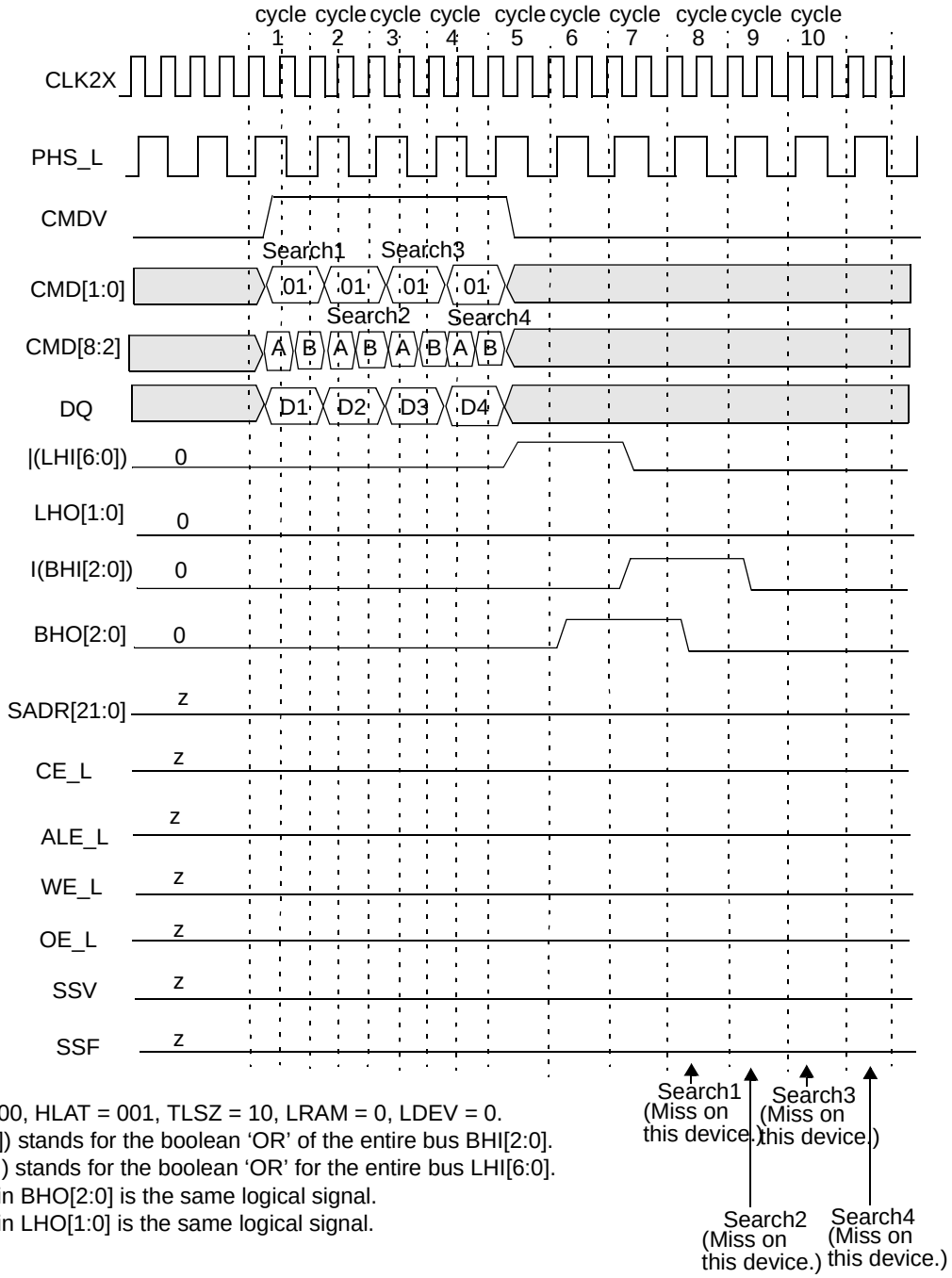
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-22. Timing Diagram for Devices Above the Winning Device in Block Number 3



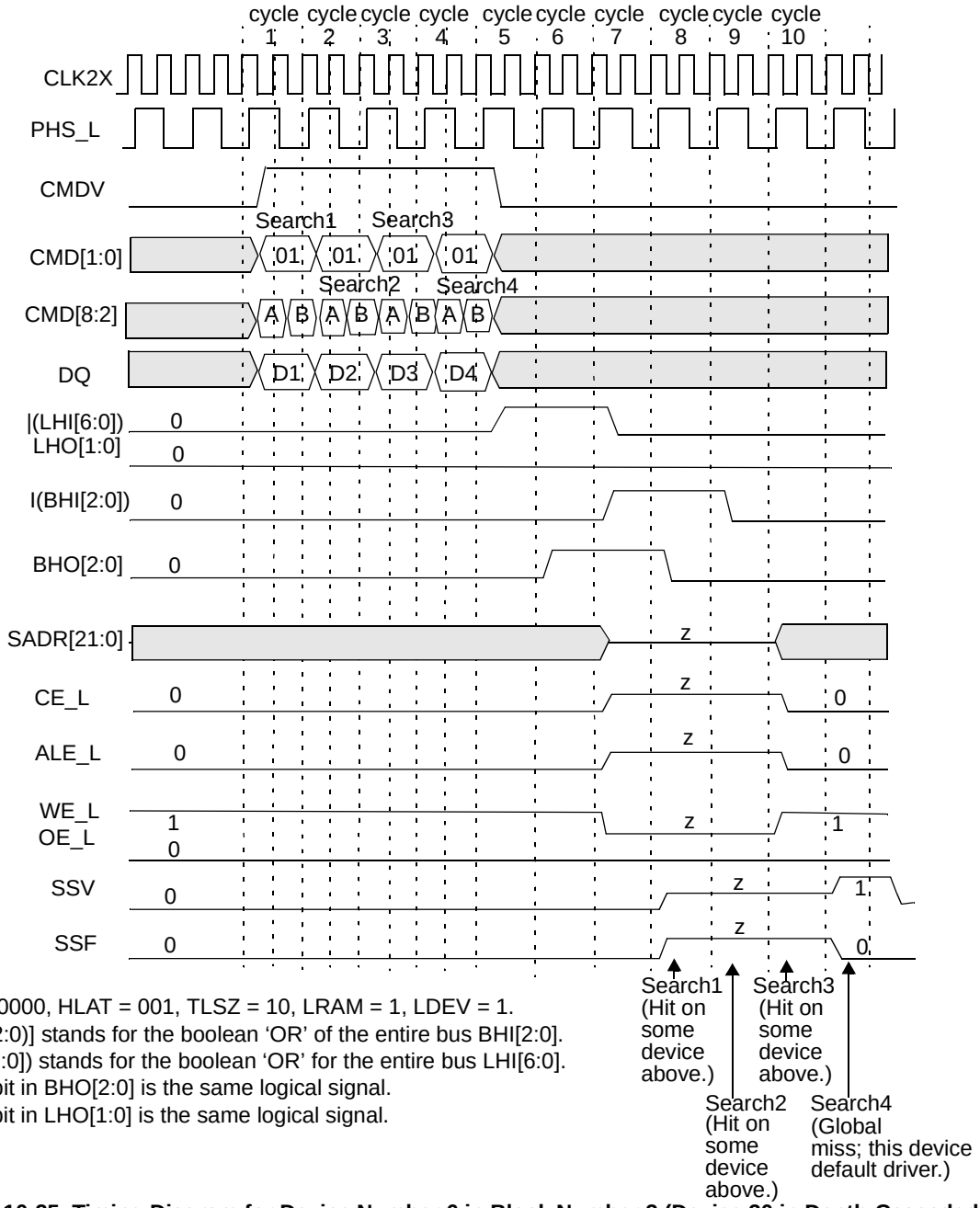
CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-23. Timing Diagram for Globally Winning Device in Block Number 3



CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-24. Timing Diagram for Devices Below the Winning Device in Block Number 3 (Except the Last Device [Device 30])



CFG = 00000000, HLAT = 001, TLSZ = 10, LRAM = 1, LDEV = 1.
Note: |(BHI[2:0)] stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-25. Timing Diagram for Device Number 6 in Block Number 3 (Device 30 in Depth-Cascaded Table)

The following is the sequence of operation for a single 68-bit Search command (also refer to the "Command and Command Parameters," Subsection 10.2 on page 18).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to a logic 0.
- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and applies Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note. For 68-bit searches, the host ASIC must supply the same 68-bit data on DQ[67:0] during both cycles A and B and the even and odd pair of global mask registers selected for the compare must be programmed with the same value.

The logical 68-bit Search operation is shown in *Figure 10-26*. The entire table (31 devices of 68-bit entries) is compared to a 68-bit word K (presented on the DQ bus in both cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected by the GMR Index in the command's cycle A. The 68-bit word K (presented on the DQ bus in both cycles A and B of the command) is also stored in both even and odd comparand register pairs in each of the eight devices and selected by the Comparand Register Index in command's cycle B. In the ×68 configuration, the even comparand register can be subsequently used by the Learn command only in the first non-full device. The word K (presented on the DQ bus in both cycles A and B of the command) is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 100). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 and LDEV = 1 will be the default driver for such missed cycles.

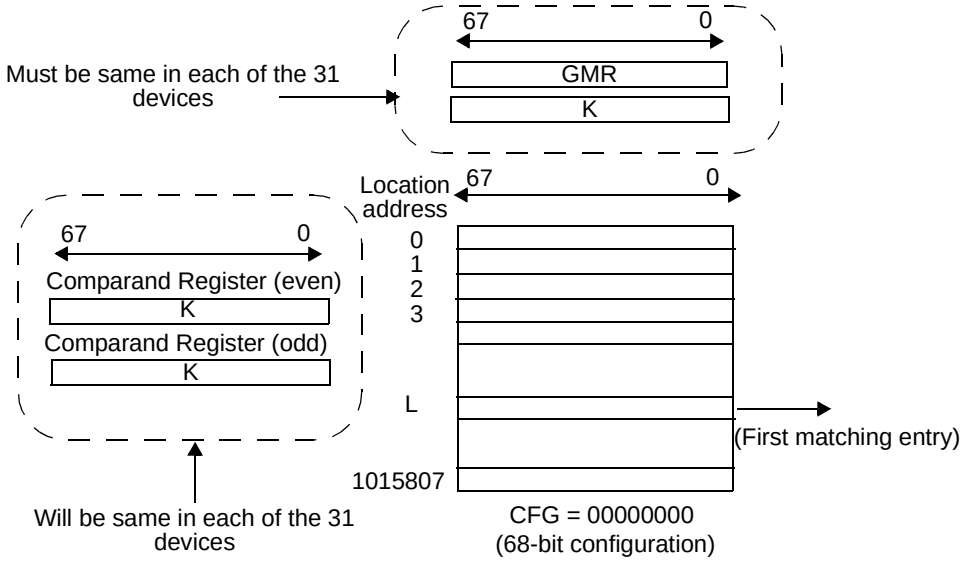


Figure 10-26. ×68 Table with 31 Devices

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 68-bit searches in ×68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit Search command cycle (two CLK2X cycles) is shown in *Table 10-16*.

Table 10-16. The Latency of Search from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K × 68 bits	4
1–8 (TLSZ = 01)	256K × 68 bits	5
1–31 (TLSZ = 10)	996K × 68 bits	6

For up to 31 devices in the table (TLSZ = 10), Search latency from command to SRAM access cycle is 6. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 10-17*.

Table 10-17. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.9 136-bit Search on Tables Configured as ×136 Using a Single CYNSE70064A Device

Figure 10-27 shows the timing diagram for a Search command in the 136-bit-configured table (CFG = 01010101) consisting of a single device for one set of parameters: TLSZ = 00, HLAT = 001, LRAM = 1, and LDEV = 1. The hardware diagram for this Search subsystem is shown in *Figure 10-28*.

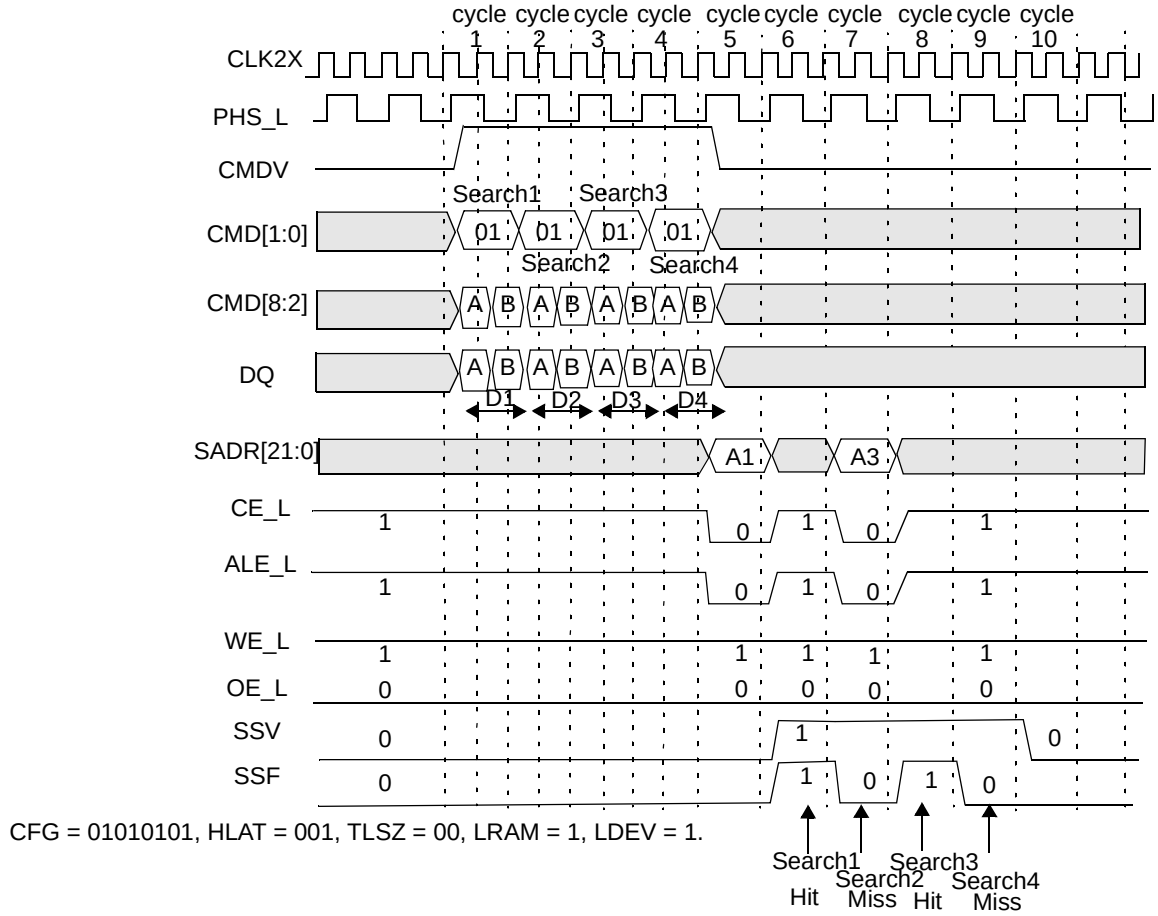


Figure 10-27. Timing Diagram for 136-bit Search (One Device)

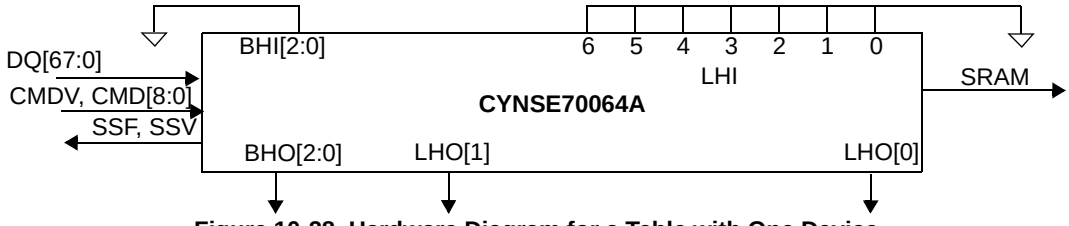


Figure 10-28. Hardware Diagram for a Table with One Device

The following is the operation sequence for a single 136-bit Search command (also refer to “Command and Command Parameters,” Subsection 10.2 on page 18).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) to CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared against all even locations. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and applies the command code of Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with 68-bit data ([67:0]), compared to all odd locations.

Note. For 136-bit searches, the host ASIC must supply two distinct 68-bit data words on DQ[67:0] during cycles A and B. The even-numbered GMR of the pair specified by the GMR Index is used for masking the word in cycle A. The odd-numbered GMR of the pair specified by the GMR Index is used for masking the word in cycle B.

The logical 136-bit Search operation is shown in *Figure 10-29*. The entire table of 136-bit entries is compared to a 136-bit word K (presented on the DQ bus in cycles A and B of the command) using the GMR and the local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's cycle A. The 136-bit word K (presented on the DQ bus in cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command's cycle B. The two comparand registers can subsequently be used by the Learn command with the even comparand register stored in an even location, and the odd comparand register stored in an adjacent odd location. The word K (presented on the DQ bus in cycles A and B of the command) is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 100). ***Note***. The matching address is always going to an even address for a 136-bit Search.

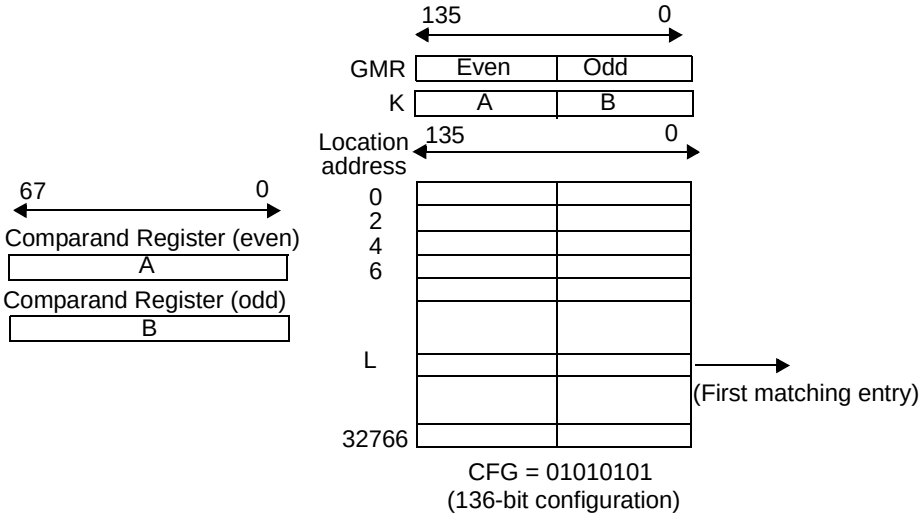


Figure 10-29. ×136 Table with One Device

The Search command is a pipelined operation that executes searches at half the rate of the frequency of CLK2X for 136-bit searches in ×136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit Search command cycle (two CLK2X cycles) is shown in *Table 10-18*.

Table 10-18. The Latency of Search from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K × 136 bits	4
1–8 (TLSZ = 01)	128K × 136 bits	5
1–31 (TLSZ = 10)	496K × 136 bits	6

For a single device in the table with TLSZ = 00, the latency of the Search from command to SRAM access cycle is 4. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 10-19*.

Table 10-19. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.10 136-bit Search on Tables Configured as ×136 Using up to Eight CYNSE70064A Devices

The hardware diagram of the Search subsystem of eight devices is shown in *Figure 10-30*. The following are parameters programmed into the eight devices.

- First seven devices (devices 0–6): CFG = 01010101, TLSZ = 01, HLAT = 010, LRAM = 0, and LDEV = 0.
- Eighth device (device 7): CFG = 01010101, TLSZ = 01, HLAT = 010, LRAM = 1, and LDEV = 1.

Note. All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (device number 7 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (devices 0 through 6 in this case).

Figure 10-31 shows the timing diagram for a Search command in the 136-bit-configured table of eight devices for device 0. *Figure 10-32* shows the timing diagram for a Search command in the 136-bit-configured table consisting of eight devices for device number 1. *Figure 10-33* shows the timing diagram for a Search command in the 136-bit configured table consisting of eight devices for device number 7 (the last device in this specific table). For these timing diagrams, four 136-bit searches are performed sequentially, and the following Hit/Miss assumptions were made (see *Table 10-20*).

Table 10-20. Hit/Miss Assumption

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Miss
Device 1	Miss	Hit	Hit	Miss
Devices 2–6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

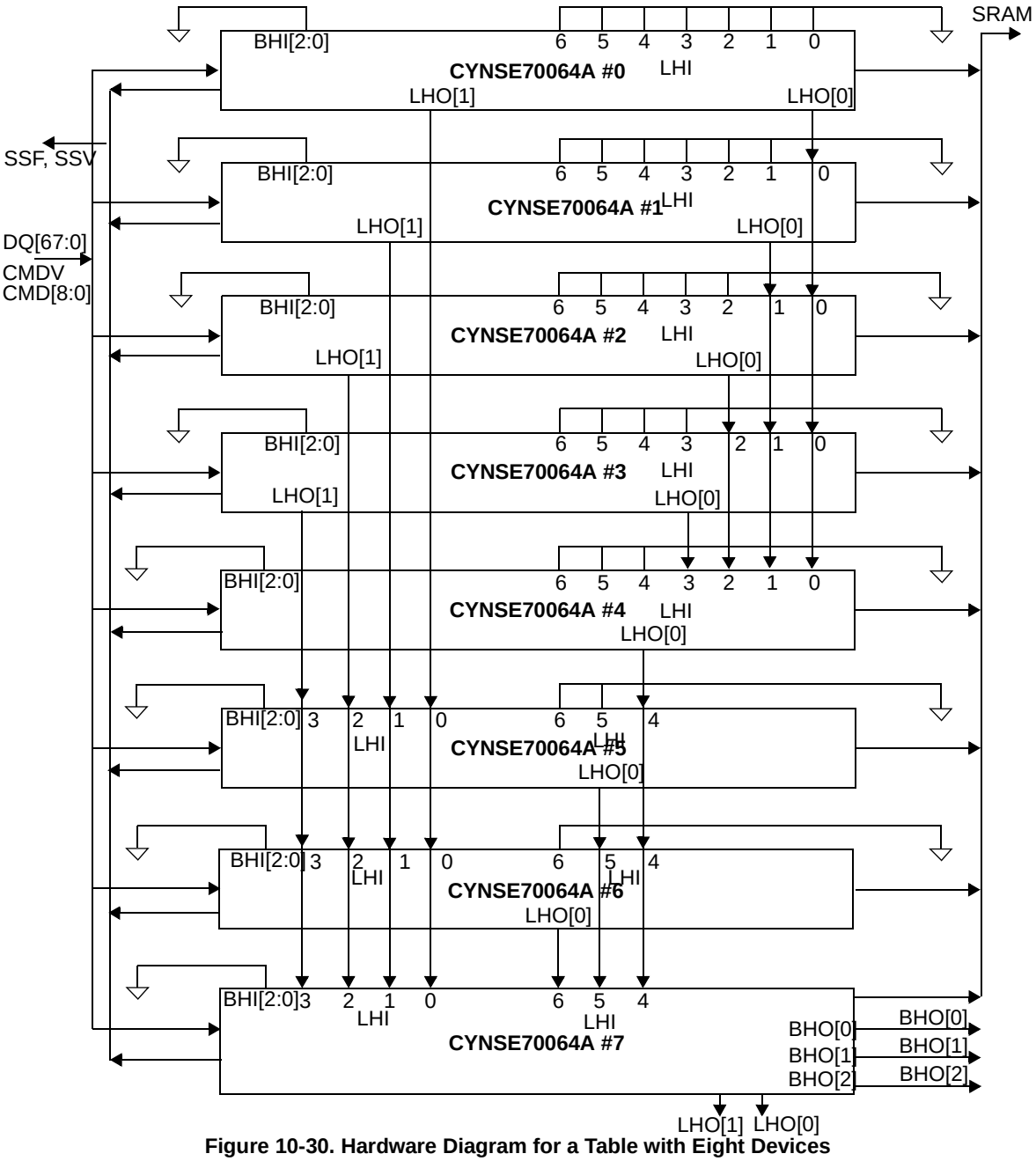
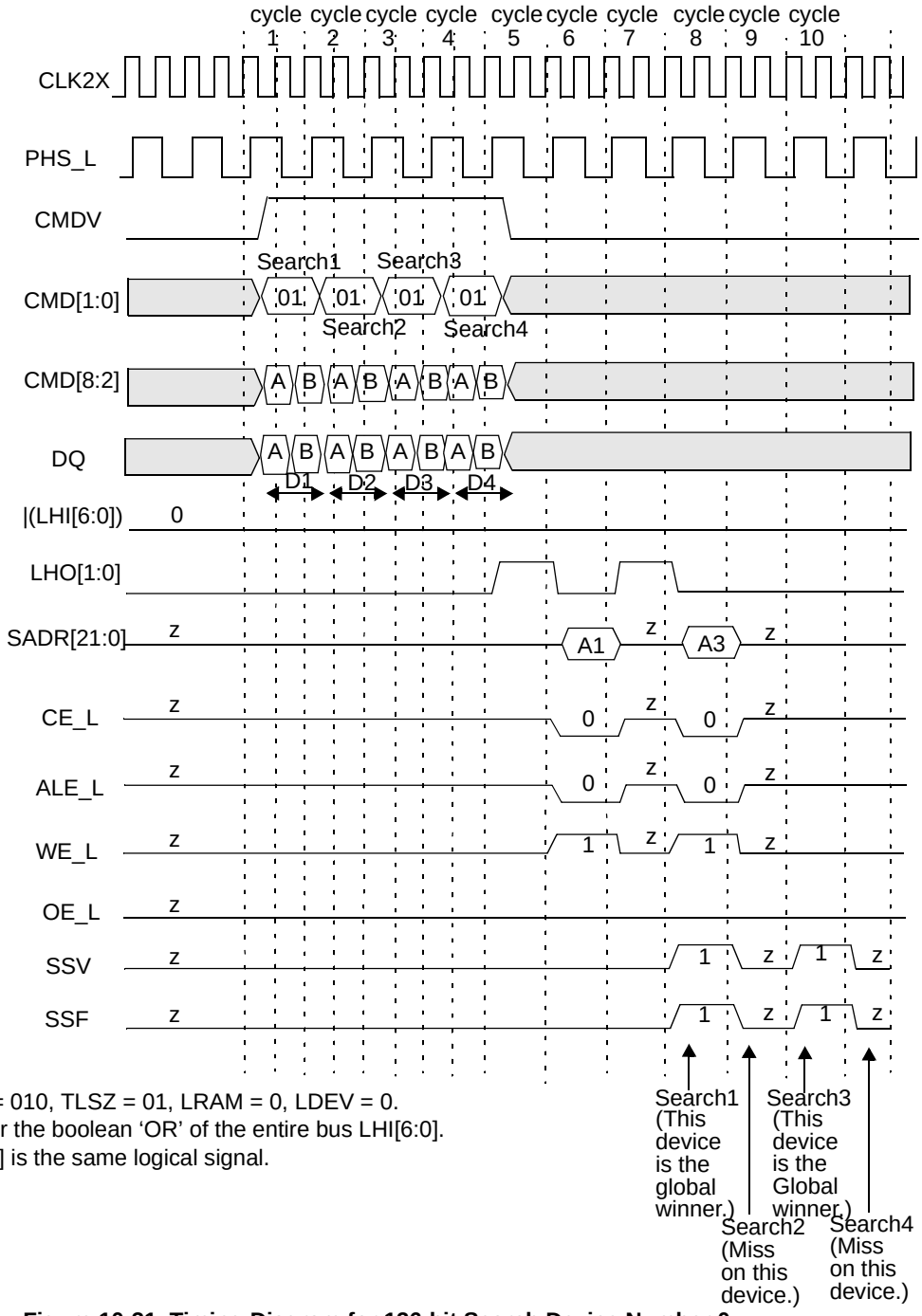
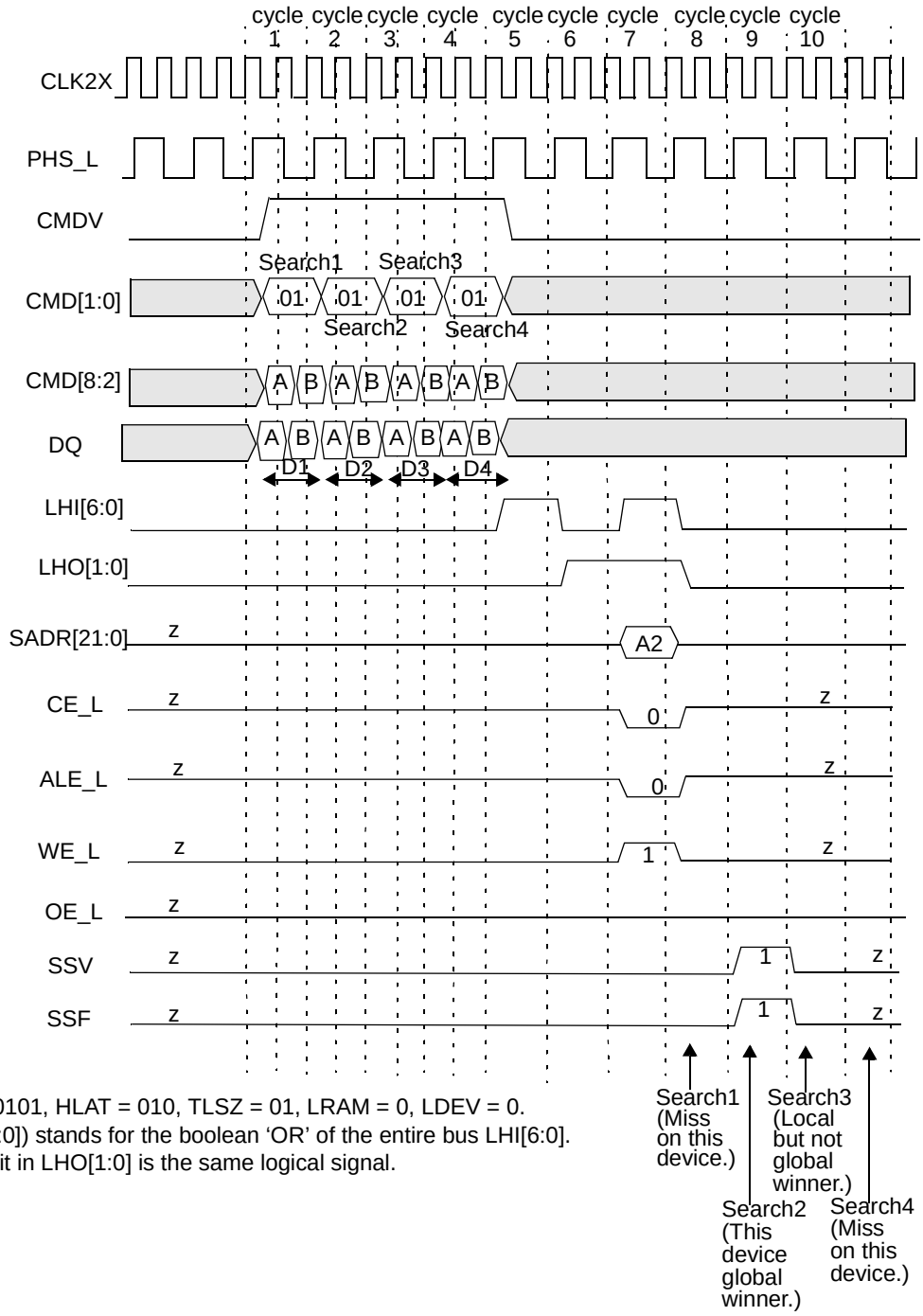


Figure 10-30. Hardware Diagram for a Table with Eight Devices



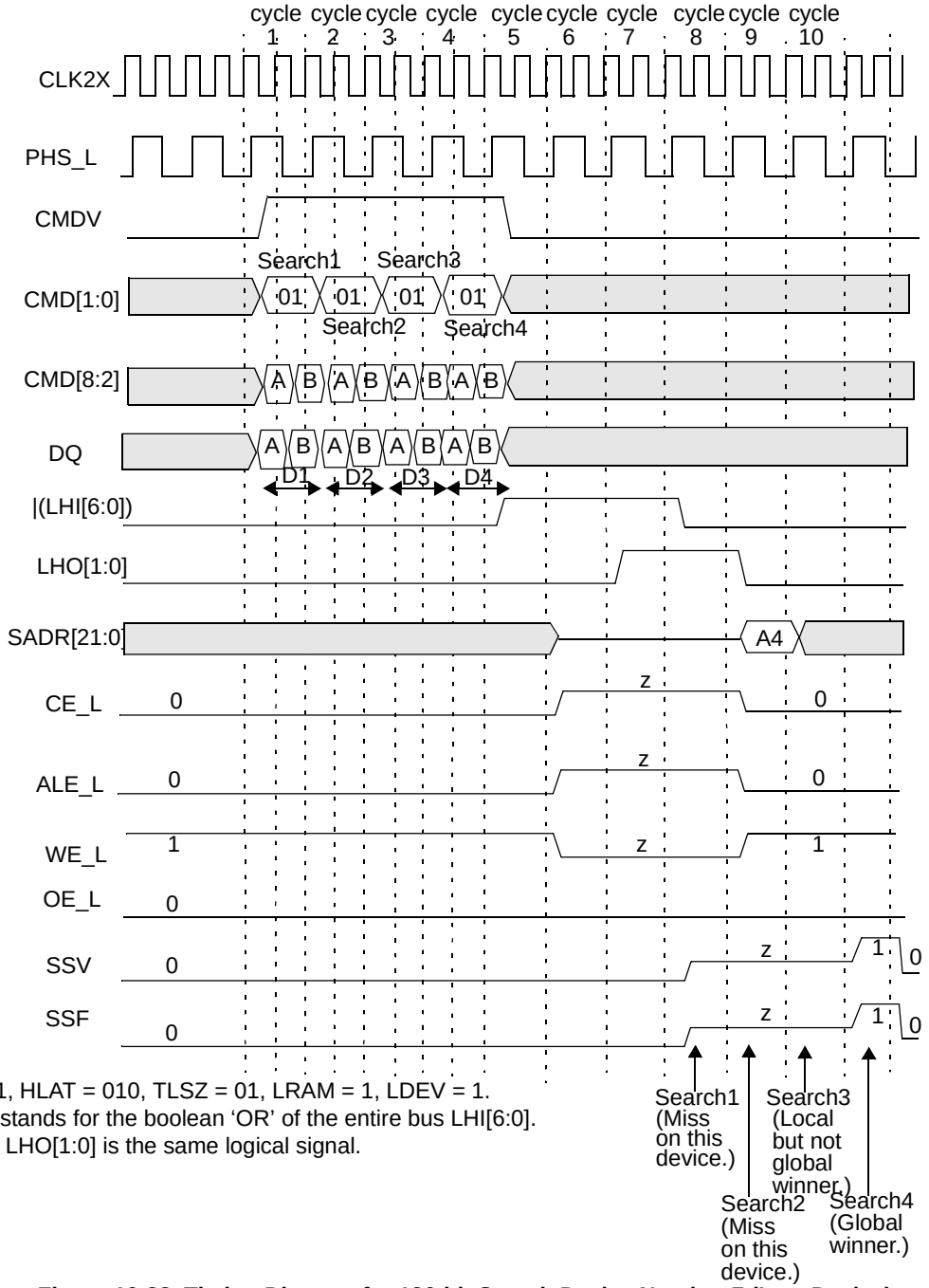
CFG = 01010101, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-31. Timing Diagram for 136-bit Search Device Number 0



CFG = 01010101, HLAT = 010, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-32. Timing Diagram for 136-bit Search Device Number 1



CFG = 01010101, HLAT = 010, TLSZ = 01, LRAM = 1, LDEV = 1.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-33. Timing Diagram for 136-bit Search Device Number 7 (Last Device)

The following is the sequence of operation for a single 136-bit Search command (also see Subsection 10.2, "Commands and Command Parameters" on page 18).

- **Cycle A**: The host ASIC drives CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:7] signals must be driven with the same bits that will be driven by this device on SADR[21:20] if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) in order to be compared against all even locations. The CMD[2] signal must be driven to a logic 0.
- **Cycle B**: The host ASIC continues to drive CMDV HIGH and to apply the command code for Search command (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the SSR index that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with 68-bit data ([67:0]) compared against all odd locations.

The logical 136-bit Search operation is shown in *Figure 10-34*. The entire table (eight devices of 136-bit entries) is compared to a 136-bit word K (presented on the DQ bus in cycles A and B of the command) using the GMR and local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's cycle A.

The 136-bit word K (presented on the DQ bus in cycles A and B of the command) is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's cycle B. In ×136 configurations, the even and odd comparand registers can subsequently be used by the Learn command in only one of the devices (the first non-full device). The word K (presented on the DQ bus in cycles A and B of the command) is compared to each entry in the table starting at location 0. The first matching entry's location, address L, is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see "SRAM Addressing" on page 100). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 (the default driving device for the SRAM bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles. ***Note***. During 136-bit searches of 136-bit-configured tables, the Search hit will always be at an even address.

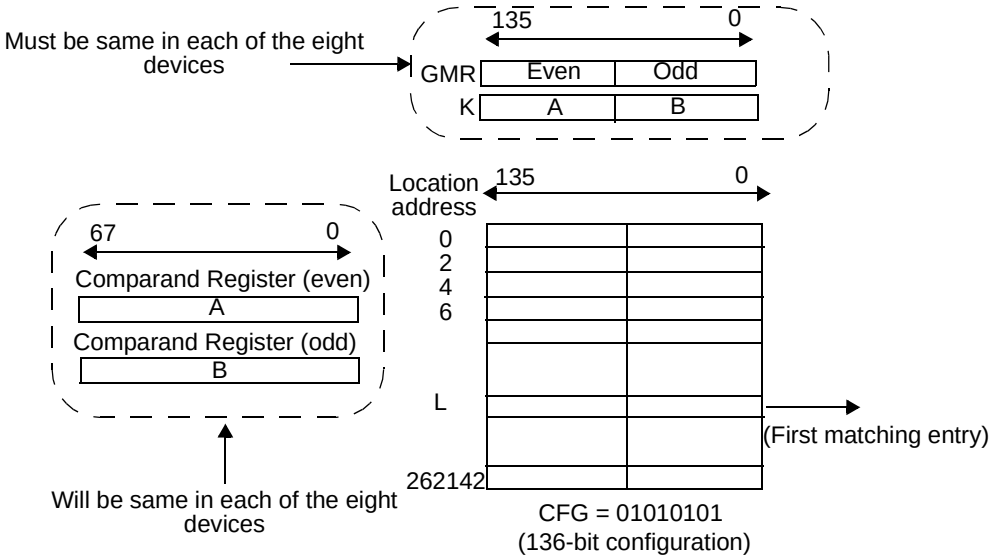


Figure 10-34. ×136 Table with Eight Devices

The Search command is a pipelined operation and executes a Search at half the rate of the frequency of CLK2X for 136-bit searches in ×136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit Search command cycle (two CLK2X cycles) is shown in *Table 10-21*.

Table 10-21. Search Latency from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K × 136 bits	4
1–8 (TLSZ = 01)	128K × 136 bits	5
1–31 (TLSZ = 10)	496K × 136 bits	6

For one to eight devices in the table and TLSZ = 01, the latency of a Search from command to SRAM access cycle is 5. In addition, SSV and SSF shift further to the right for different values of HLAT as specified in *Table 10-22*.

Table 10-22. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.11 136-bit Search on Tables Configured as ×136 Using up to 31 CYNSE70064A Devices

The hardware diagram of the Search subsystem of 31 devices is shown in *Figure 10-35*. Each of the four blocks in the diagram represents a block of eight CYNSE70064A devices (except the last, which has seven devices). The diagram for a block of eight devices is shown in *Figure 10-36*. Following are the parameters programmed into the 31 devices.

- First thirty devices (devices 0–29): CFG = 01010101, TLSZ = 10, HLAT = 001, LRAM = 0, and LDEV = 0.
- Thirty-first device (device 30): CFG = 01010101, TLSZ = 10, HLAT = 001, LRAM = 1, and LDEV = 1.

Note. All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (device number 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the Hit/Miss assumptions defined in *Table 10-23*. For the purpose of illustrating timings, it is further assumed that the there is only one device with a matching entry in each of the blocks. *Figure 10-37* shows the timing diagram for a Search command in the 136-bit-configured table (31 devices) for each of the eight devices in block number 0. *Figure 10-38* shows the timing diagram for Search command in the 68-bit-configured table (31 devices) for all the devices in block number 1 above the winning device in that block. *Figure 10-39* shows the timing diagram for the globally winning device (the final winner within its own block and all blocks) in block number 1. *Figure 10-40* shows the timing diagram for all the devices below the globally winning device in block number 1. *Figure 10-41*, *Figure 10-42*, and *Figure 10-43* respectively show the timing diagrams of the devices above globally winning device, the globally winning device and devices below the globally winning device for block number 2. *Figure 10-44*, *Figure 10-45*, *Figure 10-46*, and *Figure 10-47* respectively show the timing diagrams of the devices above the globally winning device, the globally winning device, and devices below the globally winning device except the last device (device 30), and the last device (device 30) for block number 3.

The 136-bit Search operation is pipelined and executes as follows. Four cycles from the Search command, each of the devices knows the outcome internal to it for that operation. In the fifth cycle after the Search command, the devices in a block (being less than or equal to eight devices resolving the winner within them using the LHI[6:0] and LHO[1:0] signalling mechanism) arbitrate for a winner amongst them. In the sixth cycle after the Search command, the blocks (of devices) resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanism. The winning device in the winning block is the global winning device for a Search operation.

Table 10-23. Hit/Miss Assumption

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

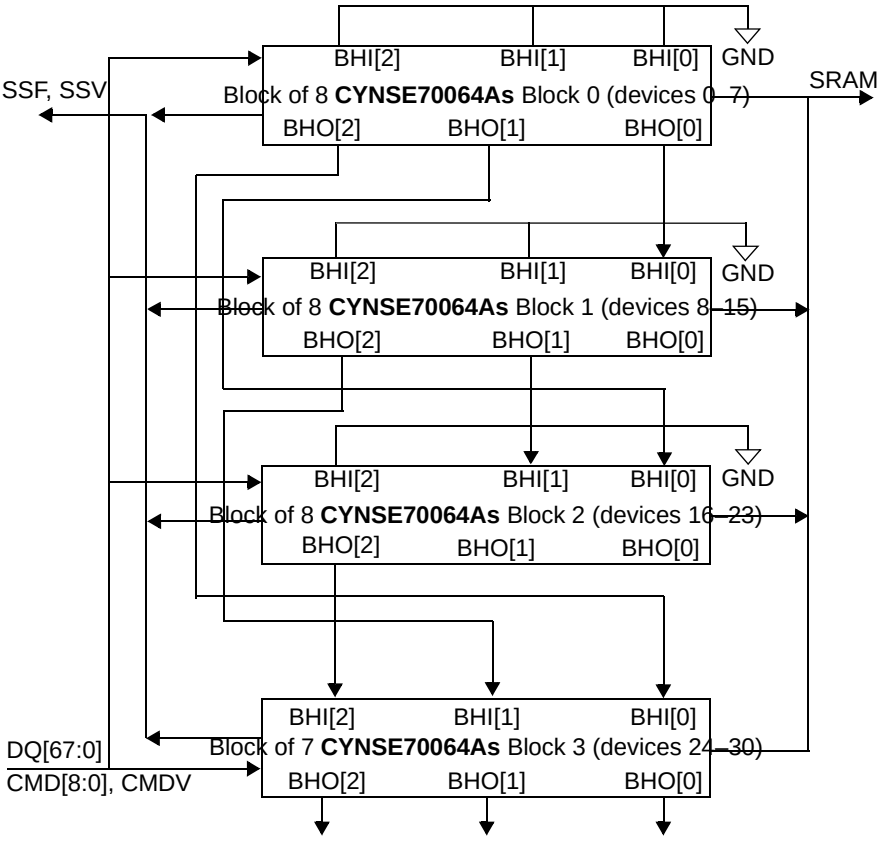


Figure 10-35. Hardware Diagram for a Table with 31 Devices

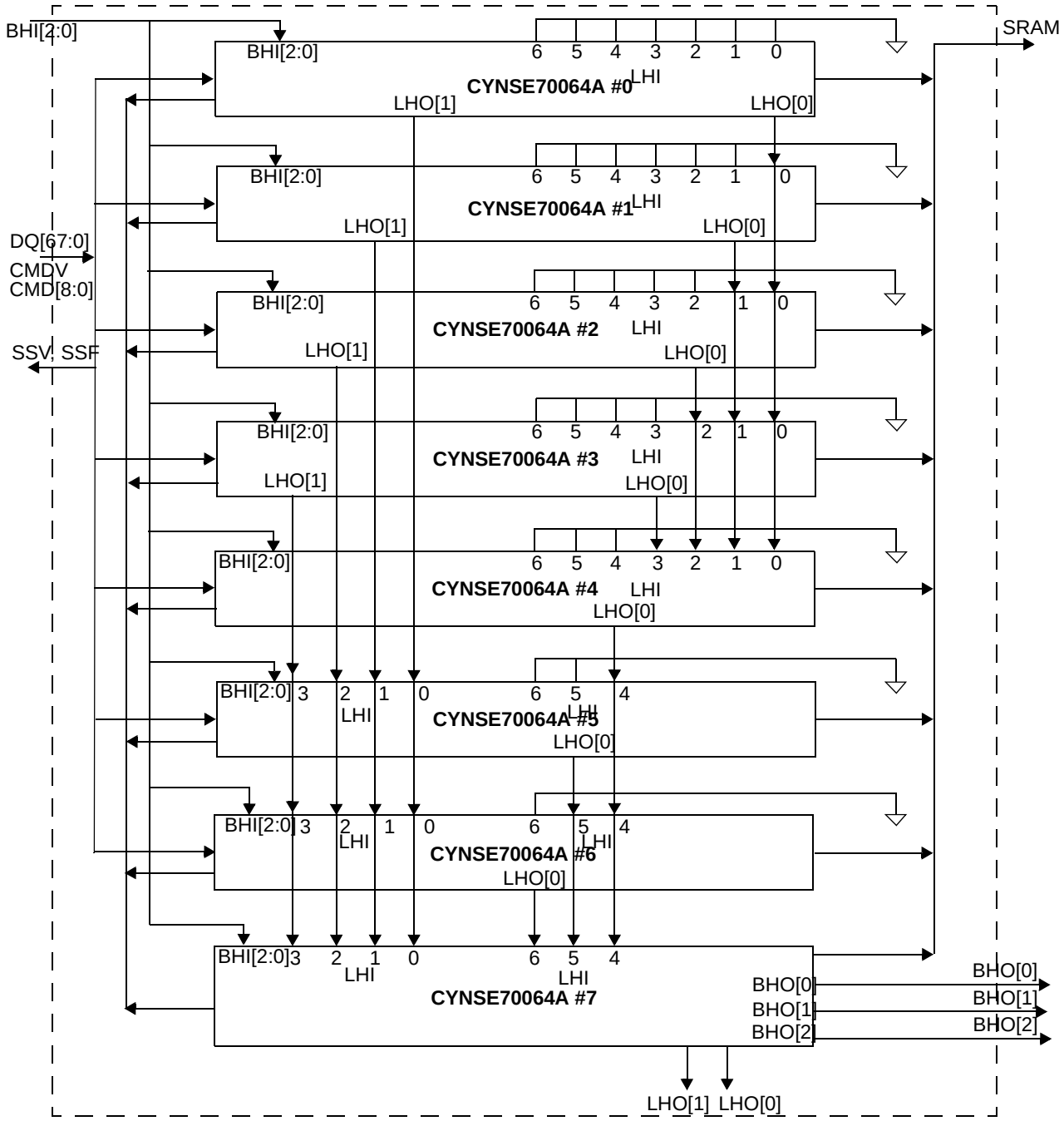
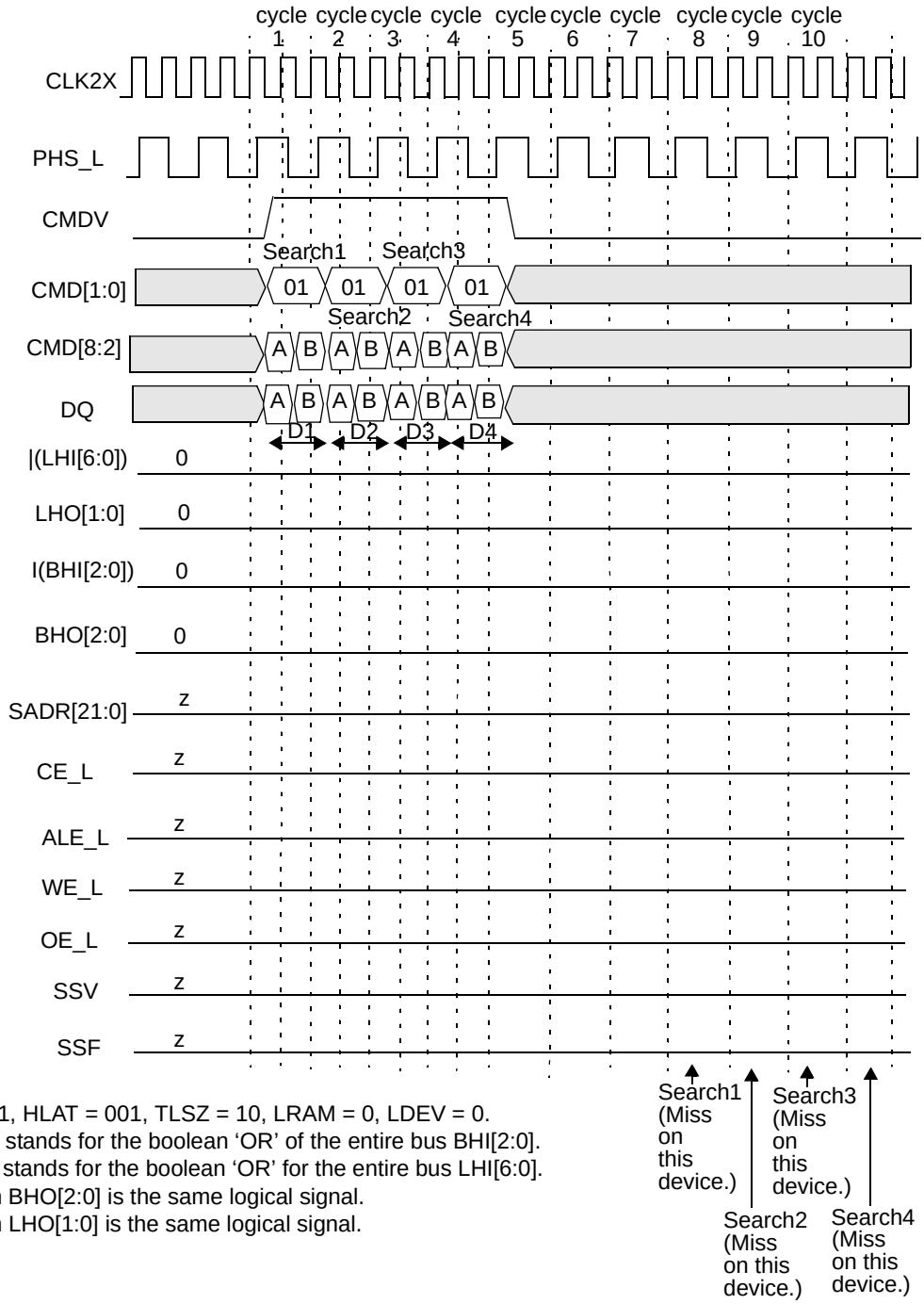
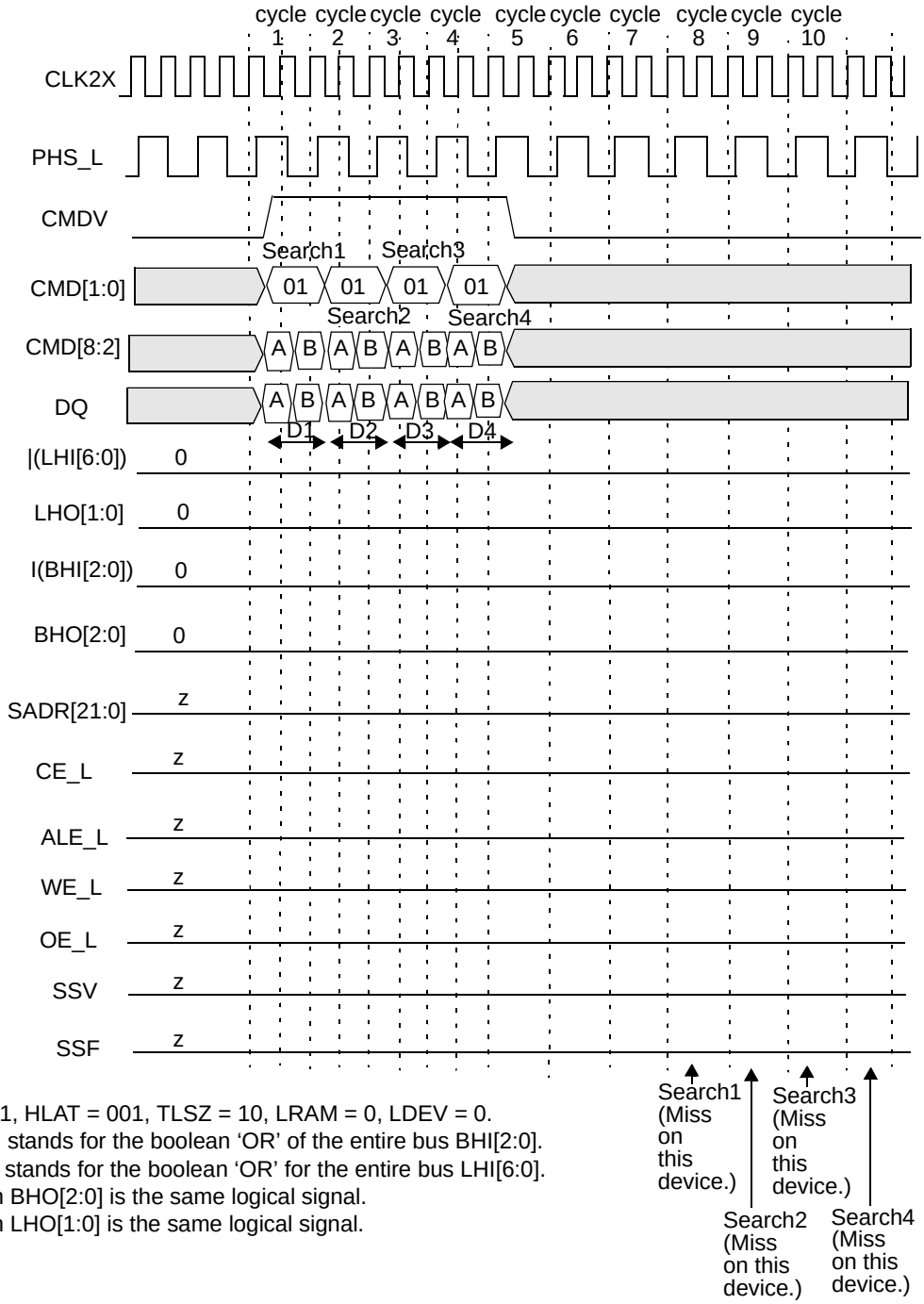


Figure 10-36. Hardware Diagram for a Block of Up to Eight Devices



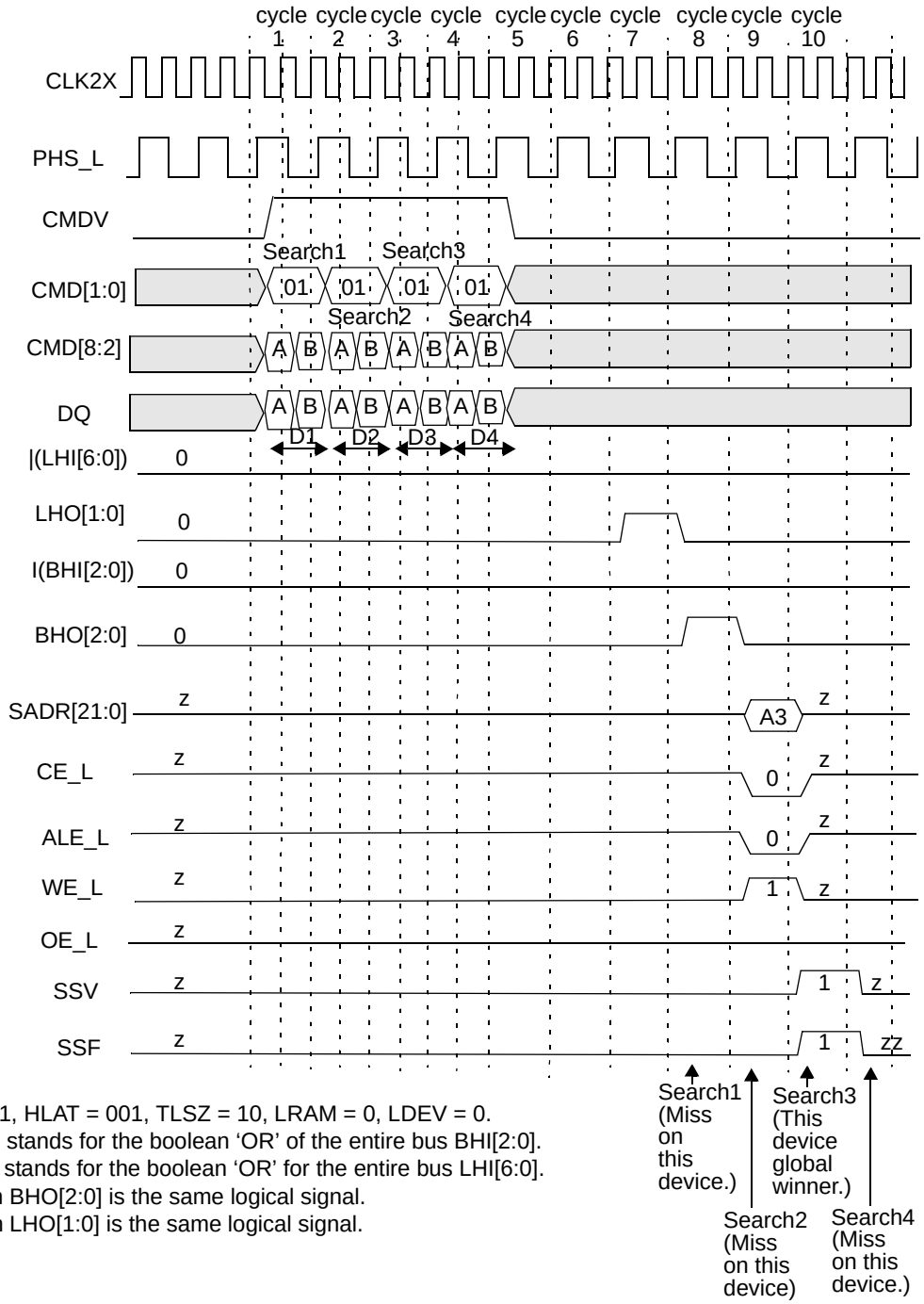
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-37. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



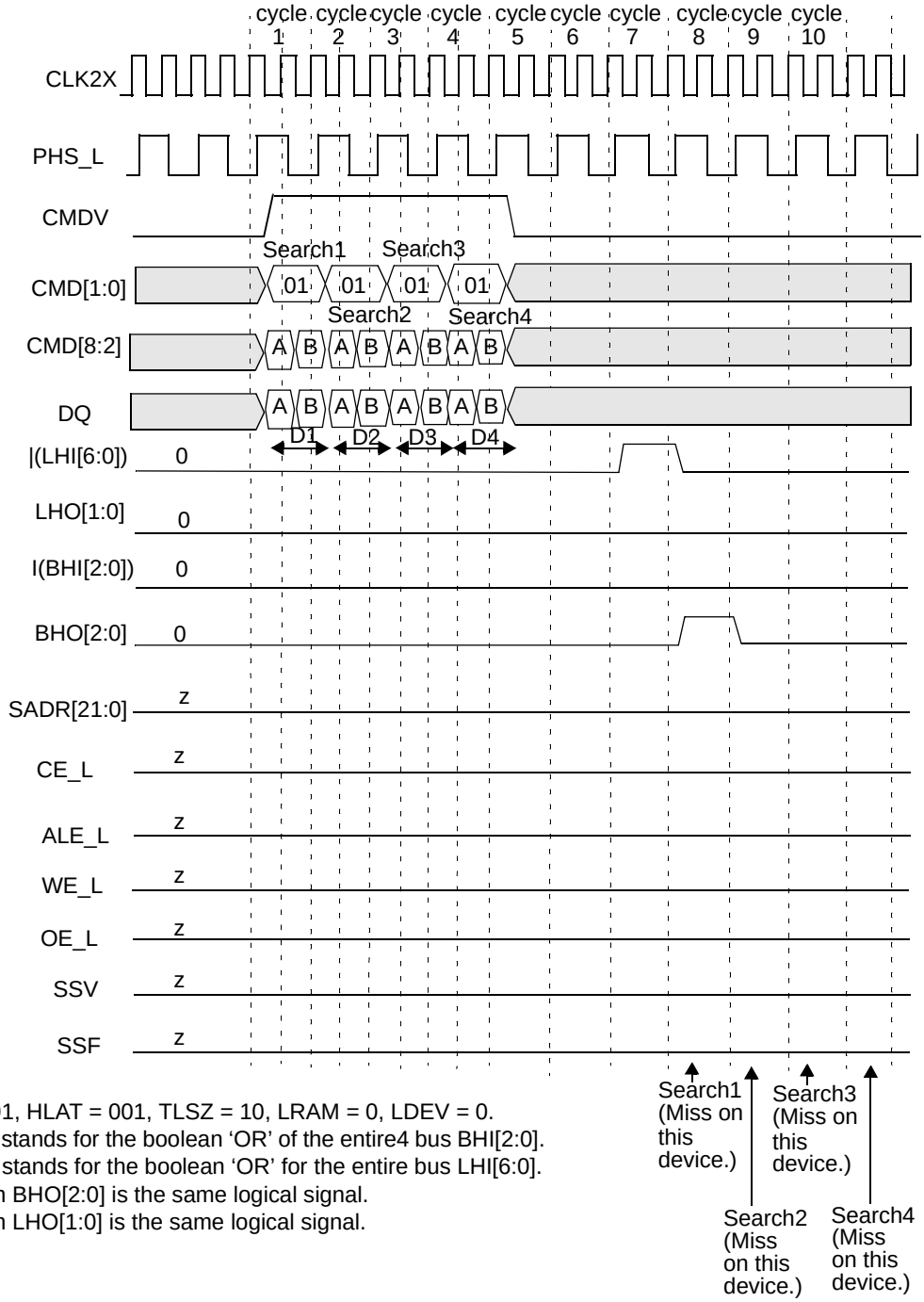
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-38. Timing Diagram for Each Device Above the Winning Device in Block Number 1



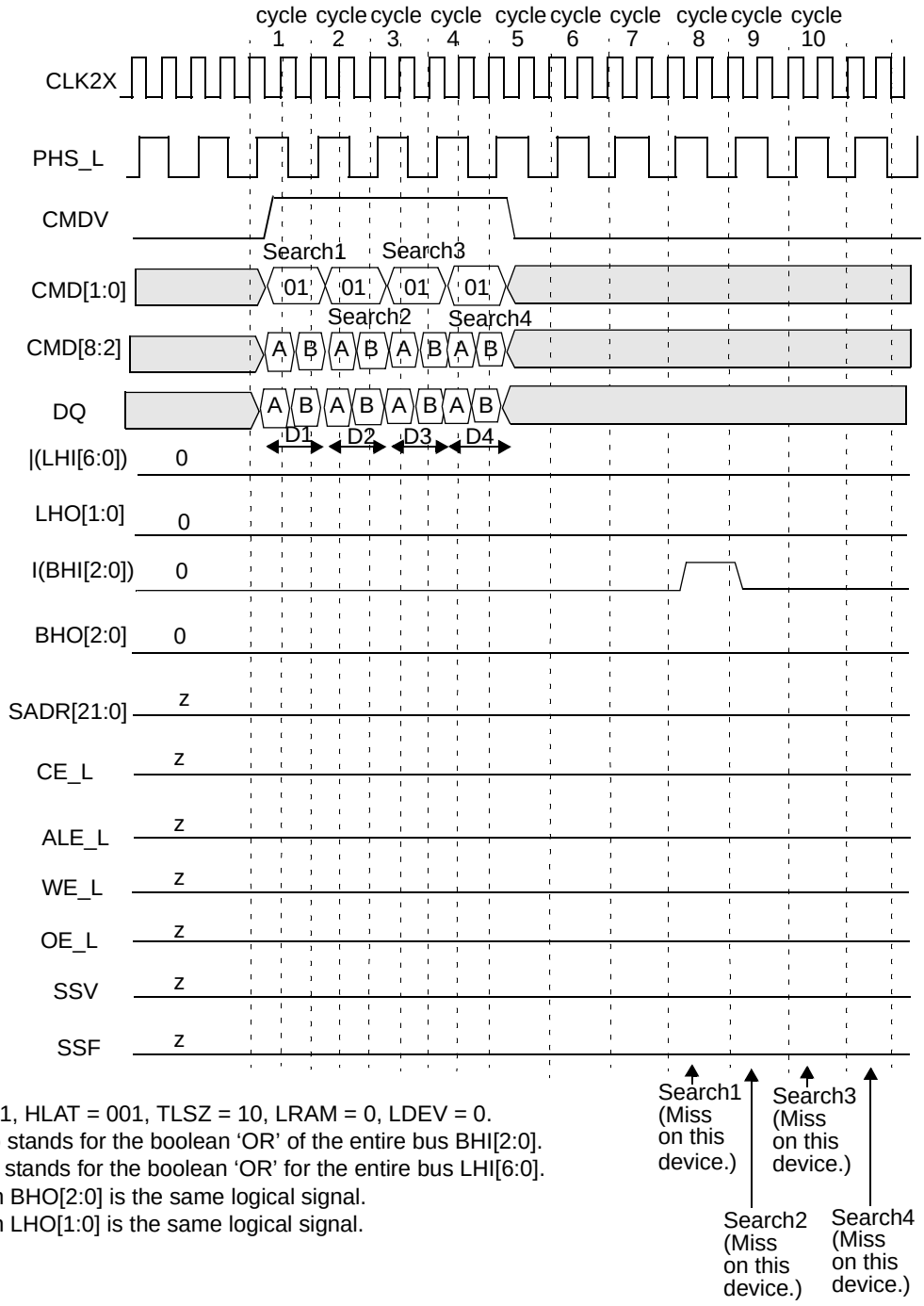
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-39. Timing Diagram for Globally Winning Device in Block Number 1



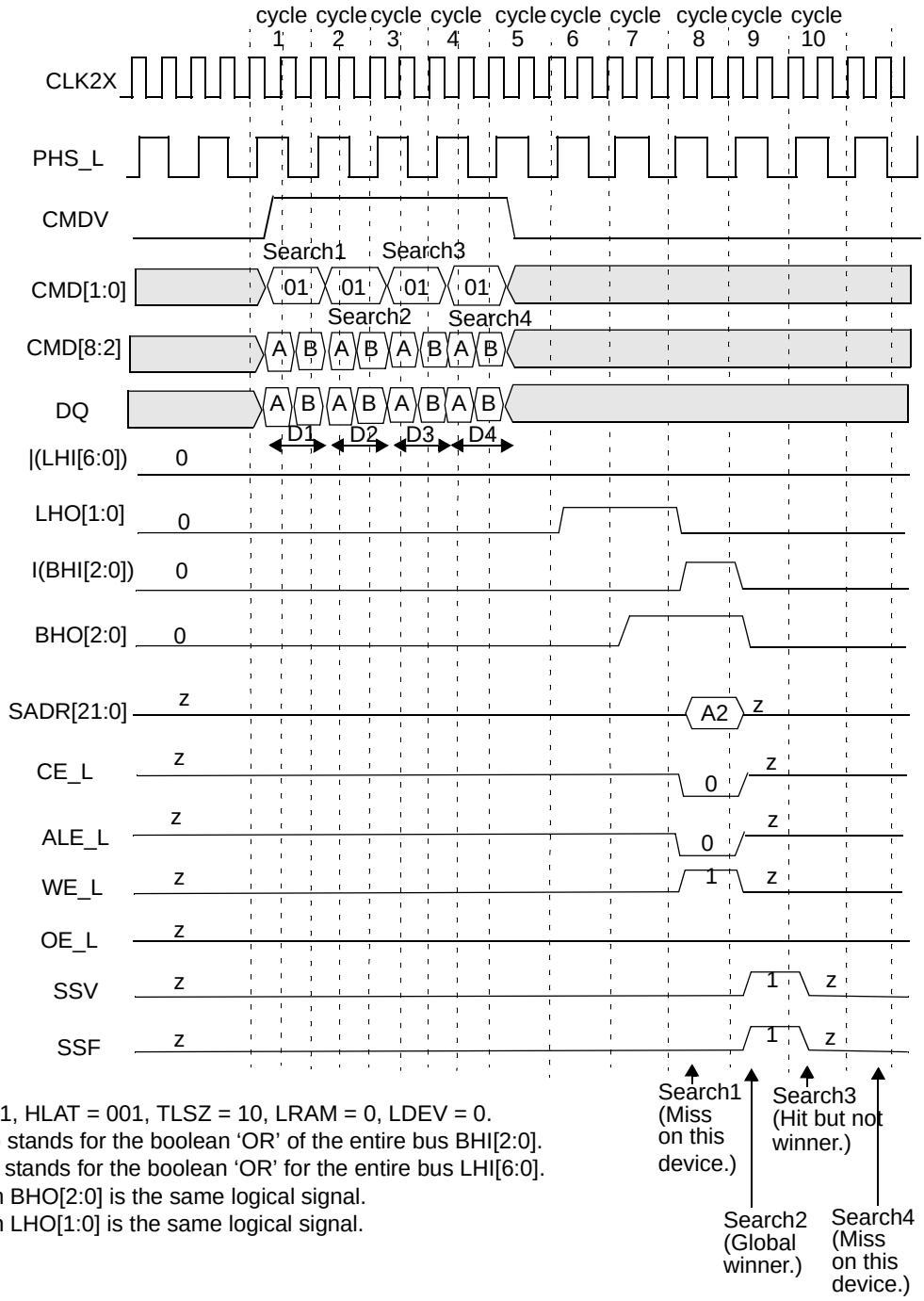
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0] stands for the boolean 'OR' of the entire4 bus BHI[2:0].
Note: |(LHI(6:0) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-40. Timing Diagram for Devices Below the Winning Device in Block Number 1



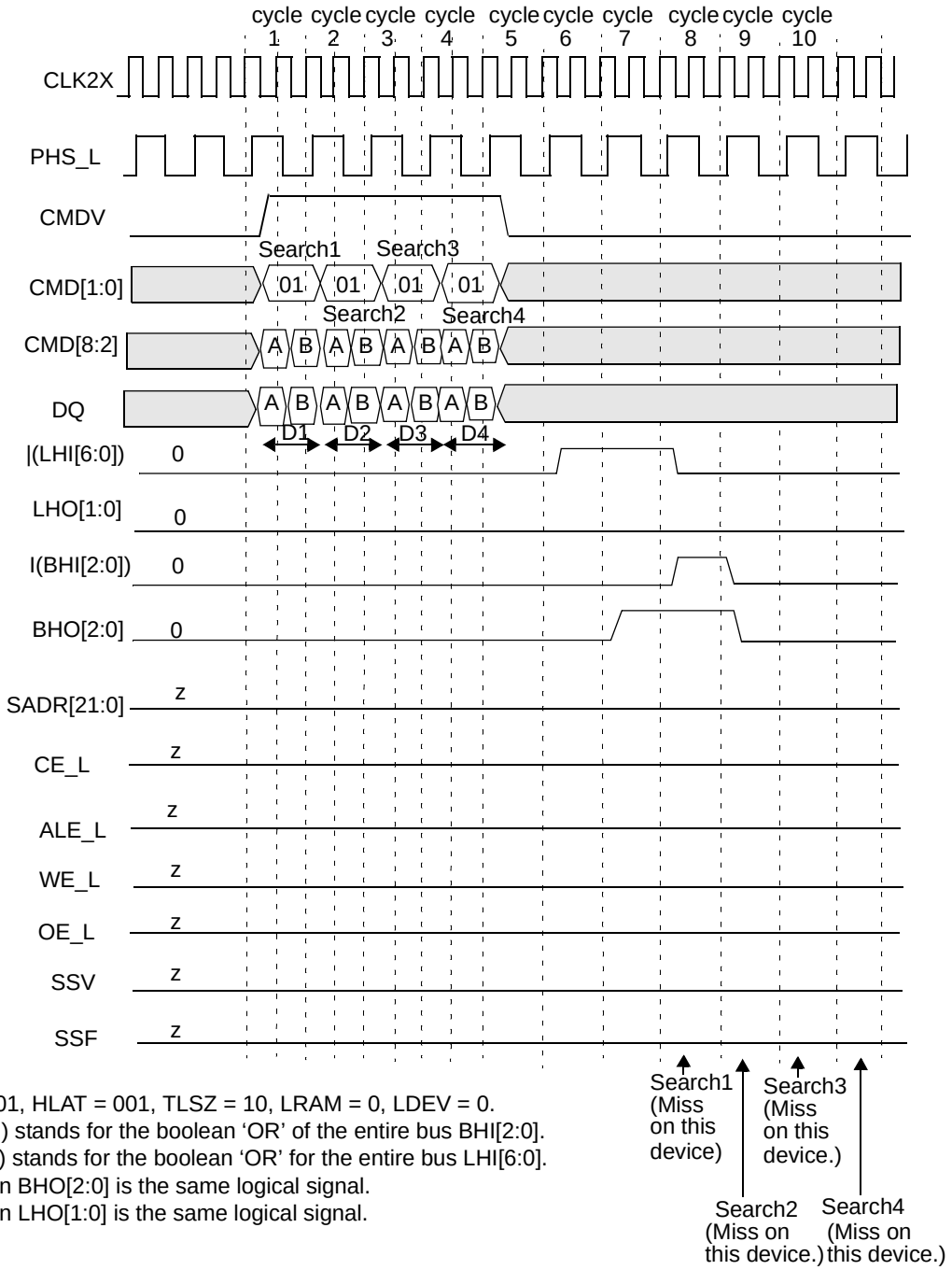
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-41. Timing Diagram for Devices Above the Winning Device in Block Number 2



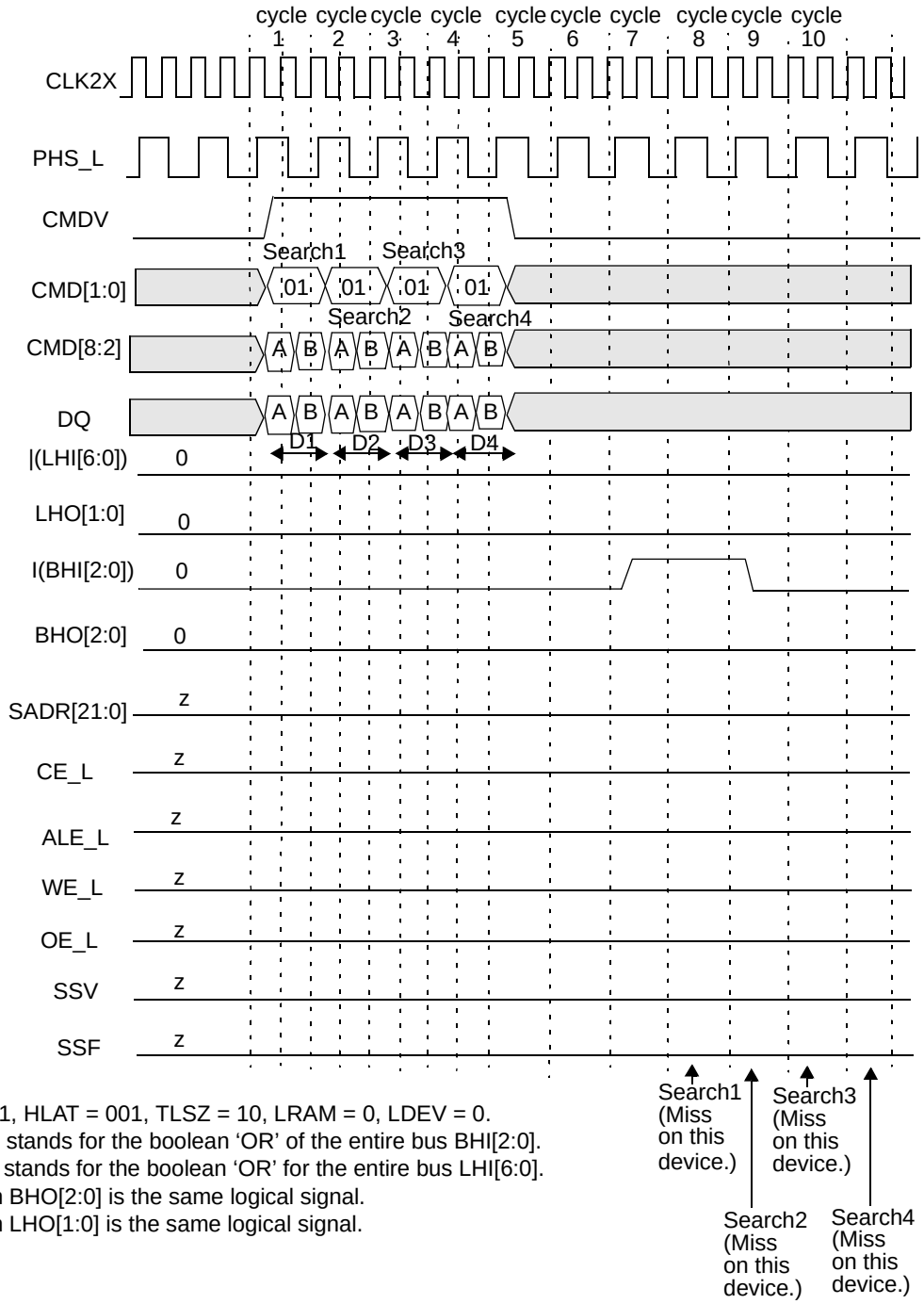
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-42. Timing Diagram for Globally Winning Device in Block Number 2



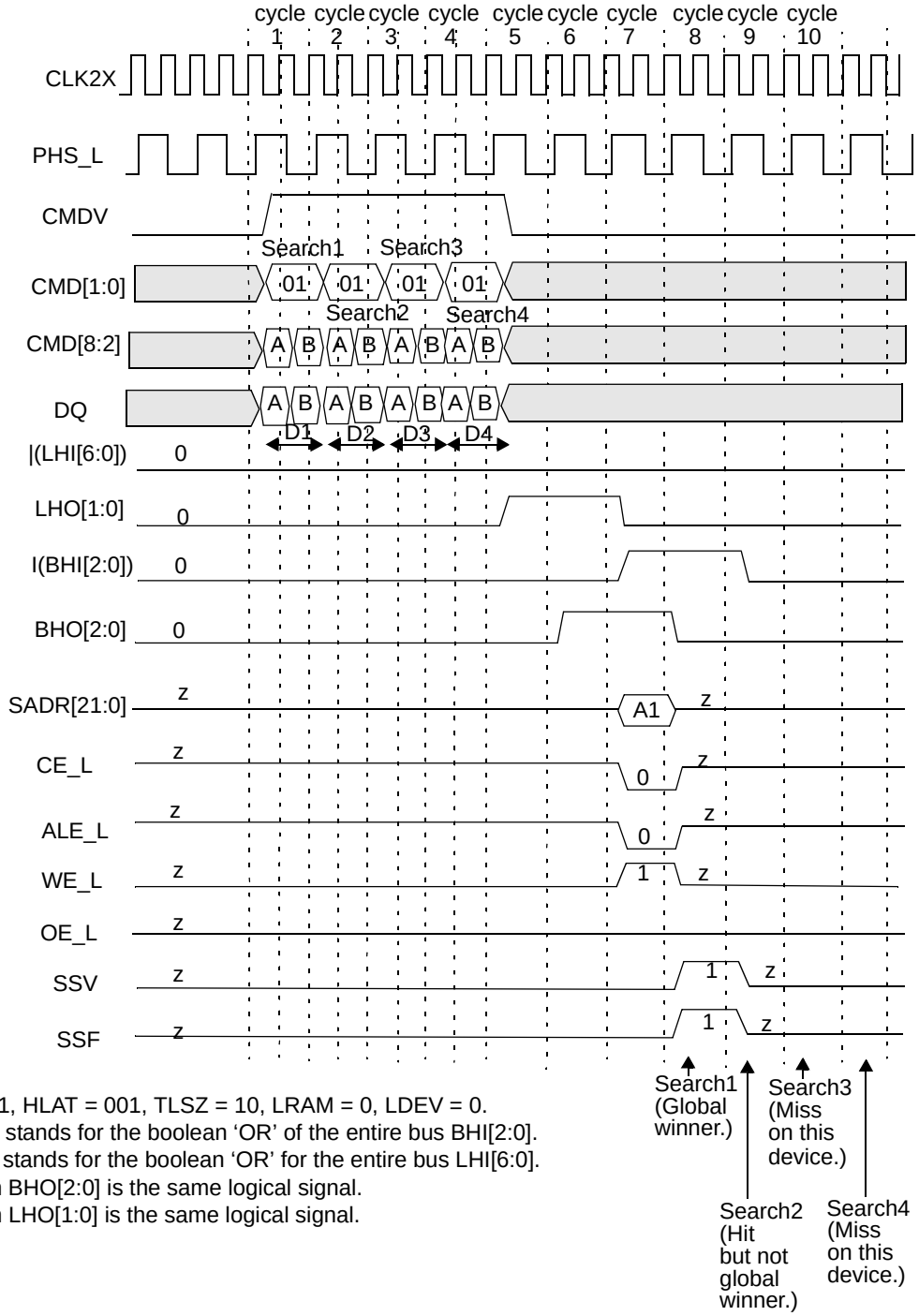
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-43. Timing Diagram for Devices Below the Winning Device in Block Number 2



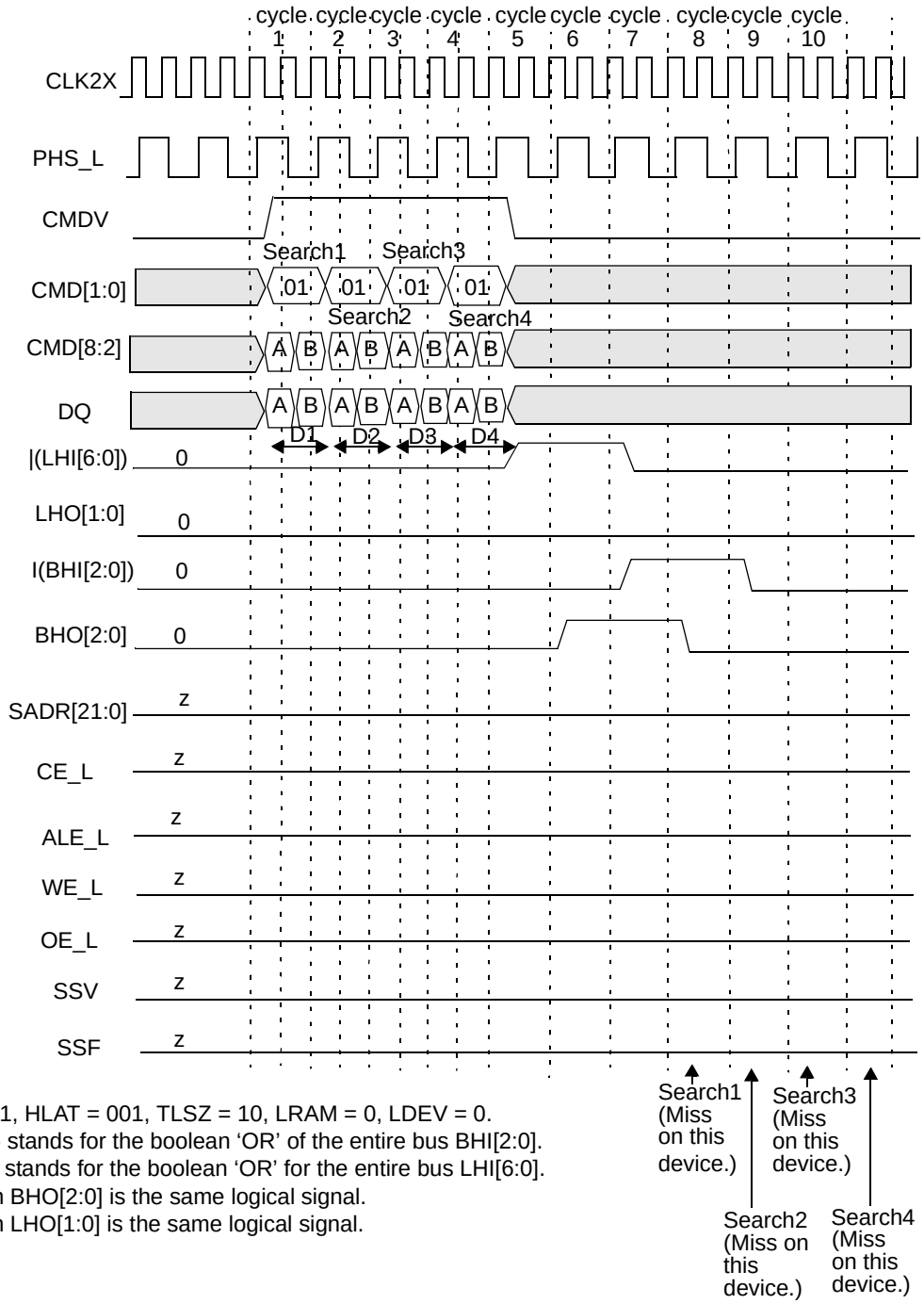
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-44. Timing Diagram for Devices Above the Winning Device in Block Number 3



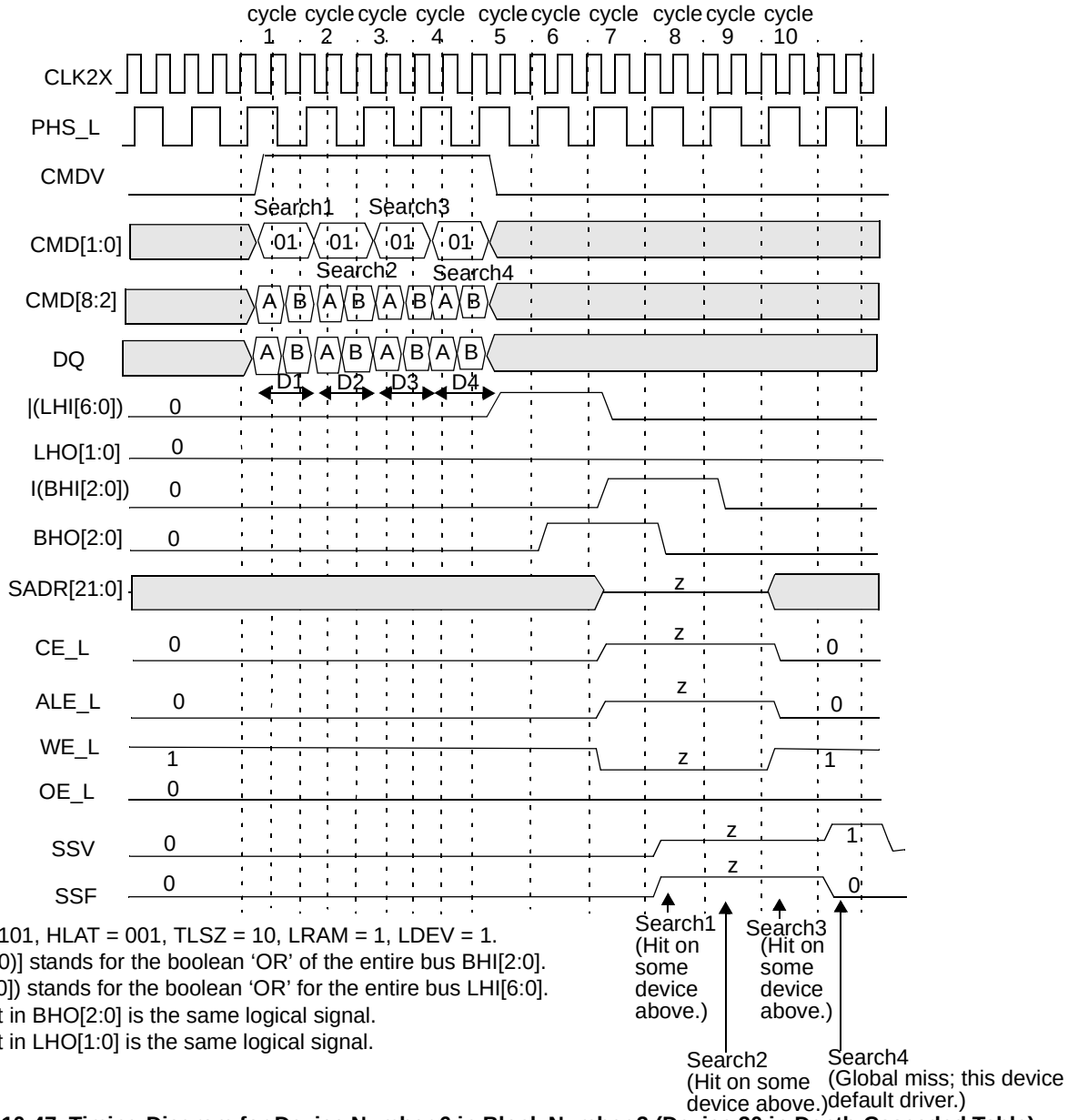
CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-45. Timing Diagram for Globally Winning Device in Block Number 3



CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-46. Timing Diagram for Devices Below the Winning Device in Block Number 3 Except Device 30 (the Last Device)



CFG = 01010101, HLAT = 001, TLSZ = 10, LRAM = 1, LDEV = 1.
Note: |(BHI[2:0)] stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-47. Timing Diagram for Device Number 6 in Block Number 3 (Device 30 in Depth-Cascaded Table)

The following is the sequence of operation for a single 136-bit Search command (also refer to "Command and Command Parameters," Subsection 10.2 on page 18).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this Search operation. CMD[8:7] signals must be driven with the bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) in order to be compared against all even locations. The CMD[2] signal must be driven to logic 0.
- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and to apply Search command code (10) on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ bus during cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with 68-bit data ([67:0])to be compared against all odd locations.

The logical 136-bit Search operation is as shown in the following *Figure 10-48*. The entire table of 31 devices (consisting of 136-bit entries) is compared against a 136-bit word K that is presented on the DQ bus in cycles A and B of the command using the GMR and local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's cycle A.

The 136-bit word K that is presented on the DQ bus in cycles A and B of the command is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's cycle B. In ×136 configurations, the even and odd comparand registers can subsequently be used by the Learn command in only the first non-full device. ***Note***. The Learn command is supported for only one of the blocks consisting of up to eight devices in a depth-cascaded table of more than one block. The word K that is presented on the DQ bus in cycles A and B of the command is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see Section 12.0, "SRAM Addressing" on page 100). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 (the default driving device for the SRAM bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles. ***Note***. During 136-bit searches of 136-bit-configured tables, the Search hit will always be at an even address.

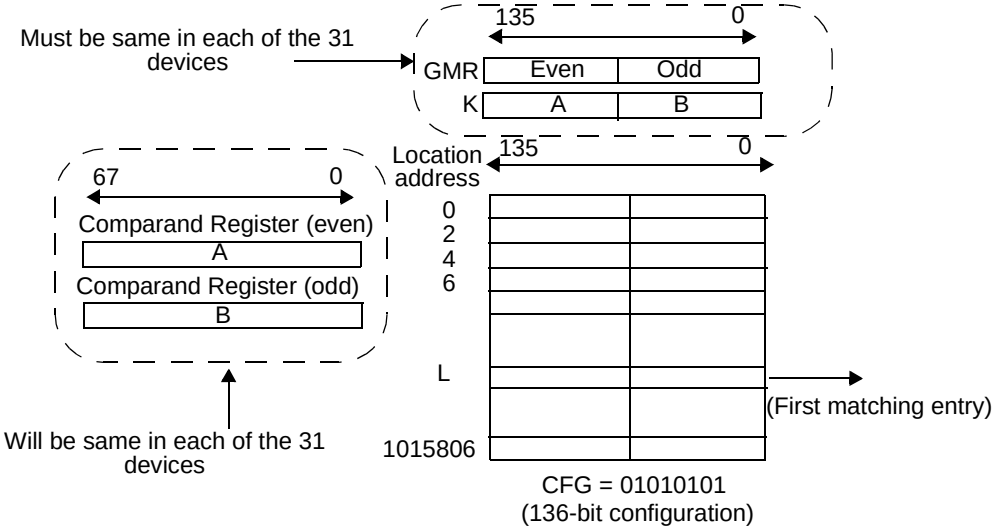


Figure 10-48. ×136 Table with 31 Devices

The Search command is a pipelined operation. It executes a Search at half the rate of the frequency of CLK2X for 136-bit searches in ×136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit Search command cycle (two CLK2X cycles) is shown in *Table 10-24*.

Table 10-24. The Latency of Search from Instruction to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K × 136 bits	4
1–8 (TLSZ = 01)	128K × 136 bits	5
1–31 (TLSZ = 10)	496K × 136 bits	6

The latency of a Search from command to the SRAM access cycle is 6 for 1–31 devices in the table and where TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 10-25*.

Table 10-25. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.12 272-bit Search on Tables Configured as û272 Using a Single CYNSE70064A Device

Figure 10-49 shows the timing diagram for a Search command in the 272-bit-configured table (CFG = 10101010) consisting of a single device for one set of parameters: TLSZ = 00, HLAT = 001, LRAM = 1, and LDEV = 1. The hardware diagram for this Search subsystem is shown in *Figure 10-50*.

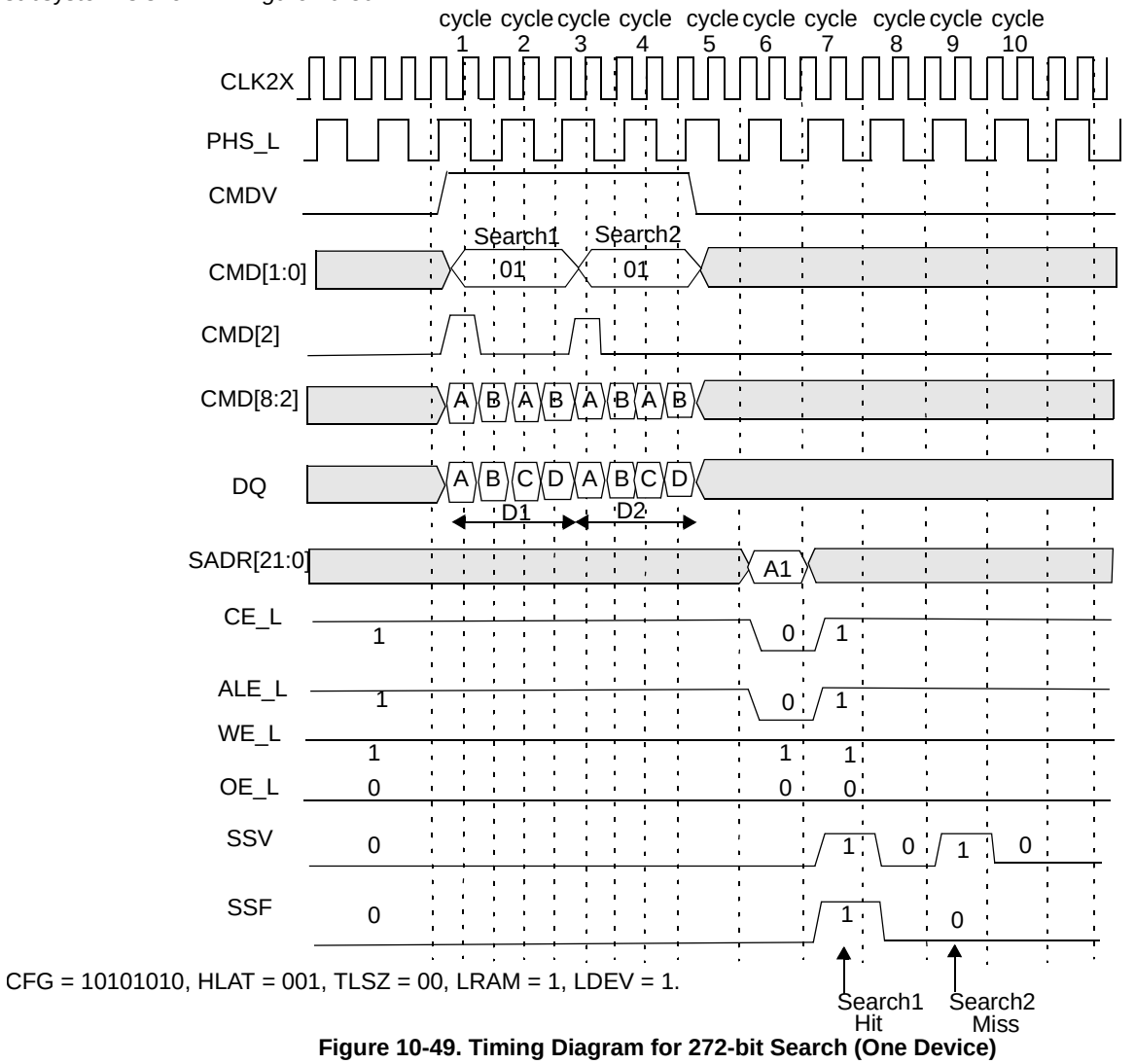


Figure 10-49. Timing Diagram for 272-bit Search (One Device)

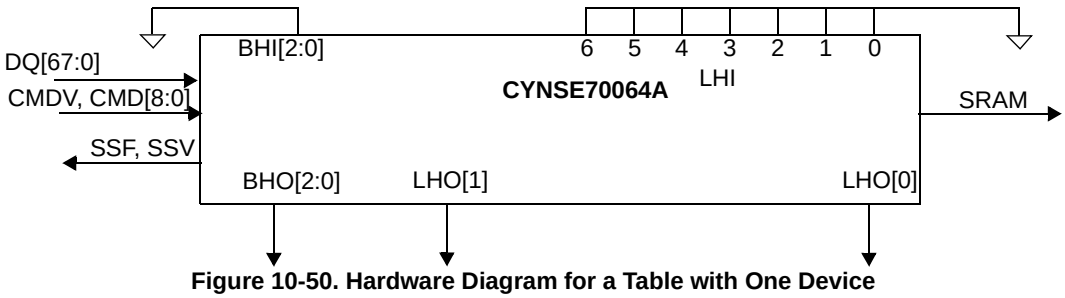


Figure 10-50. Hardware Diagram for a Table with One Device

The following is the sequence of operation for a single 136-bit Search command (also refer to Subsection 10.2, “Commands and Command Parameters” on page 18).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared to all locations 0 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 1. ***Note***. CMD[2] = 1 signals that the Search is a ×272-bit Search. CMD[8:3] in this cycle is ignored.

- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and continues to apply the command code of Search command (10) on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([204:136]) to be compared to all locations 1 in the four 68-bits-word page.
- **Cycle C**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [135:0] of the data being searched. CMD[8:7] signals must be driven with the bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared to all locations 2 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 0.
- **Cycle D**: The host ASIC continues to drive the CMDV HIGH and applies Search command code (10) on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations 3 in the four 68-bits-word page. CMD[5:2] is ignored because the Learn instruction is not supported for x272 tables.

Note. For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during cycles A, B, C, and D. The GMR index in cycle A selects a pair of GMRs that apply to DQ data in cycles A and B. The GMR index in cycle C selects a pair of GMRs that apply to DQ data in cycles C and D.

The logical 272-bit Search operation is shown in *Figure 10-51*. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's cycles A and C. The 272-bit word K that is presented on the DQ bus in cycles A, B, C and D of the command is compared with each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on SADR[21:0] lines (See "SRAM Addressing" on page 100.). ***Note***. The matching address is always going to be location 0 in a four-entry page for a 272-bit Search (two LSBs of the matching index will be 00).

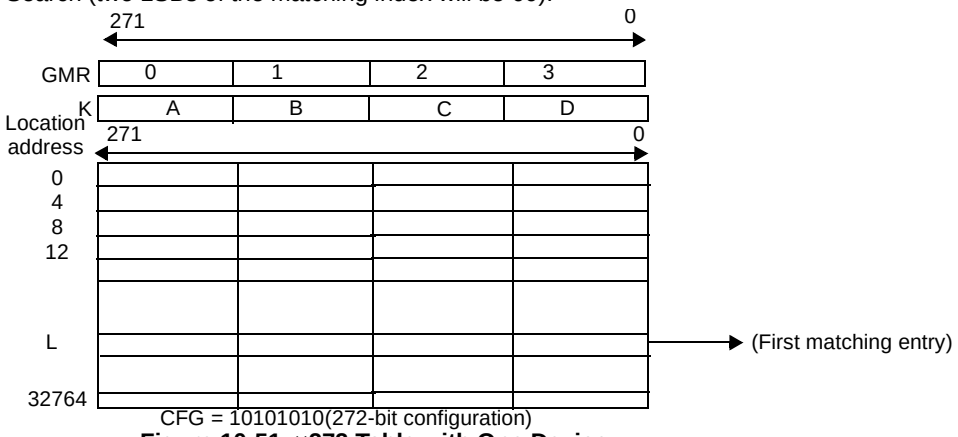


Figure 10-51. ×272 Table with One Device

The Search command is a pipelined operation and executes at one-fourth the rate of the frequency of CLK2X for 272-bit searches in ×272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit Search command (measured in CLK cycles) from the CLK2X cycle that contains the C and D cycles is shown in *Table 10-26*.

Table 10-26. The Latency of Search from C and D Cycles to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K × 272 bits	4
1–8 (TLSZ = 01)	64K × 272 bits	5
1–31 (TLSZ = 10)	248K × 272 bits	6

The latency of a Search from command to SRAM access cycle is 4 for only a single device in the table and TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 10-27*.

Table 10-27. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.13 272-bit Search on Tables x272-configured Using up to Eight CYNSE70064A Devices

The hardware diagram of the Search subsystem of eight devices is shown in *Figure 10-52*. The following are the parameters programmed in the eight devices.

- First seven devices (devices 0–6): CFG = 10101010, TLSZ = 01, HLAT = 000, LRAM = 0, and LDEV = 0.
- Eighth device (device 7): CFG = 10101010, TLSZ = 01, HLAT = 000, LRAM = 1, and LDEV = 1.

Note. All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (device number 7 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (devices 0 through 6 in this case).

Figure 10-53 shows the timing diagram for a Search command in the 272-bit-configured table of eight devices for device number 0. *Figure 10-54* shows the timing diagram for a Search command in the 272-bit-configured table of eight devices for device number 1. *Figure 10-55* shows the timing diagram for a Search command in the 272-bit-configured table of eight devices for device number 7 (the last device in this specific table). For these timing diagrams three 272-bit searches are performed sequentially. The following Hit/Miss assumptions were made as shown in *Table 10-28*.

Table 10-28. Hit/Miss Assumption

Search Number	1	2	3
Device 0	Hit	Miss	Miss
Device 1	Miss	Hit	Miss
Devices 2–6	Miss	Miss	Miss
Device 7	Miss	Miss	Miss

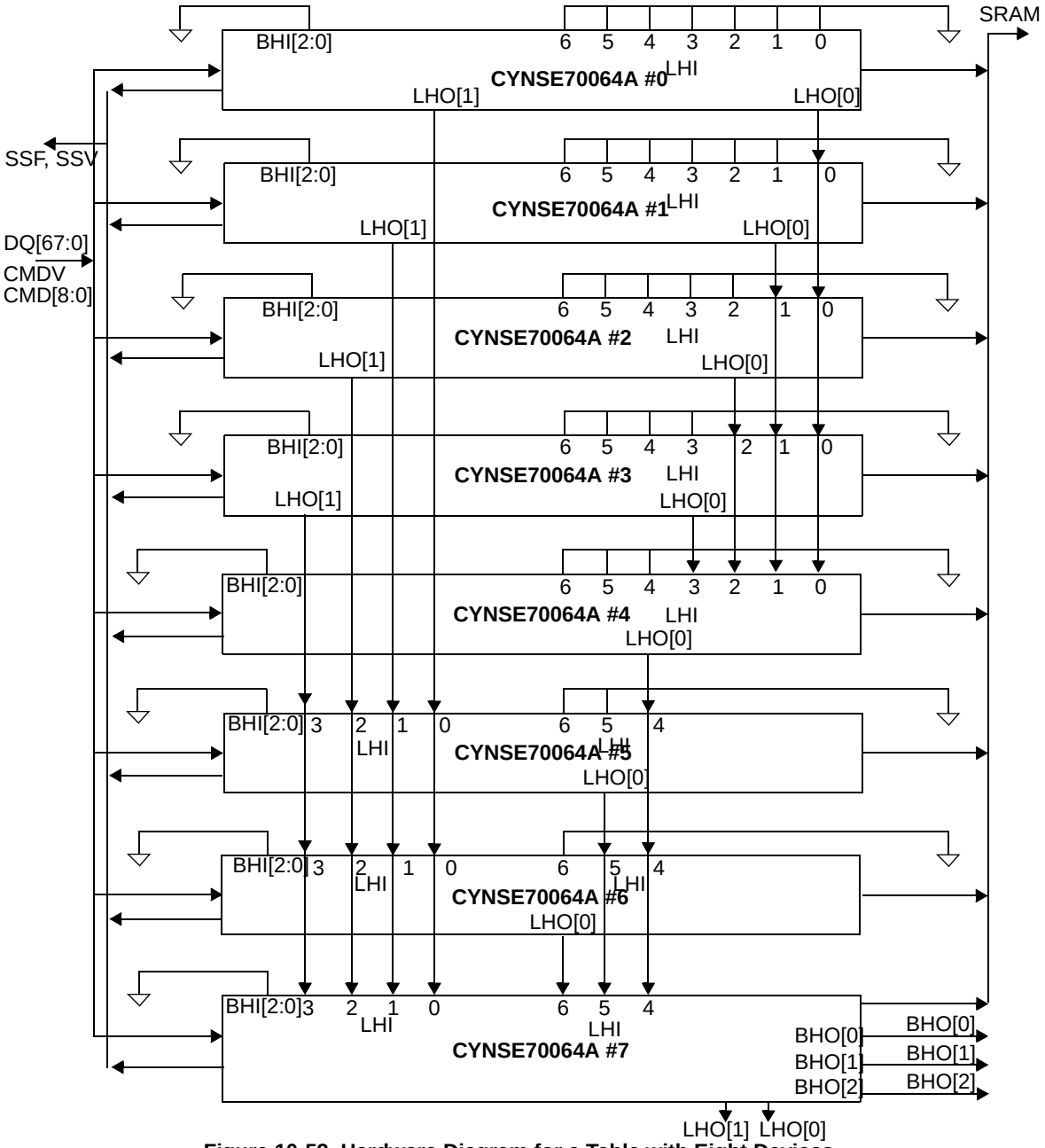
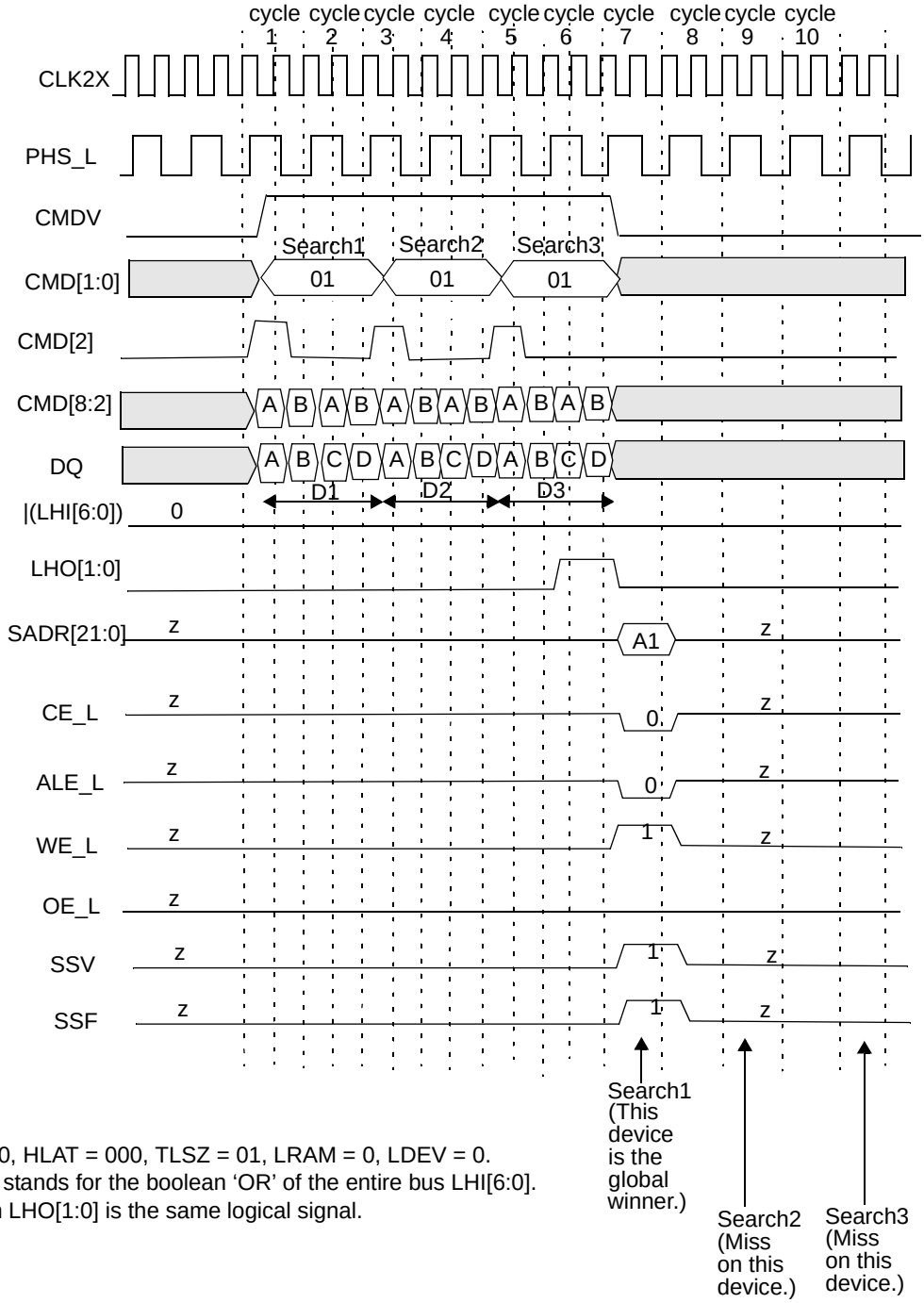
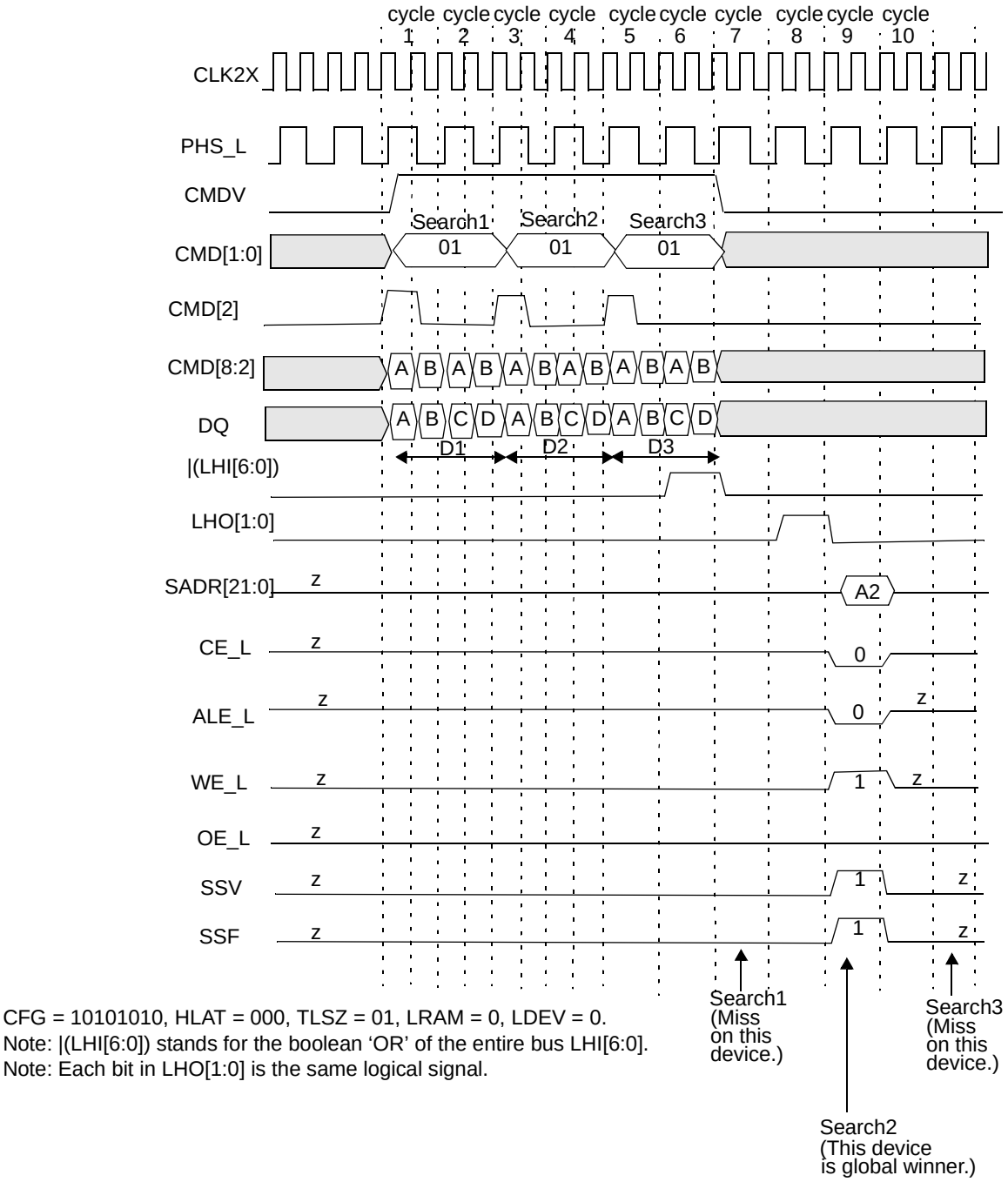


Figure 10-52. Hardware Diagram for a Table with Eight Devices



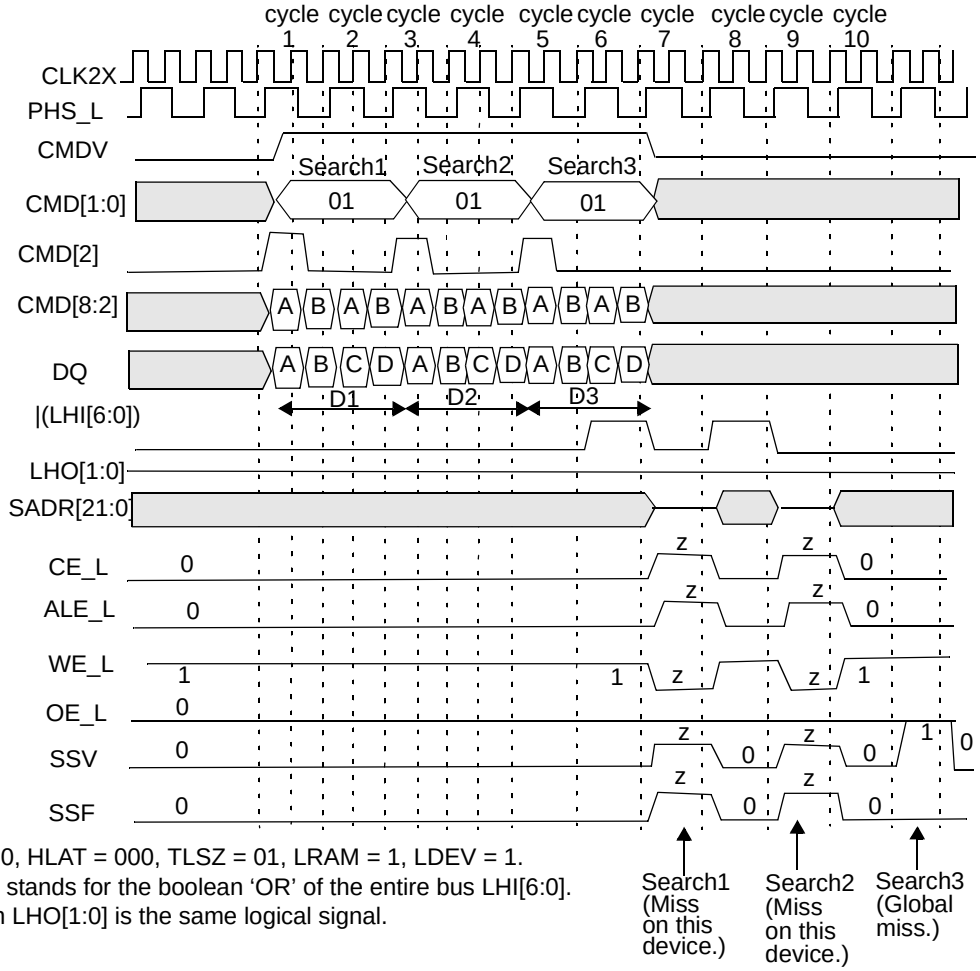
CFG = 10101010, HLAT = 000, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-53. Timing Diagram for 272-bit Search Device Number 0



CFG = 10101010, HLAT = 000, TLSZ = 01, LRAM = 0, LDEV = 0.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-54. Timing Diagram for 272-bit Search Device Number 1



CFG = 10101010, HLAT = 000, TLSZ = 01, LRAM = 1, LDEV = 1.
Note: |(LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-55. Timing Diagram for 272-bit Search Device Number 7 (Last Device)

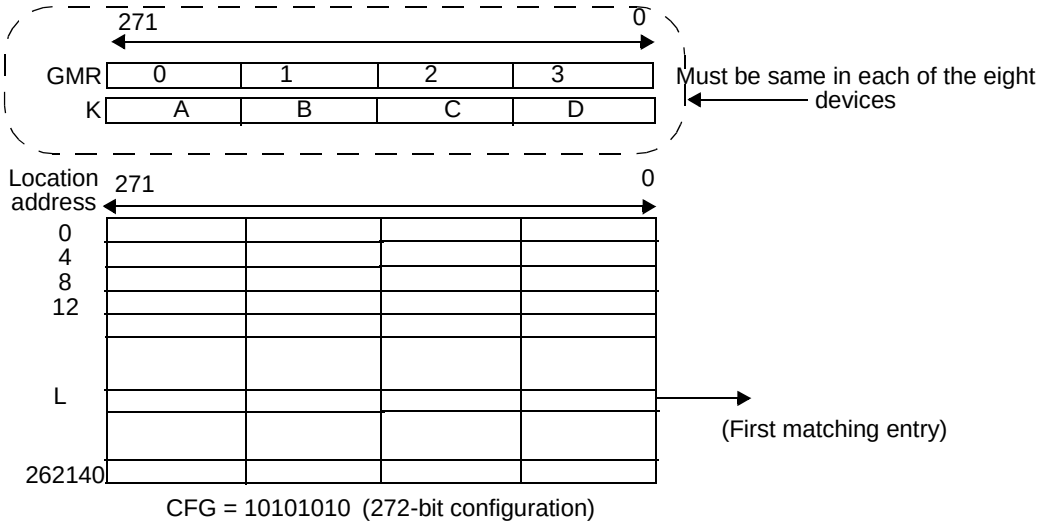
The following is the sequence of operation for a single 272-bit Search command (also See "Commands and Command Parameters" on page 18.).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched in this operation. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared against all locations 0 in the four-word 68-bit page. The CMD[2] signal must be driven to logic 1. ***Note***. CMD[2] = 1 signals that the Search is a ×272 bit Search. CMD[8:3] in this cycle is ignored.
- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and applies Search command code (10) on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([203:136]) to be compared against all locations 1 in the four 68-bits-word page.
- **Cycle C**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [135:0] of the data being searched. CMD[8:7] signals must be driven with the bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared against all locations 2 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 0.
- **Cycle D**: The host ASIC continues to drive the CMDV HIGH and applies Search command code (10) on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for the description of SSR[0:7]). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations 3 in the four 68-bits-word page. CMD[5:2] is ignored because the Learn instruction is not supported for x272 tables.

Note. For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during cycles A, B, C, and D. The GMR index in cycle A selects a pair of GMRs in each of the eight devices that apply to DQ data in cycles A and B. The GMR index in cycle C selects a pair of GMRs in each of the eight devices that apply to DQ data in cycles C and D.

The logical 272-bit Search operation is shown in *Figure 10-56*. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command using the GMR and the local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's cycles A and C in each of the eight devices. The 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command is compared to

each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (See "SRAM Addressing" on page 100.). ***Note***. The matching address is always going to be a location 0 in a four-entry page for 272-bit Search (two LSBs of the matching index will be 00).



CFG = 10101010 (272-bit configuration)

Figure 10-56. ×272 Table with Eight Devices

The Search command is a pipelined operation and executes Search at one fourth the rate of the frequency of CLK2X for 272-bit searches in x272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit Search command (measured in CLK cycles) from the CLK2X cycle that contains the C and D cycles is shown in *Table 10-29*.

Table 10-29. The Latency of Search from C and D cycles to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K × 272 bits	4
1–8 (TLSZ = 01)	64K × 272 bits	5
1–31 (TLSZ = 10)	248K × 272 bits	6

The latency of Search from command to SRAM access cycle is 5 for only a single device in the table and TLSZ = 01. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 10-30*.

Table 10-30. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.14 272-bit Search on Tables Configured as ×272 Using up to 31 CYNSE70064A Devices

The hardware diagram of the Search subsystem of 31 devices is shown in *Figure 10-57*. Each of the four blocks in the diagram represents a block of eight CYNSE70064A devices, except the last which has seven devices. The diagram for a block of eight devices is shown in *Figure 10-58*. The following are the parameters programmed into the 31 devices.

- First thirty devices (devices 0–29): CFG = 10101010, TLSZ = 10, HLAT = 000, LRAM = 0, and LDEV = 0.
- Thirty-first device (device 30): CFG = 10101010, TLSZ = 10, HLAT = 000, LRAM = 1, and LDEV = 1.

Note. All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (device number 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the Hit/Miss assumptions defined in *Table 10-31*. For the purpose of illustrating the timings, it is further assumed that there is only one device with the matching entry in each block. *Figure 10-59*

shows the timing diagram for a Search command in the 272-bit-configured table consisting of 31 devices for each of the eight devices in block number 0. *Figure 10-60* shows the timing diagram for a Search command in the 272-bit-configured table of 31 devices for all devices above the winning device in block number 1. *Figure 10-61* shows the timing diagram for the globally winning device (the final winner within its own and all blocks) in block number 1. *Figure 10-62* shows the timing diagram for all the devices below the globally winning device in block number 1. *Figure 10-63*, *Figure 10-64*, and *Figure 10-65*, respectively, show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device for block number 2. *Figure 10-66*, *Figure 10-67*, *Figure 10-68*, and *Figure 10-69*, respectively, show the timing diagrams of the device above the globally winning device, the globally winning device, the devices below the globally winning device (except device 30), and last device (device 30) for block number 3.

The 272-bit Search operation is pipelined and executes as follows. Four cycles from the last cycle of the Search command each of the devices knows the outcome internal to it for that operation. In the fifth cycle from the Search command, the devices in a block (which is less than or equal to eight devices resolving the winner within them using an LHI[6:0] and LHO[1:0] signalling mechanism) arbitrate for a winner. In the sixth cycle after the Search command, the blocks of devices resolve the winning block through a BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for the Search operation.

Table 10-31. Hit/Miss Assumption

Search Number	1	2	3
Block 0	Miss	Miss	Miss
Block 1	Miss	Miss	Hit
Block 2	Miss	Hit	Hit
Block 3	Hit	Hit	Miss

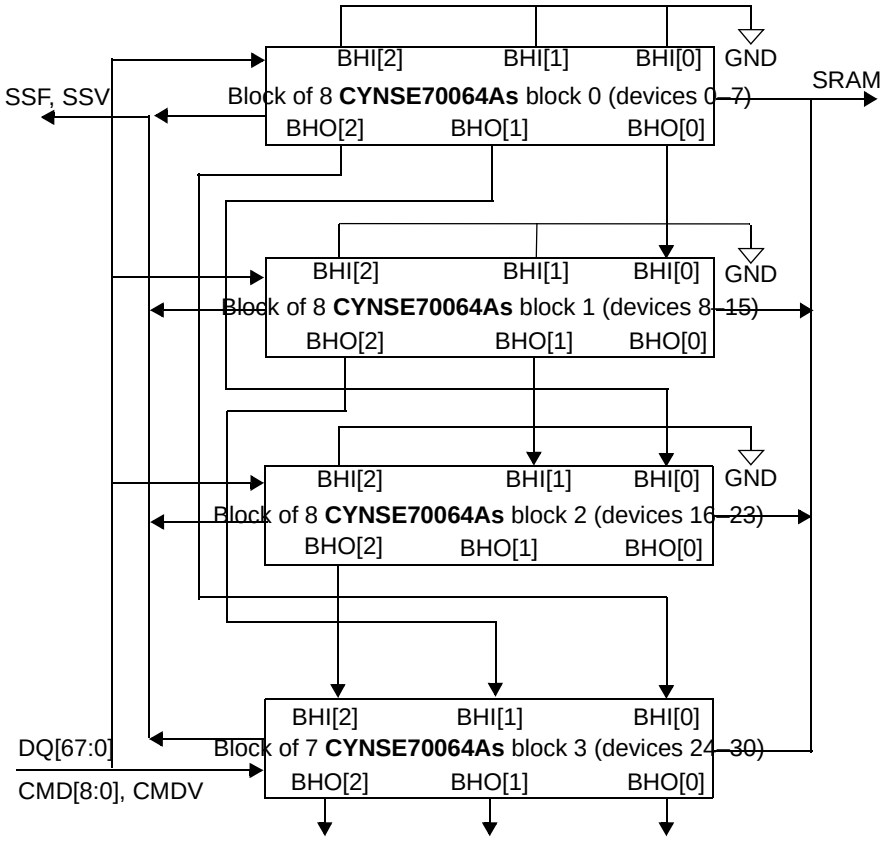


Figure 10-57. Hardware Diagram for a Table with 31 Devices

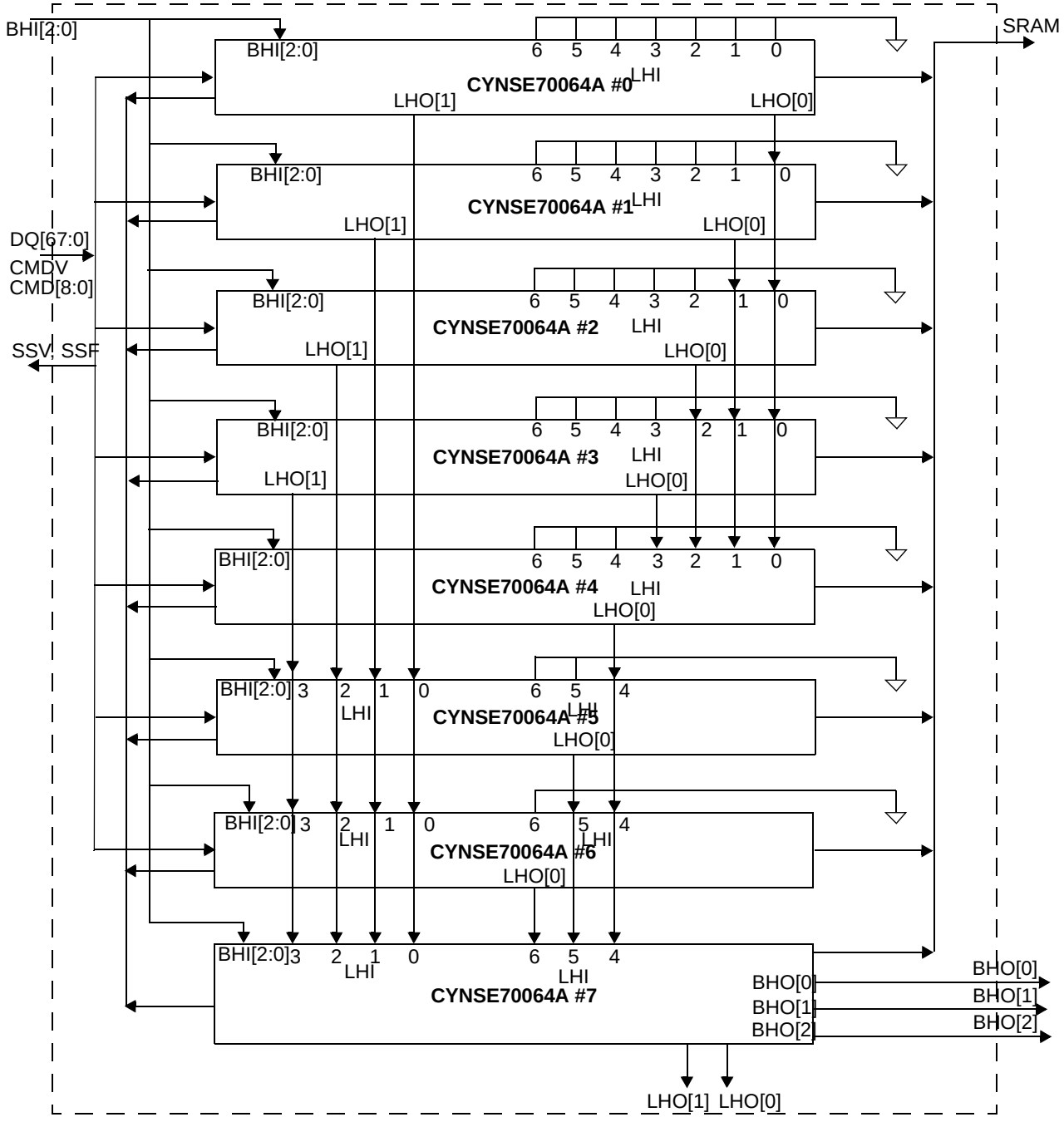
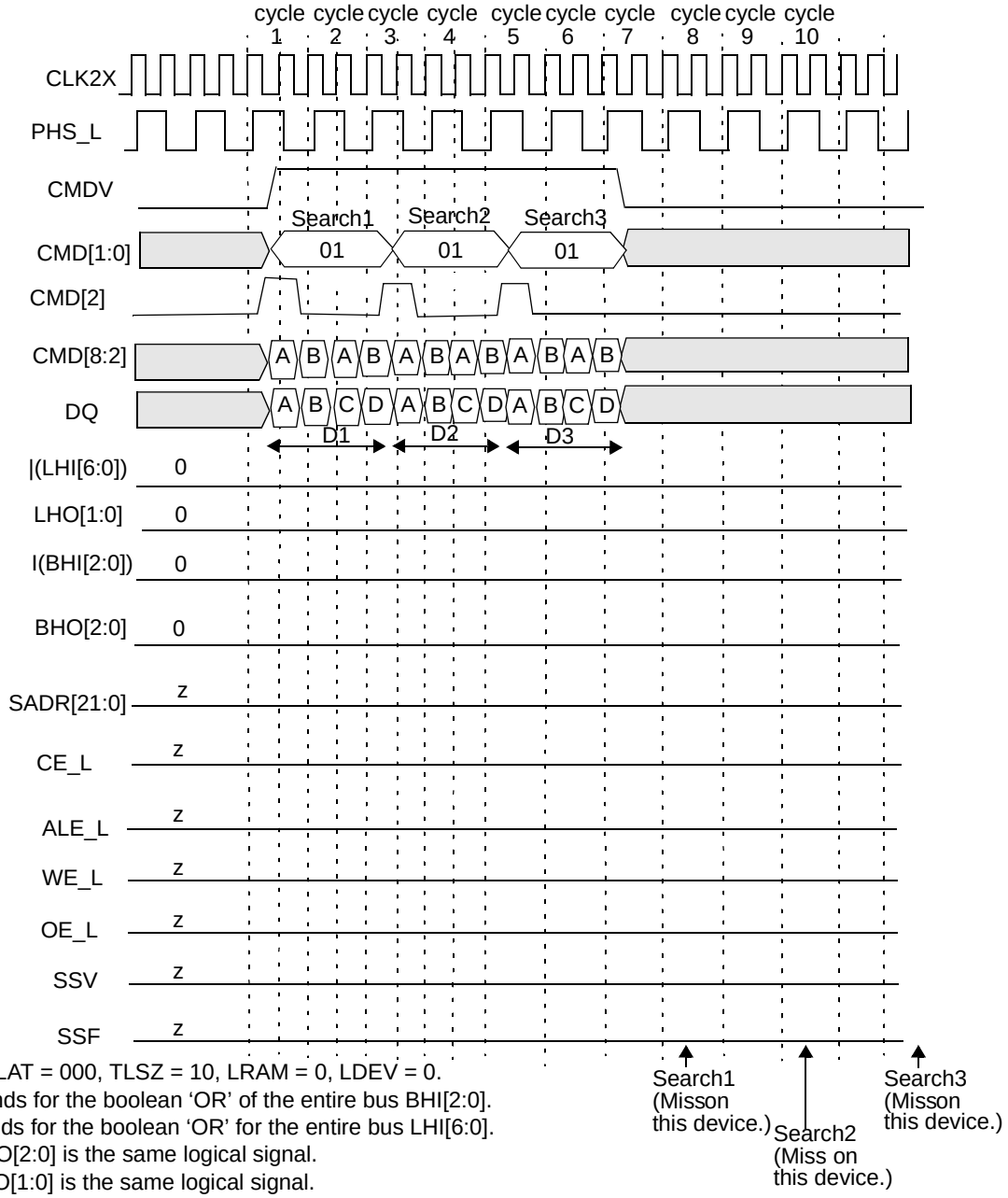
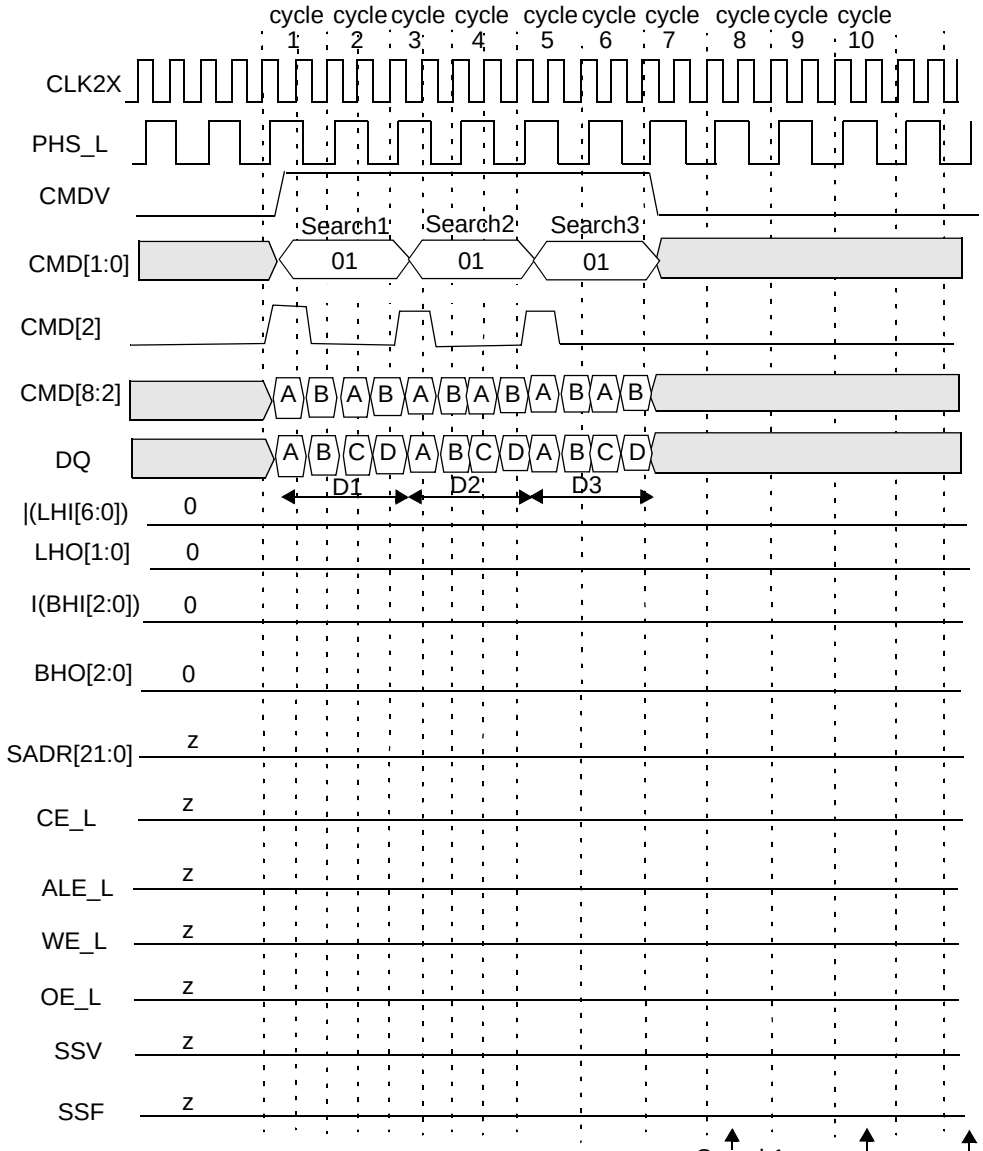


Figure 10-58. Hardware Diagram for A Block of up to Eight Devices



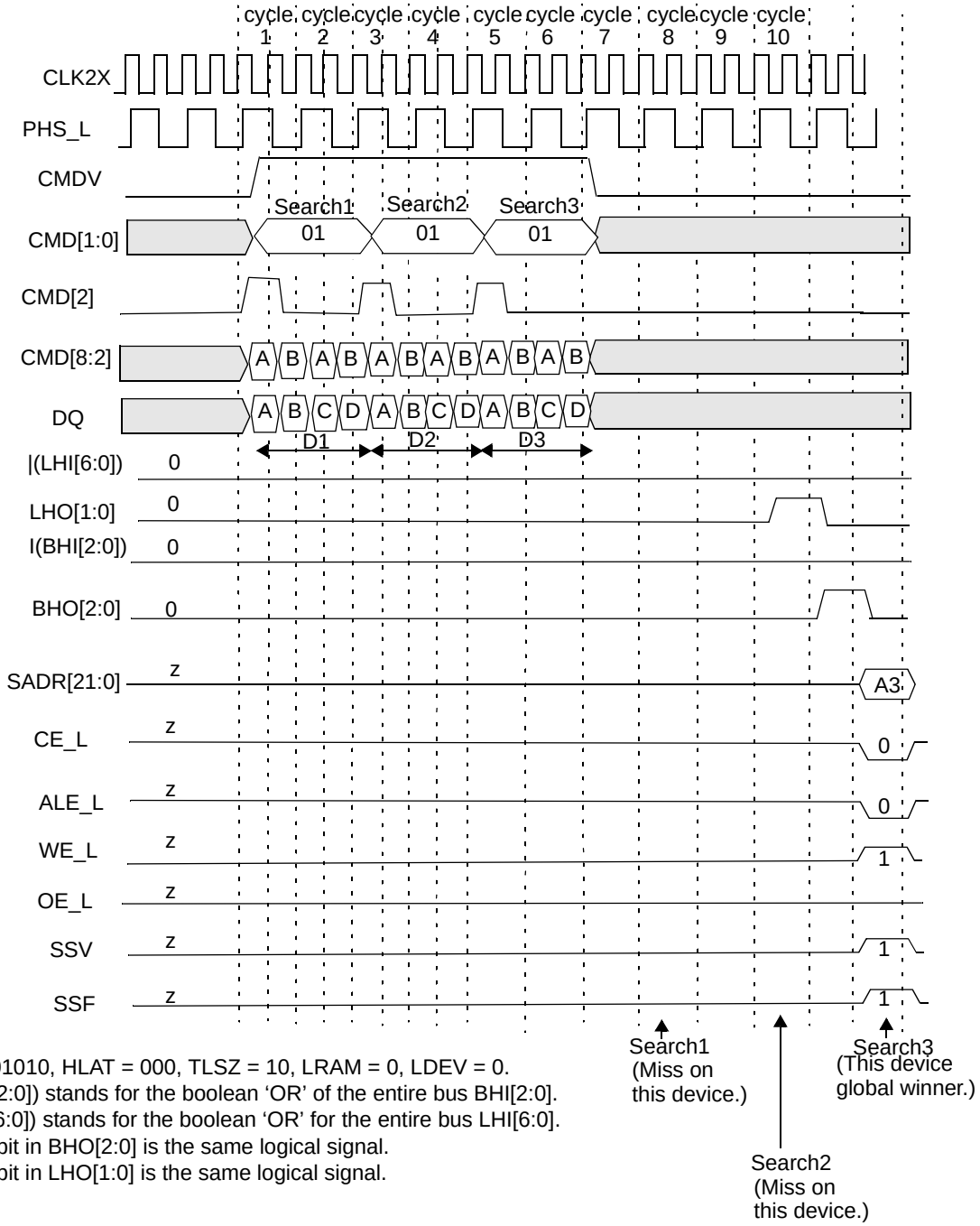
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-59. Timing Diagram for Each Device in Block Number 0 (Miss on Each Device)



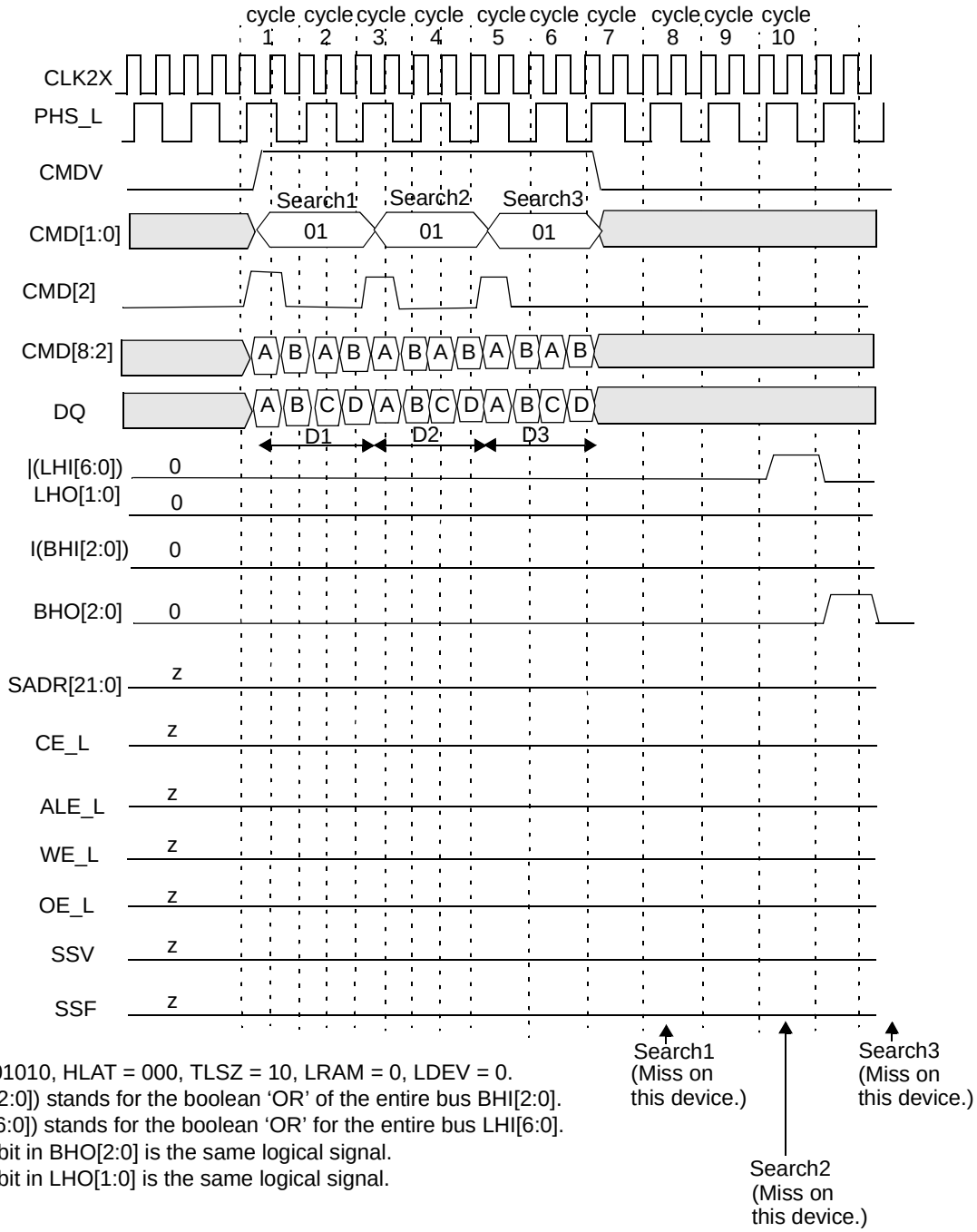
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-60. Timing Diagram for Each Device Above the Winning Device in Block Number 1



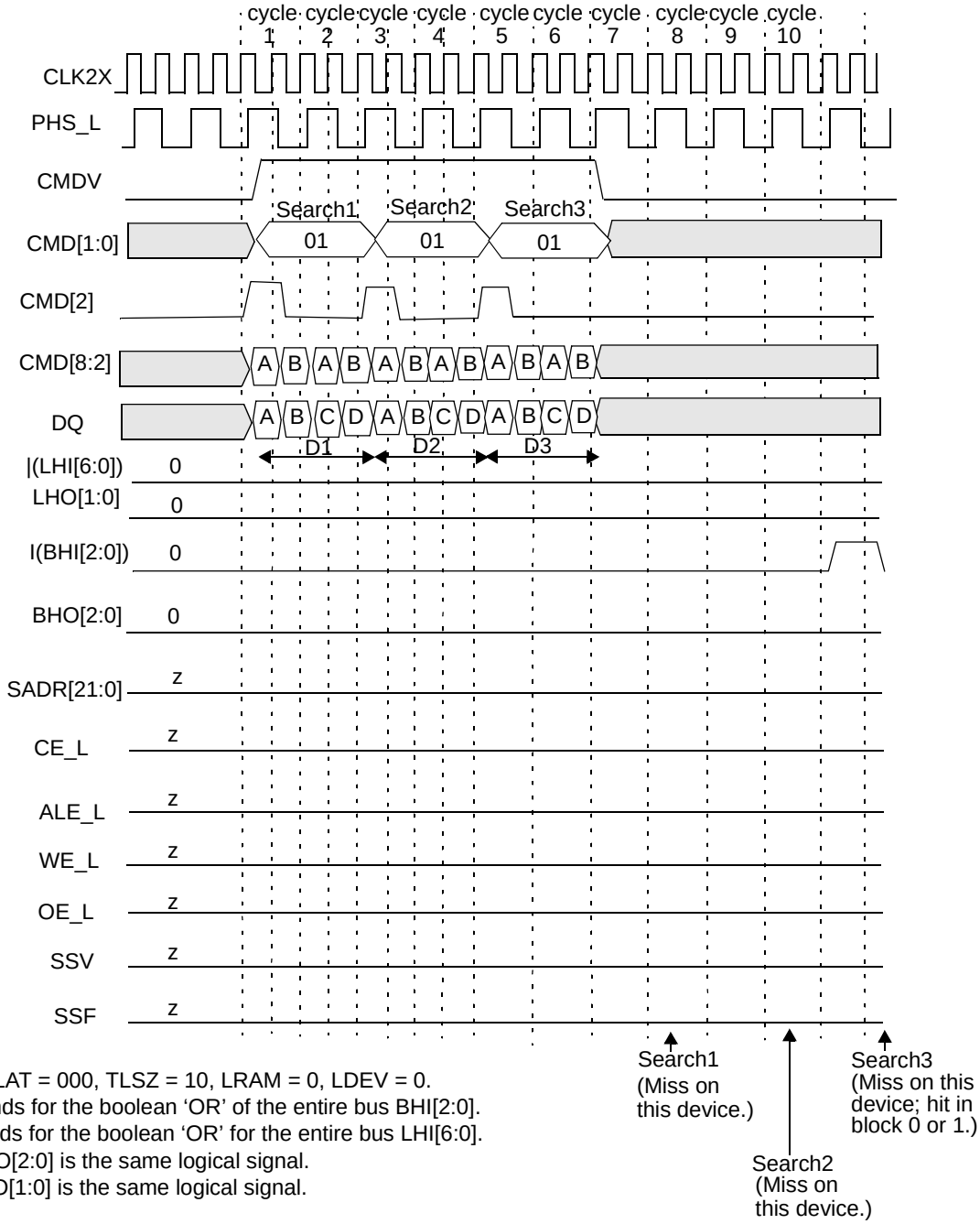
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-61. Timing Diagram for Globally Winning Device in Block Number 1



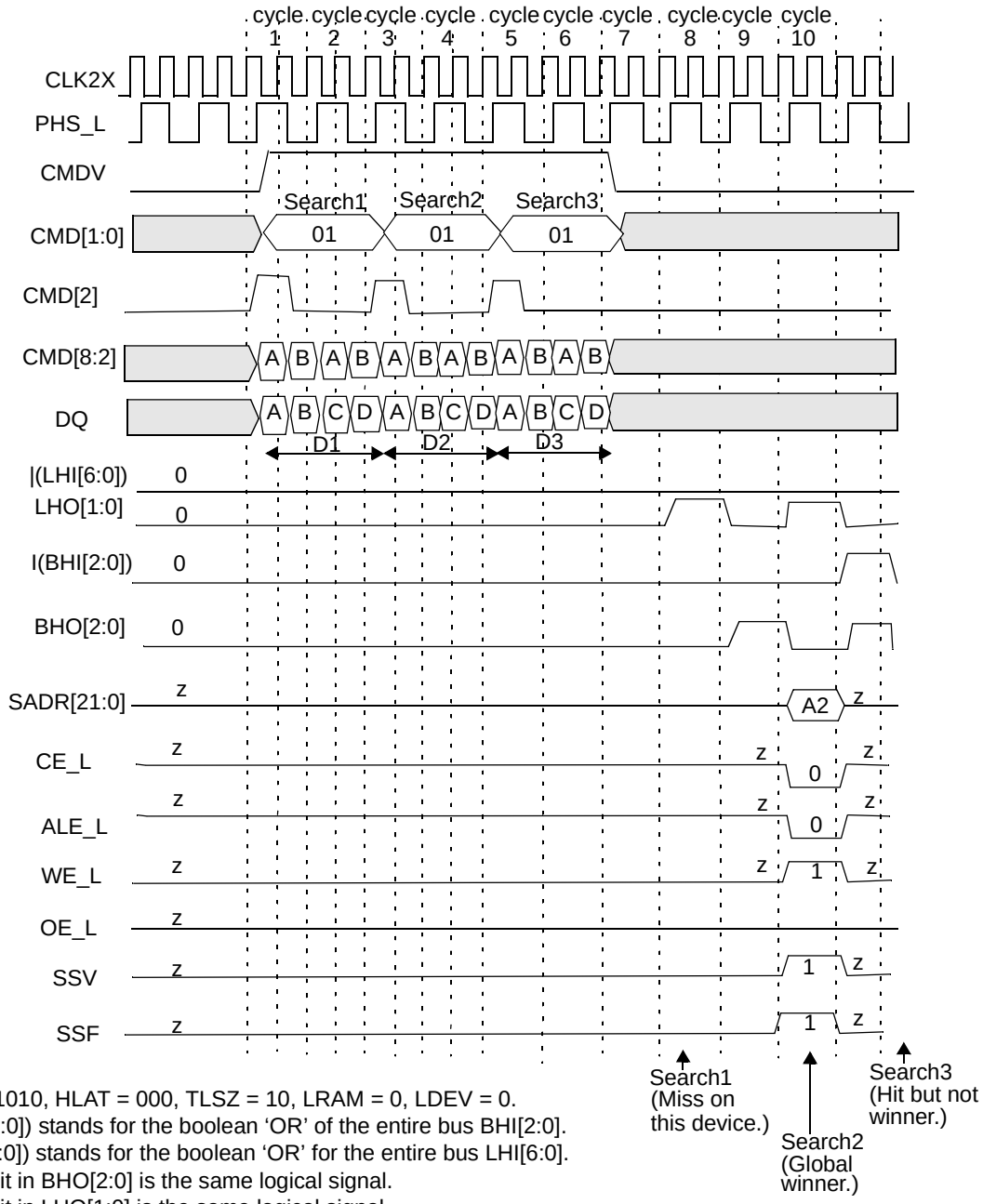
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-62. Timing Diagram for Devices Below the Winning Device in Block Number 1



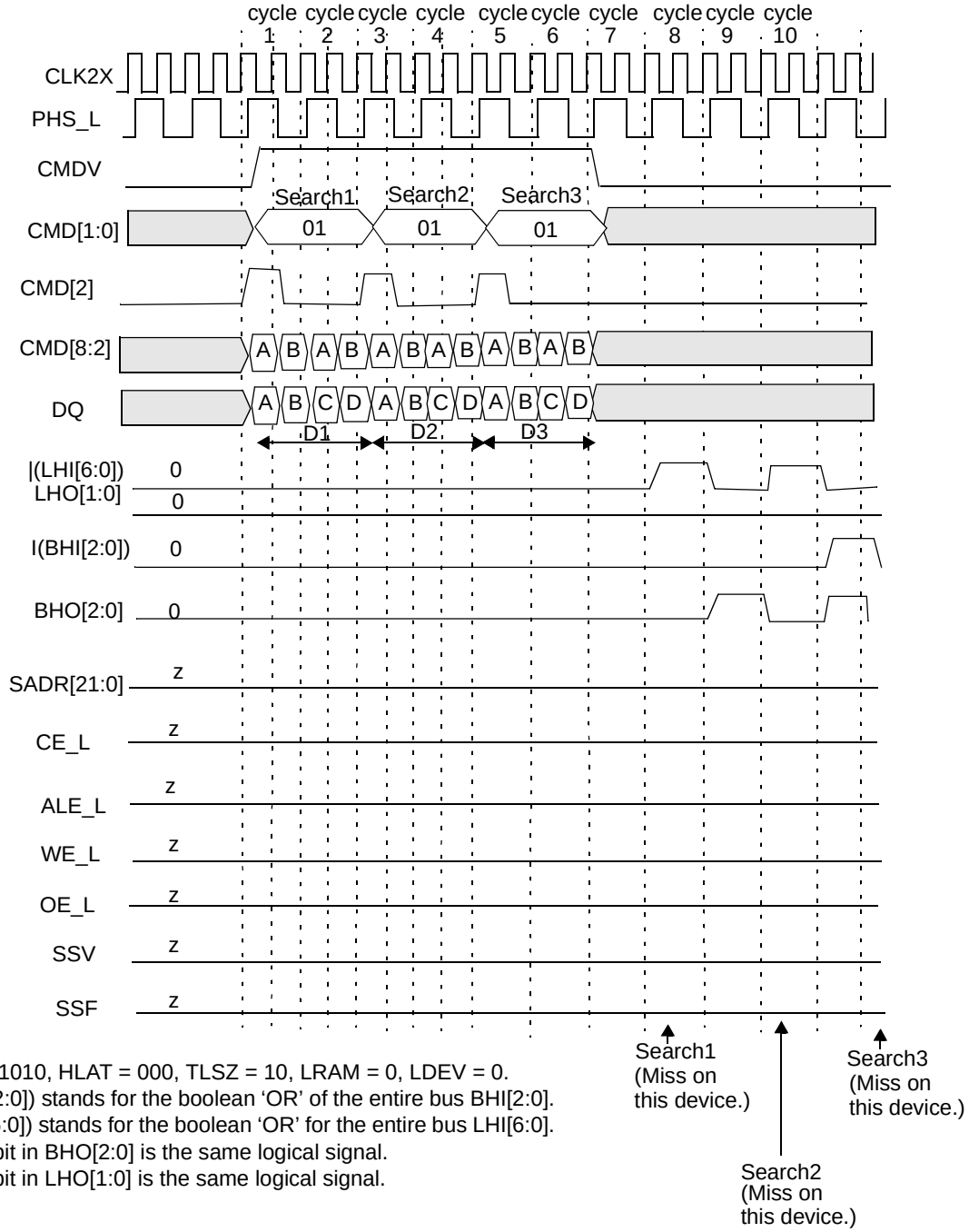
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-63. Timing Diagram for Devices Above the Winning Device in Block Number 2



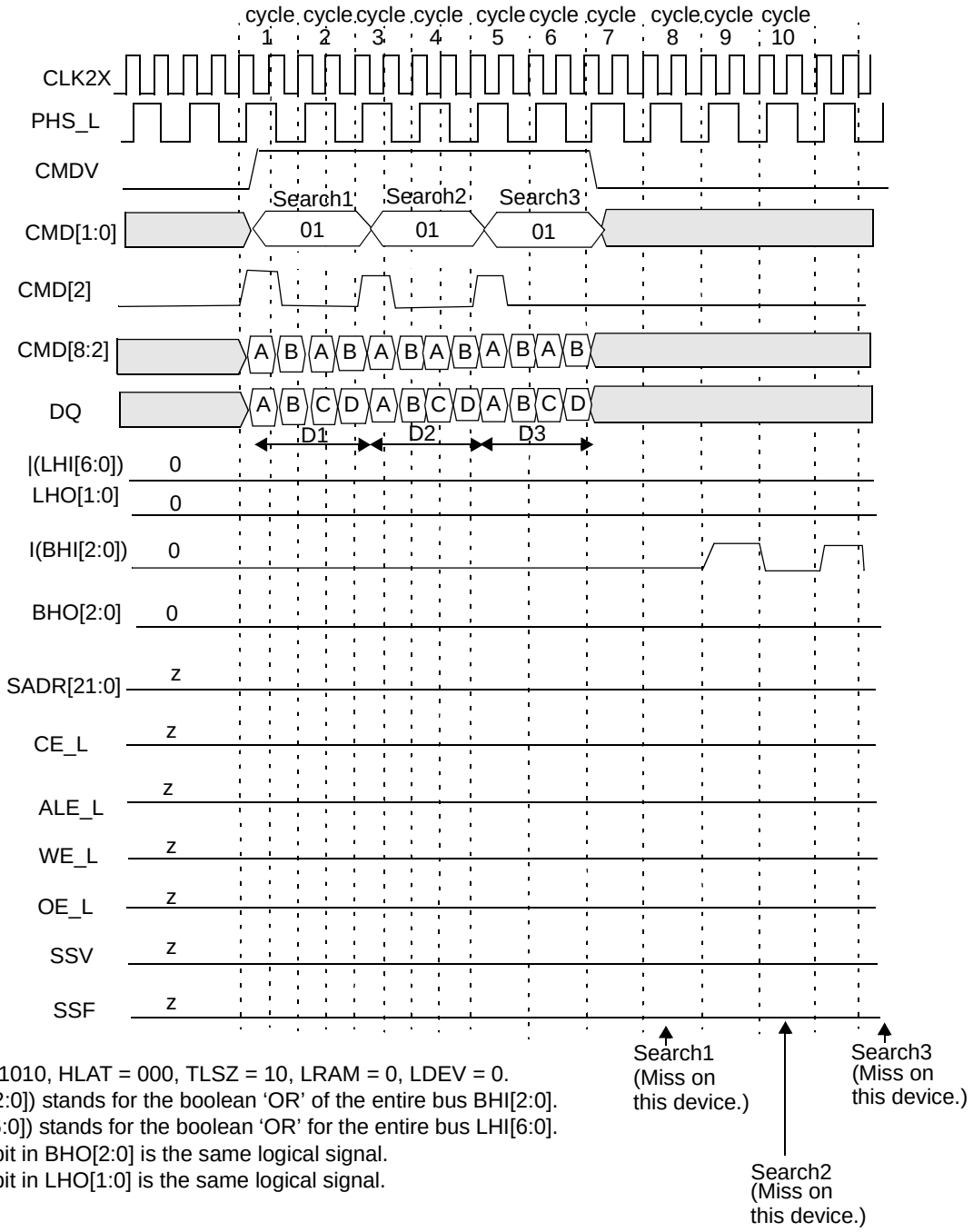
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-64. Timing Diagram for Globally Winning Device in Block Number 2



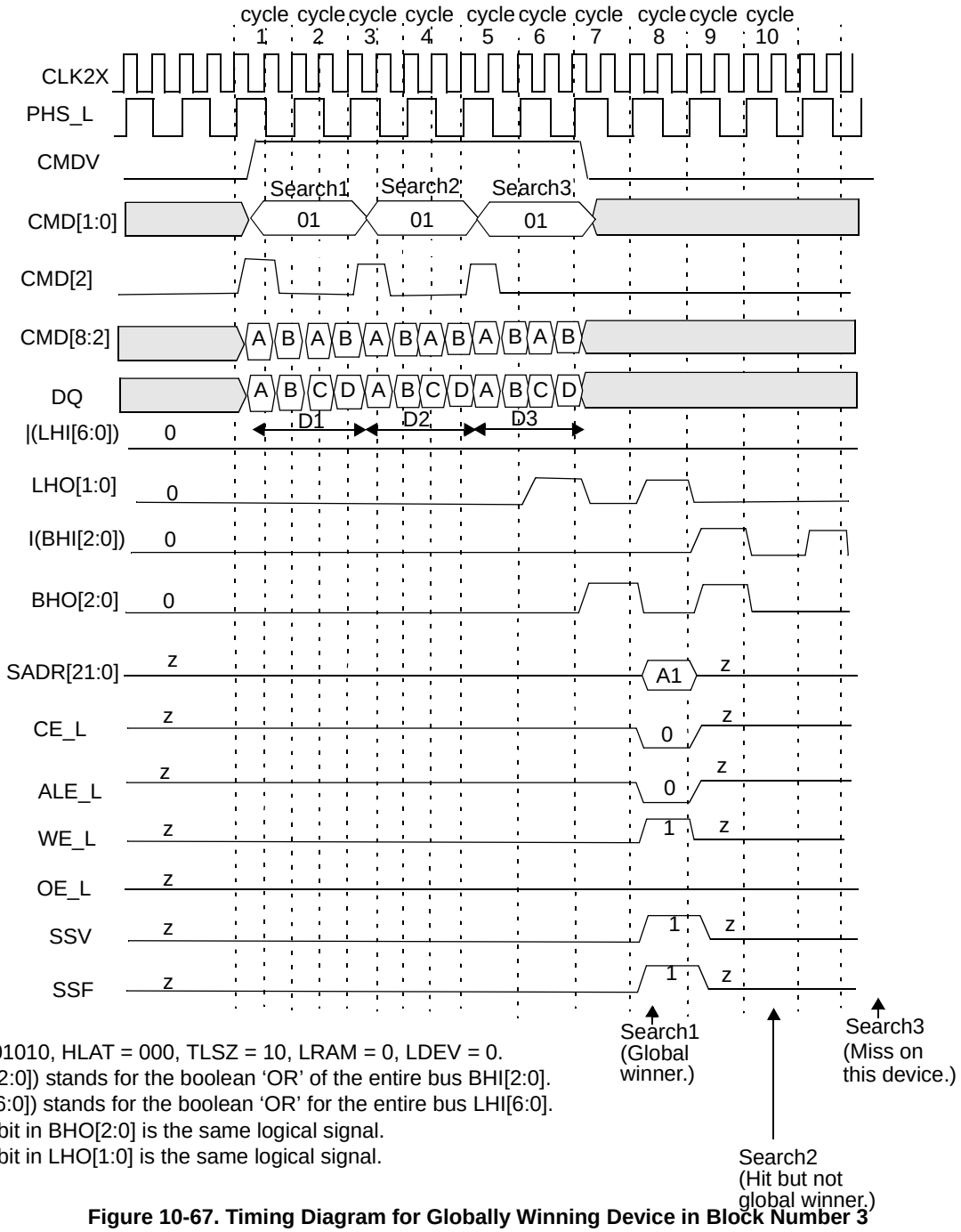
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-65. Timing Diagram for Devices Below the Winning Device in Block Number 2



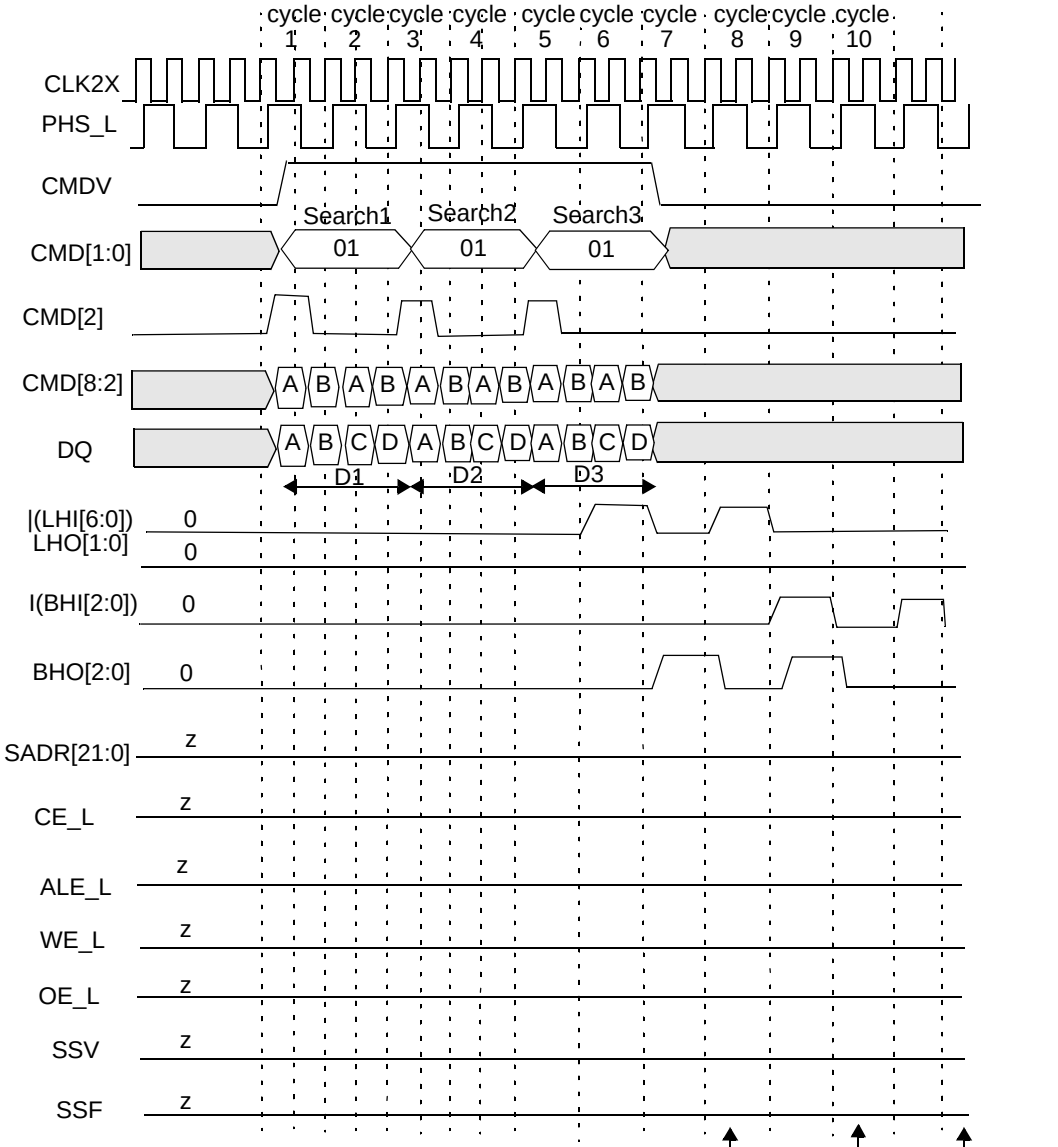
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-66. Timing Diagram for Devices Above the Winning Device in Block Number 3



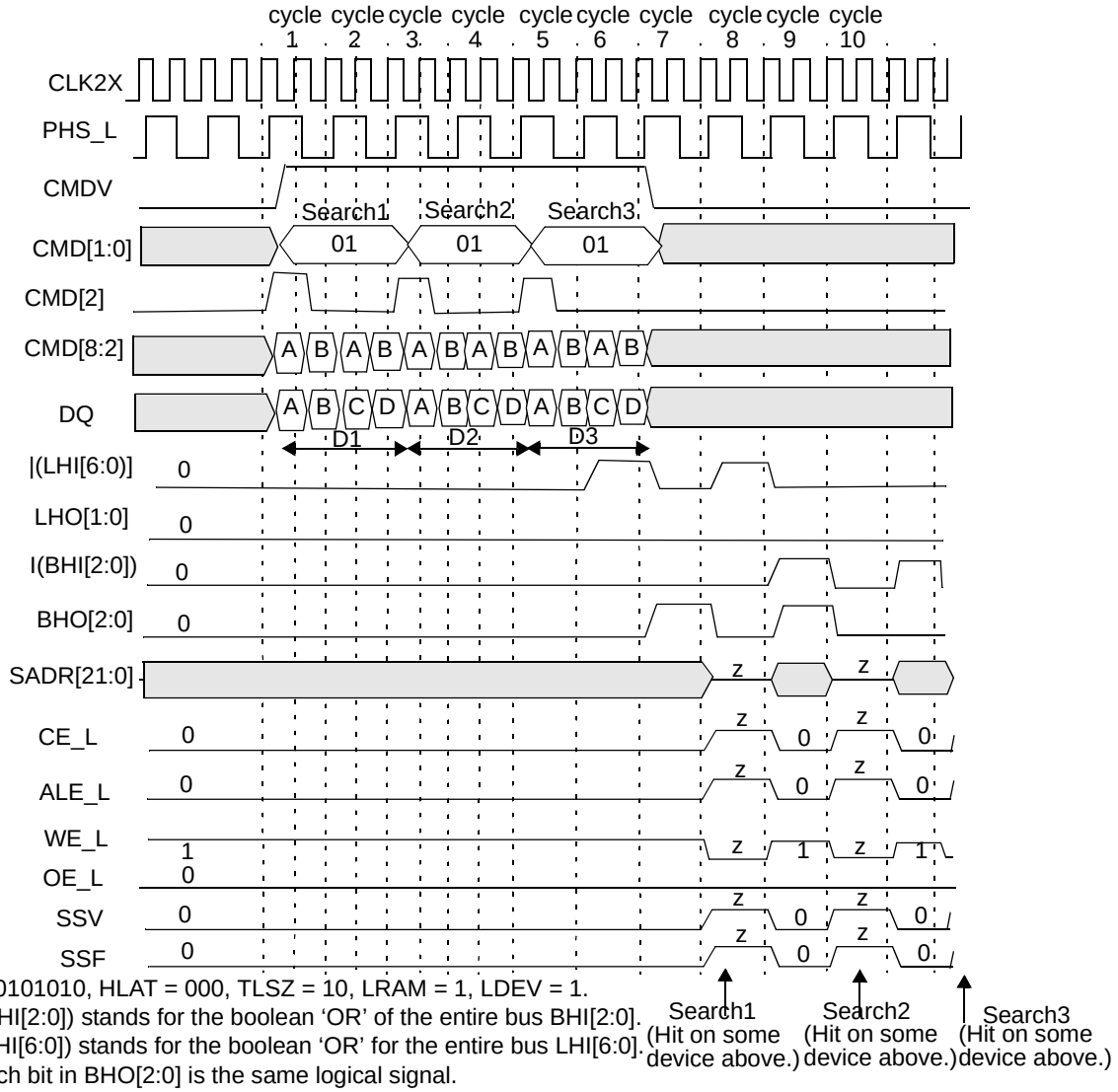
CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-67. Timing Diagram for Globally Winning Device in Block Number 3



CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 0, LDEV = 0.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-68. Timing Diagram for Devices Below the Winning Device in Block Number 3 Except Device 30 (the Last Device)



CFG = 10101010, HLAT = 000, TLSZ = 10, LRAM = 1, LDEV = 1.
Note: |(BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
Note: |(LHI[6:0]) stands for the boolean 'OR' for the entire bus LHI[6:0].
Note: Each bit in BHO[2:0] is the same logical signal.
Note: Each bit in LHO[1:0] is the same logical signal.

Figure 10-69. Timing Diagram of the Last Device in Block Number 3 (Device 30 in the Table)

The following is the sequence of operation for a single 272-bit Search command (also refer to Subsection 10.2, "Commands and Command Parameters" on page 18).

- **Cycle A**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched. DQ[67:0] must be driven with the 68-bit data ([271:204])to be compared to all locations 0 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 1. ***Note***. CMD[2] = 1 signals that the Search is a ×272-bit Search. CMD[8:7] is ignored in this cycle.
- **Cycle B**: The host ASIC continues to drive the CMDV HIGH and applies Search command (10) on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([203:136]) to be compared to all locations 1 in the four 68-bits-word page.
- **Cycle C**: The host ASIC drives the CMDV HIGH and applies Search command code (10) on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for the bits [135:0] of the data being searched. CMD[8:7] signals must be driven with the bits that will be driven by this device on SADR[21:20] if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared to all locations 2 in the four 68-bits-word page. The CMD[2] signal must be driven to logic 0.
- **Cycle D**: The host ASIC continues to drive the CMDV HIGH and continues to apply Search command code (10) on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the hit flag (see page 14 for a description of SSR[0:7]). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations 3 in the four 68-bits-word page. CMD[5:2] is ignored because the Learn instruction is not supported for x272 tables.

Note. For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during cycles A, B, C, and D. The GMR Index in cycle A selects a pair of GMRs in each of the 31 devices that apply to DQ data in cycles A and B. The GMR Index in cycle C selects a pair of GMRs in each of the 31 devices that apply to DQ data in cycles C and D.

The logical 272-bit Search operation is as shown in *Figure 10-70*. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's cycles A and C in each of the 31 devices. The 272-bit word K that is presented on the DQ bus in cycles A, B, C, and D of the command is compared to each entry in the table starting at location 0. The first matching entry's location address L is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (See "SRAM Addressing" on page 100.). ***Note***. The matching address is always going to be location 0 in a four-entry page for 272-bit Search (two LSBs of the matching index will be 00).

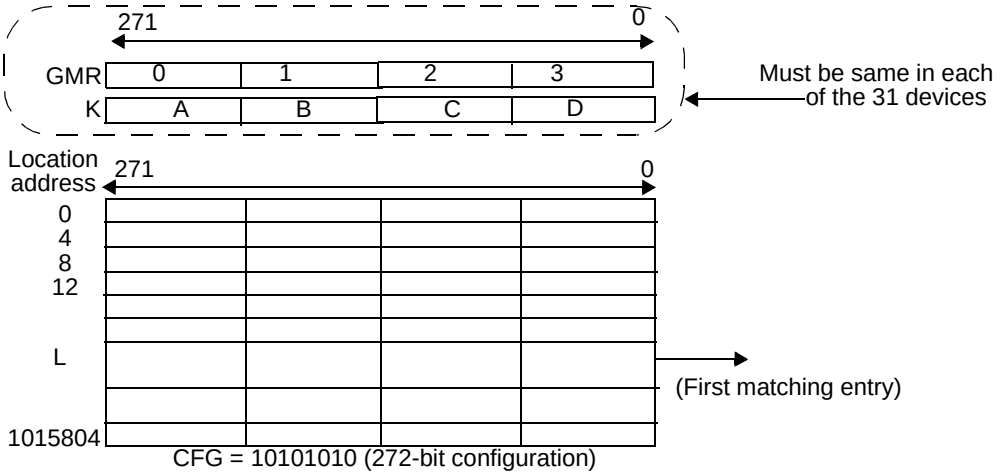


Figure 10-70. ×272 Table with 31 Devices

The Search command is a pipelined operation and executes a Search at one-fourth the rate of the frequency of CLK2X for 272-bit searches in ×272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit Search command (measured in CLK cycles) from the CLK2X cycle that contains the C and D cycles is shown in *Table 10-32*.

Table 10-32. The Latency of Search from C and D cycles to SRAM Access Cycle

Number of Devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K × 272 bits	4
1–8 (TLSZ = 01)	64K × 272 bits	5
1–31 (TLSZ = 10)	248K × 272 bits	6

The latency of a Search from command to SRAM access cycle is 6 for only a single device in the table and TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in *Table 10-33*.

Table 10-33. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

10.15 Mixed-Sized Searches on Tables Configured with Different Widths Using an CYNSE70064A Device

This subsection will cover mixed searches (×68, ×136, and ×272) with tables of different widths (×68, ×136, ×272). The sample operation shown is for a single device with CFG = 10010000 containing three tables of ×68, ×136, and ×272 widths. The operation can be generalized to a block of eight to 31 devices using four blocks; the timing and the pipeline operation is the same as described previously for fixed searches on a table of one-width-size.

Figure 10-71 shows three sequential searches: first, a 68-bit Search on the table configured as ×68, then a 136-bit Search on a table configured as ×136, and finally a 272-bit Search on the table configured as ×272 bits that each results in a hit. ***Note***. The DQ[67:66] will be 00 in each of the two A and B cycles of the ×68-bit Search (Search1). DQ[67:66] is 01 in each of the A and B cycles of the ×136-bit Search (Search2). DQ[67:66] is 10 in each of the A, B, C, and D cycles of the ×272-bit Search (Search3). By having table designation bits, the CYNSE70064A enables the creation of many tables in a bank of search engines of different widths.

Figure 10-72 shows the sample table. Two bits in each 68-bit entry will need to designated as the table number bits. One example choice can be the 00 values for the table configured as ×68, 01 values for tables configured as ×136, and 10 values for tables configured as ×272. For the above explanation, it is further assumed that bits [67:66] for each entry will be designed as such table designation bits.

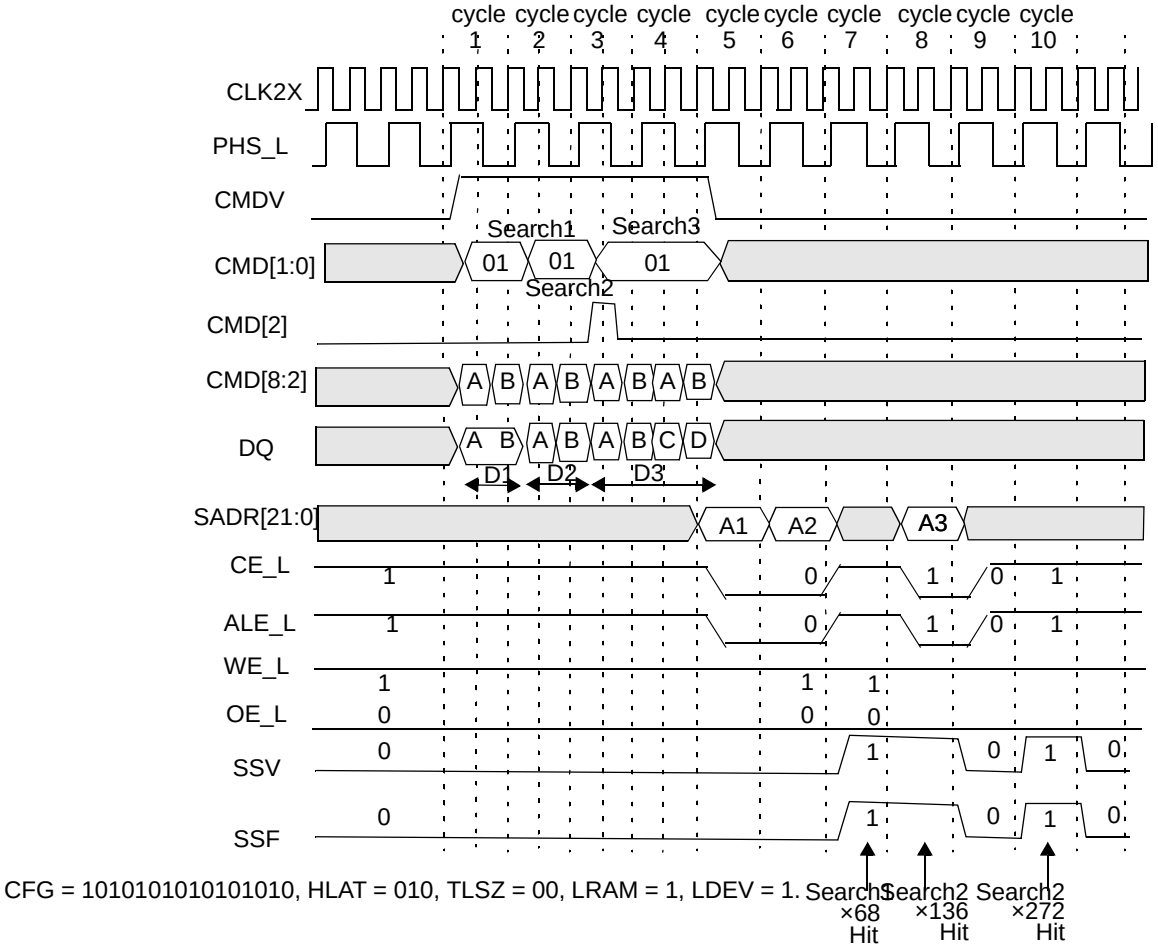


Figure 10-71. Timing Diagram for Mixed Search (One Device)

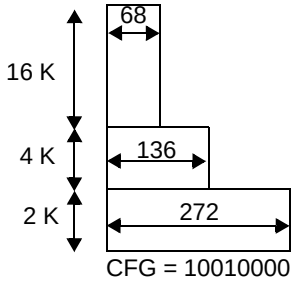


Figure 10-72. Multiwidth Configurations Example

10.16 LRAM and LDEV Description

When search engines are cascaded using multiple CYNSE70064As, the SADR, CE_L, and WE_L (three-state signals) are all tied together. In order to eliminate external pull-ups and pull-downs, one device in a bank is designated as the default driver. For non-Search or non-Learn cycles (see Subsection 10.17, “Learn Command” on page 94) or Search cycles with a global miss, the SADR, CE_L, and WE_L signals are driven by the device with the LRAM bit set. It is important that only one device in a bank of search engines that are cascaded have this bit set. Failure to do so will cause contention on SADR, CE_L, and WE_L and can potentially cause damage to the device(s).

Similarly, when search engines using multiple CYNSE70064As are cascaded, SSF and SSV (also three-state signals) are tied together. In order to eliminate external pull-up and pull downs, one device in a bank is designated as the default driver. For nonSearch cycles or Search cycles with a global miss the SSF and SSV signals are driven by the device with the LDEV bit set. It is important that only one device in a bank of search engines that are cascaded together have this bit set. Failure to do so will cause contention on SSV and SSF and can potentially cause damage to the device(s).

10.17 Learn Command

Bit[0] of each 68-bit data location specifies whether an entry in the database is occupied. If all the entries in a device are occupied, the device asserts FULO signal to inform the downstream devices that it is full. The result of this communication between depth-cascaded devices determines the global FULL signal for the entire table. The FULL signal in the last device determines the fullness of the depth-cascaded table.

The device contains 16 pairs of internal, 68-bit-wide comparand registers that store the comparands as the device executes searches. On a miss by the Search signalled to ASIC through the SSV and SSF signals (SSV = 1, SSF = 0), the host ASIC can apply the Learn command to learn the entry from a comparand register to the next-free location (see Subsection 7.8, “NFA Register” on page 16). The NFA updates to the next-free location following each Write or Learn command.

In a depth-cascaded table, only a single device will learn the entry through the application of a Learn instruction. The determination of which device is going to learn is based on the FULI and FULO signalling between the devices. The first non-full device learns the entry by storing the contents of the specified comparand registers to the location(s) pointed to by NFA.

In a ×68-configured table the Learn command writes a single 68-bit location. In a ×136-configured table the Learn command writes the next even and odd 68-bit locations. In 136-bit mode, bit[0] of the even and odd 68-bit locations is 0, which indicates that they are cascaded empty, or 1, which indicates that they are occupied.

The global FULL signal indicates to the table controller (the host ASIC) that all entries within a block are occupied and that no more entries can be learned. The CYNSE70064A updates the signal after each Write or Learn command to a data array. The Learn command generates a Write cycle to the external SRAM, also using the NFA register as part of the SRAM address (see Section 12.0, “SRAM Addressing” on page 100).

The Learn command is supported on a single block containing up to eight devices if the table is configured either as a ×68 or a ×136. The Learn command is not supported for ×272-configured tables.

Learn is a pipelined operation and lasts for two CLK cycles, as shown in *Figure 10-73* where TLSZ = 00, and *Figure 10-74* and *Figure 10-75* where TLSZ = 01. *Figure 10-74* and *Figure 10-75* assume that the device performing the Learn operation is not the last device in the table and has its LRAM bit set to 0. ***Note***. The OE_L for the device with the LRAM bit set goes HIGH for two cycles for each Learn (one during the SRAM Write cycle, and one the cycle before). The latency of the SRAM Write cycle from the second cycle of the instruction is shown in *Table 10-34*.

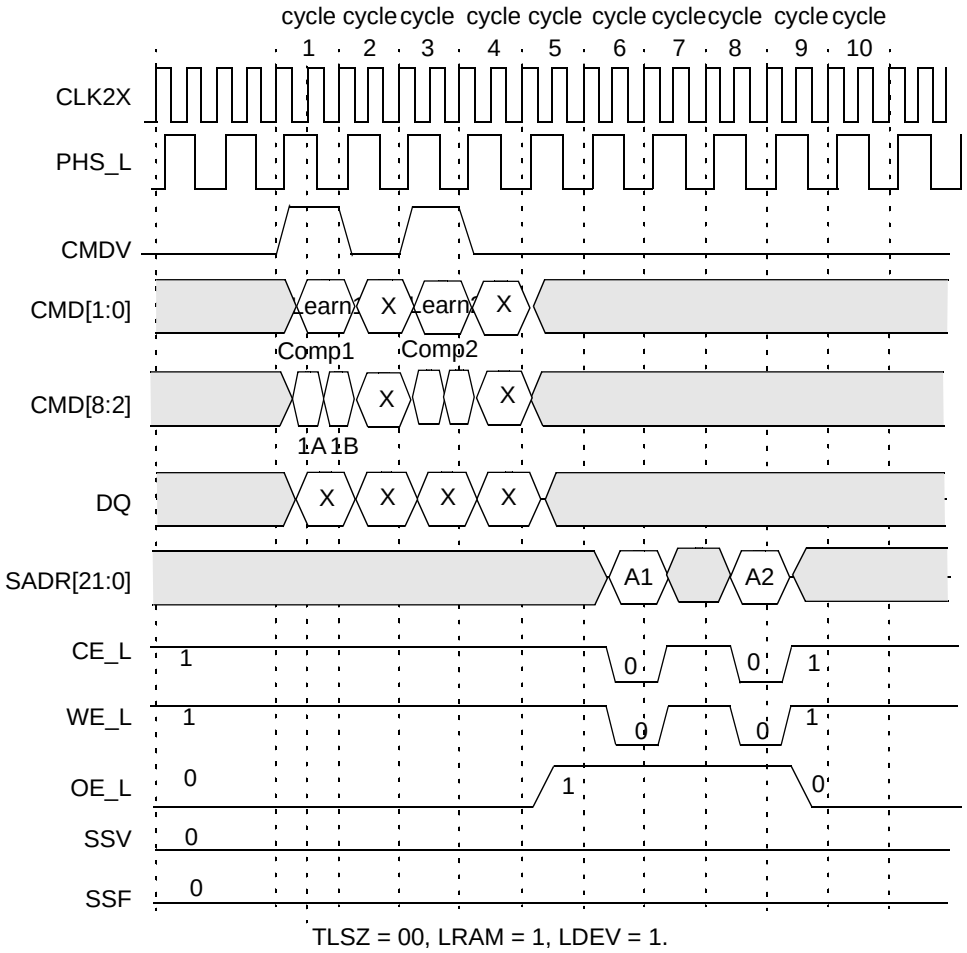
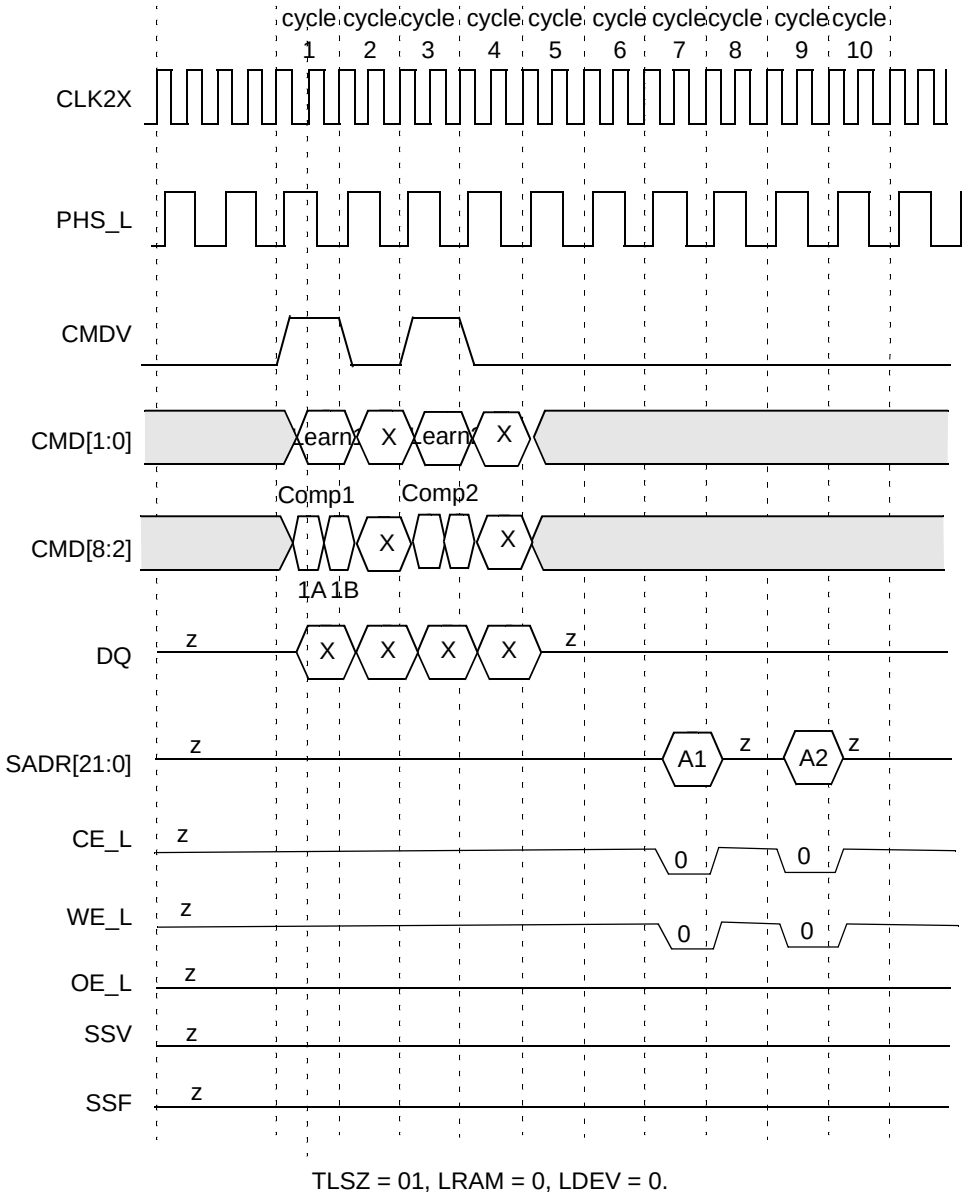
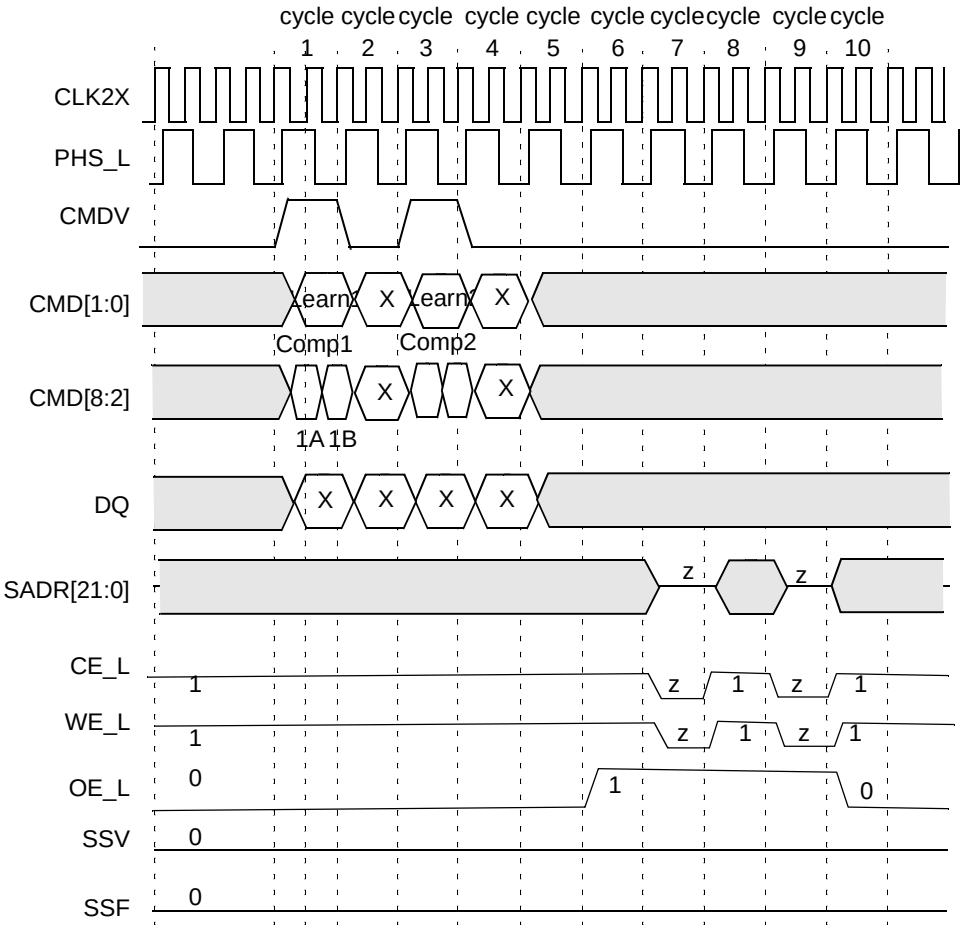


Figure 10-73. Timing Diagram of Learn (TLSZ = 00)



TLSZ = 01, LRAM = 0, LDEV = 0.

Figure 10-74. Timing Diagram of Learn (Except on the Last Device [TLSZ = 01])



TLSZ = 01, LRAM = 1, LDEV = 1.

Figure 10-75. Timing Diagram of Learn on Device Number 7 (TLSZ = 01)

Table 10-34. The Latency of SRAM Write Cycle from Second Cycle of Learn Instruction

Number of Devices	Latency in CLK Cycles
1 (TLSZ = 00)	4
1–8 (TLSZ = 01)	5
1–31 (TLSZ = 10)	6

The Learn operation lasts two CLK cycles. The sequence of operation is as follows.

- **Cycle 1A**: The host ASIC applies the Learn instruction on CMD[1:0] using CMDV = 1. The CMD[5:2] field specifies the index of the comparand register pair that will be written in the data array in the 136-bit-configured table. For a Learn in a 68-bit-configured table, the even-numbered comparand specified by this index will be written. CMD[8:7] carries the bits that will be driven on SADR[21:20] in the SRAM Write cycle.
- **Cycle 1B**: The host ASIC continues to drive the CMDV to 1, the CMD[1:0] to 11, and the CMD[5:2] with the comparand pair index. CMD[6] must be set to 0 if the Learn is being performed on a 68-bit-configured table, and to 1 if the Learn is being performed on a 136-bit-configured table.
- **Cycle 2**: The host ASIC drives the CMDV to 0.

At the end of cycle 2, a new instruction can begin. The latency of the SRAM Write is the same as the Search to the SRAM Read cycle. It is measured from the second cycle of the Learn instruction.

11.0 Depth-Cascading

The Search engine application can depth-cascade the devices to various table sizes of different widths (68 bits, 136 bits, or 272 bits). The devices perform all the necessary arbitration to decide which device will drive the SRAM bus. The latency of the searches increases as the table size increases; the Search rate remains constant.

11.1 Depth-Cascading up to Eight Devices (One Block)

Figure 11-1 shows how up to eight devices can be cascaded to form 256K × 68, 128K × 136, or 64K × 272 tables. It also shows the interconnection between the devices for depth-cascading. Each Search engine asserts the LHO[1] and LHO[0] signals to inform downstream devices of its result. The LHI[6:0] signals for a device are connected to LHO signals of the upstream devices. The host ASIC must program the TLSZ to 01 for each of up to eight devices in a block. Only a single device drives the SRAM bus in any single cycle.

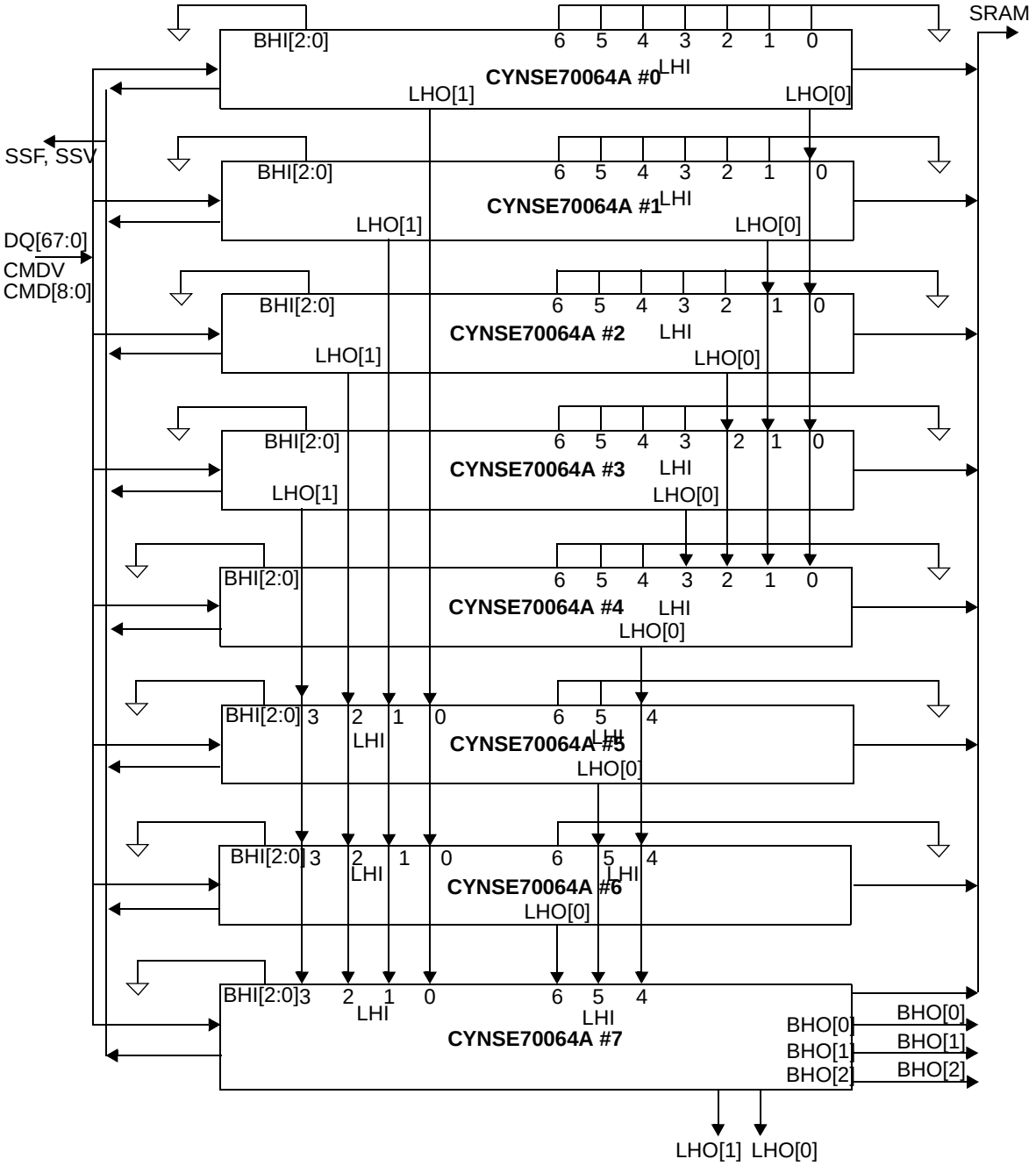


Figure 11-1. Depth-Cascading to Form a Single Block

11.2 Depth-Cascading up to 31 Devices (Four Blocks)

Figure 11-2 shows how to cascade up to four blocks. Each block contains up to eight CYNSE70064A devices except the last, and the interconnection within each was shown in the previous subsection with the cascading of up to eight devices in a block. ***Note***. The interconnection between blocks for depth-cascading is important. For each Search, a block asserts BHO[2], BHO[1], and BHO[0]. The BHO[2:0] signals for a block are the signals taken only from the last device in the block. For all other devices within that block, these signals stay open and floating. The host ASIC must program the table size (TLSZ) field to 10 in each of the devices for cascading up to 31 devices (in up to four blocks).

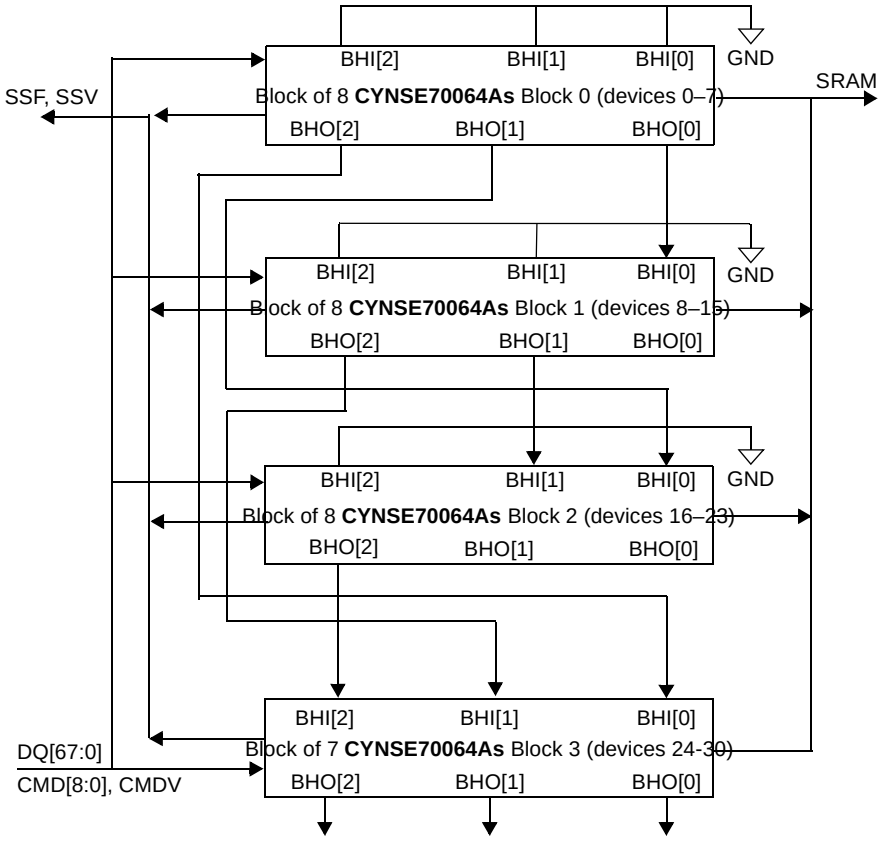


Figure 11-2. Depth-Cascading Four Blocks

11.3 Depth-Cascading for a FULL Signal

Bit[0] of each of the 68-bit entries is designated as a special bit (1 = occupied; 0 = empty). For each Learn or PIO Write to the data array, each device asserts FULO[1] and FULO[0] if it does not have any empty locations within it (see *Figure 11-3*). Each device combines the FULO signals from the devices above it with its own full status to generate a FULL signal that gives the full status of the table up to the device asserting the FULL signal. *Figure 11-3* shows the hardware connection diagram for generating the FULL signal that goes back to the ASIC. In a depth-cascaded block of up to eight devices, the FULL signal from the last device should be fed back to the ASIC controller to indicate the fullness of the table. The FULL signal of the other devices should be left open. ***Note***. The Learn instruction is supported for only up to eight devices, whereas FULL cascading is allowed only for one block in tables containing more than eight devices. In tables for which a Learn instruction is not going to be used, the bit[0] of each 68-bit entry should always be set to 1.

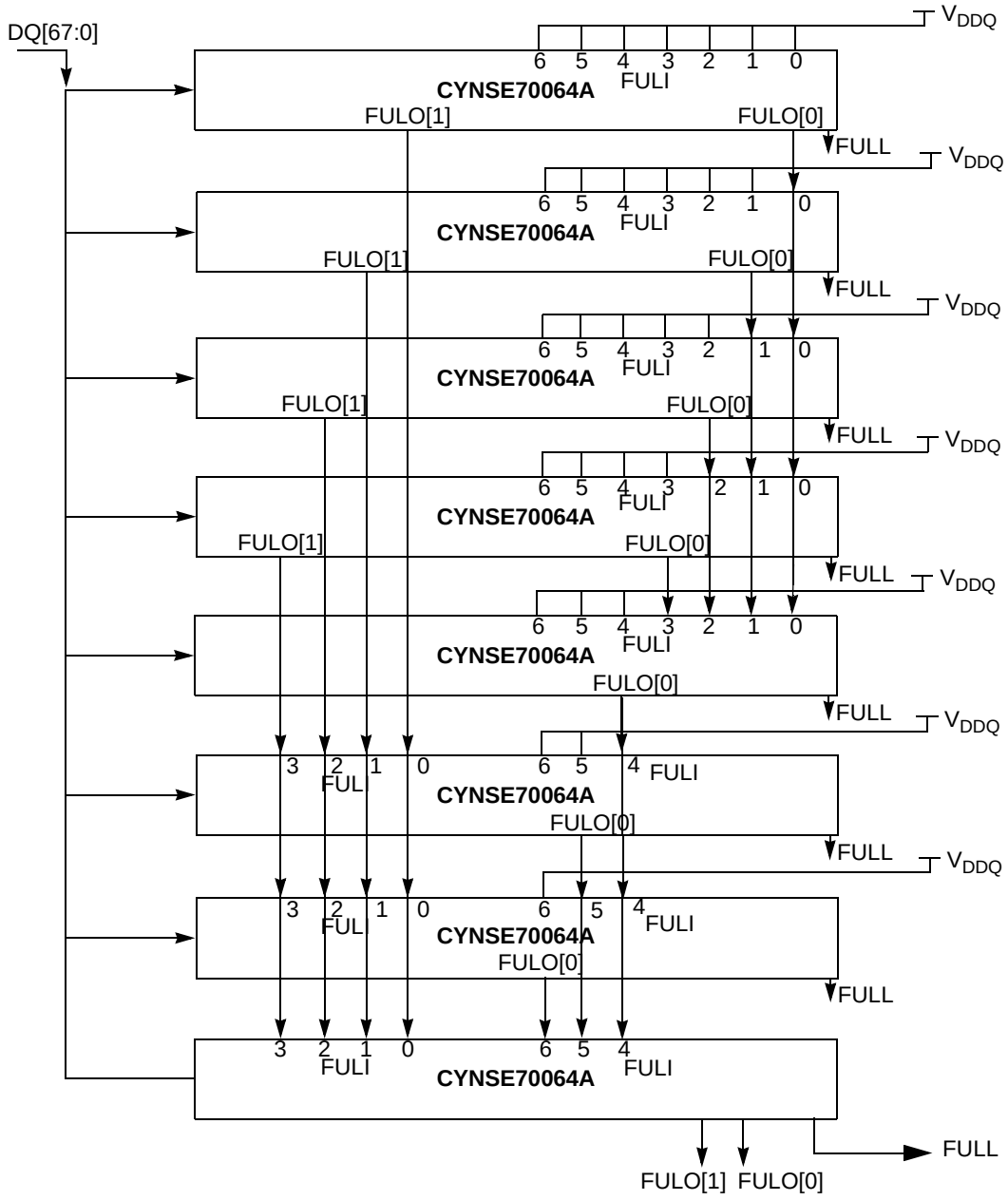


Figure 11-3. Full Generation in a Cascaded Table

12.0 SRAM Addressing

Table 12-1 describes the commands used to generate addresses on the SRAM address bus. The index [14:0] field contains the address of a 68-bit entry that results in a hit in 68-bit-configured partition. It is the address of the 68-bit entry that lies at the 136-bit page, and the 272-bit page boundaries in 136-bit- and 272-bit-configured quadrants, respectively.

Section 7.0, “Registers” on page 13 of this specification, describes the NFA and SSR registers. ADR[14:0] contains the address supplied on the DQ bus during PIO access to the CYNSE70064A. Command bits 8, and 7 {CMD[8:7]} are passed from the command to the SRAM address bus. See Section 10.0, “Commands” on page 18, for more information. ID[4:0] is the ID of the device driving the SRAM bus (see Section 18.0, “Pinout Descriptions and Package Diagrams” on page 121, for more information).

12.1 Generating an SRAM BUS Address

Table 12-1. SRAM Bus Address

Command	SRAM Operation	21	20	[19:15]	[14:0]
Search	Read	C8	C7	ID[4:0]	Index[14:0]
Learn	Write	C8	C7	ID[4:0]	NFA[14:0]
PIO Read	Read	C8	C7	ID[4:0]	ADR14:0]
PIO Write	Write	C8	C7	ID[4:0]	ADR[14:0]
Indirect Access	Write/Read	C8	C7	ID[4:0]	SSR[14:0]

12.2 SRAM PIO Access

The remainder of Section 12.0 describes SRAM Read and SRAM Write operations.

SRAM Read enables Read access to the off-chip SRAM containing associative data. The latency from the issuance of the Read instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction and will be depend on the value programmed for the TLSZ parameter in the device configuration register. The latency of the ACK from the Read instruction is the same as the latency of the Search instruction to the SRAM address plus the HLAT programmed in the configuration register. ***Note***. SRAM Read is a blocking operation—no new instruction can begin until the ACK is returned by the selected device performing the access.

SRAM Write enables Write access to the off-chip SRAM containing associative data. The latency from the second cycle of the Write instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction and will depend on the TLSZ value parameter programmed in the device configuration register. ***Note***. SRAM Write is a pipelined operation—new instruction can begin right after the previous command has ended.

12.3 SRAM Read with a Table of One Device

SRAM Read enables Read access to the off-chip SRAM containing associative data. The latency from the issuance of the Read instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction and will depend on the TLSZ value parameter programmed in the device configuration register. The latency of the ACK from the Read instruction is the same as the latency of the Search instruction to the SRAM address plus the HLAT programmed in the configuration register. The following explains the SRAM Read operation in a table with only one device that has the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. *Figure 12-1* shows the associated timing diagram. For the following description, the selected device refers to the only device in the table because it is the only device to be accessed.

- **Cycle 1A**: The host ASIC applies the Read instruction on the CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[21:20] on CMD[8:7].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction on the CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[67:0] and drives ACK from High-Z to LOW.
- **Cycle 5**: The selected device drives the Read address on SADR[21:0]; it also drives ACK HIGH, CE_L LOW, and ALE_L LOW.
- **Cycle 6**: The selected device drives CE_L HIGH, ALE_L HIGH, the SADR bus, the DQ bus in a three-state condition, and ACK LOW.

At the end of cycle 6, the selected device floats ACK in a three-state condition, and a new command can begin.

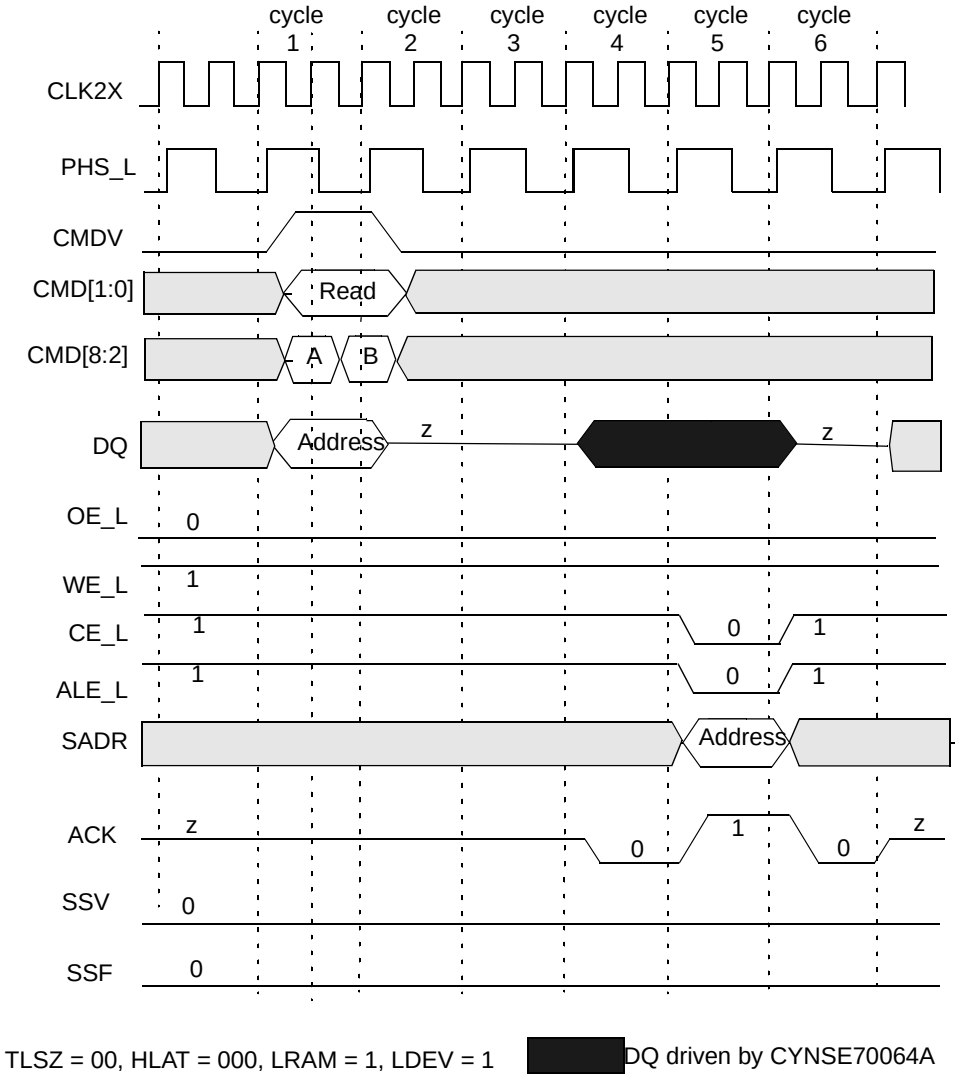


Figure 12-1. SRAM Read Access (TLSZ = 00, HLAT = 000, LRAM = 1, LDEV = 1)

12.4 SRAM Read with a Table of up to Eight Devices

The following explains the SRAM Read operation completed through a table of up to eight devices using the following parameters: TLSZ = 01. *Figure 12-2* diagrams a block of eight devices. The following assumes that SRAM access is successfully achieved through CYNSE70064A device number 0. *Figure 12-3* and *Figure 12-4* show timing diagrams for device number 0 and device number 7, respectively.

- **Cycle 1A**: The host ASIC applies the Read instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. During this cycle the host ASIC also supplies SADR[21:20] on CMD[8:7].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction on CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10 to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[67:0].
- **Cycle 5**: The selected device continues to drive DQ[67:0] and drives ACK from High-Z to LOW.
- **Cycle 6**: The selected device drives the Read address on SADR[21:0]. It also drives ACK HIGH, CE_L LOW, WE_L HIGH, and ALE_L LOW.
- **Cycle 7**: The selected device drives CE_L, ALE_L, WE_L, and DQ bus in a three-state condition. It continues to drive ACK LOW.

At the end of cycle 7, the selected device floats ACK in three-state condition and a new command can begin.

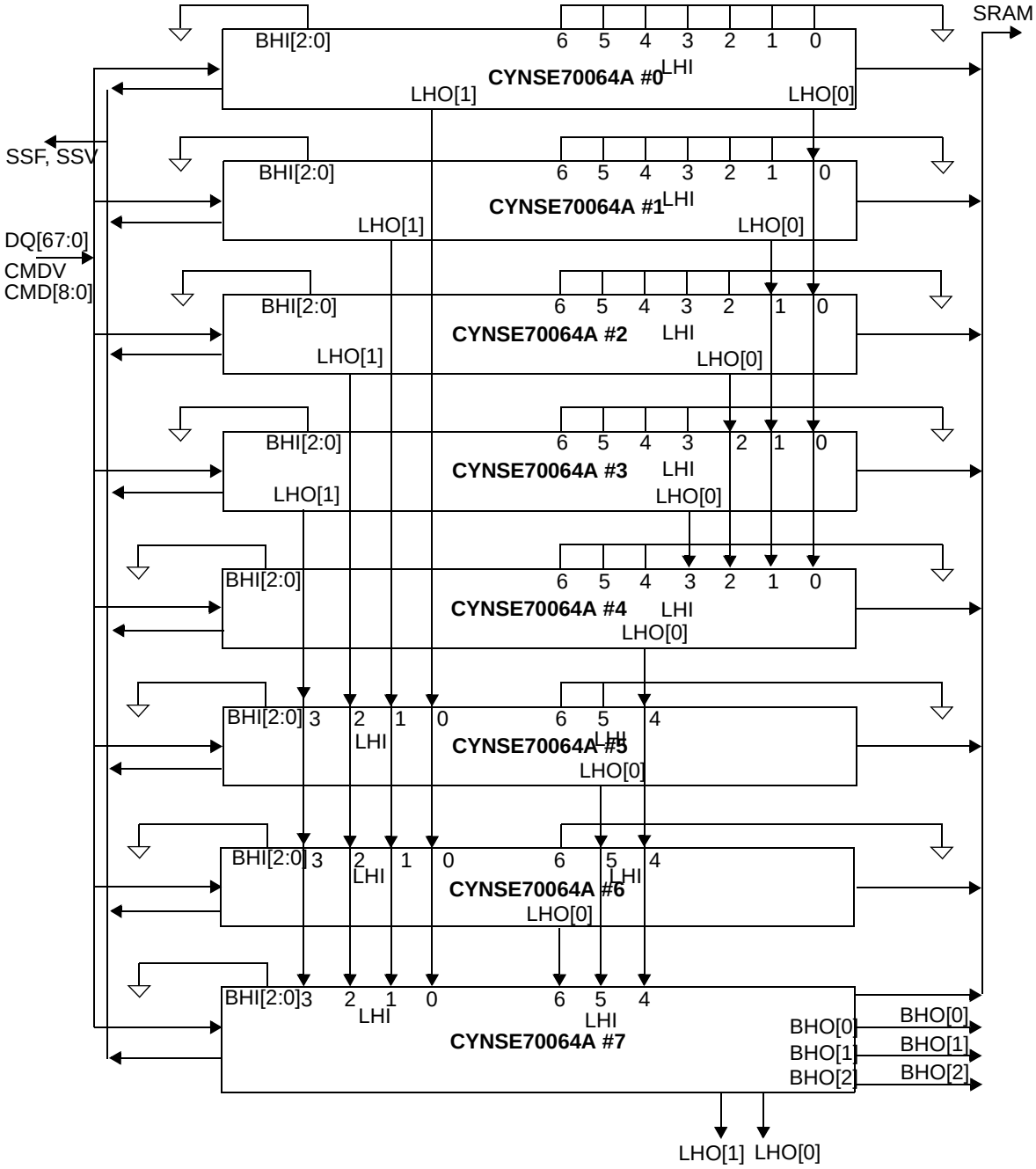


Figure 12-2. Table of a Block of Eight Devices

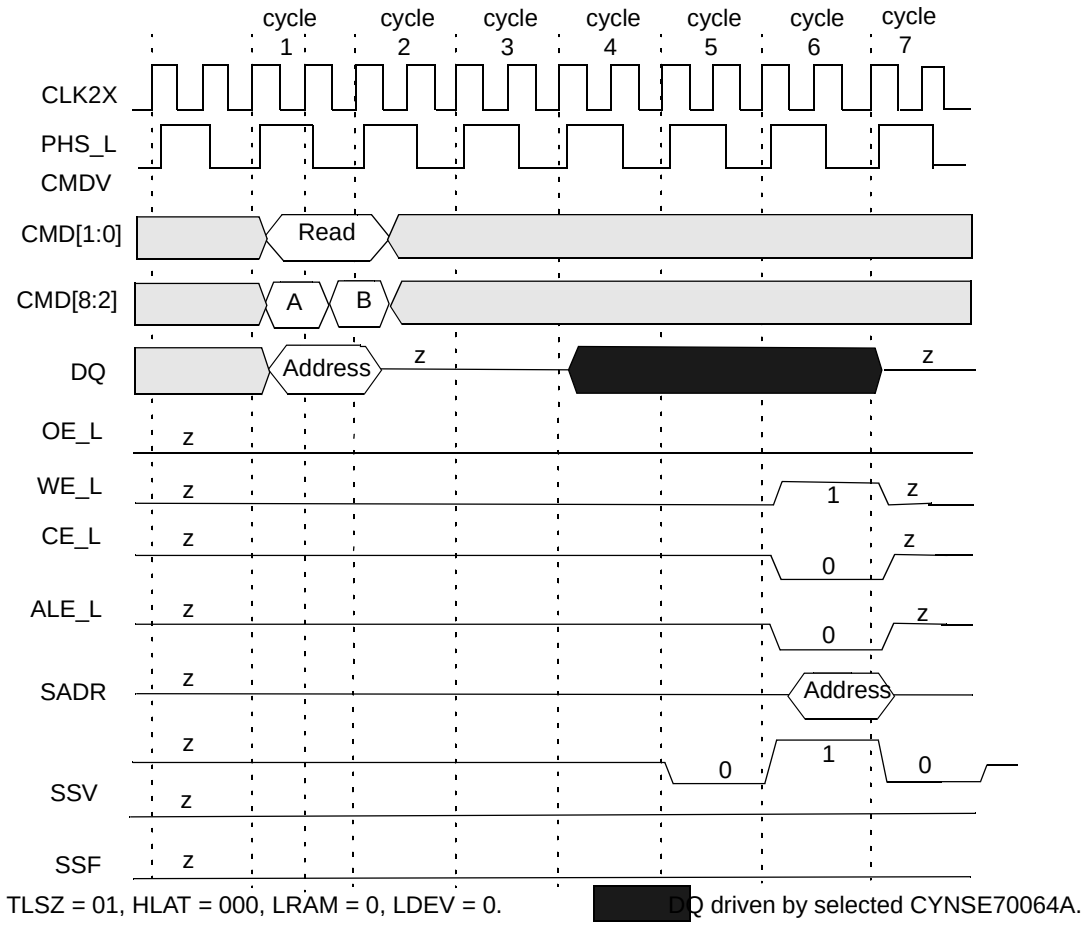
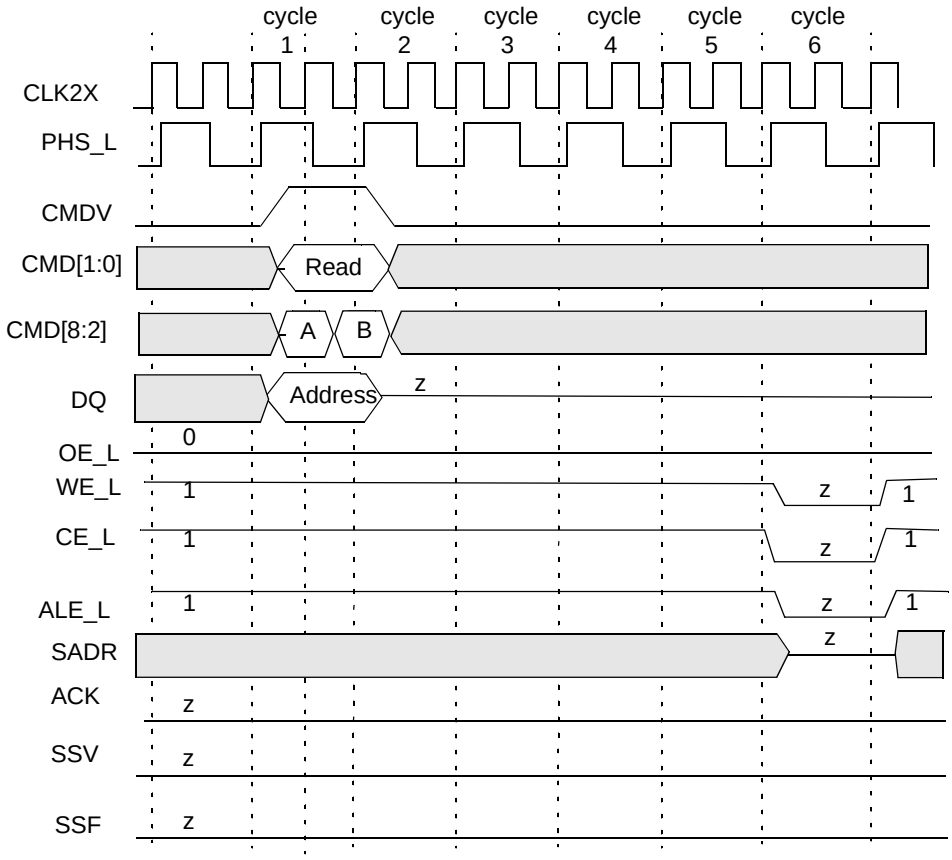


Figure 12-3. SRAM Read Through Device Number 0 in a Block of Eight Devices



TLSZ = 01, HLAT = 000, LRAM = 1, LDEV = 1.

Figure 12-4. SRAM Read Timing for Device Number 7 in a Block of Eight Devices

12.5 SRAM Read with a Table of up to 31 Devices

The following explains the SRAM Read operation accomplished through a table of up to 31 devices, using the following parameters: TLSZ = 10. The diagram of such a table is shown in *Figure 12-5*. The following assumes that SRAM access is being accomplished through CYNSE70064A device number 0, that device number 0 is the selected device. *Figure 12-6* and *Figure 12-7* show the timing diagrams for device number 0 and device number 30, respectively.

- **Cycle 1A**: The host ASIC applies the Read instruction to CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[21:20] on CMD[8:7].
- **Cycle 1B**: The host ASIC continues to apply the Read instruction to CMD[1:0] using CMDV = 1. The DQ bus supplies the address, with DQ[20:19] set to 10, to select the SRAM address.
- **Cycle 2**: The host ASIC floats DQ[67:0] to a three-state condition.
- **Cycle 3**: The host ASIC keeps DQ[67:0] in a three-state condition.
- **Cycle 4**: The selected device starts to drive DQ[67:0].
- **Cycles 5 to 6**: The selected device continues to drive DQ[67:0].
- **Cycle 7**: The selected device continues to drive DQ[67:0] and drives an SRAM Read cycle.
- **Cycle 8**: The selected device drives ACL from Z to LOW.
- **Cycle 9**: The selected device drives ACK to HIGH.
- **Cycle 10**: The selected device drives ACK from HIGH to LOW.

At the end of cycle 10, the selected device floats ACL in a three-state condition.

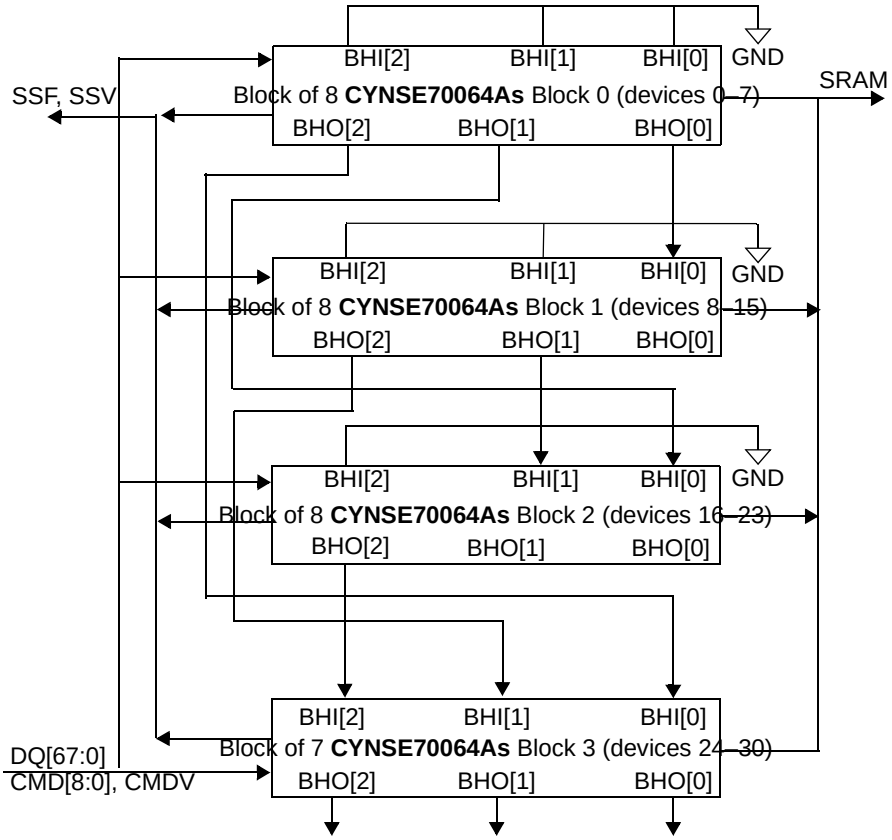


Figure 12-5. Table of 31 Devices Made of Four Blocks

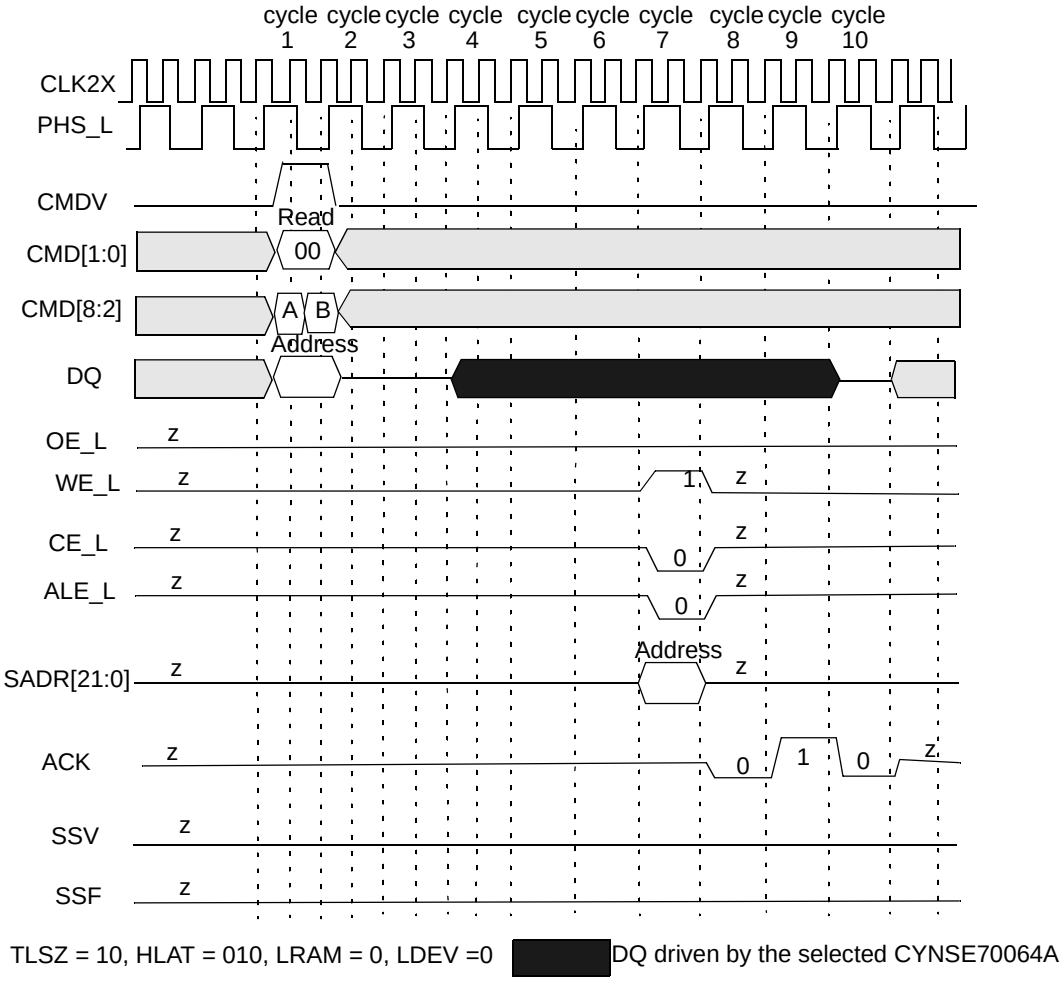


Figure 12-6. SRAM Read Through Device Number 0 in a Bank of 31 Devices (Device Number 0 Timing)

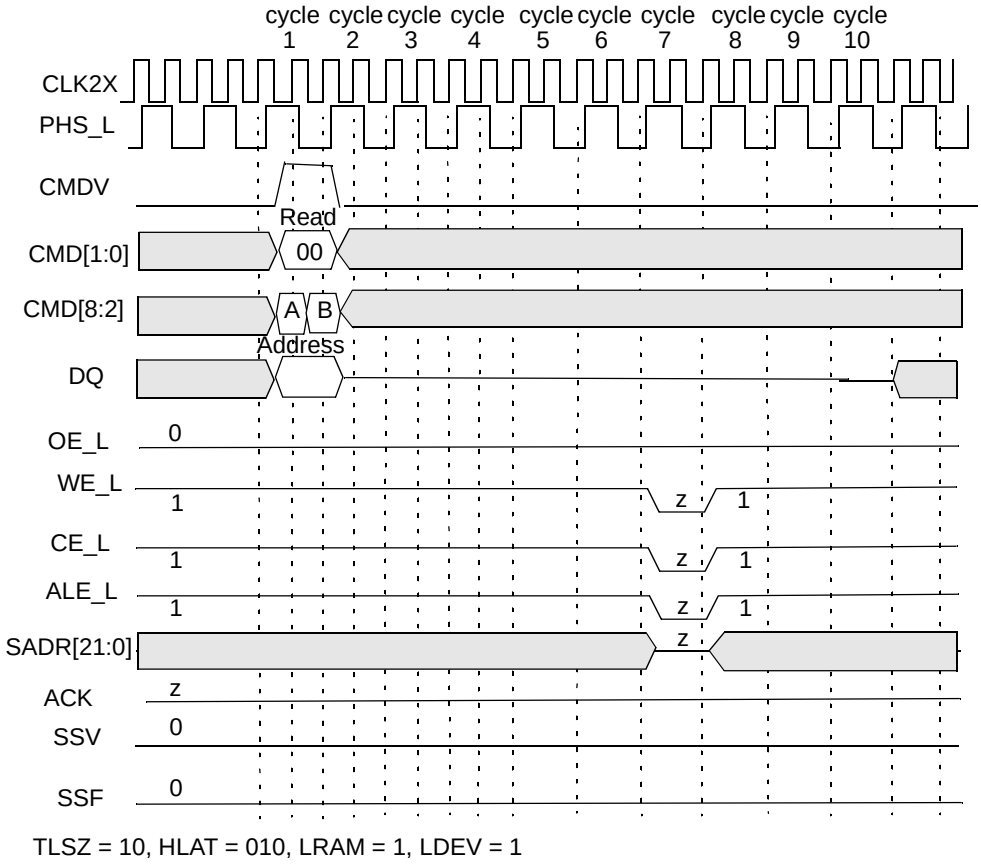


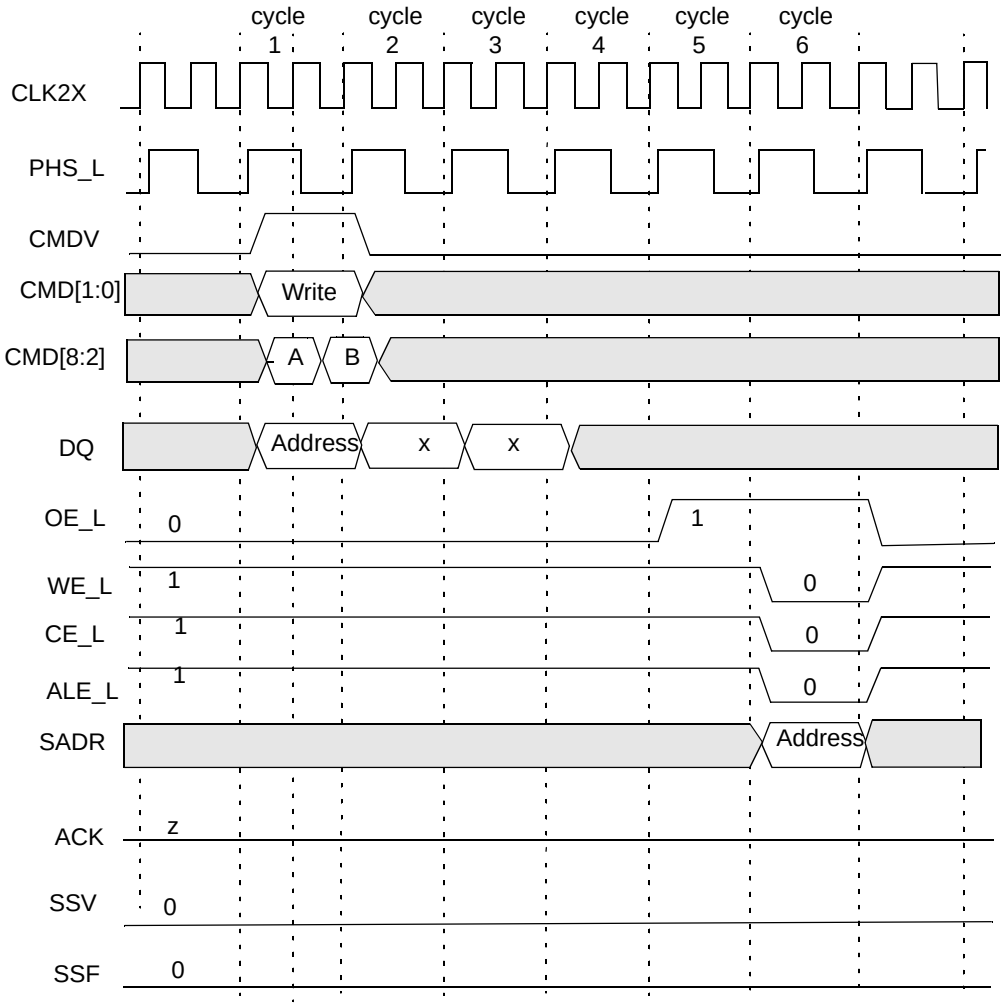
Figure 12-7. SRAM Read Through Device Number 0 in Bank of 31 Devices (Device Number 30 Timing)

12.6 SRAM Write with a Table of One Device

SRAM Write enables Write access to the off-chip SRAM that contains associative data. The latency from the second cycle of the Write instruction to the address appearing on the SRAM bus is the same as the latency of the Search instruction, and will depend on the TLSZ value parameter programmed in the device configuration register. The following explains the SRAM Write operation accomplished through a table of only one device with the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. *Figure 12-8* shows the timing diagram. For the following description the selected device refers to the only device in the table as it is the only device that will be accessed.

- **Cycle 1A**: The host ASIC applies the Write instruction on the CMD[1:0], using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:20] on CMD[8:7] in this cycle. **Note**. CMD[2] must be set to 0 for SRAM Write as burst Writes into the SRAM are not supported.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on the CMD[1:0], using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. Note that CMD[2] must be set to 0 for SRAM Write as burst Writes into the SRAM are not supported.
- **Cycle 2**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70064A.
- **Cycle 3**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70064A.

At the end of cycle 3, a new command can begin. The Write is a pipelined operation, however the Write cycle appears at the SRAM bus with the same latency as the latency of Search instruction as measured from the second cycle of the Write command.



TLSZ = 00, HLAT = 000, LRAM = 1, LDEV = 1.

Figure 12-8. SRAM Write Access (TLSZ = 00, HLAT = 000, LRAM = 1, LDEV = 1)

12.7 SRAM Write with a Table of up to Eight Devices

The following explains the SRAM Write operation done through a table(s) of up to eight devices with the following parameters (TLSZ = 01). The diagram of such a table is shown in *Figure 12-9*. The following assumes that SRAM access is done through CYNSE70064A device number 0. *Figure 12-10* and *Figure 12-11* show the timing diagram for device number 0 and device number 7, respectively.

- **Cycle 1A**: The host ASIC applies the Write instruction on the CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:20] on CMD[8:7] in this cycle. ***Note***. CMD[2] must be set to 0 for SRAM Write, as burst Writes into the SRAM are not supported.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on the CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. ***Note***. CMD[2] must be set to 0 for SRAM Write, as burst Writes into the SRAM are not supported.
- **Cycle 2**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70064A.
- **Cycle 3**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70064A.

At the end of cycle 3, a new command can begin. The Write is a pipelined operation, but the Write cycle appears at the SRAM bus with the same latency as that of a Search instruction as measured from the second cycle of the Write command.

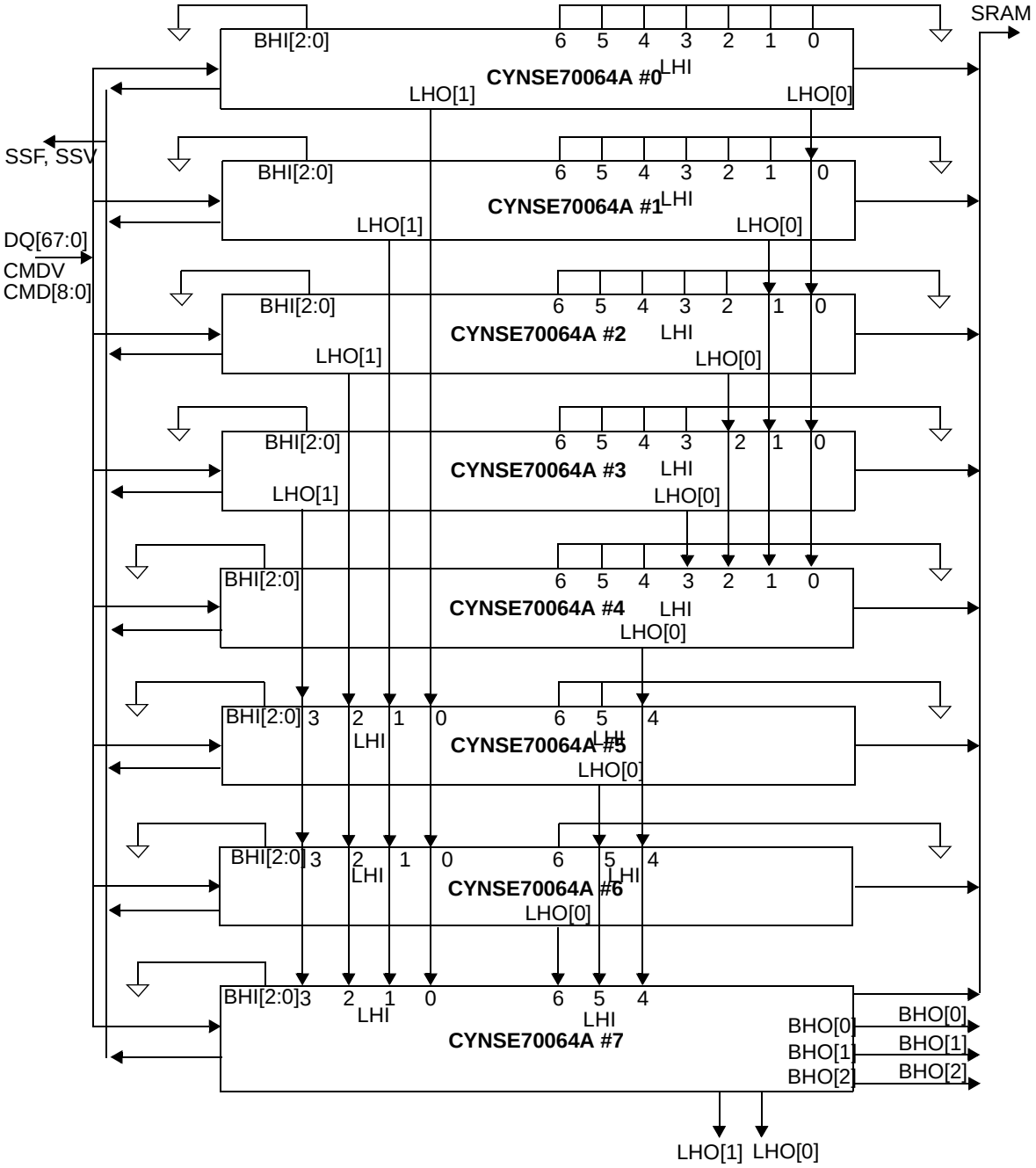


Figure 12-9. Table of a Block of Eight Devices

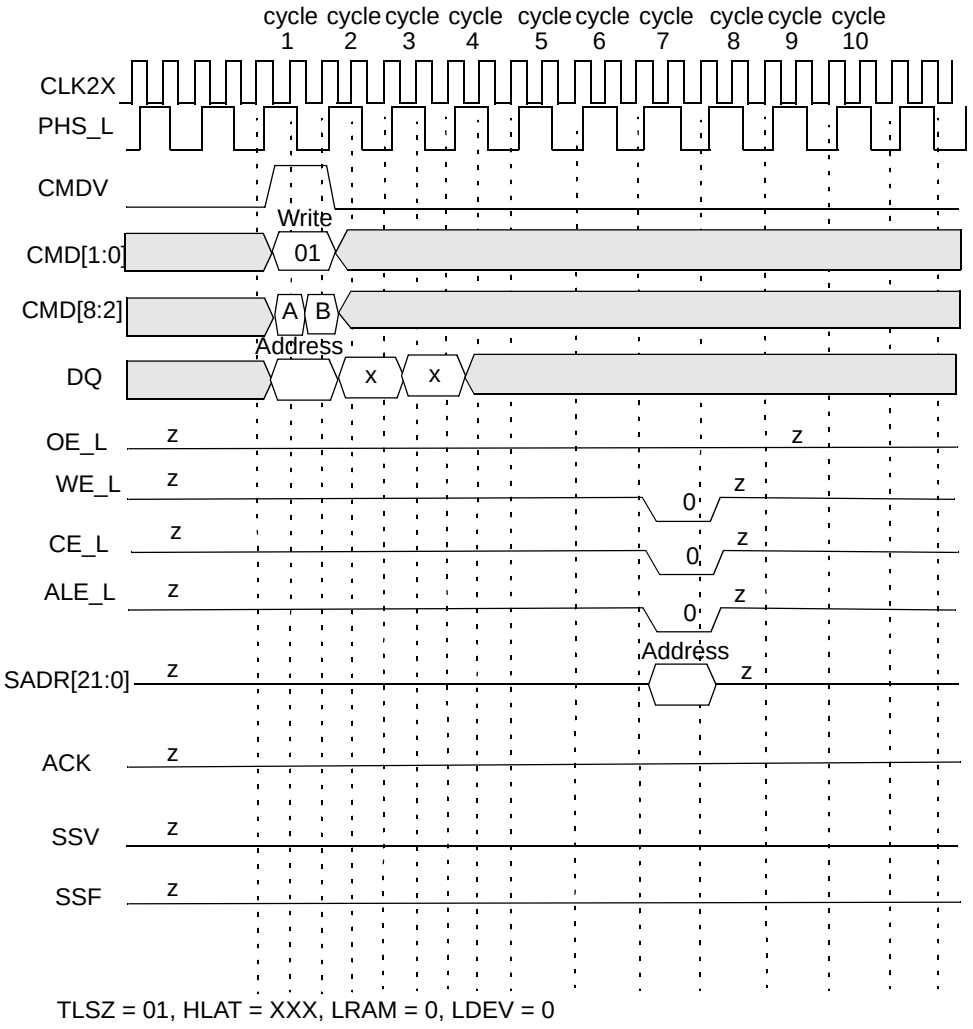


Figure 12-10. SRAM Write Through Device Number 0 in a Block of Eight Devices

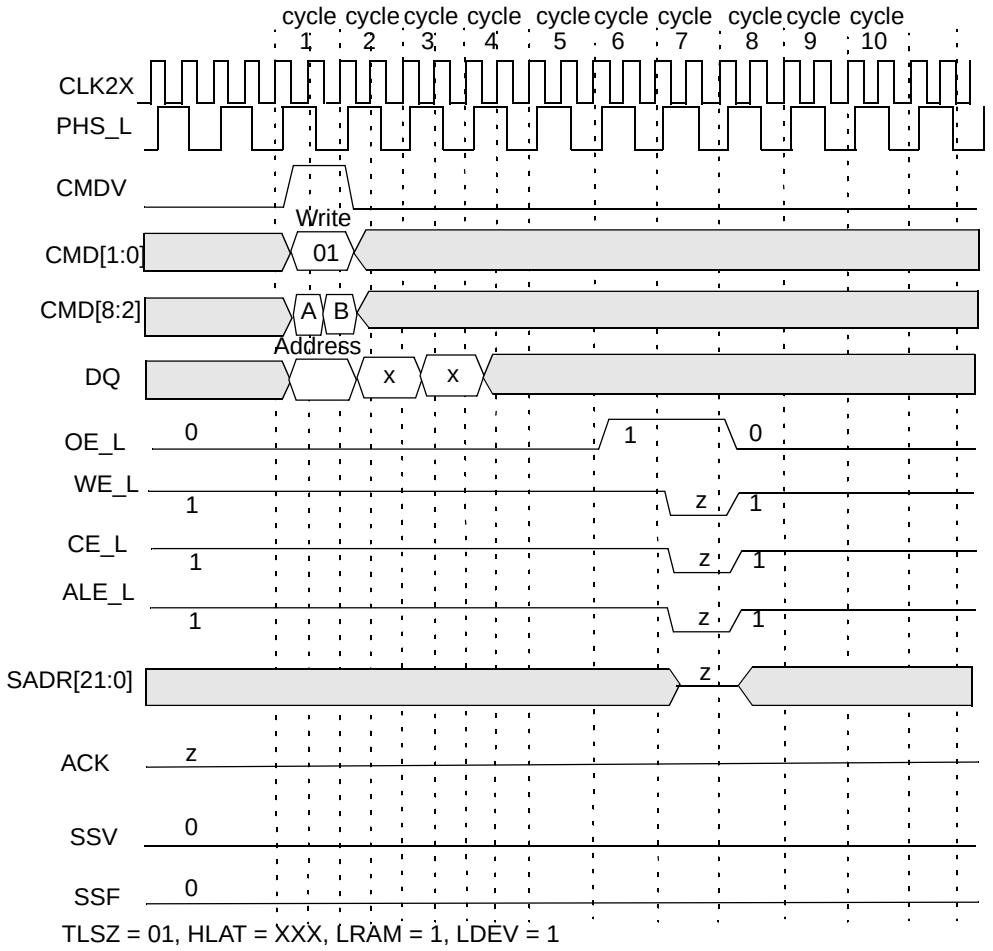


Figure 12-11. SRAM Write Timing for Device Number 7 in Block of Eight Devices

12.8 SRAM Write with Table(s) of up to 31 Devices

The following explains the SRAM Write operation done through a table(s) of up to 31 devices with the following parameters (TLSZ = 10). The diagram of such table(s) is shown in *Figure 12-12*. The following assumes that SRAM access is done through CYNSE70064A device number 0—device 0 is the selected device. *Figure 12-13* and *Figure 12-14* show the timing diagram for device number 0 and device number 30, respectively.

- **Cycle 1A**: The host ASIC applies the Write instruction on the CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:20] on CMD[8:7] in this cycle. ***Note***. CMD[2] must be set to 0 for SRAM Write, as burst Writes into the SRAM are not supported.
- **Cycle 1B**: The host ASIC continues to apply the Write instruction on the CMD[1:0] using CMDV = 1. The DQ bus supplies the address with DQ[20:19] set to 10 to select the SRAM address. ***Note***. CMD[2] must be set to 0 for SRAM Write, as burst Writes into the SRAM are not supported.
- **Cycle 2**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70064A.
- **Cycle 3**: The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the CYNSE70064A.

At the end of cycle 3, a new command can begin. The Write is a pipelined operation, but the Write cycle appears at the SRAM bus with the same latency as that of a Search instruction, as measured from the second cycle of the Write command.

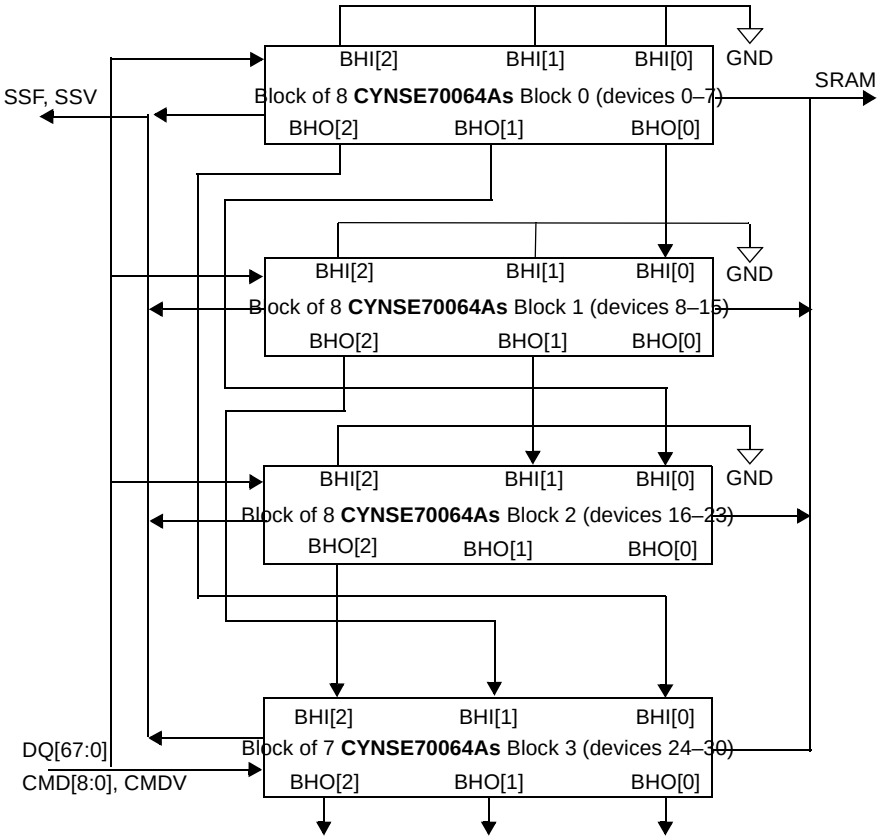
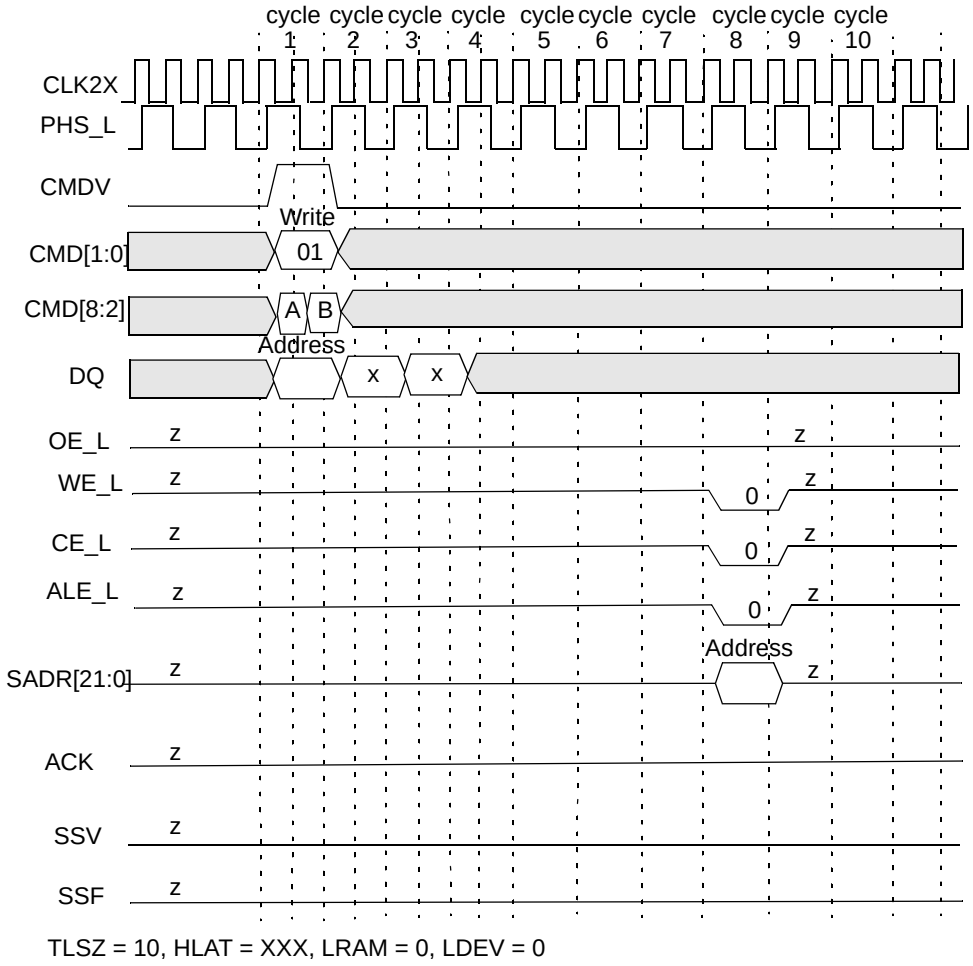


Figure 12-12. Table of 31 Devices (Four Blocks)



TLSZ = 10, HLAT = XXX, LRAM = 0, LDEV = 0

Figure 12-13. SRAM Write Through Device Number 0 in Bank of 31 Devices (Device 0 Timing)

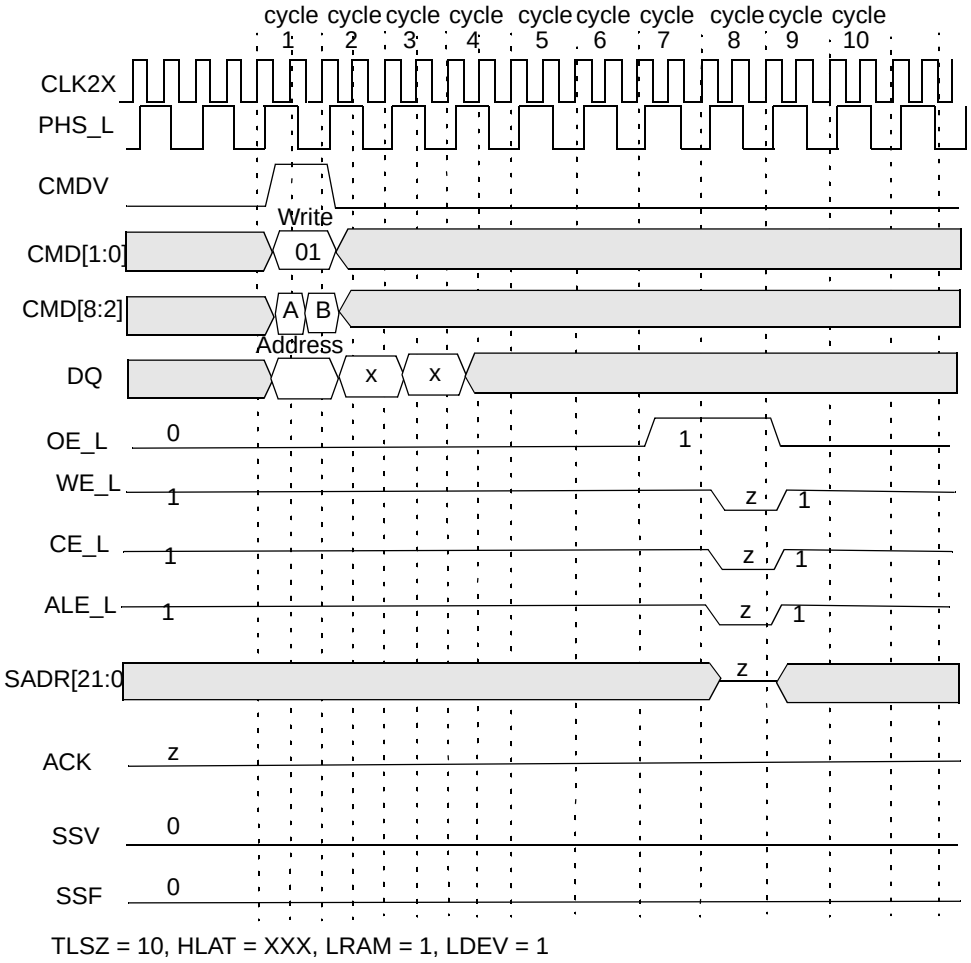


Figure 12-14. SRAM Write Through Device Number 0 in Bank of 31 CYNSE70064A Devices (Device Number 30 Timing)

13.0 Power

13.1 Proper Power-up Sequence

The proper power-up sequence is required to correctly initialize the Cypress NSEs before functional access to the device can begin. RST_L and TRST_L should be held low before the power supplies ramp-up. RST_L must be set low for a duration of time afterward and then set high. The following steps describe the proper power-up sequence.

1. Set RST_L and TRST_L low.
2. Power up V_{DD}, V_{DDQ} and start running CLK2X and PHS_L. The order in which these signals (including V_{DD} and V_{DDQ}) are applied is not critical.
3. Hold RST_L low for a minimum of 64 CLK2X cycles. The counting starts on the first rising edge of CLK2X when PHS_L is high, after both V_{DD} and V_{DDQ} have reached their steady state voltages. Set RST_L high afterward to complete the power-up sequence. For JTAG reset, TRST_L can be brought high after both V_{DD} and V_{DDQ} have reached their steady state voltages.

Figure 13-1 illustrates the proper sequences of the power-up operation.

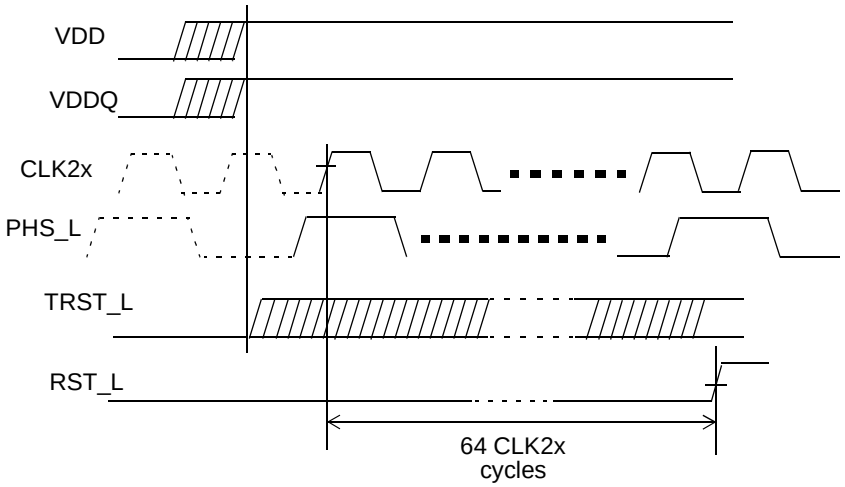


Figure 13-1. Power-up Sequence

14.0 Application

Figure 14-1 shows how a Search engine subsystem can be formed using a host ASIC and an CYNSE70064A bank. It also shows how this Search engine subsystem is integrated in a switch or router. The CYNSE70064A can access synchronous and asynchronous SRAMs by allowing the host ASIC to set the same HLAT parameter in all search engines within a bank of search engines.

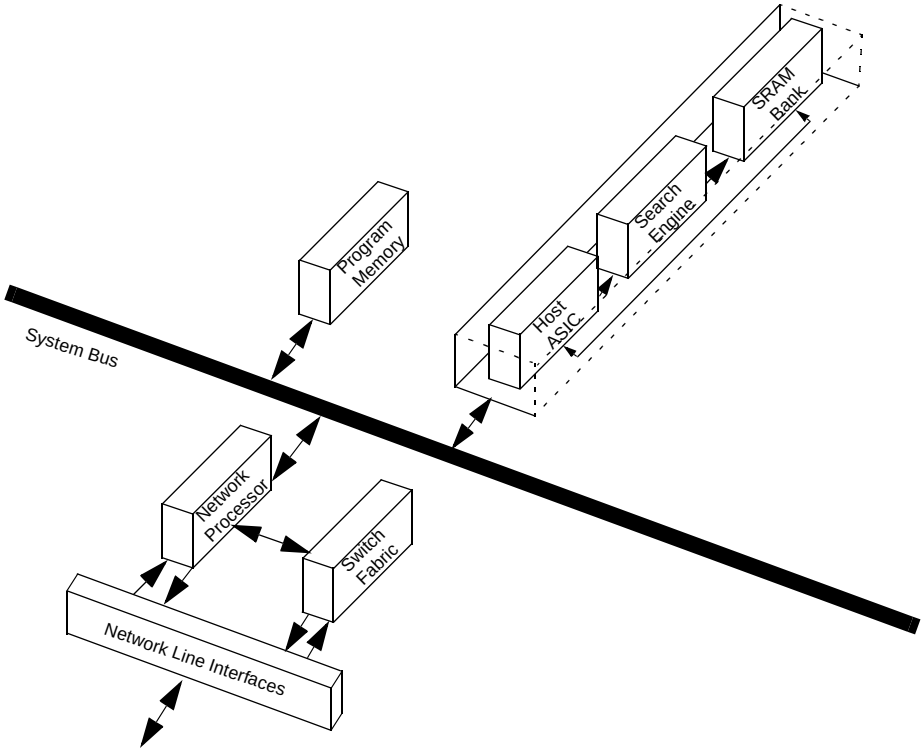


Figure 14-1. Sample Switch/Router Using the CYNSE70064A Device

15.0 JTAG (1149.1) Testing

The CYNSE70064A supports the Test Access Port and Boundary Scan Architecture as specified in the IEEE JTAG standard number 1149.1. The pin interface to the chip consists of five signals with the standard definitions: TCK, TMS, TDI, TDO, and TRST_L. *Table 15-1* describes the operations that the test access port controller supports, and *Table 15-2* describes the TAP Device ID Register. ***Note***. To disable JTAG functionality, connect the TCK, TMS and TDI pins to V_{DDQ} through a pull-up, and TRST_L to ground through a pull-down.

Table 15-1. Supported Operations

Instruction	Type	Description
SAMPLE/PRELOAD	Mandatory	Sample/Preload. This operation loads the values of signals going to and from I/O pins into the boundary scan shift register to provide a snapshot of the normal functional operation, and to initialize boundary scan.
EXTEST	Mandatory	External Test. This operation uses boundary scan values shifted in from TAP to test connectivity external to the device.
BYPASS	Mandatory	This operation loads a single bit shift register between TDI and TDO and provides a minimum-length serial path when no test operation is required
IDCODE	Optional	This operation selects the Identification register between TDI and TDO and allows the “idcode” to be read serially through TDO.
CLAMP	Optional	This operation drives preset values onto the outputs of devices
HighZ	Optional	This operation leaves the device output pins in a high-impedance state.

Table 15-2. TAP Device ID Register

Field	Range	Initial Value	Description
Revision	[31:28]	0001	Revision Number. This is the current device revision number. Numbers start from 1 and increment by 1 for each revision of the device.
Part Number	[27:12]	0000 0000 0000 0001	This is the part number for the device.
MFID	[11:1]	000_1101_1100	Manufacturer ID. This field is the same as the manufacturer ID used in the TAP controller.
LSB	[0]	1	Least significant bit.

16.0 Electrical Specifications

This section describes the electrical specifications, capacitance, operating conditions, DC characteristics, and AC timing parameters for the CYNSE70064A, as shown in *Table 16-1* and *Table 16-2*.

Table 16-1. DC Electrical Characteristics for CYNSE70064A

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{DDQ} = V_{DDQ}$ Max., V_{IN} = 0 to V_{DDQ} Max.	–10	10	µA
I_{LO}	Output leakage current	$V_{DDQ} = V_{DDQ}$ Max., V_{IN} = 0 to V_{DDQ} Max.	–10	10	µA
V_{IL}	Input LOW voltage (V_{DDQ} = 3.3V)		–0.3	0.8	V
V_{IH}	Input HIGH voltage (V_{DDQ} = 3.3V)		2.0	V_{DDQ} + 0.3	V
V_{OL}	Output LOW voltage (V_{DDQ} = 3.3V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH voltage (V_{DDQ} = 3.3V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OH} = 8 mA	2.4		V
V_{IL}	Input LOW voltage (V_{DDQ} = 2.5V)		–0.3	0.7	V
V_{IH}	Input HIGH voltage (V_{DDQ} = 2.5V)		1.7	V_{DDQ} + 0.3	V
V_{OL}	Output LOW voltage (V_{DDQ} = 2.5V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH voltage (V_{DDQ} = 2.5V)	$V_{DDQ} = V_{DDQ}$ Min., I_{OH} = 8 mA	2.0		V
I_{DD2}	3.3V supply current at V_{DD} Max.	83-MHz Search rate, I_{OUT} = 0 mA		270	mA
I_{DD2}	3.3V supply current at V_{DD} Max.	66-MHz Search rate, I_{OUT} = 0 mA		200	mA
I_{DD2}	3.3V supply current at V_{DD} Max.	50-MHz Search rate, I_{OUT} = 0 mA		150	mA
I_{DD2}	2.5V supply current at V_{DD} Max.	83-MHz Search rate, I_{OUT} = 0 mA		220	mA
I_{DD2}	2.5V supply current at V_{DD} Max.	66-MHz Search rate, I_{OUT} = 0 mA		160	mA
I_{DD2}	2.5V supply current at V_{DD} Max.	50-MHz Search rate, I_{OUT} = 0 mA		120	mA
I_{DDI}	1.8V supply current at V_{DD} Max.	83-MHz Search rate		3000	mA
I_{DDI}	1.8V supply current at V_{DD} Max.	66-MHz Search rate		2300	mA
I_{DDI}	1.8V supply current at V_{DD} Max.	50-MHz Search rate		1800	mA

Parameter	Description	Max	Unit
C_{IN}	Input capacitance	6	pF[7]
C_{OUT}	Output capacitance	6	pF[8]

Table 16-2. Operating Conditions for CYNSE70064A

Parameter	Description	Min (3.3V)	Max (3.3V)	Min (2.5V)	Max (2.5V)	Unit
V_{DDQ}	Operating voltage for IO	3.135	3.465	2.4	2.6	V
V_{DD}	Operating supply voltage	1.7	1.9	1.7	1.9	V
V_{IH}	Input HIGH voltage[9]	2.0	V_{DDQ} + 0.3	1.7	V_{DDQ} + 0.3	V
V_{IL}	Input LOW voltage[10]	–0.3	0.8	–0.3	0.7	V
t_A	Ambient operating temperature	0	70	0	70	°C
	Supply voltage tolerance	–5%	+5%	–5%	+5%	

Notes:
7. f = 1 MHz, V_{IN} = 0V.
8. f = 1 MHz, V_{OUT} = 0V.
9. Maximum allowable applies to overshoot only (V_{DDQ} is 2.5V supply).
10. Minimum allowable applies to undershoot only.

17.0 AC Timing Waveforms

Table 17-1 shows the AC timing parameters for the CYNSE70064A device; *Table 17-2* shows the same parameters but for 2.5V.

Table 17-1. AC Timing Parameters with CLK2X

Parameter	Description	CYNSE70064A-50		CYNSE70064A-66		CYNSE70064A-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	CLK2X frequency		100		133		166	MHz
t_{CLK}	CLK2X period	10		7.5		6.0		ns
t_{CKHI}	CLK2X HIGH pulse[11]	4.0		3.0		2.4		ns
t_{CKLO}	CLK2X LOW pulse[11]	4.0		3.0		2.4		ns
t_{ISCH}	Input set-up time to CLK2X rising edge[11]	2.5		2.5		1.8		ns
t_{IHCH}	Input hold time to CLK2X rising edge[11]	0.6		0.6		0.6		ns
t_{ICSCH}	Cascaded input set-up time to CLK2X rising edge[11]	4.2		4.2		3.5		ns
t_{ICHCH}	Cascaded input hold time to CLK2X rising edge[11]	0.6		0.6		0.6		ns
t_{CKHOV}	Rising edge of CLK2X to LHO, FULO, BHO, FULL valid[12]		9.5		8.5		7.0	ns
t_{CKHDV}	Rising edge of CLK2X to DQ valid[12]		10.0		9.0		7.5	ns
t_{CKHDZ}	Rising edge of CLK2X to DQ High-Z[13]	1.2	9.5	1.2	8.5	1.2	7.0	ns
t_{CKHSV}	Rising edge of CLK2X to SRAM bus valid[12]		10.0		9.0		7.5	ns
t_{CKHSHZ}	Rising edge of CLK2X to SRAM bus High-Z[13]		7.0		6.5		6.0	ns
t_{CKHSLZ}	Rising edge of CLK2X to SRAM bus LOW-Z[13]	7.5		7.0		6.5		ns

Table 17-2. 2.5V AC Table for Test Condition of CYNSE70064A

Conditions	Results
Input pulse levels (V_{DDQ} = 3.3V)	GND to 3.0V
Input pulse levels (V_{DDQ} = 2.5V)	GND to 2.5V
Input rise and fall times measured at 0.3V and 2.7V (V_{DDQ} = 3.3V)	≤ 2 ns see (*Figure 17-1*)
Input rise and fall times measured at 0.25V and 2.25V (V_{DDQ} = 2.5V)	≤ 2 ns see (*Figure 17-1*)
Input timing reference levels (V_{DDQ} = 3.3V)	1.5V
Input timing reference levels (V_{DDQ} = 2.5V)	1.25V
Output reference levels (V_{DDQ} = 3.3V)	1.5V
Output reference levels (V_{DDQ} = 2.5V)	1.25V
Output load	See *Figure 17-2* and *Figure 17-3*

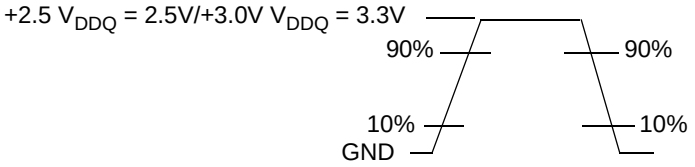


Figure 17-1. Input Waveform for CYNSE70064A

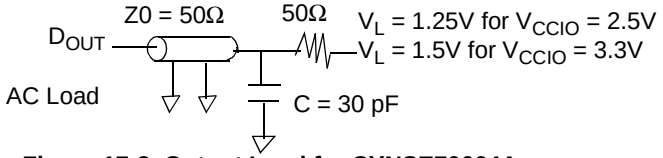


Figure 17-2. Output Load for CYNSE70064A

Notes:

11. Values are based on 50% signal levels.
12. Based on an AC load of C_L = 30 pF (see *Figure 17-1*, *Figure 17-2*, and *Figure 17-3*).
13. These parameters are sampled but not 100% tested, and are based on an AC load of 5 pF.

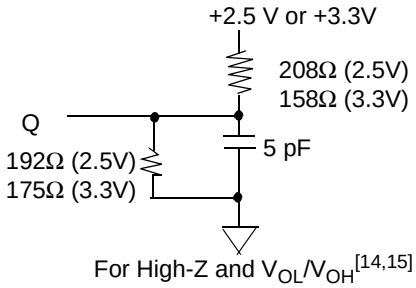
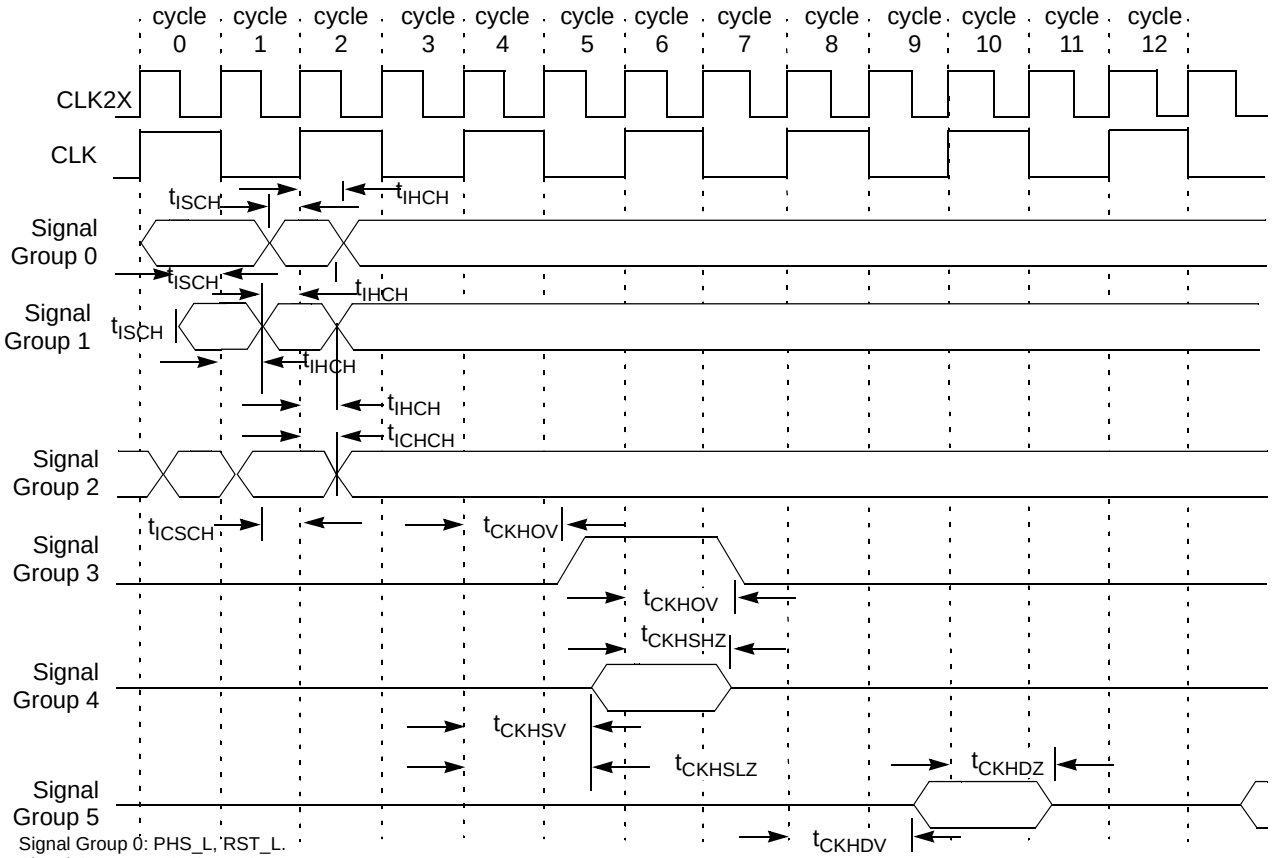


Figure 17-3. 2.5 I/O Output Load Equivalent for CYNSE70064A

Figure 17-4 shows timing waveform diagrams.



Signal Group 0: PHS_L, RST_L.
Signal Group 1: DQ, CMD, CMDV.
Signal Group 2: LHI, BHI, FULI.
Signal Group 3: LHO, BHO, FULO, FULL.
Signal Group 4: SADR, CE_L, OE_L, WE_L, ALE_L, SSF, SSV.
Signal Group 5: DQ, ACK, EOT.

Figure 17-4. AC Timing Wave Forms with CLK2X

Notes:
14. Output loading is specified with C_L = 5 pF as in *Figure 17-3*. Transition is measured at ± 200 mV from steady-state voltage.
15. The load used for V_{OH}, V_{OL} testing is shown in *Figure 17-3*.

18.0 Pinout Descriptions and Package Diagrams

In the following figure and table the CYNSE70064A device pinout diagram and pinout descriptions are shown.

	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	NC	GND	EOT	NC	NC	V_{DD}	FULI5	FULI4	FULI1	BHO0	V_{DD}	BHI0	LHI6	NC	V_{DD}	ID2	ID0	TDO	NC	NC	1
2	NC	NC	ACK	FULL	NC	FULO1	NC	FULI6	FULI2	BHO1	BHI2	V_{DDQ}	LHI5	LHI3	LHI2	ID3	TMS	TDI	V_{DD}	NC	2
3	DQ64	NC	NC	V_{DDQ}	V_{DD}	V_{DDQ}	NC	NC	V_{DDQ}	BHO2	V_{DD}	LHO1	LHI4	V_{DDQ}	LHIO	ID1	TCK	NC	NC	DQ65	3
4	DQ62	NC	V_{DD}	GND	RSTL	NC	FULO0	GND	FULI3	FULI0	BHI1	LHO0	GND	LHI1	ID4	TRST_L	GND	DQ63	DQ61	DQ57	4
5	DQ60	V_{DDQ}	NC	DQ66						TOP							DQ67	DQ59	NC	DQ53	5
6	V_{DD}	NC	DQ56	DQ58													V_{DDQ}	DQ55	DQ49	V_{DD}	6
7	DQ50	V_{DDQ}	DQ52	DQ54													DQ47	V_{DDQ}	DQ51	V_{DDQ}	7
8	NC	DQ46	DQ48	GND													GND	NC	DQ45	DQ43	8
9	DQ40	DQ42	V_{DDQ}	DQ44					GND	GND	GND	GND					DQ41	DQ39	V_{DD}	DQ37	9
10	V_{DD}	NC	DQ36	DQ38					GND	GND	GND	GND					V_{DDQ}	DQ35	DQ33	DQ31	10
11	V_{DDQ}	DQ34	DQ32	DQ30	LEFT				GND	GND	GND	GND				RIGHT	V_{DDQ}	NC	DQ29	V_{DD}	11
12	NC	DQ28	V_{DDQ}	DQ26					GND	GND	GND	GND					NC	DQ23	DQ25	DQ27	12
13	DQ24	V_{DD}	DQ20	GND													GND	DQ19	V_{DDQ}	DQ21	13
14	DQ22	DQ16	DQ14	V_{DDQ}													V_{DDQ}	NC	DQ15	DQ17	14
15	V_{DD}	DQ18	V_{DDQ}	DQ6													DQ9	DQ11	DQ13	V_{DD}	15
16	NC	DQ12	DQ8	DQ0						BOTTOM							DQ1	DQ5	DQ7	NC	16
17	DQ10	NC	V_{DDQ}	GND	NC	CMD4	CMD2	GND	WE_L	CLK2X	V_{DD}	SAD15	GND	V_{DDQ}	SAD5	V_{DDQ}	GND	**NC**	NC	V_{DDQ}	17
18	DQ2	DQ4	V_{DD}	SSF	CMD6	CMD3	CMD0	ALE_L	OE_L	SAD21	SAD18	SAD16	SAD12	SAD9	SAD7	SAD6	NC	SAD0	V_{DD}	DQ3	18
19	NC	NC	NC	SSV	CMD5	CMD1	CMDV	V_{DDQ}	PHS_L	V_{DDQ}	SAD19	V_{DDQ}	NC	SAD10	SAD11	NC	SAD4	SAD3	NC	NC	19
20	NC	NC	CMD8	CMD7	V_{DDQ}	V_{DD}	NC	CE_L	NC	V_{DD}	SAD20	SAD17	SAD14	SAD13	V_{DD}	SAD8	V_{DDQ}	SAD2	SAD1	NC	20
	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 18-1. Pinout Diagram

Table 18-1. Pinout Descriptions for Pinout Diagram

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
A1	NC		C4	DQ63	I/O
A2	NC		C5	DQ59	I/O
A3	DQ65	I/O	C6	DQ55	I/O
A4	DQ57	I/O	C7	VDDQ	3.3V/2.5V
A5	DQ53	I/O	C8	NC	
A6	VDD	1.8V	C9	DQ39	I/O
A7	VDDQ	3.3V/2.5V	C10	DQ35	I/O
A8	DQ43	I/O	C11	NC	
A9	DQ37	I/O	C12	DQ23	I/O
A10	DQ31	I/O	C13	DQ19	I/O
A11	VDD	1.8V	C14	NC	
A12	DQ27	I/O	C15	DQ11	I/O
A13	DQ21	I/O	C16	DQ5	I/O
A14	DQ17	I/O	C17	NC	
A15	VDD	1.8V	C18	SAD0	Output-T
A16	NC		C19	SAD3	Output-T
A17	VDDQ	3.3V/2.5V	C20	SAD2	Output-T
A18	DQ3	I/O	D1	ID0	Input
A19	NC		D2	TMS	Input
A20	NC		D3	TCK	Input
B1	NC		D4	GND	Ground
B2	VDD	1.8V	D5	DQ67	I/O
B3	NC		D6	VDDQ	3.3V/2.5V
B4	DQ61	I/O	D7	DQ47	I/O
B5	NC		D8	GND	Ground
B6	DQ49	I/O	D9	DQ41	I/O
B7	DQ51	I/O	D10	VDDQ	3.3V/2.5V
B8	DQ45	I/O	D11	VDDQ	3.3V/2.5V
B9	VDD	1.8V	D12	NC	
B10	DQ33	I/O	D13	GND	Ground
B11	DQ29	I/O	D14	VDDQ	3.3V/2.5V
B12	DQ25	I/O	D15	DQ9	I/O
B13	VDDQ	3.3V/2.5V	D16	DQ1	I/O
B14	DQ15	I/O	D17	GND	Ground
B15	DQ13	I/O	D18	NC	
B16	DQ7	I/O	D19	SAD4	Output-T
B17	NC		D20	VDDQ	3.3V/2.5V
B18	VDD	1.8V	E1	ID2	Input
B19	NC		E2	ID3	Input
B20	SAD1	Output-T	E3	ID1	Input
C1	TDO	Output-T	E4	TRST_L	Input
C2	TDI	Input	E17	VDDQ	3.3V/2.5V
C3	NC		E18	SAD6	Output-T

Table 18-1. Pinout Descriptions for Pinout Diagram (continued)

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
E19	NC		L2	BHO1	Output
E20	SAD8	Output-T	L3	BHO2	Output
F1	VDD	1.8V	L4	FULI0	Input
F2	LHI2	Input	L17	CLK2X	Input
F3	LHI0	Input	L18	SAD21	Output-T
F4	ID4	Input	L19	VDDQ	3.3V/2.5V
F17	SAD5	Output-T	L20	VDD	1.8V
F18	SAD7	Output-T	M1	FULI1	Input
F19	SAD11	Output-T	M2	FULI2	Input
F20	VDD	1.8V	M3	VDDQ	3.3V/2.5V
G1	NC		M4	FULI3	Input
G2	LHI3	Input	M17	WE_L	Output-T
G3	VDDQ	3.3V/2.5V	M18	OE_L	Output-T
G4	LHI1	Input	M19	PHS_L	Input
G17	VDDQ	3.3V/2.5V	M20	NC	
G18	SAD9	Output-T	N1	FULI4	Input
G19	SAD10	Output-T	N2	FULI6	Input
G20	SAD13	Output-T	N3	NC	
H1	LHI6	Input	N4	GND	Ground
H2	LHI5	Input	N17	GND	Ground
H3	LHI4	Input	N18	ALE_L	Output-T
H4	GND	Ground	N19	VDDQ	3.3V/2.5V
H17	GND	Ground	N20	CE_L	Output-T
H18	SAD12	Output-T	P1	FULI5	Input
H19	NC		P2	NC	
H20	SAD14	Output-T	P3	NC	
J1	BHI0	Input	P4	FULO0	Output
J2	VDDQ	3.3V/2.5V	P17	CMD2	Input
J3	LHO1	Output	P18	CMD0	Input
J4	LHO0	Output	P19	CMDV	Input
J17	SAD15	Output-T	P20	NC	
J18	SAD16	Output-T	R1	VDD	1.8V
J19	VDDQ	3.3V/2.5V	R2	FULO1	Output
J20	SAD17	Output-T	R3	VDDQ	3.3V/2.5V
K1	VDD	1.8V	R4	NC	
K2	BHI2	Input	R17	CMD4	Input
K3	VDD	1.8V	R18	CMD3	Input
K4	BHI1	Input	R19	CMD1	Input
K17	VDD	1.8V	R20	VDD	1.8V
K18	SAD18	Output-T	T1	NC	
K19	SAD19	Output-T	T2	NC	
K20	SAD20	Output-T	T3	VDD	1.8V
L1	BHO0	Output	T4	RSTL	Input

Table 18-1. Pinout Descriptions for Pinout Diagram (continued)

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
T17	NC		V20	CMD8	Input
T18	CMD6	Input	W1	GND	Ground
T19	CMD5	Input	W2	NC	
T20	VDDQ	3.3V/2.5V	W3	NC	
U1	NC		W4	NC	
U2	FULL	Output	W5	VDDQ	3.3V/2.5V
U3	VDDQ	3.3V/2.5V	W6	NC	
U4	GND	Ground	W7	VDDQ	3.3V/2.5V
U5	DQ66	I/O	W8	DQ46	I/O
U6	DQ58	I/O	W9	DQ42	I/O
U7	DQ54	I/O	W10	NC	
U8	GND	Ground	W11	DQ34	I/O
U9	DQ44	I/O	W12	DQ28	I/O
U10	DQ38	I/O	W13	VDD	1.8V
U11	DQ30	I/O	W14	DQ16	I/O
U12	DQ26	I/O	W15	DQ18	I/O
U13	GND	Ground	W16	DQ12	I/O
U14	VDDQ	3.3V/2.5V	W17	NC	
U15	DQ6	I/O	W18	DQ4	I/O
U16	DQ0	I/O	W19	NC	
U17	GND	Ground	W20	NC	
U18	SSF	Output-T	Y1	NC	
U19	SSV	Output-T	Y2	NC	
U20	CMD7	Input	Y3	DQ64	I/O
V1	EOT	Output-T	Y4	DQ62	I/O
V2	ACK	Output-T	Y5	DQ60	I/O
V3	NC		Y6	VDD	1.8V
V4	VDD	1.8V	Y7	DQ50	I/O
V5	NC		Y8	NC	
V6	DQ56	I/O	Y9	DQ40	I/O
V7	DQ52	I/O	Y10	VDD	1.8V
V8	DQ48	I/O	Y11	VDDQ	3.3V/2.5V
V9	VDDQ	3.3V/2.5V	Y12	NC	
V10	DQ36	I/O	Y13	DQ24	I/O
V11	DQ32	I/O	Y14	DQ22	I/O
V12	VDDQ	3.3V/2.5V	Y15	VDD	1.8V
V13	DQ20	I/O	Y16	NC	
V14	DQ14	I/O	Y17	DQ10	I/O
V15	VDDQ	3.3V/2.5V	Y18	DQ2	I/O
V16	DQ8	I/O	Y19	NC	
V17	VDDQ	3.3V/2.5V	Y20	NC	
V18	VDD	1.8V	J9	GND	Ground
V19	NC		J10	GND	Ground

Table 18-1. Pinout Descriptions for Pinout Diagram (continued)

Package Ball Number	Signal Name	Signal Type	Package Ball Number	Signal Name	Signal Type
J11	GND	Ground	L10	GND	Ground
J12	GND	Ground	L11	GND	Ground
K9	GND	Ground	L12	GND	Ground
K10	GND	Ground	M9	GND	Ground
K11	GND	Ground	M10	GND	Ground
K12	GND	Ground	M11	GND	Ground
L9	GND	Ground	M12	GND	Ground

19.0 Ordering Information

Table 19-1 provides ordering information.

Table 19-1. Ordering Information

Part Number	Description	Frequency	Temperature Range
CYNSE70064A-50BGC	Search engine	50 MHz	Commercial
CYNSE70064A-66BGC	Search engine	66 MHz	Commercial
CYNSE70064A-83BGC	Search engine	83 MHz	Commercial

20.0 Package Diagram

272-lead PBGA (27 x 27 x 2.33 mm) BG272

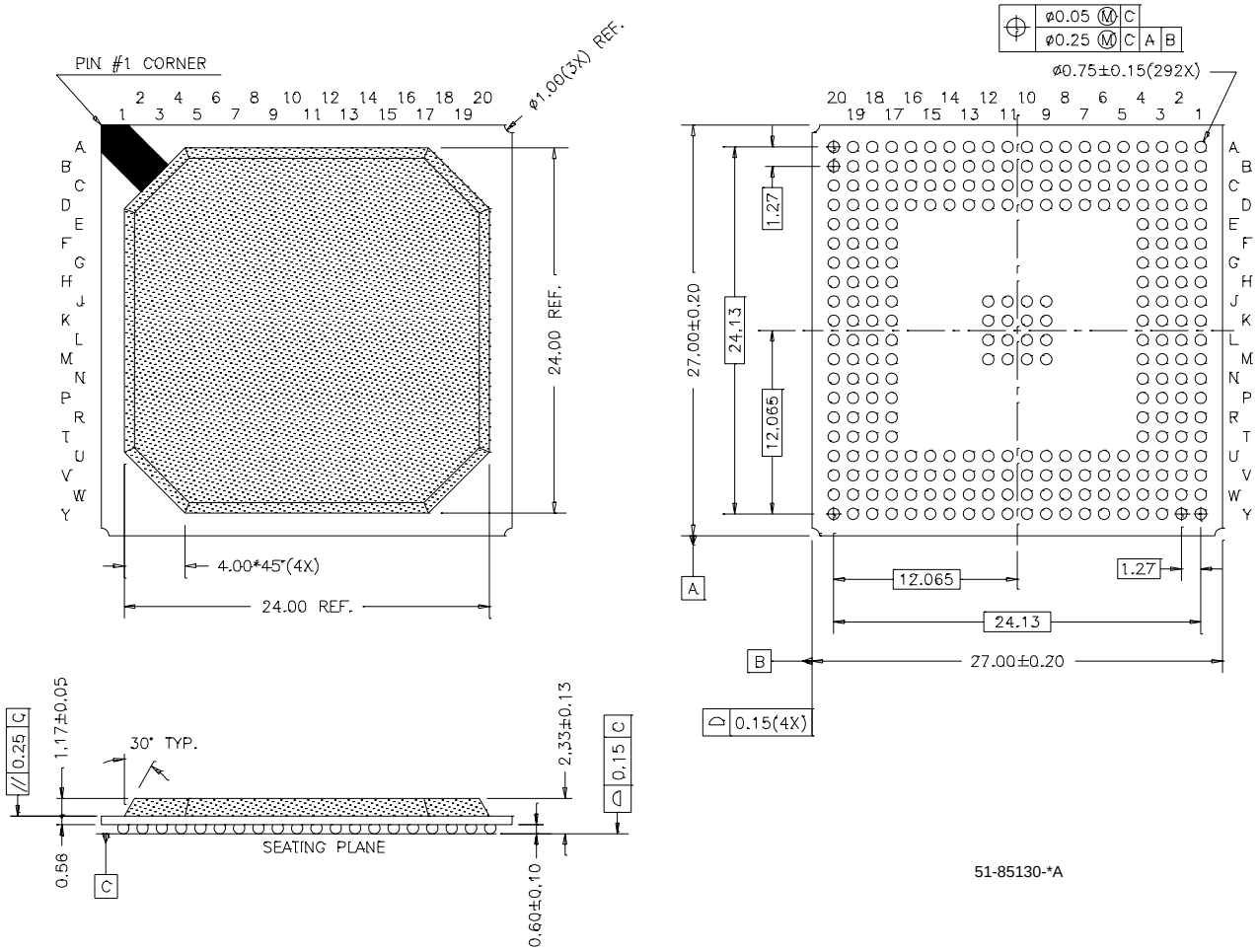


Figure 20-1. Package

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Document History Page

Document Title: CYNSE70064A Network Search Engine Document Number: 38-02041				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111438	02/21/02	AFX	New Data Sheet
*A	116610	07/10/02	OOR	Changed every CYNSE70064 to CYNSE70064A
*B	118153	09/19/02	OOR	Added Power section covering power-up sequence Updated JTAG section with the Supported Operations table
*C	119282	11/19/02	ED	Added 83-MSPS part information to Overview, DC Electrical Specifications, AC Timing Parameters Added note to Power-up Sequence Removed CYNSE70128/256-specific instructions Removed alternative method from power-up sequence instructions
*D	123686	02/20/03	KOS	Removed TEST from Signal Description *Table 5-1* Added Pin A10 to the pinout descriptions *Table 18-1* Added ”Output-T” in the Signal Type field of the Pin E18 *Table 18-1* Changed F1 Signal Name and Type from VDDQ to VDD and 3.3V/2.5V to 1.8V *Table 18-1* Added “1.8V” in the Signal Type field of Pin F20 *Table 18-1* Changed U6 Package Ball Number from U6I/O to U6 *Table 18-1* Reordered the pinouts list *Table 18-1*
*E	126020	05/08/03	ITL	Updated *Figure 13-1* on page 116 to reselect the correct waveforms. Corrected the power-up sequence description above the figure.