



# Quad Power Sequencing Controller

## Features

- ❑ Sequencing of Four or More\* Supplies, ICs, or Sub-systems
- ❑ Independently Programmable Delays Between Open Drain PWRGD Flags (5ms to 200ms)
- ❑ ±10V to ±90V Operation
- ❑ Tracking in Combination with Schottky Diodes
- ❑ Input Supervisors Including:
  - UV/OV Lock Out/Enable
  - Power-On-Reset (POR)
- ❑ Low Power Consumption, 0.4mA Supply Current
- ❑ Small SO-14 Package

\*By Daisy-Chaining PS10/11's

## Applications

- ❑ Power Supply Sequencing
- ❑ -48V Telecom and Networking Distributed Systems
- ❑ -24V Cellular and Fixed Wireless Systems
- ❑ -24V PBX Systems
- ❑ +48V Storage Systems
- ❑ FPGA, Microprocessor Tracking
- ❑ Industrial/Embedded System Timing/Sequencing
- ❑ High Voltage MEMs Driver's Supply Sequencing
- ❑ High Voltage Display Driver's Supply Sequencing

## Description

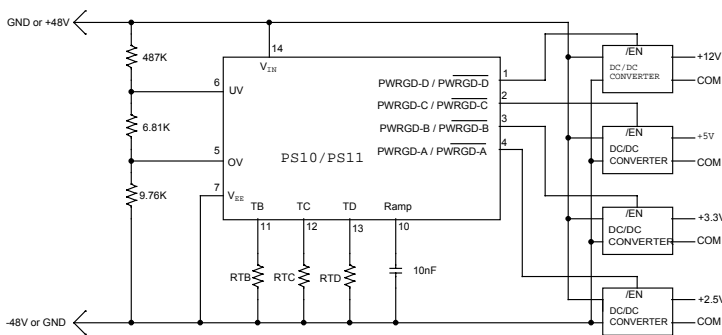
Many of today's high performance FPGA's, Microprocessors, DSP and industrial/embedded subsystems require sequencing of the input power. Historically this has been accomplished: i) discretely using comparators, references & RC circuits; ii) using expensive programmable controllers; or iii) with low voltage sequencers requiring resistor drop downs and several high voltage optocoupler or level shift components.

The PS10/11 saves board space, improves accuracy, eliminates optocouplers or level shifts and reduces overall component count by combining four timers, programmable input UV/OV supervisors, a programmable POR and four 90V open drain outputs. A high reliability, high voltage, junction isolated process allows the PS10/11 to be connected directly across the high voltage input rails.

The power-on-reset interval (POR) may be programmed by a capacitor on Cramp. To sequence additional systems, PS10/11 may be daisy chained together. If at any time the input supply falls outside the UV/OV detector range the PWRGD outputs will immediately become IN-ACTIVE. Down sequencing may be accomplished with additional components (see page 11).

The PS10/PS11 is available in a space saving SO-14 package.

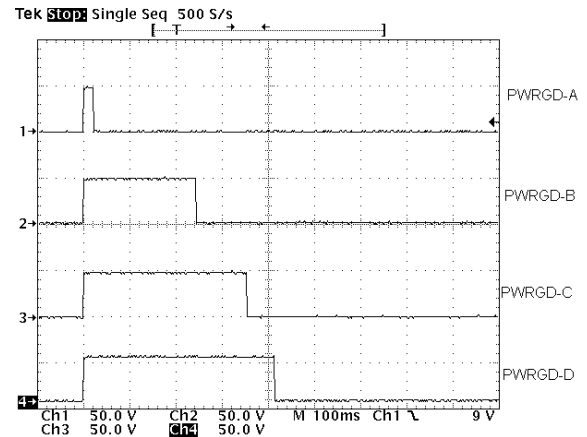
## Typical Application Circuit



- Notes:
1. Under Voltage Shutdown (UV) set to 37V.
  2. Over Voltage Shutdown (OV) to 57.8V.

## Waveform

(49.9k pull-up on PS11 PWRGD pins)



Relative to Negative Rail

## Absolute Maximum Ratings\*

$V_{EE}$ referenced to $V_{IN}$ pin	+0.3V to -100V
$V_{PWRGD}$ referenced to $V_{EE}$ voltage	-0.3V to +100V
$V_{UV}$ and $V_{OV}$ referenced to $V_{EE}$ Voltage	-0.3V to 12V
Operating Ambient Temperature	-40°C to +85°C
Operating Junction Temperature	-40°C to +125°C
Storage Temperature Range	-65° to +150°C
Power Dissipation @ 25°C, 14-Pin SOIC	750mW

\*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Ordering Information

Active State of Power Good Flags	Package Options
	14 Pin SOIC
High	PS10NG
Low	PS11NG

## Electrical Characteristics ( $-10V \leq V_{IN} \leq -90V$ , $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
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### Supply (Referenced to $V_{IN}$ pin)

$V_{EE}$	Supply Voltage	-90		-10	V	
$I_{EE}$	Supply Current		400	450	$\mu\text{A}$	$V_{EE} = -48\text{V}$

### OV and UV Control (Referenced to $V_{EE}$ pin)

$V_{UVH}$	UV High Threshold <sup>#</sup>	1.16	1.22	1.28	V	Low to High Transition
$V_{UVL}$	UV Low Threshold <sup>#</sup>	1.06	1.12	1.18	V	High to Low Transition
$V_{UVHY}$	UV Hysteresis <sup>#</sup>		100		mV	
$I_{UV}$	UV Input Current			1.0	nA	$V_{UV} = V_{EE} + 1.9\text{V}$
$V_{OVH}$	OV High Threshold <sup>#</sup>	1.16	1.22	1.28	V	Low to High Transition
$V_{OVL}$	OV Low Threshold <sup>#</sup>	1.06	1.12	1.18	V	High to Low Transition
$V_{OVHY}$	OV Hysteresis <sup>#</sup>		100		mV	
$I_{OV}$	OV Input Current			1.0	nA	$V_{UV} = V_{EE} + 1.9\text{V}$

<sup>#</sup>Specifications apply over  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$

### Power Good Timing (Test Conditions: $C_{RAMP} = 10\text{nF}$ , $V_{UV} = V_{EE} + 1.9\text{V}$ , $V_{OV} = V_{EE} + 0.5\text{V}$ )

$I_{RAMP}$	Ramp Pin Output Current		10		$\mu\text{A}$	
$t_{PWRGD-A}$	Time from UV High to PWRGD-A		8.8		ms	$V_{EE} = -48\text{V}$ , $C_{RAMP} = 10\text{nF}$ , see Typical Application Circuit
$t_{PWRGD-B}$	Maximum time from PWRGD-A to PWRGD-B	150	200*	250	ms	RTB = 120k $\Omega$
$t_{PWRGD-B}$	Minimum time from PWRGD-A to PWRGD-B	3.0	5.0*	8.0	ms	RTB = 3k $\Omega$
$t_{PWRGD-C}$	Maximum time from PWRGD-B to PWRGD-C	150	200*	250	ms	RTC = 120k $\Omega$
$t_{PWRGD-C}$	Minimum time from PWRGD-B to PWRGD-C	3.0	5.0*	8.0	ms	RTC = 3k $\Omega$
$t_{PWRGD-D}$	Maximum time from PWRGD-C to PWRGD-D	150	200*	250	ms	RTD = 120k $\Omega$
$t_{PWRGD-D}$	Minimum time from PWRGD-C to PWRGD-D	3.0	5.0*	8.0	ms	RTD = 3k $\Omega$

\*Note: Variations will track. For example if  $t_{PWRGD-A}$  is 250ms then so will be  $t_{PWRGD-B/C/D}$ . Contact factory for tighter tolerance version.

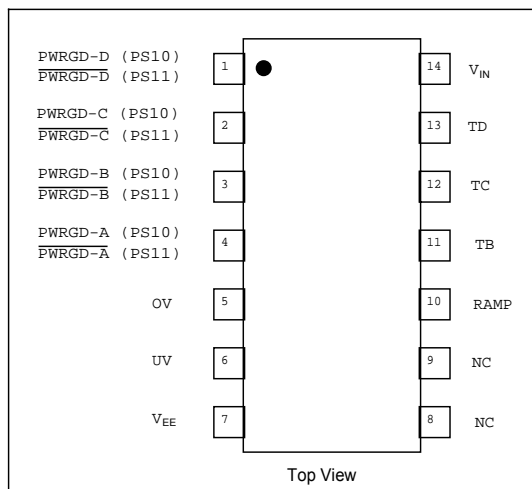
### Power Good Outputs (Test Conditions: $V_{UV} = V_{EE} + 1.9\text{V}$ , $V_{OV} = V_{EE} + 0.5\text{V}$ )

$V_{PWRGD-x(hi)}$	Power Good Pin Breakdown Voltage	90			V	PWRGD-x = HI Z
$V_{PWRGD-x(lo)}$	Power Good Pin Output Low Voltage		0.4	0.5	V	$I_{PWRGD} = 1\text{mA}$ , PWRGD-x = LOW
$I_{PWRGD-x(lk)}$	Maximum Leakage Current		<1.0	10	$\mu\text{A}$	$V_{PWRGD} = 90\text{V}$ , PWRGD-x = HI Z

## PWRGD Logic

Model	Condition	PWRGD-A/B/C/D	
PS10	INACTIVE (not ready)	0	$V_{EE}$
	ACTIVE (Ready)	1	HI Z
PS11	INACTIVE (not ready)	1	HI Z
	ACTIVE (Ready)	0	$V_{EE}$

## Pinout



## Pin Description

**PWRGD-D** – This open drain Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-C goes active.

**PWRGD-C** – This open drain Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-B goes active.

**PWRGD-B** – This open drain Power Good Output Pin is held inactive on initial power application and goes active a programmed time delay after PWRGD-A goes active.

**PWRGD-A** – This open drain Power Good Output Pin is held inactive on initial power application and goes active one POR delay after the UV pin goes above its High threshold (provided  $V_{IN}$  stays within the UV/OV window during this period).

To function as an indicator a pullup resistor must be connected from this pin to a voltage rail no more than 90V from  $V_{EE}$ .

**OV** – This Over Voltage (OV) sense pin, when raised above its high threshold will immediately cause the Power Good Outputs to be pulled low. These outputs will remain low until the voltage on this pin falls below the low threshold limit, initiating a new start-up cycle.

**UV** – This Under Voltage (UV) sense pin, when lowered below its low threshold will immediately cause the Power Good Outputs to be pulled low. These outputs will remain low until the voltage on this pin rises above the low threshold limit, initiating a new start-up cycle.

**$V_{EE}$**  – This pin is the negative terminal of the power supply input to the circuit.

**$V_{IN}$**  – This pin is the positive terminal of the power supply input to the circuit and can withstand 90V with respect to  $V_{EE}$ .

**TD** – The resistor connected from this pin to  $V_{EE}$  pin sets the time delay from PWRGD-C going active to PWRGD-D going active.

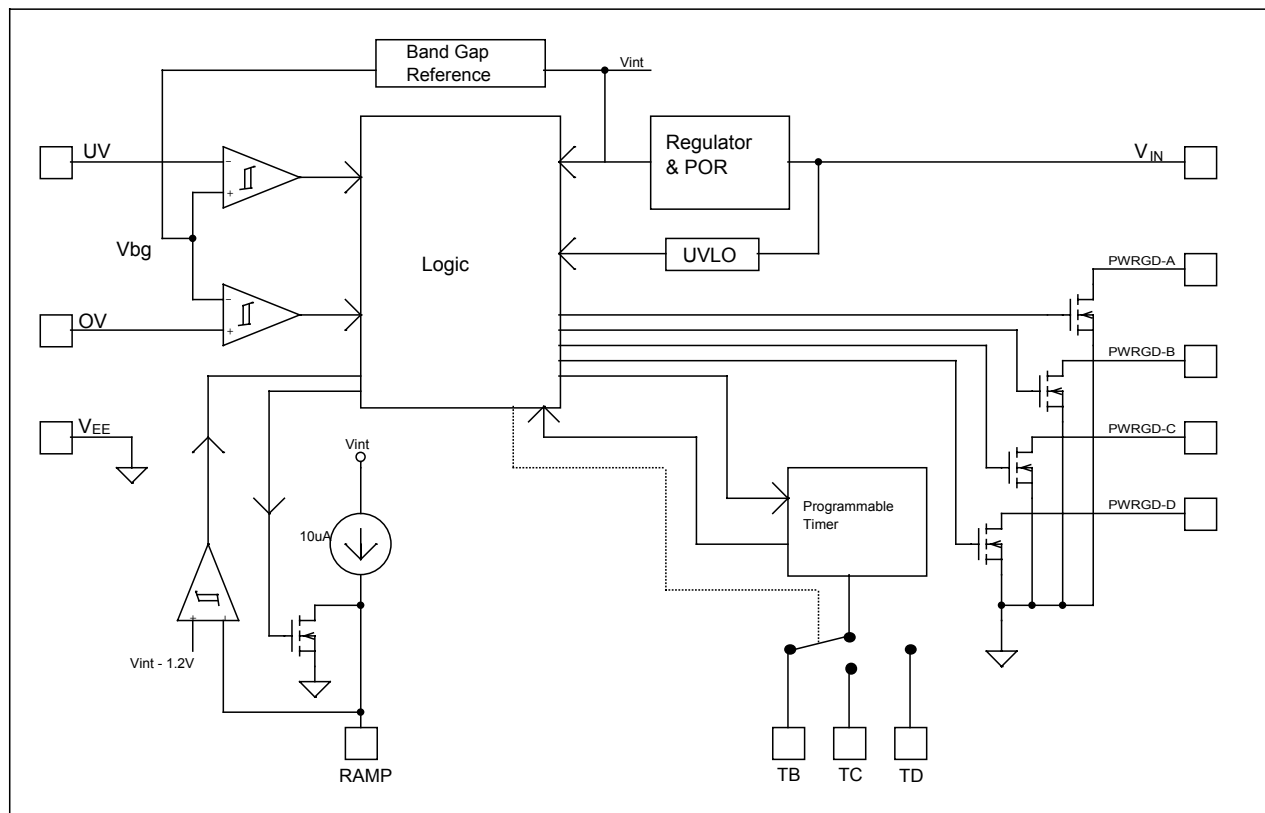
**TC** – The resistor connected from this pin to  $V_{EE}$  pin sets the time delay from PWRGD-B going active to PWRGD-C going active.

**TB** – The resistor connected from this pin to  $V_{EE}$  pin sets the time delay from PWRGD-A going active to PWRGD-B going active.

**RAMP** – This pin provides a current output so that a timing ramp is generated when a capacitor is connected. This timing Ramp is used to program POR and the time from satisfaction of the UV/OV supervisors to PWRGD-A.

**NC** – No Connect. This pin can be grounded or left floating.

## Functional Block Diagram



## Functional Description

The PS10/PS11 are designed to sequence up to 4 power supply modules, ICs or subsystems when the backplane voltage is within the programmed Under-voltage and Over-voltage limits. The power good open drain outputs are sequentially enabled starting from PWRGD-A to PWRGD-D. The time delay between power goods is programmable up to 200ms simply by changing the value(s) of RTB, RTC, and RTD. The initial time between satisfaction of the UV/OV supervisors & PWRGD-A can be programmed with Cramp.

### Description of Operation

During the initial power application, the Power Good pins are held low (rising with  $V_{IN}$ ) for PS10 and high for the PS11. Once the internal under voltage lock out has been satisfied, the circuit checks the input supply under voltage (UV) and over voltage (OV) sense circuits to ensure that the input voltage is within programmed limits. These limits are determined by the selected values for R1, R2, and R3, which form a voltage divider.

At the same time, a  $10\mu\text{A}$  current source is enabled, charging the external capacitor connected to the ramp pin. The rise time of the ramp pin is determined by the value of the capacitor ( $10\mu\text{A}/\text{Cramp}$ ). When the ramp voltage reaches 8.8V, the PWRGD-A pin will change into an active state. PWRGD-B will change into an active state after a programmed time delay from PWRGD-A inactive to active transition. PWRGD-C will change into an active state after a programmed time delay from PWRGD-B inactive to ac-

tive transition. PWRGD-D will change into an active state after a programmed time delay from PWRGD-C inactive to active transition.

The controller continuously monitors the UV and OV pins as long as the internal UVLO and POR circuits are satisfied. At any time during the start up cycle or thereafter, crossing the UV low and OV high limits will cause an immediate discharge on Cramp and reset on the power good pins. When the input voltage returns to a value within the programmed UV and OV limits, a new start up sequence will initiate immediately.

### Programming the Under and Over Voltage Limits

The UV and OV pins are connected to comparators with nominal 1.17V thresholds and 100mV of hysteresis ( $1.17\text{V} \pm 50\text{mV}$ ). They are used to detect under voltage and over voltage conditions at the input to the circuit. Whenever the OV pin rises above its high threshold (1.22V) or the UV pin falls below its low threshold (1.12V), the PWRGD outputs immediately deactivate.

Calculations can be based on either the desired input voltage operating limits or the input voltage shutdown limits. In the following equations the shutdown limits are assumed.

The undervoltage and overvoltage shut down thresholds can be programmed by means of the three resistor divider formed by R1, R2 and R3. Since the input currents on the UV and OV pins are negligible the resistor values may be calculated as follows:

$$UV_{OFF} = V_{UVL} = 1.12 = (V_{EEUV(off)}) \times (R2+R3)/(R1+R2+R3)$$

$$OV_{OFF} = V_{OVL} = 1.22 = (V_{EEOV(off)}) \times R3/(R1+R2+R3)$$

Where  $(V_{EEUV(off)})$  and  $(V_{EEOV(off)})$  relative to  $V_{EE}$  are Under and Over Voltage Shut Down Threshold points.

If we select a divider current of 100  $\mu$ A at a nominal operating input voltage of 50 Volts, then

$$R1+R2+R3 = 50V/100\mu A = 500k\Omega$$

From the second equation, for an OV shut down threshold of 65V, the value of R3 may be calculated.

$$OV_{OFF} = 1.22 = (65 \times R3)/500k$$

$$R3 = (1.22 \times 500k)/65 = 9.38k$$

The closest 1% value is 9.31k $\Omega$ .

From the first equation, for a UV shut down threshold of 35V, the value of R2 can be calculated.

$$UV_{OFF} = 1.12 = 35 \times (R2+R3)/500k$$

$$R2 = ((1.12 \times 500k)/35) - 9.76k = 6.69k$$

6.65k $\Omega$  is a standard 1% value

Then

$$R1 = 500k - R2 - R3 = 484.04k\Omega.$$

487k $\Omega$ , is a standard 1% value.

From the calculated resistor values the OV and UV start up threshold voltages can be calculated as follows:

$$UV_{ON} = V_{UVH} = 1.22 = (V_{EEUV(on)}) \times (R2+R3)/(R1+R2+R3)$$

$$OV_{ON} = V_{OVL} = 1.12 = (V_{EEOV(on)}) \times R3/(R1+R2+R3)$$

Where  $(V_{EEUV(on)})$  and  $(V_{EEOV(on)})$  are Under and Over Voltage Start Up Threshold points relative to  $V_{EE}$ .

Then

$$(V_{EEUV(on)}) = 1.22 \times (R1+R2+R3)/(R2+R3)$$

$$(V_{EEUV(on)}) = 1.22 \times (487k+6.65k+9.31k)/(6.65k+9.31k) = 38.45V$$

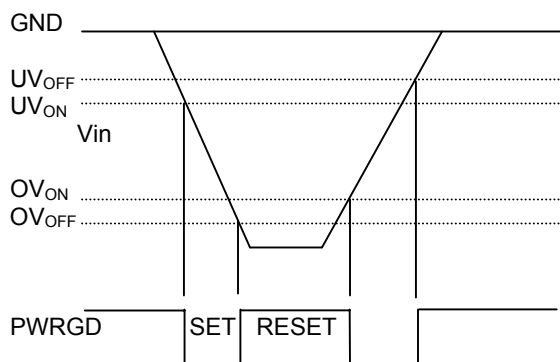
And

$$(V_{EEOV(on)}) = 1.12 \times (R1+R2+R3)/R3$$

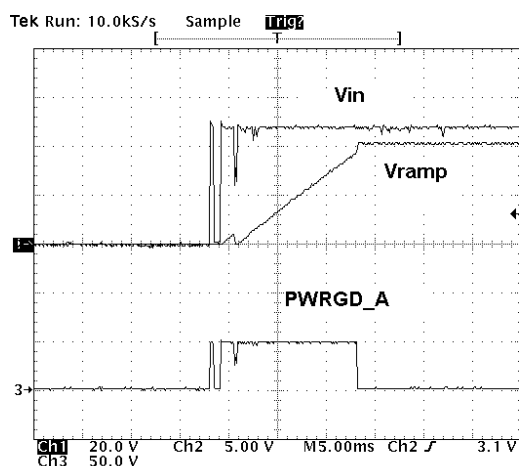
$$(V_{EEOV(on)}) = 1.12 \times (487k + 6.65k + 9.31k)/9.31k = 60.51V$$

Therefore, the circuit will start when the input supply voltage is in the range of 38.45V to 60.51V.

## Undervoltage/Overvoltage Operation



## Start-up Timing (PS11 PWRGD-A Active Low)



$t_{PWRGD-A}$  is the time delay from  $V_{EEUV(on)}$  to PWRGD-A going active. It can be approximated by

$$t_{PWRGD-A} = C_{RAMP} \times (V_{INT} - 1.17) / I_{RAMP}$$

where

$C_{RAMP}$  = capacitor connected from RAMP pin to  $V_{EE}$  pin

$V_{INT}$  = internal regulated power supply voltage (10V typ)

$I_{RAMP}$  = 10 $\mu$ A charge current

## PWRGD Flags Delay Programming

When the ramp voltage hits  $V_{int} - 1.17V$ , PWRGD-A becomes active indicating that the input supply voltage is within the programmed limits. PWRGD-B goes active after a programmed time delay after PWRGD-A went active. PWRGD-C goes active after a programmed time delay after PWRGD-B went active. PWRGD-D goes active after a programmed time delay after PWRGD-C went active.

The resistors connected from TB, TC, and TD to  $V_{EE}$  pin determines the delay times between the PWRGD flags.

The value of the resistors determines the capacitor charging and discharging current of a triangular wave oscillator. The oscillator output is fed into an 8-bit counter to generate the desired time delay.

The respective time delay is defined by the following equation:

$$t_{TX} = (255 \times 2 \times C_{OSC} \times V_{PP}) / I_{CD}$$

and

$$I_{CD} = V_{bg} / (4 \times R_{TX})$$

Where

$t_{TX}$  = Time delay between respective PWRGD flags  
 $C_{OSC}$  = 120pF (internal oscillator capacitor)  
 $V_{PP}$  = 8.2V (peak-to-peak voltage swing of oscillator)  
 $I_{CD}$  = Charge and discharge current of oscillator  
 $V_{bg}$  = 1.17V (internal band gap reference)  
 $R_{TX}$  = Programming resistor at TB, TC, or TD

Combining the two equations and solving for  $R_{TX}$  yields:

$$\begin{aligned} R_{TX} &= (V_{bg} \times t_{TX}) / (2040 \times C_{OSC} \times V_{PP}) \\ &= 0.585 \times 10^6 \times t_{TX} \end{aligned}$$

For a time delay of 200ms

$$R_{TX} = 0.585 \times 10^6 \times 0.2 = 117k$$

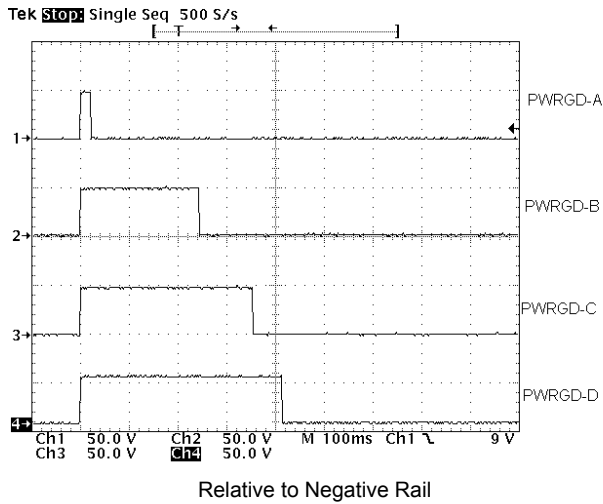
For a time delay of 5ms

$$R_{TX} = 0.585 \times 10^6 \times 0.005 = 2.925k$$

The following waveforms demonstrate the sequencing of the PWRGD flags:

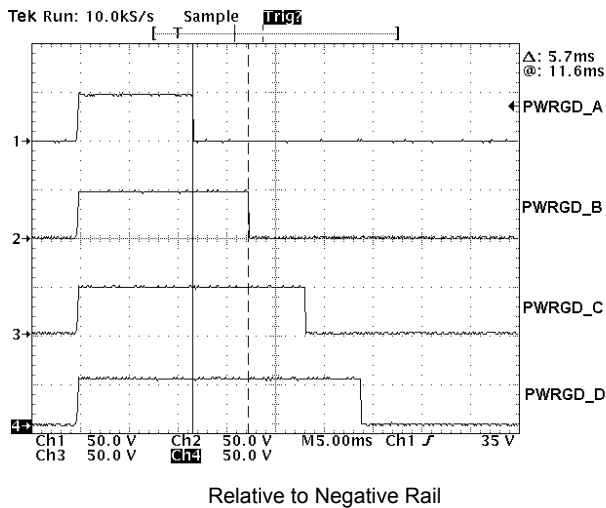
### PWRGD Timing (PS11)

Test conditions:  $V_{IN} = 48V$ ,  $C_{RAMP} = 10nF$ ,  $R_{TB} = 118k$ ,  $R_{TC} = 59k$ , and  $R_{TD} = 46.4k$ .



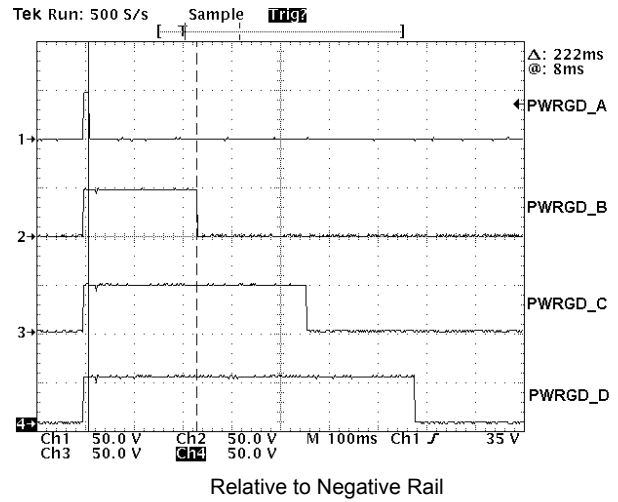
### PWRGD Timing (Minimum Delays)

Test conditions:  $V_{IN} = 48V$ ,  $C_{RAMP} = 10nF$ ,  $R_{TB} = 3.24k$ ,  $R_{TC} = 3.24k$ ,  $R_{TD} = 3.24k$ ,  $R_{PULL-UP} = 47k$ .



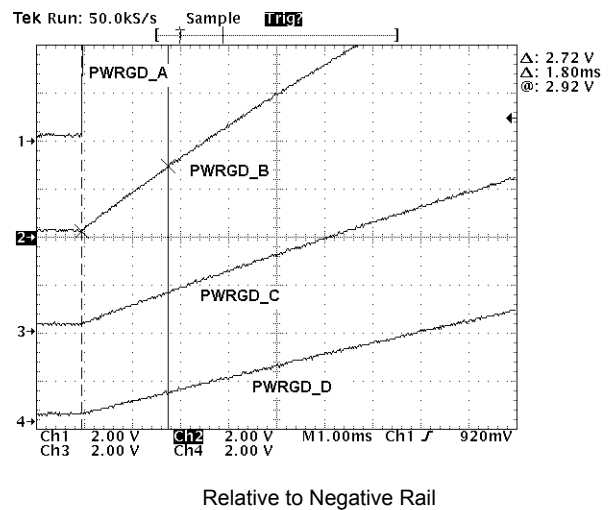
### PWRGD Timing (Maximum Delays)

Test conditions:  $V_{IN} = 48V$ ,  $C_{RAMP} = 10nF$ ,  $R_{TB} = 118k$ ,  $R_{TC} = 118k$ ,  $R_{TD} = 118k$ ,  $R_{PULL-UP} = 47k$ .



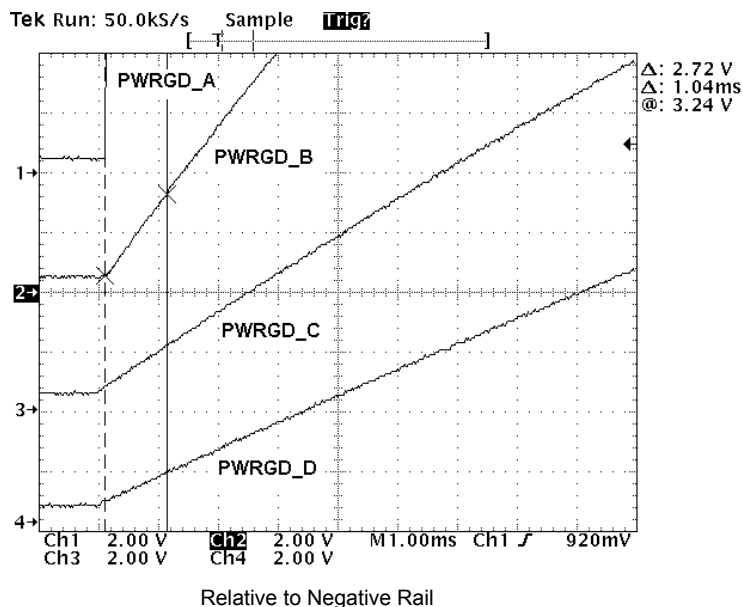
### PS11 Power Down Sequence after UV<sub>OFF</sub>

Test conditions:  $C_{RAMP} = 10nF$ ,  $R_{TB} = 3.24k$ ,  $R_{TC} = 3.24k$ ,  $R_{TD} = 3.24k$ ,  $R_{PULL-UP} = 47k$ ,  $C_{PWRGD\_B} = 0.47\mu F$ ,  $C_{PWRGD\_C} = 0.94\mu F$ ,  $C_{PWRGD\_D} = 1.41\mu F$ ,  $V_{UVOFF} = 33.4V$ , the assumed brick turn-off threshold is 2.7V min TTL logic high. See power down sequencing on Page 11.



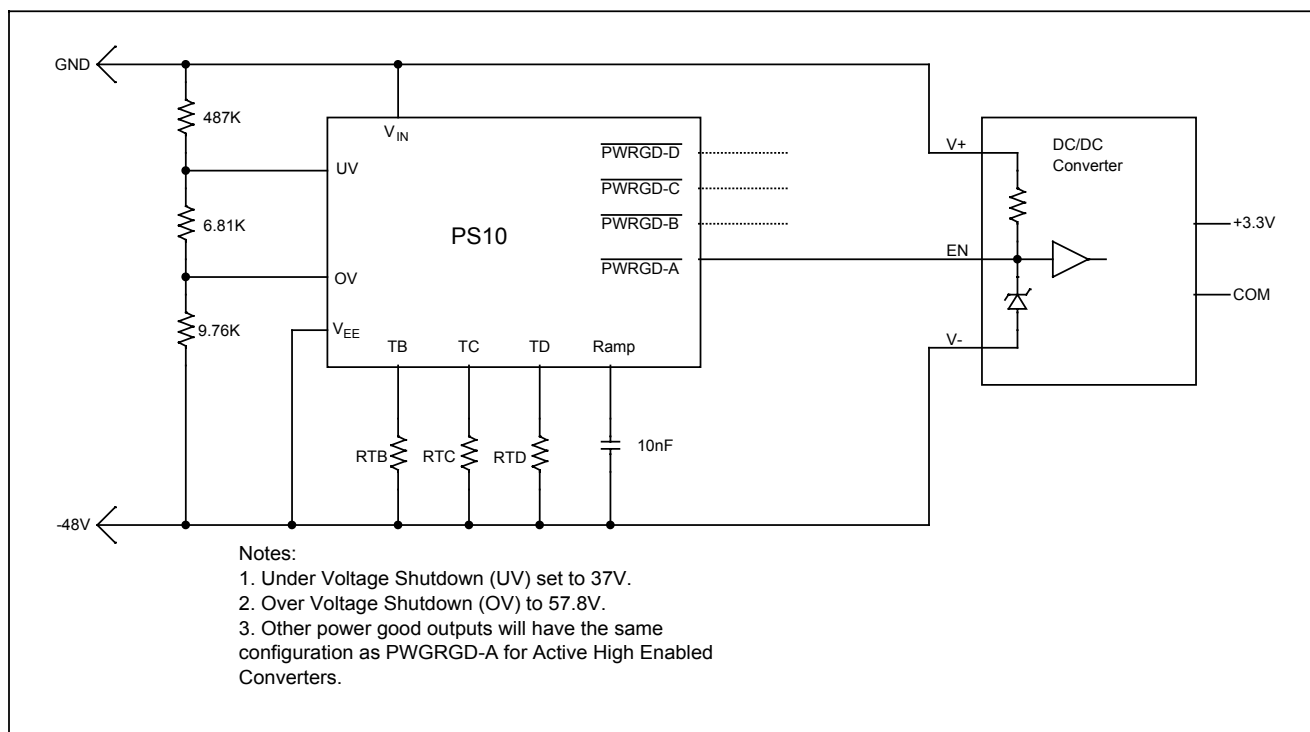
### PS11 Power Down Sequence after $OV_{OFF}$

Test conditions:  $C_{RAMP} = 10nF$ ,  $R_{TB} = 3.24k$ ,  $R_{TC} = 3.24k$ ,  $R_{TD} = 3.24k$ ,  $R_{PULL-UP} = 47k$ ,  $C_{PWRGD\_B} = 0.47\mu F$ ,  $C_{PWRGD\_C} = 0.94\mu F$ ,  $C_{PWRGD\_D} = 1.41\mu F$ ,  $V_{OV_{OFF}} = 61.6V$ , the assumed brick turn-off threshold is 2.7V min TTL logic high. See power down sequencing on Page 11.



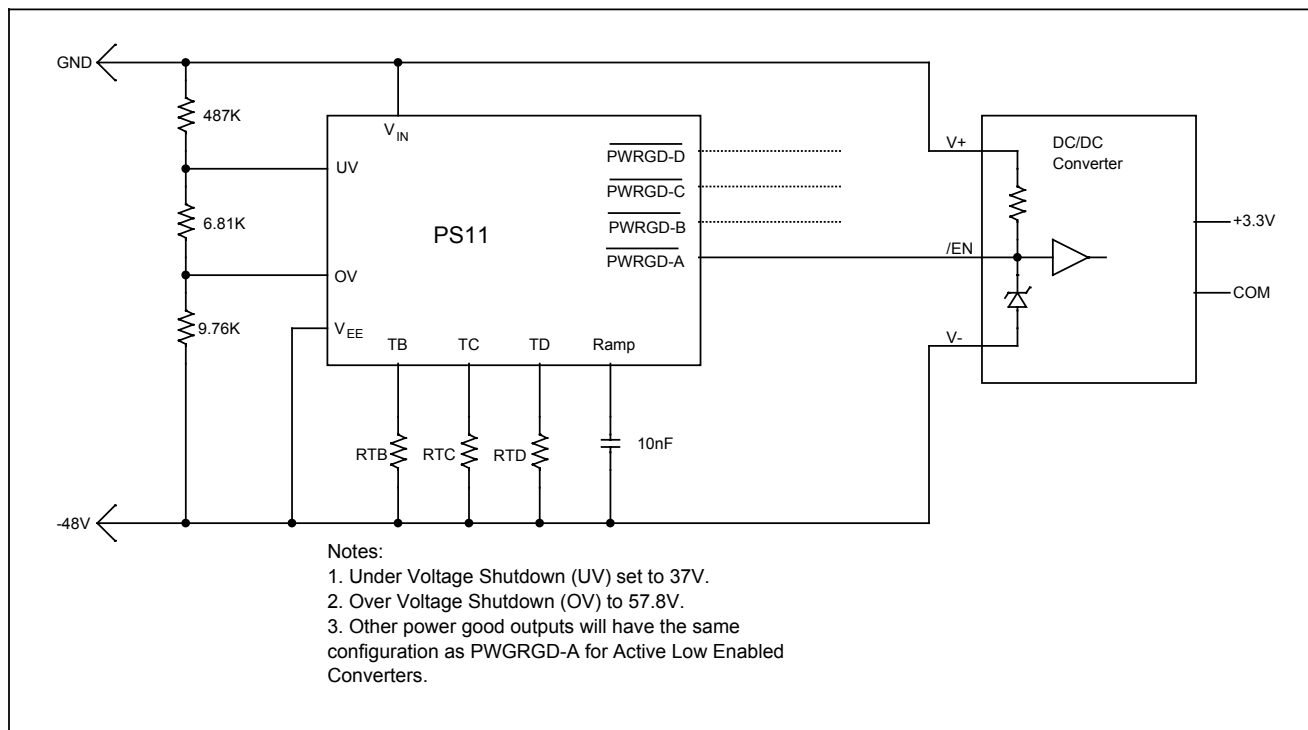
### PWRGD Output Configuration

The PS10 and PS11 open drain power good outputs can be connected directly to the Enable pins of the DC/DC converter. The internal pull-up and clamp of the DC/DC converter sets the logic High Enable/Disable voltage.



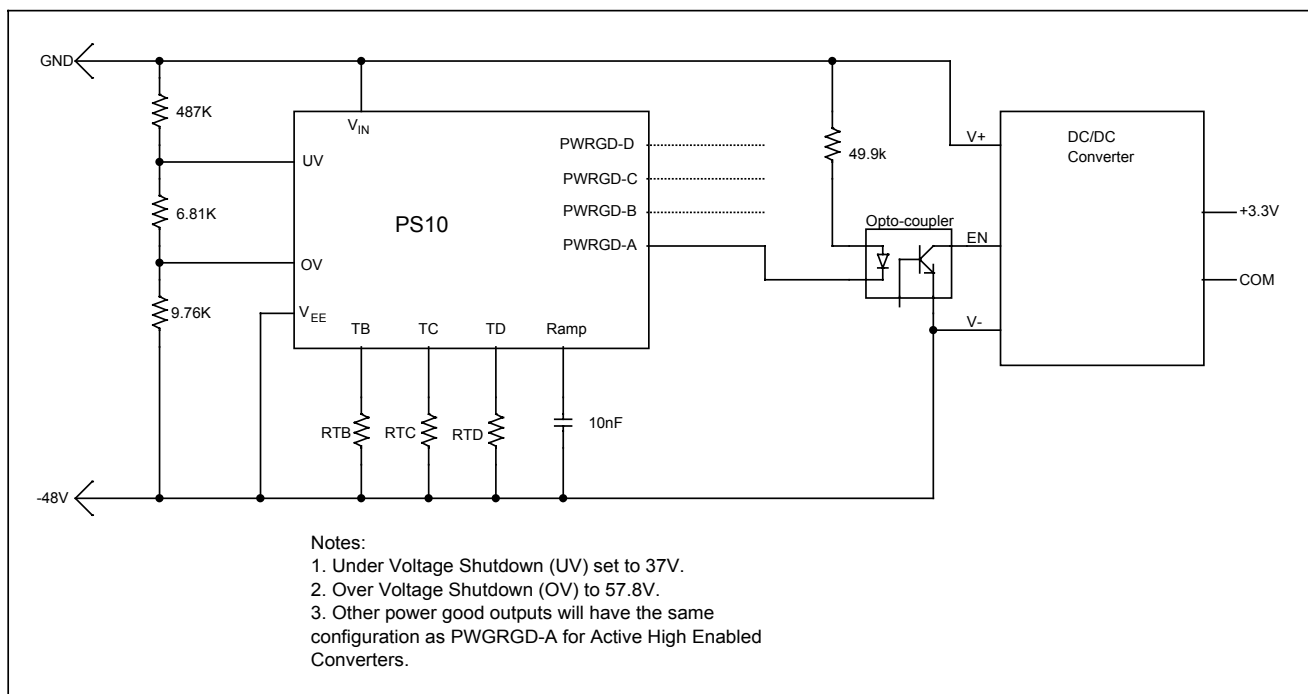


## PWRGD Output Configuration, *continued*

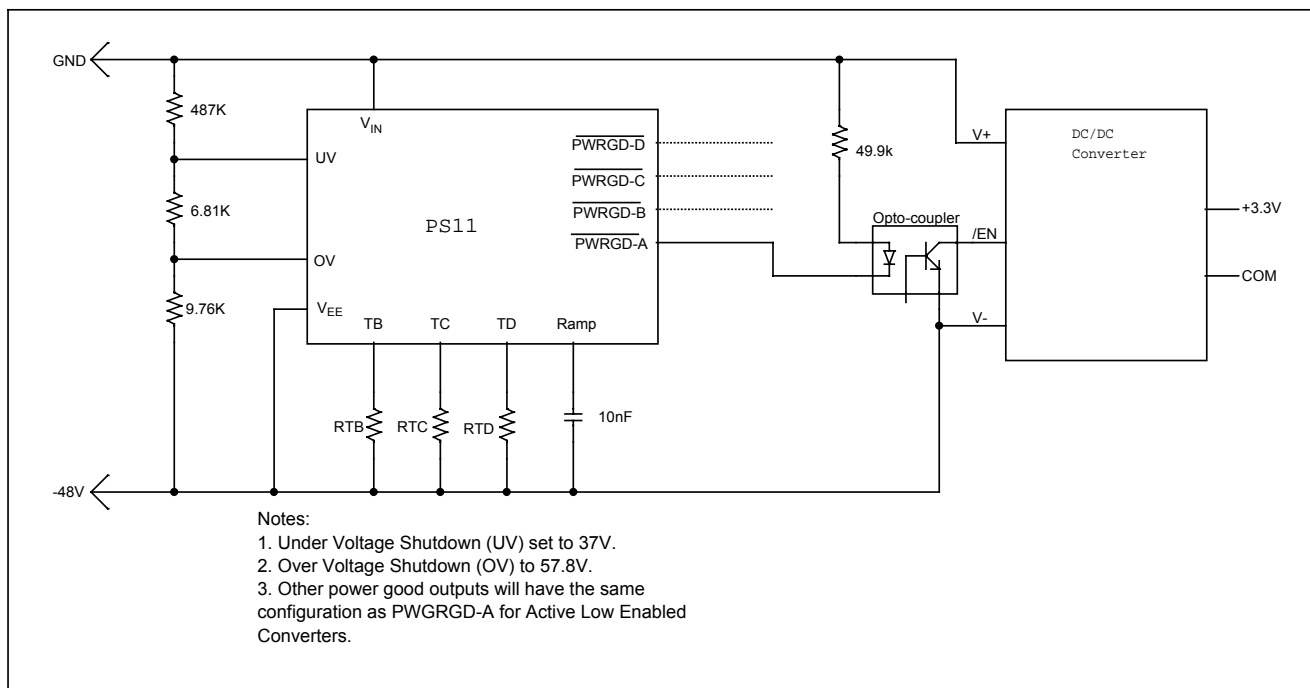


## Opto-isolated Enable

Some applications require opto-isolator interface to the Enable pin of the DC/DC converter. Make sure that the current transfer ratio of the opto-coupler selected is at least 100% to ensure proper pull-down current on the Enable pin.

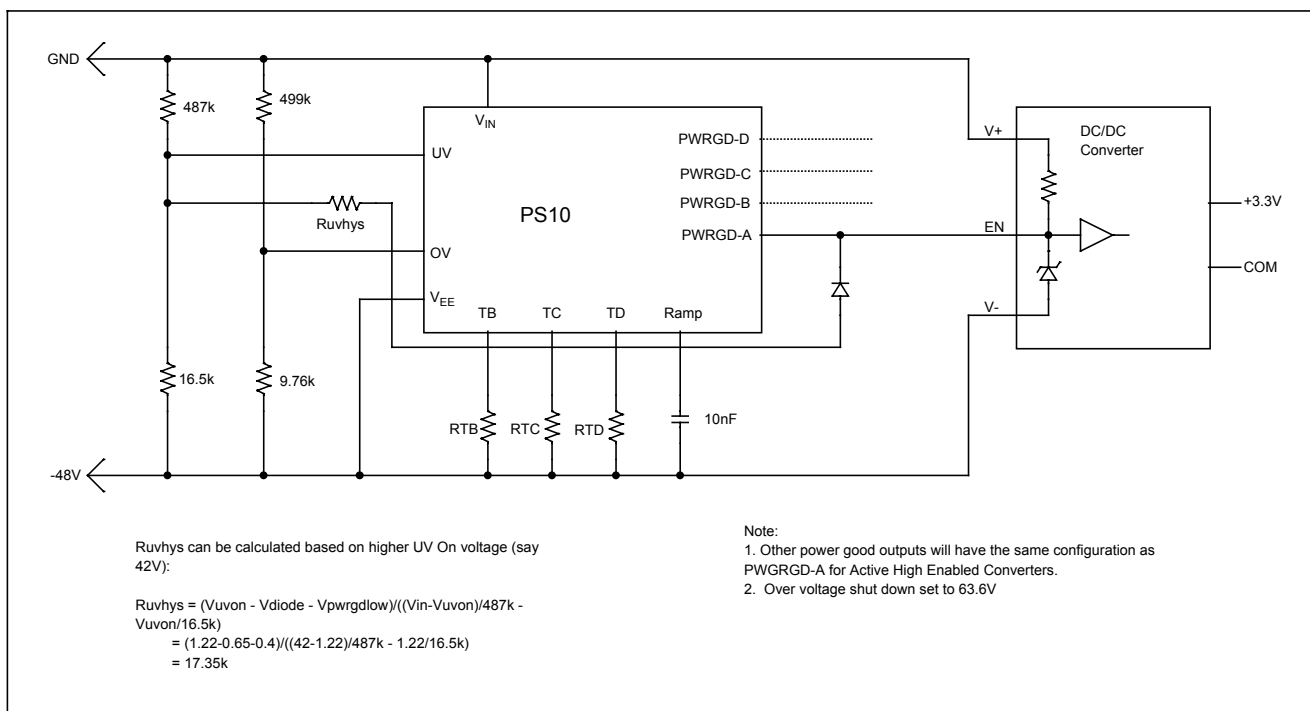


## Opto-isolated Enable, *continued*

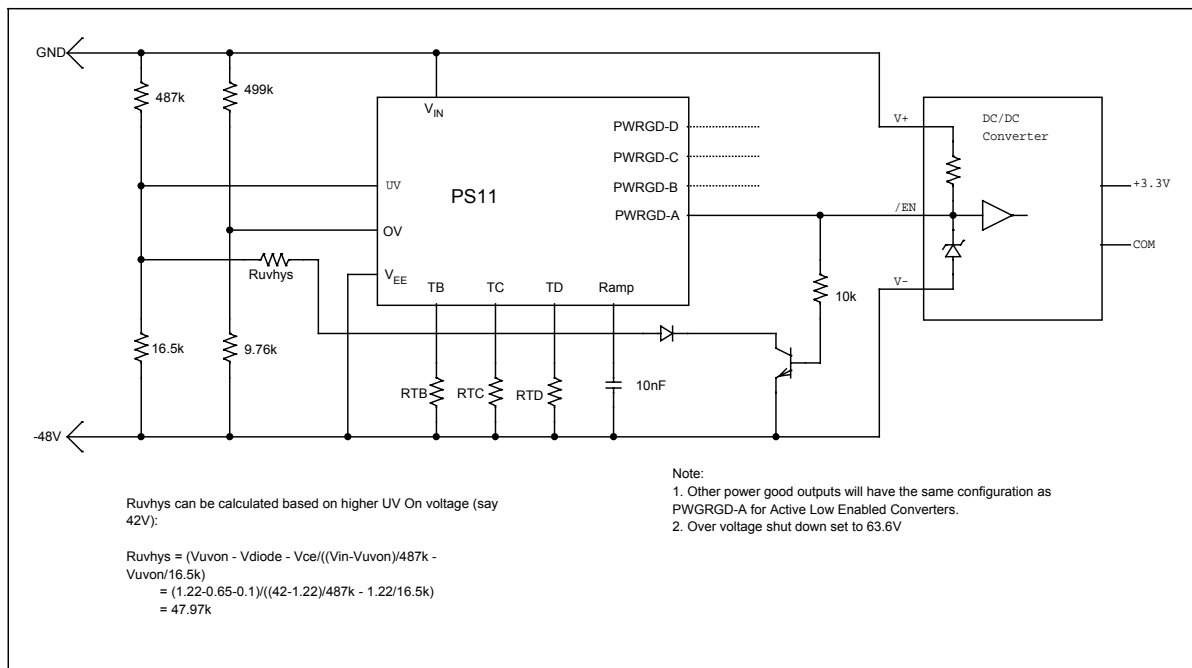


## Increasing the Under and Over Voltage Hysteresis

If the internal UV hysteresis is insufficient for a particular system application, then it may be increased by using separate resistor dividers for UV and OV and providing a resistor feedback from UV pin to the PWRGD pin.



## Increasing the Under and Over Voltage Hysteresis, *continued*



## Power Down Sequencing

In some applications, a power down sequence may be required. To accomplish this, a capacitor is connected to the power good pins that need to be sequenced down. The power good turn off delays can be approximated by

$$T_{PWRGD-B(off)} = C1 \times V_{ENOFF} / I_{PULLUP}$$

$$T_{PWRGD-C(off)} = C2 \times V_{ENOFF} / I_{PULLUP}$$

$$T_{PWRGD-D(off)} = C3 \times V_{ENOFF} / I_{PULLUP}$$

where:

$T_{PWRGD-B(off)}$  - Time delay from PWRGD-A going High to PWRGD-B going high.

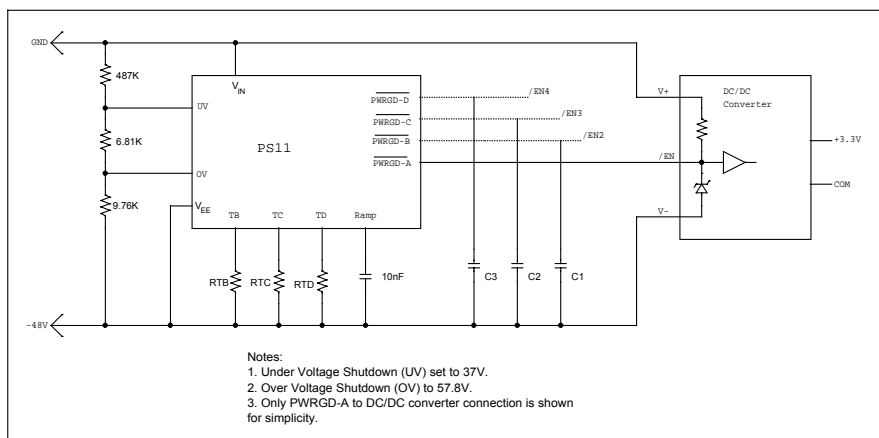
$T_{PWRGD-C(off)}$  - Time delay from PWRGD-A going High to PWRGD-C going high.

$T_{PWRGD-D(off)}$  - Time delay from PWRGD-A going High to PWRGD-D going high.

$V_{ENOFF}$  - DC/DC minimum off voltage (2.7V typ)

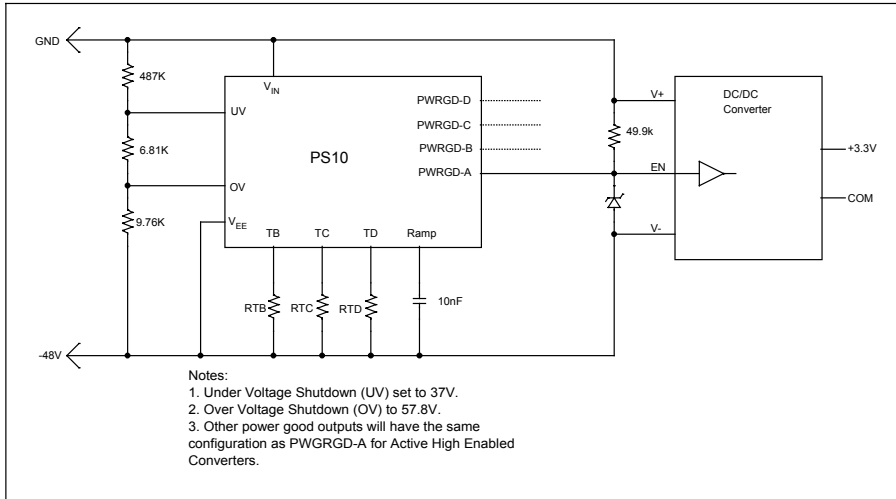
$I_{PULLUP}$  - DC/DC /EN pin pull-up current (1mA typ)

**Note:** Adding C1, C2, C3 will have a negligible affect on the power good fall time.



# PS10 Power Good Clamp

If the active high enabled dc/dc converter used does not have an internal clamp, an external zener diode may be used to protect the module.



## Typical Application Circuit for a 12V Non-Isolated System

Most FPGAs, Processors, ASICs, and DSPs require sequencing and rail voltage limitation during start-up and power down sequence of its rails. A typical requirement is:  $V_{DD\_CORE}$  must not exceed  $V_{DD\_IO}$  more than 0.6V and  $V_{DD\_IO}$  must not exceed  $V_{IN}$  at any time. This can be accomplished by sequencing the dc/dc converters by the following manner:

Turn On:  $V_{DD\_CORE}$  first,  $V_{DD\_IO}$  second, and  $V_{IN}$  last.

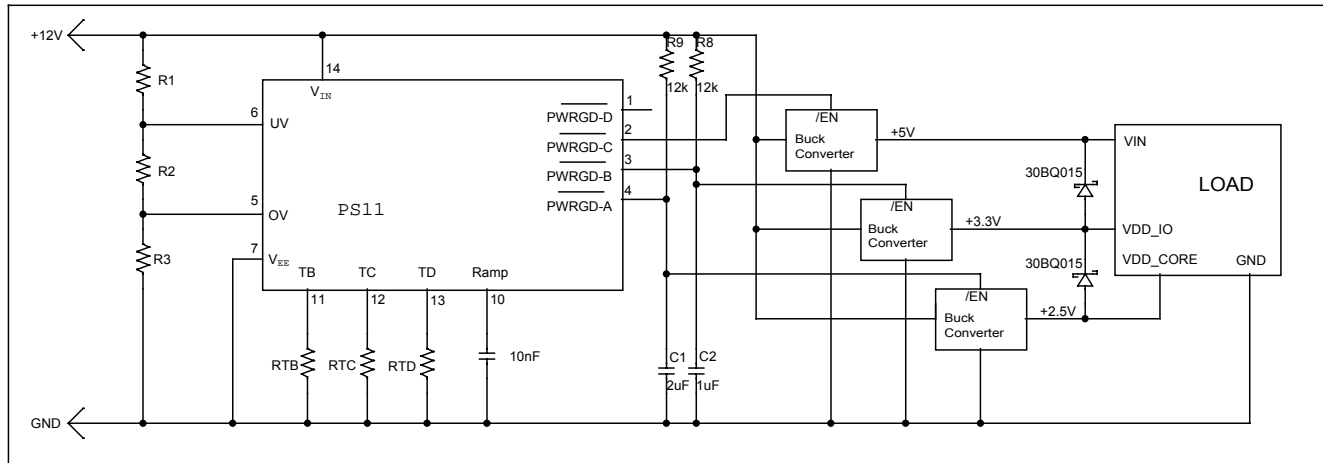
Tun-Off:  $V_{IN}$  first,  $V_{DD\_IO}$  second, and  $V_{DD\_CORE}$  last.

The Schottky diodes will limit the voltage between the rails to around 0.3V @ 3A during the power-up and power-down sequence.

Assuming that the /EN pins of the dc/dc converters have no pull-up and have a 1.0V turn-off threshold, the power-down sequence time delays can be approximated by:

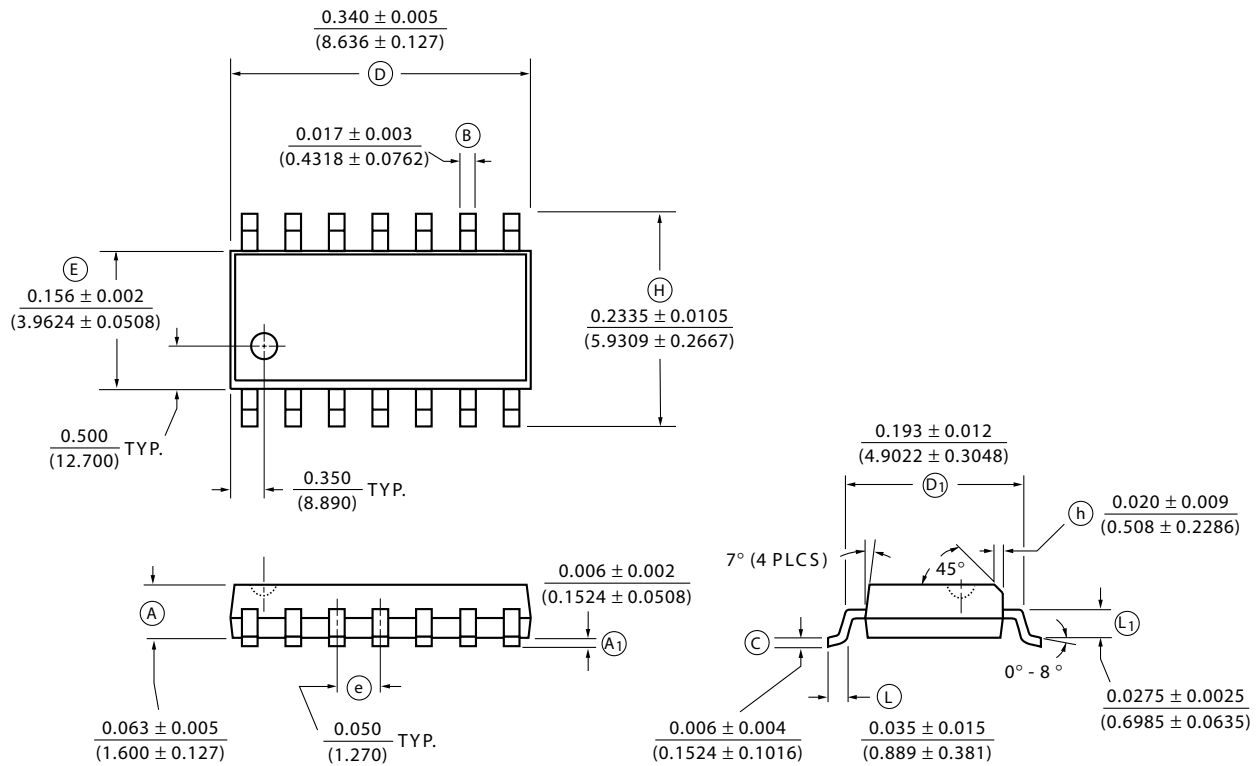
$$T_{PWRGD-C} \text{ to } T_{PWRGD-B} = 1\mu\text{F} \times 1\text{V} / 1\text{mA} = 1\text{ms}$$

$$T_{PWRGD-B} \text{ to } T_{PWRGD-A} = (2\mu\text{F}-1\mu\text{F}) \times 1\text{V} / 1\text{mA} = 1\text{ms}$$



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**14-LEAD SO PACKAGE (NG) (NARROW BODY)**



Note: Circle (e.g. (B)) indicates JEDEC Reference.

Measurement Legend =  $\frac{\text{Dimensions in Inches}}{\text{(Dimensions in Millimeters)}}$