7-Bit, 75 Ω, Digital Step Attenuator *5 to 3000 MHz*

General Description

This document describes the specification for the F1977 Digital Step Attenuator. The F1977 is part of a family of *Glitch-Free™* DSAs optimized for the demanding requirements of CATV and Satellite systems. These devices are offered in a compact 5 mm x 5 mm 32 pin QFN package with 75 Ω impedances for ease of integration.

COMPETITIVE ADVANTAGE

Digital step attenuators are used in Receivers and Transmitters to provide gain control. The F1977 is a 7-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss, low distortion (+64 dBm IIP3) and pinpoint attenuation accuracy. Most importantly, the F1977 includes IDT's *Glitch-Free™* technology which results in low overshoot & ringing during MSB transitions.

- ✓ Lowest insertion loss for best SNR
- ✓ Extremely accurate attenuation levels.
- ✓ Ultra low distortion.
- ✓ *Glitch-Free™* technology to protect PA or ADC during transitions between attenuation states.

APPLICATIONS

- CATV Infrastructure
- CATV Set-Top Boxes
- CATV Satellite Modems
- Data Network Equipment
- Fiber Networks

Ordering Information

F1977NBGI8

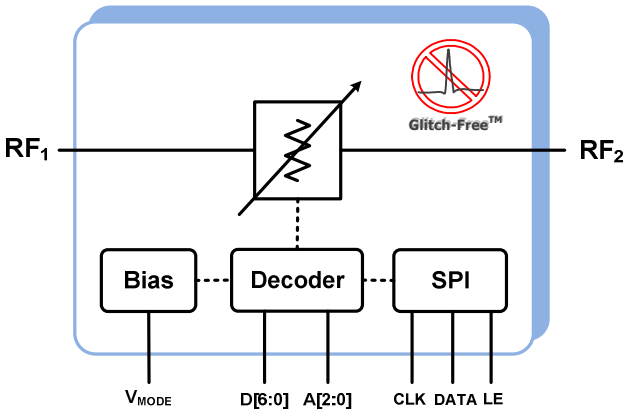
Tape & Reel

Green

Features

- Serial & 7 bit Parallel Interface
- 31.75 dB Control Range
- 0.25 dB step
- *Glitch-Free™* for low transient overshoot
- Low Insertion Loss: 1.4 dB @ 1 GHz
- Ultra linear IIP3: +64 dBm
- Attenuation Error: -0.1 dB @ 1 GHz
- Stable Attenuator Accuracy over temperature
- Bi-directional RF use
- 3.00 V to 5.25 V supply
- 1.8 V or 3.3 V control logic
- Low Current Consumption: 325 µA typical
- -40 °C to +105 °C operating temperature
- 5 mm x 5 mm Thin QFN 32 pin package

Functional Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
V_{DD} to GND	V_{DD}	-0.3	+5.5	V
D[6:0], DATA, CLK, LE, A0, A1, A2, V_{MODE}	V_{CNTL}	-0.3	Minimum (V_{DD} + 0.3, 3.9)	V
DC Voltage RF1, RF2	V_{RF}	-0.3	+0.3	V
Maximum Input Power applied to RF1 or RF2 (>100 MHz)	P_{RF}		+34	dBm
Maximum Junction Temperature	T_{Jmax}		+150	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10 s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		1000 (Class 1C)	V
ESD Voltage – CDM (Per JESD22-C101F)	V_{ESDCDM}		500 (Class C2)	V

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	40 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	4 °C/W
Moisture Sensitivity Rating (Per J-STD-02	MSL1

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F1977 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{DD}		3		5.25	V
Frequency Range	F_{RF}		5		3000	MHz
Operating Temperature Range	T_{CASE}	Exposed Paddle	-40		105	°C
RF CW Input Power	P_{CW}	RF1 or RF2			See Figure 1	dBm
RF1 Impedance	Z_{RF1}	Single Ended		75		Ω
RF2 Impedance	Z_{RF2}	Single Ended		75		Ω

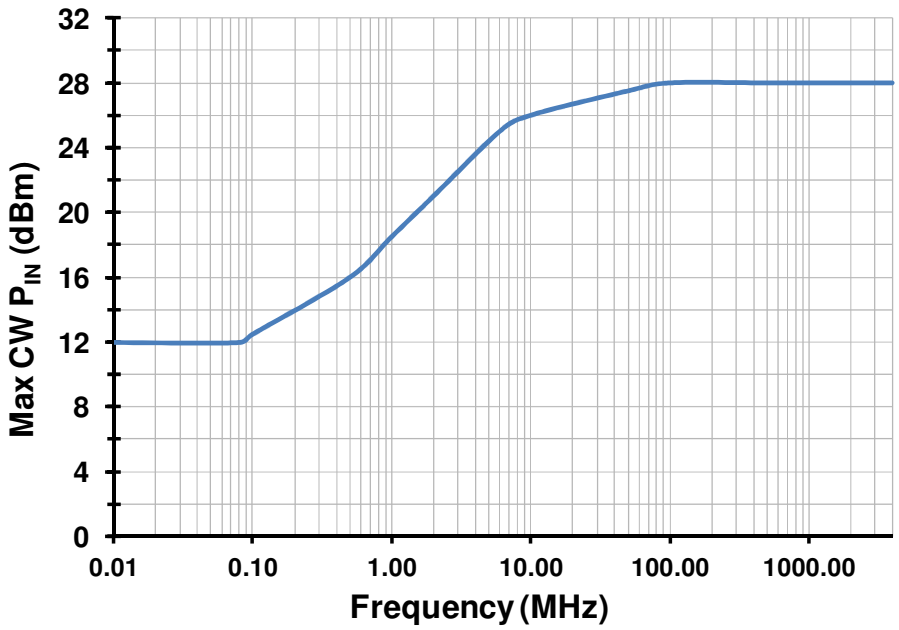

Figure 1 - Maximum Continuous Operating RF input power versus Input Frequency

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F1977 SPECIFICATION

Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25°C, F_{RF} = 1 GHz, Pin = -10 dBm unless otherwise noted. Serial Mode. $Z_{RF1} = Z_{RF2}$ = 75 Ω. EVkit losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High	V_{IH}	CLK, LE, DATA, D[6:0], A0, A1, A2, V_{MODE}				
		V_{DD} > 3.6 V	***1.17***[1]		***3.6***	V
		3.0 ≤ V_{DD} ≤ 3.6	1.17		V_{DD}	
Logic Input Low	V_{IL}	CLK, LE, DATA, D[6:0], A0, A1, A2, V_{MODE}			***0.63***	V
Logic Current	I_{IH}, I_{IL}	Individual Pins	***-40***		***+40***	µA
Supply Current	I_{DD}	V_{DD} = 3.3 V		322	***365***	µA
		V_{DD} = 5.0 V		375		
Attenuation Range	ATT_{RNG}			31.75		dB
Minimum Gain Step	LSB	Monotonic for F_{RF} ≤ 3 GHz		0.25		dB
Insertion Loss	IL	F_{RF} = 1 GHz		1.4	***1.9***	dB
		F_{RF} = 2 GHz to 3 GHz		2.2		
Relative Insertion Phase (A_{min} vs. A_{max})	Φ_{Δ}	F_{RF} = 1 GHz		18		deg
		F_{RF} = 2 GHz		36		
Step Error (Differential Non-Linearity)	DNL	Max error between adjacent steps		0.10		dB
Absolute Attenuation Error (Integral Non-Linearity)	INL	Max Error for state 19.75 dB, F_{RF} = 1 GHz	***-0.4***	0.1	***+0.5***	dB
		Max Error, over all states F_{RF} = 1 GHz	-0.8		+0.5	
Input Return Loss	S11	5 MHz ≤ F_{RF} ≤ 1.5 GHz		18		dB
		1.5 GHz < F_{RF} ≤ 3.0 GHz		15		
Output Return Loss	S22	5 MHz ≤ F_{RF} ≤ 1.5 GHz		17		dB
		1.5 GHz < F_{RF} ≤ 3.0 GHz		15		

Specification Notes:

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.

Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

Note 3. The input 0.1dB compression point is used as a linearity figure of merit. The recommended maximum input power is specified as the lesser of the two values from Figure 1 and Figure 2 above.

Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.

Note 5: Minimum time required between switching of attenuations states = 1 / (Maximum Switching Rate).

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Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25°C, F_{RF} = 1 GHz, Pin = -10 dBm unless otherwise noted. Serial Mode. $Z_{RF1} = Z_{RF2}$ = 75 Ω. EVkit losses are de-embedded unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input IP3	IIP3	P_{IN} = +10 dBm per tone 50 MHz Tone Separation				
		Attn State = 0.00 dB		64		dBm
		Attn State = 15.75 dB		64		
		Attn State = 31.75 dB		64		
Input 0.1dB Compression[3]	$P_{0.1dB}$	F_{RF} = 1 GHz Attn = 10 dB Measured in 50 ohms		32		dBm
DSA Settling Time	τ_{SET}	Max to Min Attenuation to settle to within 0.5 dB of final value		0.9		µs
		Min to Max Attenuation to settle to within 0.5 dB of final value		1.8		
Video Feedthrough RF1, RF2 ports	VID_{FT}	Measured at RF ports with 2.5 ns risetime, 0 to 3.3 V control pulse		10		mV_{pp}
Maximum spurious level on any RF port[4]	$Spur_{MAX}$	Spur Freq ~ 2.2 MHz		-119		dBm
Serial Clock Speed	F_{CLK}	SPI 3 wire bus			***25***	MHz
Parallel to Serial Setup	A	SPI 3 wire bus	***100***			ns
Serial Data Hold Time	B	SPI 3 wire bus	***10***			ns
LE Delay	C	SPI 3 wire bus Time from final serial clock rising edge	***10***			ns
Maximum Switching Rate[5]	SW_{RATE}			25		kHz

Specification Notes:
Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3. The input 0.1dB compression point is used as a linearity figure of merit. The recommended maximum input power is specified as the lesser of the two values from Figure 1 and Figure 2 above.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.
Note 5: Minimum time required between switching of attenuations states = 1 / (Maximum Switching Rate).

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PROGRAMMING OPTIONS

F1977 can be programmed using either the parallel or serial interface; selectable via V_{MODE} (pin 3). Serial mode is selected by floating V_{MODE} or pulling V_{MODE} to a logic high and parallel mode is selected by setting V_{MODE} to logic low.

SERIAL CONTROL MODE

F1977 Serial mode is selected by floating V_{MODE} (pin 3) or pulling it to logic high. The serial interface is a 16-bit shift register made up of two words. The first 8-bit word is the Attenuation word, which controls the DSA state. The second word is the address word, which uses only 3 of 8-bits that must match the hard wired A0-A2 programming in order to change the DSA state. If no external connections are made to A0 – A2 then internally they will default to 000 due to internal pull down resistors. If these 3 external preset address bits are not matched with the SPI loaded address bits then the current attenuator state will remain unchanged. This allows up to 8 serial-controlled devices to be used on a single board, which share a common DATA, CLK and LE.

When serial programming is used, all the parallel control input pins 26 – 32 can be left open or grounded. If a pin is grounded than an additional 25 µA will be drawn from the voltage supply per pin.

Set to either Logic High or Low Set to Logic Low

MSB (Last In) LSB (First In)

Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

8-Bit Address Word 8-Bit Attenuation Word

Figure 2 - Two 8-bit words are comprised of 16-bit serial in, parallel out shift register

Table 1 - Truth Table for the Serial Address Word

A7 (MSB)	A6	A5	A4	A3	A2	A1	A0	Address Setting
X	X	X	X	X	0	0	0	000
X	X	X	X	X	0	0	1	001
X	X	X	X	X	0	1	0	010
X	X	X	X	X	0	1	1	011
X	X	X	X	X	1	0	0	100
X	X	X	X	X	1	0	1	101
X	X	X	X	X	1	1	0	110
X	X	X	X	X	1	1	1	111

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Table 2 - Truth Table for the Serial Control Word

D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	Attenuation State (dB)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.25
0	0	0	0	0	0	1	0	0.5
0	0	0	0	0	1	0	0	1
0	0	0	0	1	0	0	0	2
0	0	0	1	0	0	0	0	4
0	0	1	0	0	0	0	0	8
0	1	0	0	0	0	0	0	16
0	1	1	1	1	1	1	1	31.75

SERIAL MODE DEFAULT CONDITION

When the device is first powered up it will default to the **Maximum Attenuation** setting as described below: Note that for the F1977 in all cases logic high (1) = Attenuation Stepped IN, while logic Low (0) = Attenuation Stepped OUT.

MSB (Last In) LSB (First In)

Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	0	0	0	0	1	1	1	1	1	1	1

8-Bit Address Word 8-Bit Attenuation Word

Figure 3 -Default register settings set for Max Attenuation and 000 Address Word

REGISTER TIMING DIAGRAM: (NOTE THE TIMING SPEC INTERVALS IN BLUE)

With serial control, the F1977 can be programmed via the serial port on the rising edge of Latch Enable (LE) which loads the last 8 DATA line bits [formatted LSB (D0) first] resident in the SHIFT register followed by the Address Word into the ACTIVE register.

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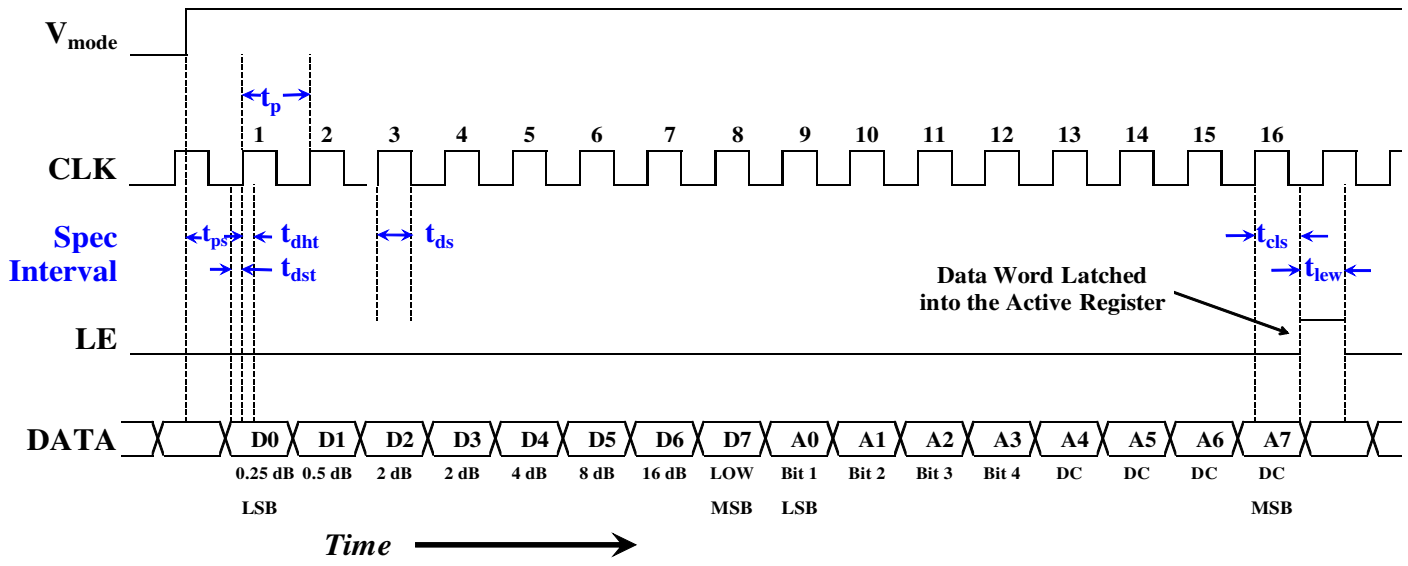

Figure 4 - Serial Timing Diagram

Note - When Latch Enable (LE) is high, the shift register is disabled and DATA is NOT continuously clocked into the shift register which minimizes noise. It is recommended that Latch enable be left high when the device is not being programmed.

Table 3 - Serial Mode Timing Table

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{ps}	Parallel to Serial Setup Time - From rising edge of Vmode to rising edge of CLK for D5	***100***		ns
t_p	Clock high pulse width	***10***		ns
t_{cls}	LE Setup Time - From the rising edge of CLK pulse for D0 to LE rising edge minus half the clock period.	***10***		ns
t_{lew}	LE pulse width	***30***		ns
t_{dst}	Data Setup Time - From the starting edge of Data bit to rising edge of CLK	***10***		ns
t_{dht}	Data Hold Time - From rising edge of CLK to falling edge of the Data bit.	***10***		ns

PARALLEL CONTROL MODE

For the F1977 the user has the option of running in one of two parallel modes. Direct Parallel Mode or Latched Parallel Mode.

Direct Parallel Mode:

Direct Parallel Mode is selected when V_{MODE} is a logic low and LE is a logic high. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 26 – 32]. Use direct parallel mode for the fastest settling time.

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Latched Parallel Mode:

Latched Parallel Mode is selected when V_{MODE} is logic low and LE is toggled from logic low to high. To utilize Latched Parallel Mode:

- Set V_{MODE} is logic low.
- Set LE to logic low.
- Adjust pins [26, 27, 28, 29, 30, 31, 32] to the desired attenuation setting. (While LE is set to a logic low, the attenuation state will not change.)
- Pull LE to a logic high. The device will then transition to the attenuation settings reflected by pins D6 - D0.

Latched Parallel Default Startup Condition:

Latched Parallel Mode implies a default state for when the device is first powered up with V_{MODE} set for logic low and LE logic low. In this case the default setting is MAXIMUM Attenuation.

Table 4 - Truth Table for the Parallel Control Word

D6	D5	D4	D3	D2	D1	D0	Attenuation (dB)
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.25
0	0	0	0	0	1	0	0.5
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	2
0	0	1	0	0	0	0	4
0	1	0	0	0	0	0	8
1	0	0	0	0	0	0	16
1	1	1	1	1	1	1	31.75

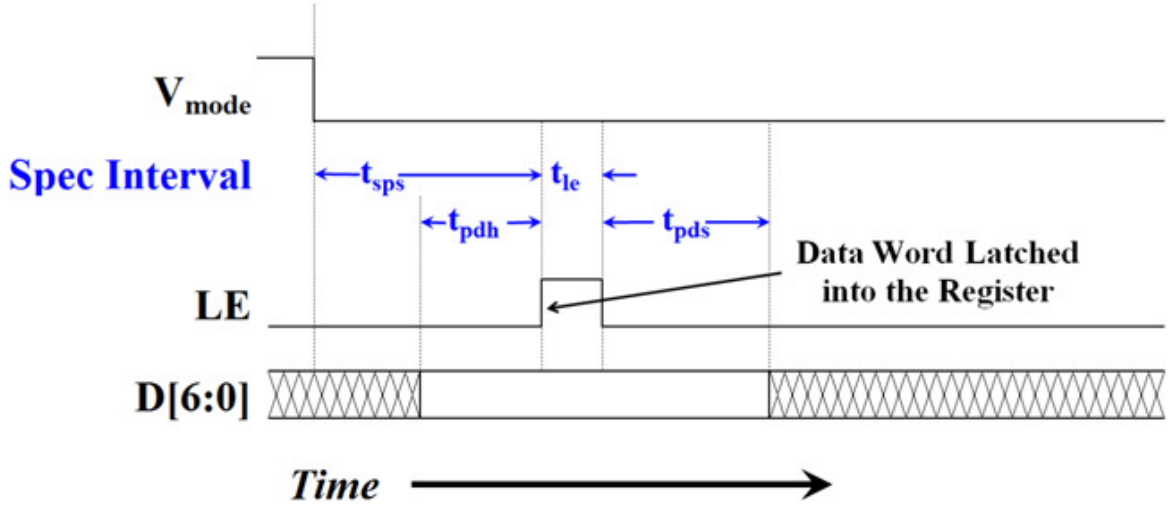

Figure 5 - Latched Parallel Mode Timing Diagram

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Table 5 - Latched Parallel Mode Timing

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{sps}	Serial to Parallel Mode Setup Time	100		ns
t_{pdh}	Parallel Data Hold Time	10		ns
t_{le}	LE minimum pulse width	10		ns
t_{pds}	Parallel Data Setup Time	10		ns

TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

- **V_{DD} = +3.30 V**
- **T_{CASE} = +25 °C**
- **P_{IN} = 0 dBm for single tone measurements**
- **P_{IN} = +15 dBm/tone for multi-tone measurements**
- **50 MHz Tone Space**
- **Serial Control**
- **RF1 Port is the input port**
- **Attenuation Setting = 0 dB**
- **Measured in a 75 ohm system**
- **EVKit losses (traces and connectors) are fully de-embedded**

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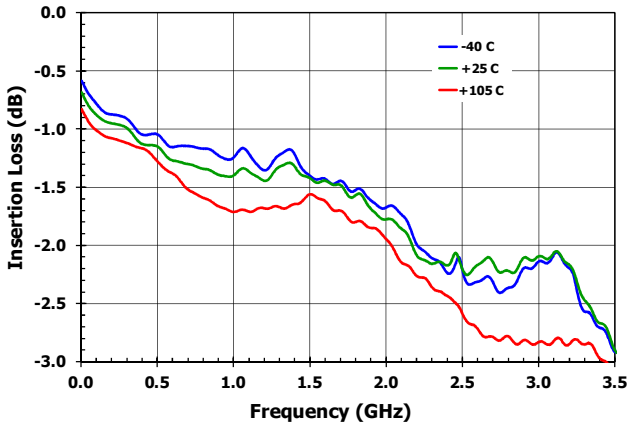
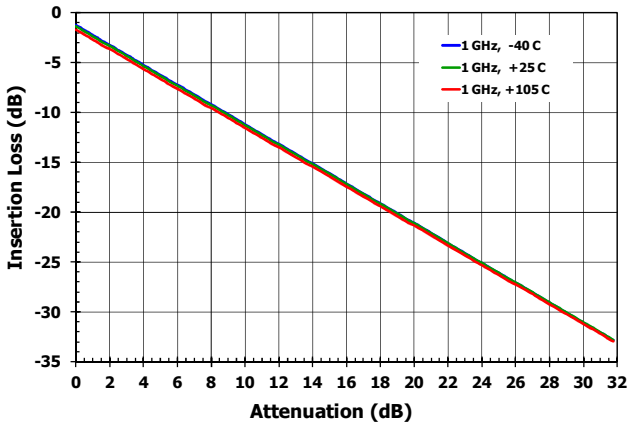
TYPICAL OPERATING CONDITIONS (- 1 -)

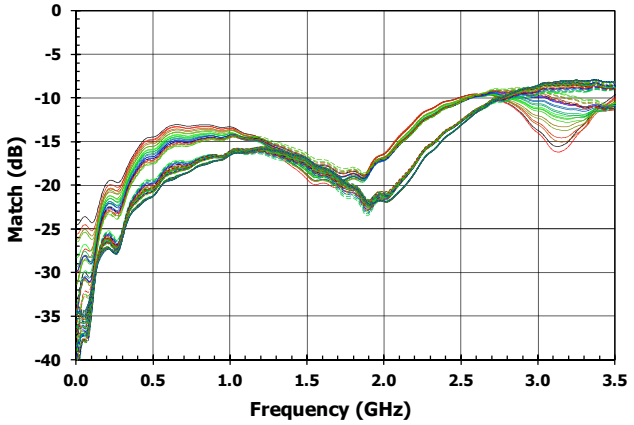
Insertion Loss vs Frequency



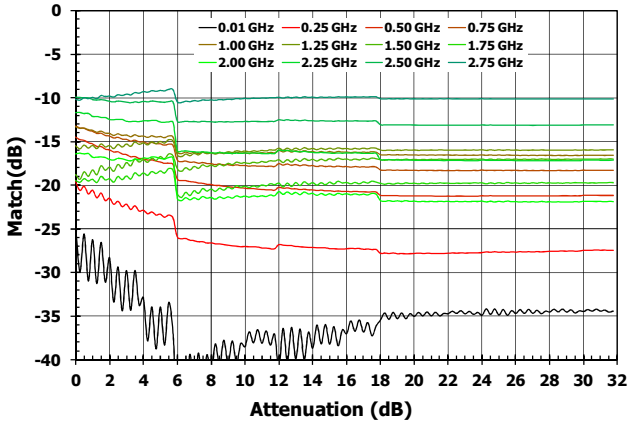
Insertion Loss vs Attenuation State



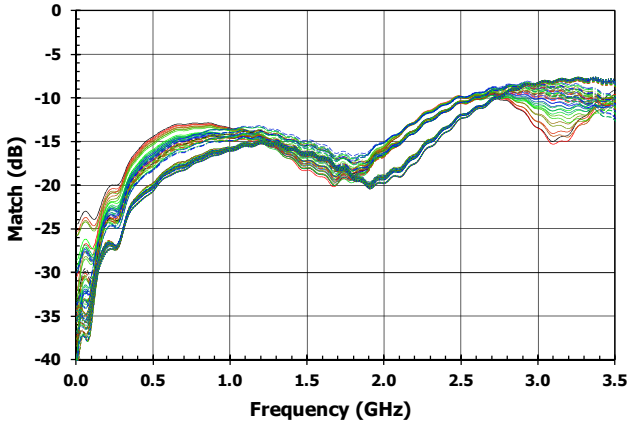
RF1 Return Loss vs Frequency [All States]



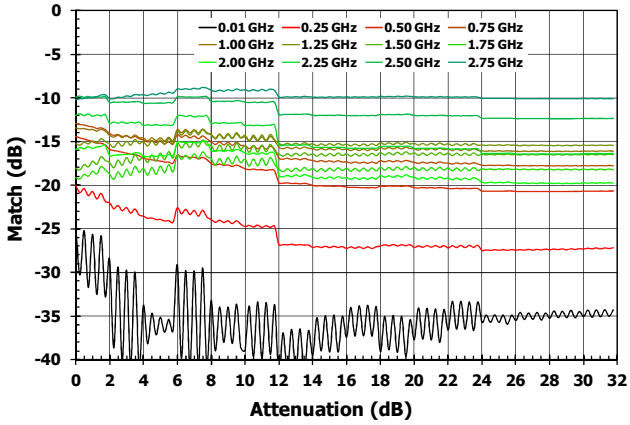
RF1 Return Loss vs Attenuation State



RF2 Return Loss vs Frequency [All States]



RF2 Return Loss vs Attenuation State



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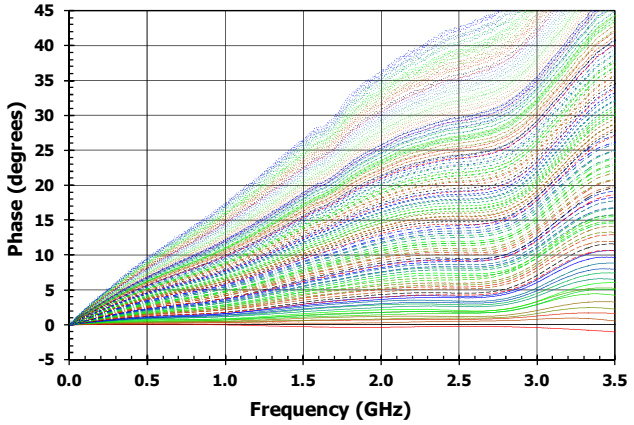
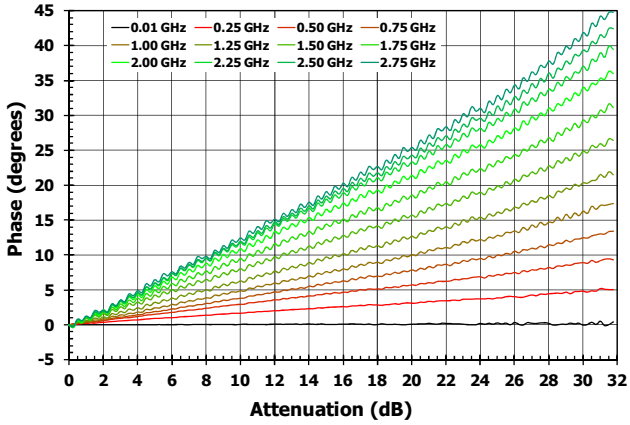
TYPICAL OPERATING CONDITIONS (- 2 -)

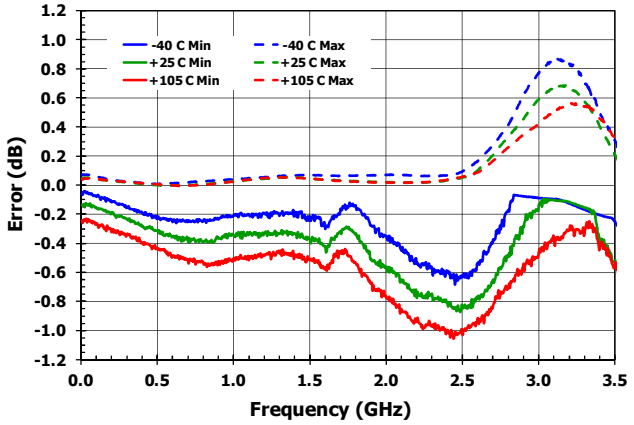
Relative Insertion Phase vs Frequency



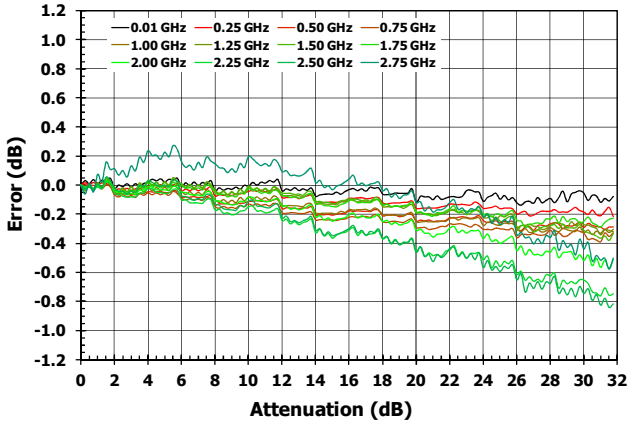
Relative Insertion Phase vs Attenuation



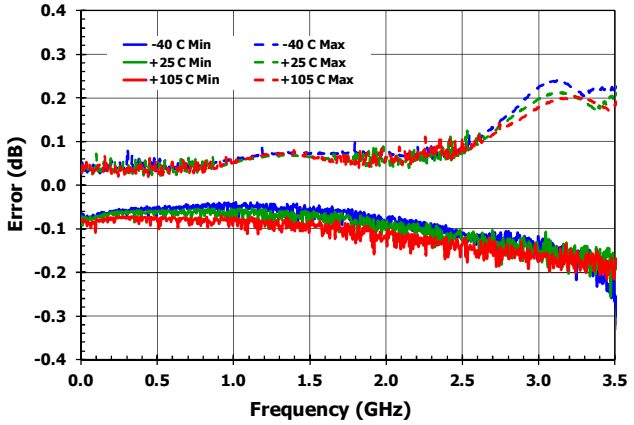
Worst Case Absolute Accuracy vs Frequency



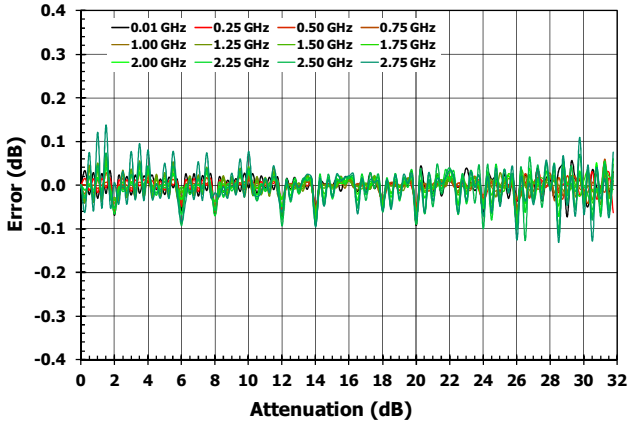
Absolute Accuracy vs Attenuation



Worst Case Step Accuracy vs Frequency



Step Accuracy vs Attenuation



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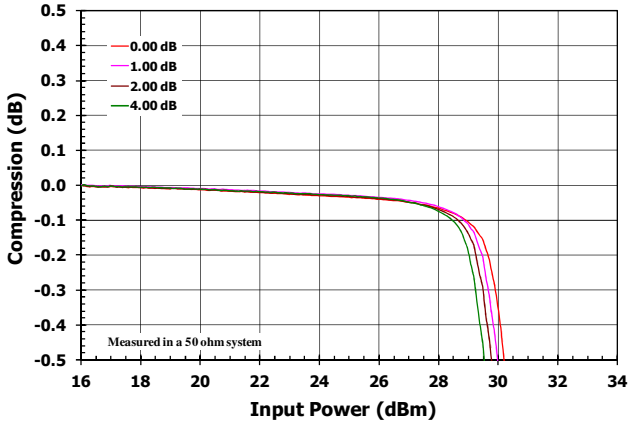
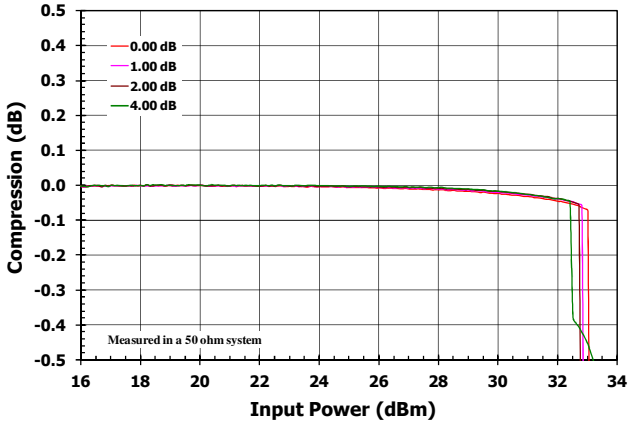
TYPICAL OPERATING CONDITIONS (- 3 -)

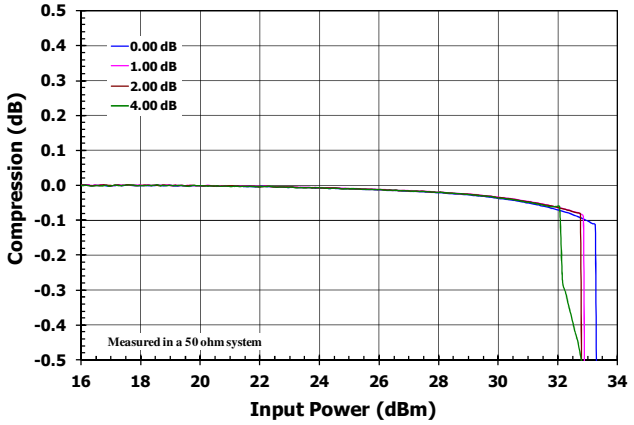
Input Compression at 50 MHz



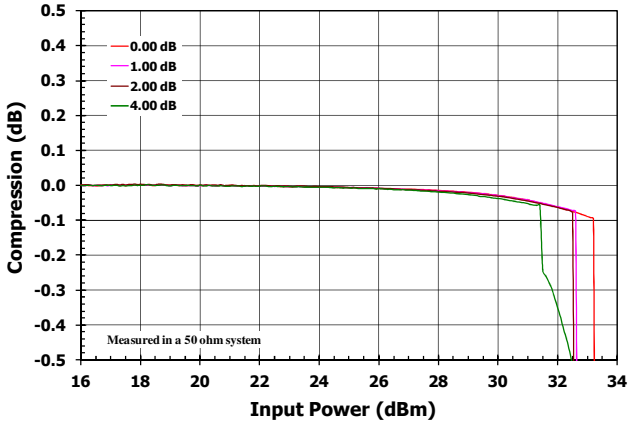
Input Compression 500 MHz



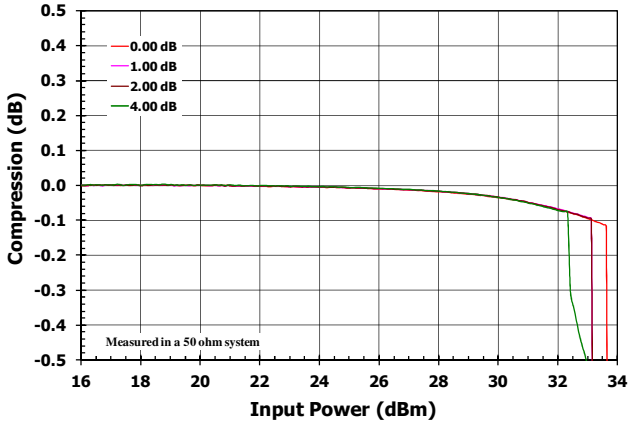
Input Compression 1.0 GHz



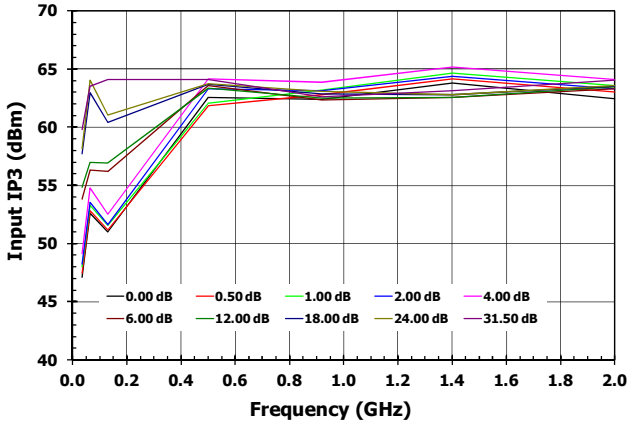
Input Compression 1.5 GHz



Input Compression 2.0 GHz



Input IP3



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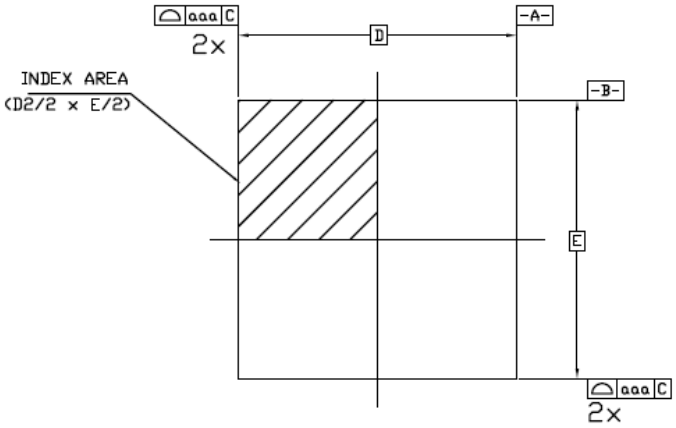
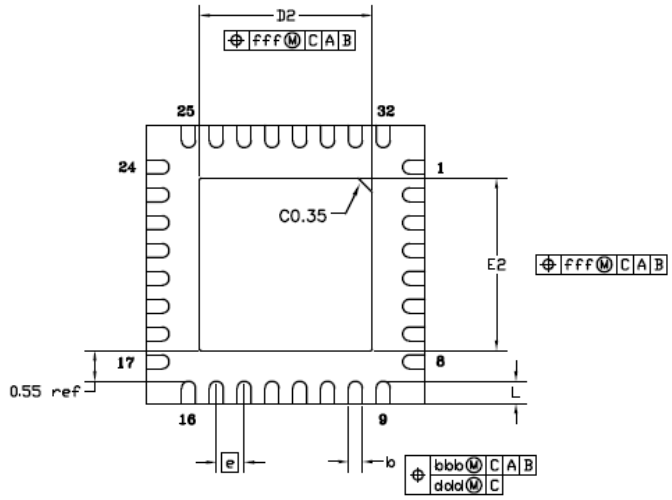
PACKAGE DRAWING

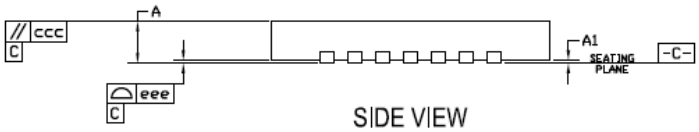
(5 mm x 5 mm 32-pin TQFN), Use Exposed PAD (EPAD) ***Option P1***



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	DIMENSION		
	MIN	NOM	MAX
L	0.30	0.40	0.50
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

EPAD OPTION

SYMBOL	P1		
	MIN	NOM	MAX
E2	3.00	3.10	3.20
D2	3.00	3.10	3.20

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

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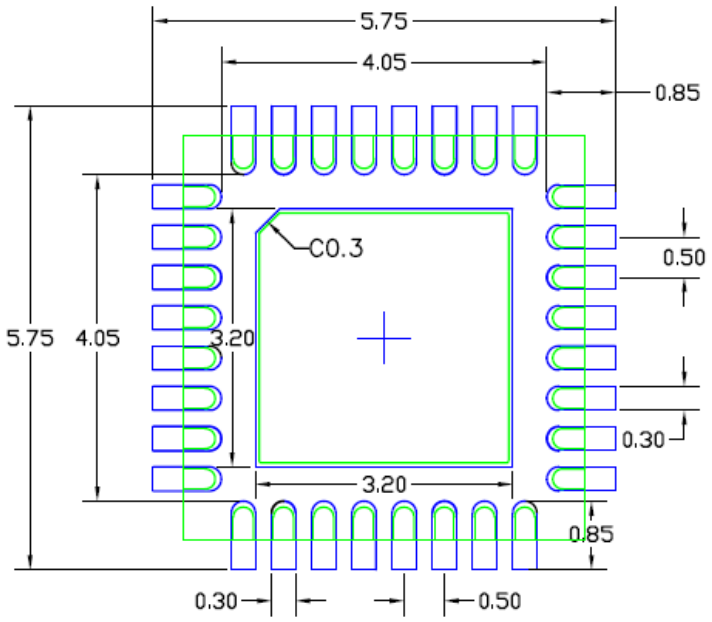
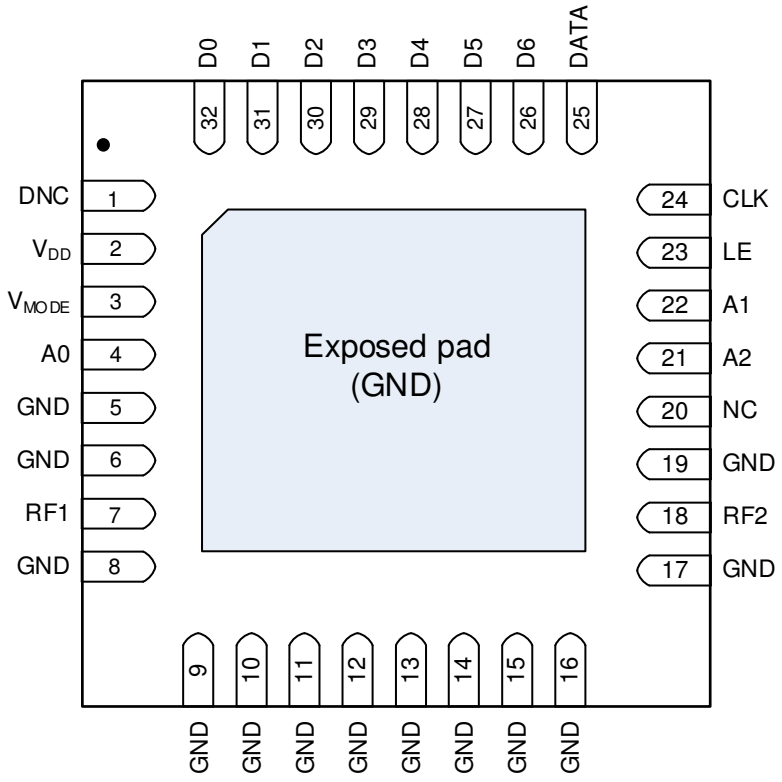
LAND PATTERN DIMENSION



PIN DIAGRAM

TOP View
(looking through the top of the package)



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PIN DESCRIPTION

Pin	Name	Function
1	DNC	**This pin must be left open.**
2	V_{DD}	Main Supply. Use 3.3 V or 5 V. Bypass capacitor as close to pin as possible.
3	V_{MODE}[1]	Logic low for parallel mode. Logic high or NC for serial mode.
4	A0[2]	Address bit A0 connection.
5	GND	Connect directly to paddle ground or as close as possible to pin with thru via. This pin is not internally connected.
6	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
7	RF1[3]	Device RF input or output (bi-directional).
8 – 17	GND	Connect each pin directly to paddle ground or as close as possible to pin with thru vias.
18	RF2[3]	Device RF input or output (bi-directional).
19	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
20	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
21	A2[2]	Address bit A2 connection
22	A1[2]	Address bit A1 connection.
23	LE[1]	Serial interface latch enable input.
24	CLK[1]	Serial interface clock input.
25	DATA[1]	Serial interface data input.
26	D6[1]	Parallel control bit, 16 dB.
27	D5[1]	Parallel control bit, 8 dB.
28	D4[1]	Parallel control bit, 4 dB.
29	D3[1]	Parallel control bit, 2 dB.
30	D2[1]	Parallel control bit, 1 dB.
31	D1[1]	Parallel control bit, 0.5 dB.
32	D0[1]	Parallel control bit, 0.25 dB.
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal and RF performance.

Pin Description Notes:

Note 1: Includes an internal 100 kΩ pullup resistor to an internal regulated 2.5V supply. If pin is grounded then there is an additional 25 µA per pin for the supply current.

Note 2: Includes an internal 100 kΩ pull-down resistor to GND.

Note 3: RF pins 7 and 18 do not require DC blocking capacitors for operation if they are at 0 V DC. If they are not at 0V DC, then they require DC blocking capacitors.

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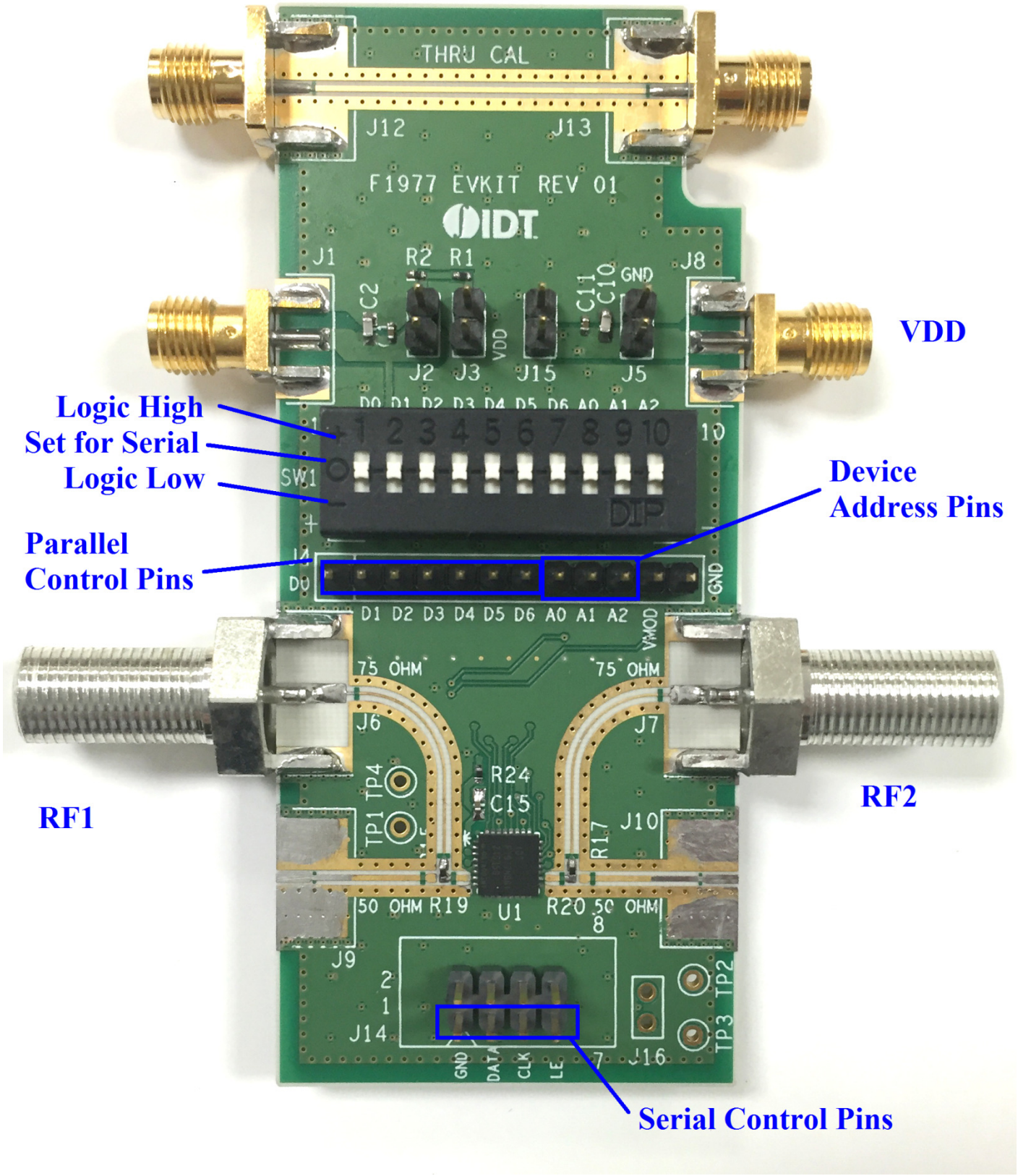
EVKIT PICTURE



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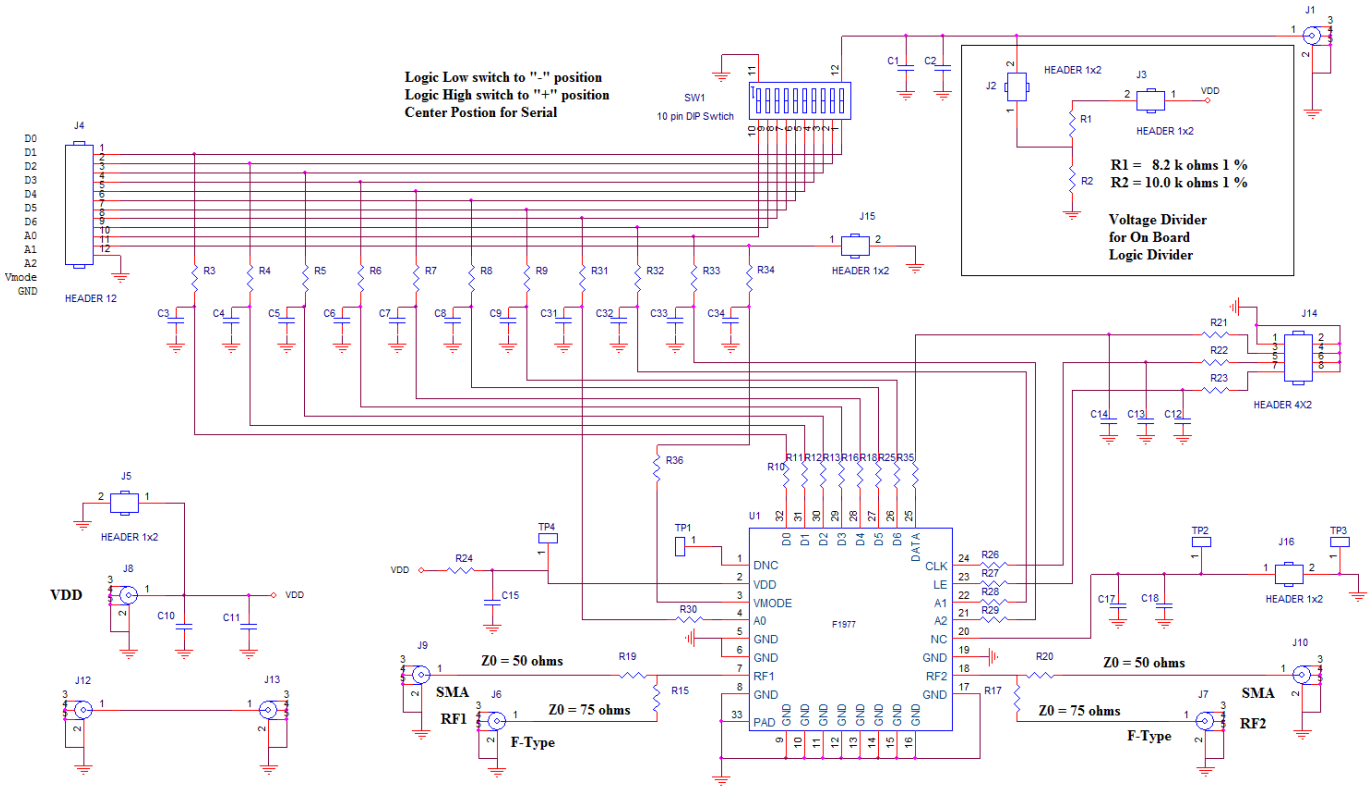
EVKIT / APPLICATIONS CIRCUIT



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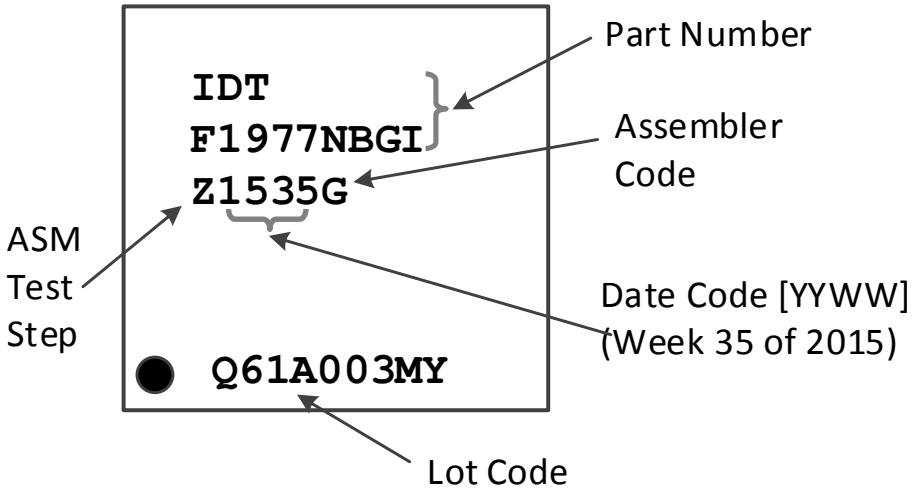
EVKIT BOM

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C1, C11, C15	3	100 nF ±10%, 16 V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	MURATA
2	C2, C10	2	10 nF ±5%, 50 V, X7R Ceramic Capacitor (0603)	GRM188R71H103J	MURATA
3	C3 - C9, C12, C13, C14, C31 - C34	14	100 pF ±5%, 50 V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
4	R3 - R9, R31 - R34	11	100 Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
5	R10-R13, R15-R18, R24-R30, R35, R36	17	0 Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
6	R21, R22, R23	3	3 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3001X	PANASONIC
7	R1	1	8.2 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF8201X	PANASONIC
8	R2	1	10 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1002X	PANASONIC
9	J2, J3, J5	3	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
10	J14, J15	1	CONN HEADER VERT DBL 4 X 2 POS GOLD	67997-108HLF	FCI
11	J4	1	CONN HEADER VERT SGL 12 X 1 POS GOLD	961112-6404-AR	3M
12	J1, J8	2	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
13	J6, J7	2	Edge Launch F TYPE 75 ohm SMA	222181	Amphenol
14	U2	1	SWITCH 10 POSITION DIP SWITCH	KAT1110E	E-Switch
15	U1	1	DSA	F1977NCGI	IDT
16		1	Printed Circuit Board	F1977 Evkit Rev 01	IDT

TOP MARKINGS



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APPLICATIONS INFORMATION

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 µS. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

Digital Pin Voltage & Resistance Values

The following table provides open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

Pin	Name	Open Circuit DC Voltage	Internal Connection
3	V_{MODE}	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V
4, 21, 22	A0, A2, A1	0 V	100 kΩ resistor to GND
23, 24, 25	LE, CLK, DATA	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V
26-32	D[6:0]	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V

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REVISION HISTORY SHEET

Rev	Date	Page	Description of Change
O	2016-Feb-19		Initial Release
1	2016-Apr-21	2	Typo on V_{HBM} rating. Voltage changed from 1.5kV to 1kV. No chng. to Class

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