19-4655; Rev 1; 5/09

Smart Card Interface

General Description

The DS8313 smart card and SIM interface IC is a low-cost, analog front-end for a smart card reader designed for smart card applications that do not require the use of the auxiliary card I/O contacts C4 and C8 (AUX1 and AUX2). The DS8313 supports 5V, 3V, and 1.8V smart cards. The absence of a charge pump reduces active power consumption, and the DS8313 also supports an ultra-low-power 10nA stop mode.

The DS8313 is designed to interface between a system microcontroller and the smart card interface, providing all power supply, protection, and level shifting required for IC card applications.

The DS8314 is similar to the DS8313, but only uses one analog (smart card) power supply. Therefore, the device has reduced ability to provide power to smart cards, but it is still sufficient for many applications, allowing the DS8314 to drop into many TDA8024 sockets without hardware changes.

The DS8313L and DS8314L use a negative polarity-presence detect instead of the default positive-polarity detect. Both devices are available in a 28-pin SO package.

Applications

Pay/Premium Television
Access Control
Banking Applications
POS Terminals
Debit/Credit Payment Terminals
PIN Pads
Automated Teller Machines
Telecommunications

Features

- **Analog Interface and Level Shifting for IC Card Communication**
- **±8kV (min) ESD (HBM) Protection on Card Interfaces**
- **Ultra-Low Stop-Mode Current, Less Than 10nA Typical**
- **Internal IC Card Supply-Voltage Generation**
  5.0V ±5%, 80mA (max)
  3.0V ±8%, 65mA (max)
  1.8V ±10%, 30mA (max)
- **Automatic Card Activation and Deactivation Controlled by Dedicated Internal Sequencer**
- **I/O Lines from Host Directly Level Shifted for Smart Card Communication**
- **Flexible Card Clock Generation, Supporting External Crystal Frequency Divided by 1, 2, 4, or 8**
- **High-Current, Short-Circuit and High-Temperature Protection**
- **Low Active-Mode Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS8313-RRX+	-40°C to +85°C	28 SO
DS8313L-RRX+*	-40°C to +85°C	28 SO
DS8314-RRX+*	-40°C to +85°C	28 SO
DS8314L-RRX+*	-40°C to +85°C	28 SO

Note: *Contact the factory for availability of other variants and package options.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*

Typical Application Circuit, Pin Configuration, and Selector Guide appear at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maxim-ic.com/errata****.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Smart Card Interface

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD} Relative to GND .....-0.5V to +6.5V
Voltage Range on V_{DDA} Relative to GND .....-0.5V to +6.5V
Voltage Range on All Other Pins
Relative to GND.....-0.5V to (V_{DD} + 0.5V)

Maximum Junction Temperature .....+125°C
Maximum Power Dissipation (T_A = -25°C to +85°C) 700mW
Storage Temperature Range .....-55°C to +150°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted. All specifications apply to both the DS8313 and DS8314, unless otherwise noted in the CONDITIONS column.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Digital Supply Voltage	V_{DD}		2.7		6.0	V
Card Voltage-Generator Supply Voltage	V_{DDA}	DS8313, DS8314	4.75		6.0	V
Reset Voltage Thresholds	V_{TH2}	Threshold voltage (falling)	2.35	2.45	2.65	V
	V_{HYS2}	Hysteresis	50	100	150	mV
CURRENT CONSUMPTION						
Active V_{DD} Current 5V Cards (Including 80mA Draw from 5V Card)	I_{DD_50V}	I_{CC} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V		80.75	85	mA
Active V_{DD} Current 5V Cards (Current Consumed by DS8313/DS8314 Only)	I_{DD_IC}	I_{CC} = 80mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)		0.75	5	mA
Active V_{DD} Current 3V Cards (Including 65mA Draw from 3V Card)	I_{DD_30V}	I_{CC} = 65mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V		65.75	70	mA
Active V_{DD} Current 3V Cards (Current Consumed by DS8313/DS8314 Only)	I_{DD_IC}	I_{CC} = 65mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)		0.75	5	mA
Active V_{DD} Current 1.8V Cards (Including 30mA Draw from 1.8V Card)	I_{DD_18V}	I_{CC} = 30mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V		30.75	40	mA
Active V_{DD} Current 1.8V Cards (Current Consumed by DS8313/DS8314 Only)	I_{DD_IC}	I_{CC} = 30mA, f_{XTAL} = 20MHz, f_{CLK} = 10MHz, V_{DDA} = 5.0V (Note 2)		0.75	5	mA
Inactive-Mode Current	I_{DD}	Card inactive, active-high PRES, DS8313/DS8314 not in stop mode		50	40	µA
Stop-Mode Current	I_{DD_STOP}	DS8313/DS8314 in ultra-low-power stop mode ($\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V set to logic 1) (Note 3)		10		µA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted. All specifications apply to both the DS8313 and DS8314, unless otherwise noted in the CONDITIONS column.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK SOURCE							
Crystal Frequency		f_{XTAL}	External crystal (Note 1)	0		20	MHz
XTAL1 Operating Conditions		f_{XTAL1}	(Note 1)	0		20	MHz
		V_{IL_XTAL1}	Low-level input on XTAL1	-0.3		0.3 x V_{DD}	V
		V_{IH_XTAL1}	High-level input on XTAL1	0.7 x V_{DD}		V_{DD} + 0.3	V
External Capacitance for Crystal		C_{XTAL1}, C_{XTAL2}				15	pF
Internal Oscillator		f_{INT}		2.2	2.7	3.4	MHz
SHUTDOWN TEMPERATURE							
Shutdown Temperature		T_{SD}			+150		°C
RST PIN							
Card-Inactive Mode	Output Low Voltage	V_{OL_RST1}	I_{OL_RST} = 1mA	0		0.3	V
	Output Current	I_{OL_RST1}	V_{OL_RST} = 0	0		-1	mA
Card-Active Mode	Output Low Voltage	V_{OL_RST2}	I_{OL_RST} = 200µA	0		0.3	V
	Output High Voltage	V_{OH_RST2}	I_{OH_RST} = -200µA	V_{CC} - 0.5		V_{CC}	V
	Rise Time	t_{R_RST}	C_L = 30pF (Note 1)			0.1	µs
	Fall Time	t_{F_RST}	C_L = 30pF (Note 1)			0.1	µs
	Current Limitation	$I_{RST(LIMIT)}$		-20		+20	mA
	RSTIN to RST Delay	$t_{D(RSTIN-RST)}$				2	µs
CLK PIN							
Card-Inactive Mode	Output Low Voltage	V_{OL_CLK1}	I_{OLCLK} = 1mA	0		0.3	V
	Output Current	I_{OL_CLK1}	V_{OLCLK} = 0	0		-1	mA
Card-Active Mode	Output Low Voltage	V_{OL_CLK2}	I_{OLCLK} = 200µA	0		0.3	V
	Output High Voltage	V_{OH_CLK2}	I_{OHCLK} = -200µA	V_{CC} - 0.5		V_{CC}	V
	Rise Time	t_{R_CLK}	C_L = 30pF (Notes 1, 4)			8	ns
	Fall Time	t_{F_CLK}	C_L = 30pF (Notes 1, 4)			8	ns
	Current Limitation	$I_{CLK(LIMIT)}$		-70		+70	mA
	Clock Frequency	f_{CLK}	Operational	0		10	MHz
	Duty Factor	δ	C_L = 30pF	45		55	%
	Slew Rate	SR	C_L = 30pF (Note 1)	0.2			V/ns
VCC PIN							
Card-Inactive Mode	Output Low Voltage	V_{CC1}	I_{CC} = 1mA	0		0.3	V
	Output Current	I_{CC1}	V_{CC} = 0	0		-1	mA

Smart Card Interface

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted. All specifications apply to both the DS8313 and DS8314, unless otherwise noted in the CONDITIONS column.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Card-Active Mode	Output Low Voltage	V_{CC2}	DS8313: $I_{CC(5V)}$ < 80mA, V_{DDA} = 4.75V (Note 1)	4.65	5	5.25	V
			DS8313: $I_{CC(5V)}$ < 65mA	4.75	5	5.25	
			DS8313: $I_{CC(3V)}$ < 65mA	2.78	3	3.24	
			DS8313: $I_{CC(1.8V)}$ < 30mA	1.64	1.8	1.98	
			DS8314: 65mA < $I_{CC(5V)}$ < 80mA	4.55	5	5.25	
			DS8314: $I_{CC(5V)}$ < 65mA	4.75	5	5.25	
			DS8314: $I_{CC(3V)}$ < 65mA	2.78	3	3.24	
			DS8314: $I_{CC(1.8V)}$ < 30mA	1.64	1.8	1.98	
			5V card; current pulses of 40nC with I < 200mA, t < 400ns, f < 20MHz	4.6		5.4	
			3V card; current pulses of 24nC with I < 200mA, t < 400ns, f < 20MHz	2.75		3.25	
			1.8V card; current pulses of 12nC with I < 200mA, t < 400ns, f < 20MHz	1.62		1.98	
	Output Current	I_{CC2}	$V_{CC(5V)}$ = 0 to 5V			-80	mA
			$V_{CC(3V)}$ = 0 to 3V			-65	
			$V_{CC(1.8V)}$ = 0 to 1.8V			-30	
	Shutdown Current Threshold	$I_{CC(SD)}$	(Note 1)		120		mA
	Slew Rate	V_{CCSR}	Up/down; C < 300nF (Note 5)	0.05	0.16	0.22	V/µs
DATA LINES (I/O AND I/OIN)							
I/O ⇔ I/OIN Falling Edge Delay		$t_{D(IO-IOIN)}$	(Note 1)			200	ns
Pullup Pulse Active Time		t_{PU}	(Note 1)			100	ns
Maximum Frequency		f_{IOMAX}				1	MHz
Input Capacitance		C_I				10	pF
I/O PIN							
Card-Inactive Mode	Output Low Voltage	V_{OL_IO1}	I_{OL_IO} = 1mA	0		0.3	V
	Output Current	I_{OL_IO1}	V_{OL_IO} = 0	0		-1	mA
	Internal Pullup Resistor	R_{PU_IO}	To V_{CC}	9	11	19	kΩ
Card-Active Mode	Output Low Voltage	V_{OL_IO2}	I_{OL_IO} = 1mA	0		0.3	V
	Output High Voltage	V_{OH_IO2}	I_{OH_IO} = < -20µA	0.8 x V_{CC}		V_{CC}	V
			I_{OH_IO} = < -40µA (3V/5V)	0.75 x V_{CC}		V_{CC}	
	Output Rise/Fall Time	t_{OT}	C_L = 30pF (Note 1)			0.1	µs
	Input Low Voltage	V_{IL_IO}		-0.3		+0.8	V
	Input High Voltage	V_{IH_IO}		1.5		V_{CC}	

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted. All specifications apply to both the DS8313 and DS8314, unless otherwise noted in the CONDITIONS column.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Card-Active Mode	Input Low Current	I_{IL_IO}	V_{IL_IO} = 0			600	µA
	Input High Current	I_{IH_IO}	V_{IH_IO} = V_{CC}			20	µA
	Input Rise/Fall Time	t_{IT}				1.2	µs
	Current Limitation	$I_{IO(LIMIT)}$	C_L = 30pF	-15		+15	mA
	Current When Pullup Active	I_{PU}	C_L = 80pF, V_{OH} = 0.9 x V_{DD}	-1			mA
I/OIN PIN							
Output Low Voltage		V_{OL}	I_{OL} = 1mA	0		0.3	V
Output High Voltage		V_{OH}	I_{OH} < -40µA	0.75 x V_{DD}		V_{DD} + 0.1	V
Output Rise/Fall Time		t_{OT}	C_L = 30pF, 10% to 90%			0.1	µs
Input Low Voltage		V_{IL}		-0.3		0.3 x V_{DD}	V
Input High Voltage		V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Low Current		I_{IL_IO}	V_{IL} = 0			600	µA
Input High Current		I_{IH_IO}	V_{IH} = V_{DD}			10	µA
Input Rise/Fall Time		t_{IT}	V_{IL} to V_{IH}			1.2	µs
Integrated Pullup Resistor		R_{PU}	Pullup to V_{DD}	9	11	13	kΩ
Current When Pullup Active		I_{PU}	C_L = 30pF, V_{OH} = 0.9 x V_{DD}	-1			mA
CONTROL PINS (CLKDIV1, CLKDIV2, $\overline{\text{CMDVCC}}$, RSTIN, 5V/$\overline{\text{3V}}$, 1_8V)							
Input Low Voltage		V_{IL}		-0.3		0.3 x V_{DD}	V
Input High Voltage		V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Low Current		I_{IL_IO}	0 < V_{IL} < V_{DD}			5	µA
Input High Current		I_{IH_IO}	0 < V_{IH} < V_{DD}			5	µA
INTERRUPT OUTPUT PIN ($\overline{\text{OFF}}$)							
Output Low Voltage		V_{OL}	I_{OL} = 2mA	0		0.3	V
Output High Voltage		V_{OH}	I_{OH} = -15µA	0.75 x V_{DD}			V
Integrated Pullup Resistor		R_{PU}	Pullup to V_{DD}	16	24	32	kΩ
PRES PIN							
Input Low Voltage		V_{IL_PRES}				0.3 x V_{DD}	V
Input High Voltage		V_{IH_PRES}		0.7 x V_{DD}			V

Smart Card Interface

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = +3.3V, V_{DDA} = +5.0V, T_A = +25°C, unless otherwise noted. All specifications apply to both the DS8313 and DS8314, unless otherwise noted in the CONDITIONS column.) (Note 1)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Current		I_{IL_PRES}	V_{IL_PRES} = 0			5	µA
Input High Current		I_{IH_PRES}	V_{IH_PRES} = V_{DD}			10	µA
TIMING							
Activation Time		t_{ACT}		50		220	µs
Deactivation Time		t_{DEACT}		50	80	100	µs
CLK to Card Start Time	Window Start	t_3		50		130	µs
	Window End	t_5		140		220	
PRES Debounce Time		$t_{DEBOUNCE}$		5	8	11	ms

Note 1: Operation guaranteed at -40°C and +85°C but not tested.

Note 2: I_{DD_IC} measures the amount of current used by the DS8313 to provide the smart card current minus the load.

Note 3: Stop mode is enabled by setting $\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V to a logic-high.

Note 4: Parameters are guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the maximum rise and fall time is 10ns.

Note 5: Parameter is guaranteed to meet all ISO 7816, GSM11-11, and EMV 2000 requirements. For the 1.8V card, the minimum slew rate is 0.05V/µs and the maximum slew rate is 0.5V/µs.

Pin Description

PIN	NAME	FUNCTION
1, 2	CLKDIV1, CLKDIV2	Clock Divider. Determines the divided-down input clock frequency (presented at XTAL1 or from a crystal at XTAL1 and XTAL2) on the CLK output pin. Dividers of 1, 2, 4, and 8 are available.
3	5V/$\overline{3V}$	5V/3V Selection Pin. Allows selection of 5V or 3V for communication with an IC card. Logic-high selects 5V operation; logic-low selects 3V operation. The 1_8V pin overrides the setting on this pin if active. See Table 3 for a complete description of choosing card voltages.
4	1_8V	1.8V Operation Selection. Active-high selection for 1.8V smart card communication. An active-high signal on this pin overrides any setting on the 5V/$\overline{3V}$ pin.
5, 7, 8, 9, 12, 13, 27, 28	N.C.	No Connection/Don't Care. These pins are not bonded out.
6, 18	V_{DDA} (N.C.)	Analog (Smart Card) Supply. Connect to 5V power supply. Pin 18 is N.C. for the DS8314.
10	PRES	Card Presence Indicator. Active-high card presence input from the DS8313 to the microcontroller. When the presence indicator becomes active, a debounce timeout begins. After 8ms (typ), the $\overline{OFF}$ signal becomes active. A trim optim defines whether or not the part provides active-low presence detection.
11	I/O	Smart Card Data-Line Output. Card data communication line, contact C7.
14	CGND	Smart Card Ground
15	CLK	Smart Card Clock. Card clock, contact C3.
16	RST	Smart Card Reset. Card reset output from contact C2.
17	V_{CC}	Smart Card Supply Voltage. Decouple to CGND (card ground) with 2 x 100nF or 100 + 220nF capacitors (ESR < 100mΩ).
19	$\overline{CMDVCC}$	Activation Sequence Initiate. Active-low input from host.
20	RSTIN	Card Reset Input. Reset input from the host.
21	V_{DD}	Supply Voltage
22	GND	Digital Ground
23	$\overline{OFF}$	Status Output. Active-low interrupt output to the host. Includes a 24kΩ integrated pullup resistor to V_{DD}.
24, 25	XTAL1, XTAL2	Crystal/Clock Input. Connect an input from an external clock to XTAL1 or connect a crystal across XTAL1 and XTAL2. For the low idle-mode current variant, an external clock must be driven on XTAL1.
26	I/OIN	I/O Input. Host-to-interface chip data I/O line.

Smart Card Interface

Detailed Description

The DS8313 is an analog front-end for communicating with 1.8V, 3V, and 5V smart cards. It is a dual input-voltage device, requiring one supply to match that of a host microcontroller and a separate +5V supply for generating correct smart card supply voltages. The DS8313 translates all communication lines to the correct voltage level and provides power for smart card operation. It is a low-power device, consuming very little current in active-mode operation (during a smart card communication session), and is suitable for use in battery-powered devices such as laptops and PDAs, consuming only 10nA in stop mode. The DS8313 is designed for applications that do not require communication using the C4 and C8 card contacts (AUX1 and AUX2). It is suitable for SIM/SAM interfacing, as well as for applications where only the I/O line is used to communicate with a smart card.

The DS8314 is nearly identical to the DS8313, but only uses one V_{DDA} input; therefore, it has reduced capacity to deliver current to 5V smart cards. However, the DS8314 can drop into many existing TDA8024 applications with minimal or no hardware changes. See Figure 1 for a functional diagram.

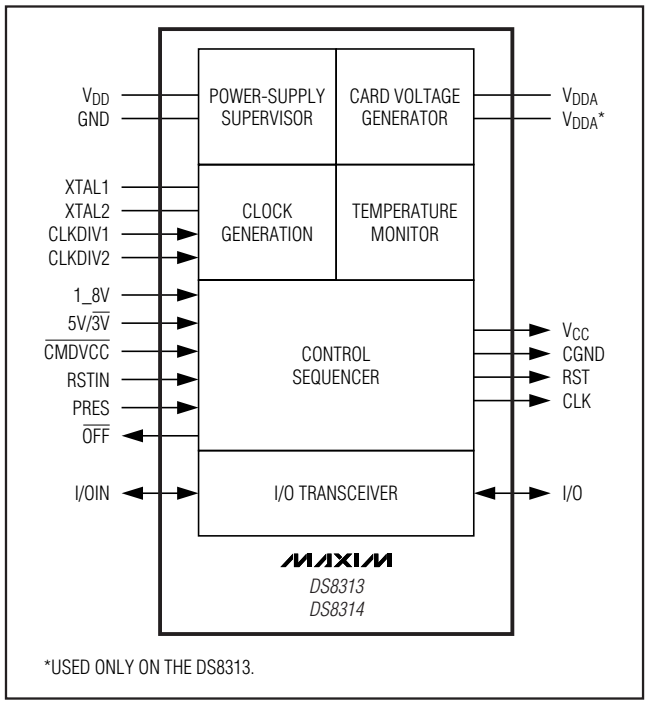


Figure 1. Functional Diagram

Power Supply

The DS8313/DS8314 are dual-supply devices. The supply pins for the devices are V_{DD}, GND, and V_{DDA}. V_{DD} should be in the 2.7V to 6.0V range, and is the supply for signals that interface with the host controller. It should, therefore, be the same supply as used by the host controller. All smart card contacts remain inactive during power-on or power-off. The internal circuits are kept in the reset state until V_{DD} reaches $V_{TH2} + V_{HYS2}$ and for the duration of the internal power-on reset pulse, t_W. A deactivation sequence is executed when V_{DD} falls below V_{TH2}.

An internal regulator generates the 1.8V, 3V, or 5V card supply voltage (V_{CC}). The regulator should be supplied separately by V_{DDA}. V_{DDA} should be connected to a minimum 4.75V supply to provide the correct supply voltage for 5V smart cards.

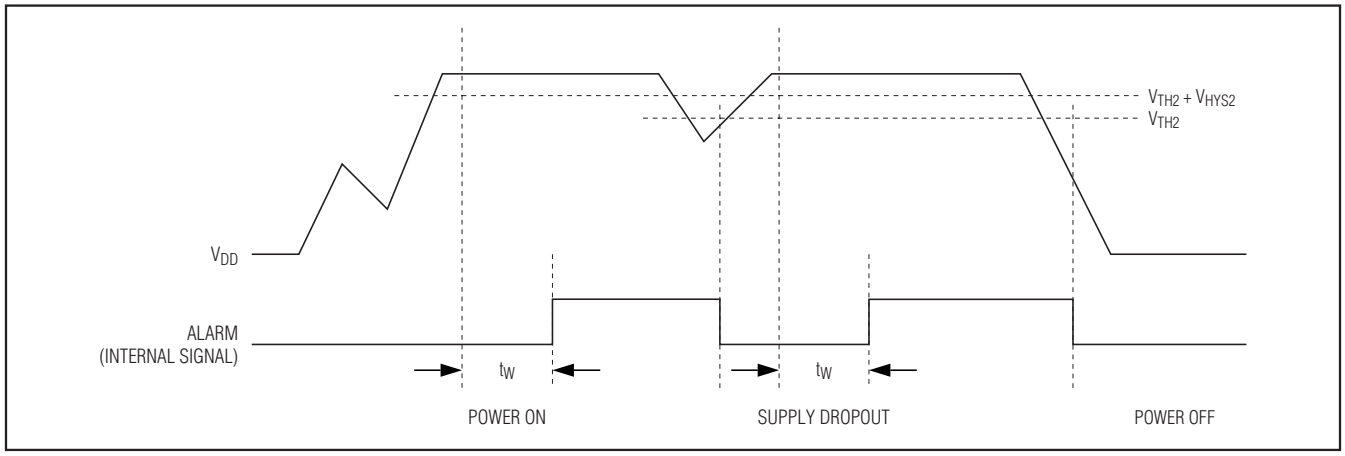


Figure 2. Voltage Supervisor Behavior

Voltage Supervisor

The voltage supervisor monitors the V_{DD} supply. A 220µs reset pulse (t_W) is used internally to keep the device inactive during power-on or power-off of the V_{DD} supply. See Figure 2.

The DS8313/DS8314 card interface remains inactive regardless of the levels on the command lines until duration t_W after V_{DD} has reached a level higher than $V_{TH2} + V_{HYS2}$. When V_{DD} falls below V_{TH2}, the DS8313/DS8314 execute a card deactivation sequence if their card interface is active.

Clock Circuitry

The card clock signal (CLK) is derived from a clock signal input to XTAL1 or from a crystal operating at up to 20MHz connected between XTAL1 and XTAL2. The output clock frequency of CLK is selectable through inputs CLKDIV1 and CLKDIV2. The CLK signal frequency can be f_{XTAL}, $f_{XTAL}/2$, $f_{XTAL}/4$, or $f_{XTAL}/8$. See Table 1 for the frequency generated on the CLK signal given the inputs to CLKDIV1 and CLKDIV2.

Note that CLKDIV1 and CLKDIV2 must not be changed simultaneously; a delay of 10ns minimum between changes is needed. The minimum duration of any state of CLK is eight periods of XTAL1.

The frequency change is synchronous: during a transition of the clock divider, no pulse is shorter than 45% of the smallest period, and the first and last clock pulses about the instant of change have the correct width. When changing the frequency dynamically, the change is effective for only eight periods of XTAL1 after the command.

The f_{XTAL} duty factor depends on the input signal on XTAL1. To reach a 45% to 55% duty factor on CLK, XTAL1 should have a 48% to 52% duty factor with transition times less than 5% of the period.

With a crystal, the duty factor on CLK can be 45% to 55% depending on the circuit layout and on the crystal characteristics and frequency. In other cases, the duty factor on CLK is guaranteed between 45% and 55% of the clock period.

I/O Transceivers

I/O and I/OIN are pulled high with an 11kΩ resistor (I/O to V_{CC} and I/OIN to V_{DD}) in the inactive state. The first side of the transceiver to receive a falling edge becomes the master. When a falling edge is detected (and the master is decided), the detection of falling edges on the line of the other side is disabled; that side then becomes a slave. After a time delay $t_{D(EDGE)}$, an n transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master side asserts a logic 1, a p transistor on the slave side is activated during the time delay t_{PU} and then both sides return to their inactive (pulled up) states. This active pullup provides fast low-to-high transitions. After the duration of t_{PU}, the output voltage depends only on the internal pullup resistor and the load current. Current to and from the card I/O lines is limited internally to 15mA. The maximum frequency on these lines is 1MHz.

Inactive Mode

The DS8313/DS8314 power up with the card interface in the inactive mode. Minimal circuitry is active while waiting for the host to initiate a smart card session.

- All card contacts are inactive (approximately 200Ω to GND).
- The I/OIN pin in the high-impedance state (11kΩ pullup resistor to V_{DD}).
- Voltage generators are stopped.
- XTAL oscillator is running (if included in the device).
- Voltage supervisor is active.
- The internal oscillator is running at its low frequency.

Activation Sequence

After power-on and the reset delay, the host microcontroller can monitor card presence with signals $\overline{OFF}$ and $\overline{CMDVCC}$, as shown in Table 2.

Table 1. Clock Frequency Selection

CLKDIV1	CLKDIV2	f_{CLK}
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

Table 2. Card Presence Indication

$\overline{OFF}$	$\overline{CMDVCC}$	STATUS
High	High	Card present.
Low	High	Card **not** present.

Smart Card Interface

If the card is in the reader (if PRES is active), the host microcontroller can begin an activation sequence (start a card session) by pulling $\overline{CMDVCC}$ low. The following events form an activation sequence (Figure 3):

1) $\overline{CMDVCC}$ is pulled low.
2) The internal oscillator changes to high frequency (t_0).
3) The voltage generator is started (between t_0 and t_1).
4) V_{CC} rises from 0 to 5V, 3V, or 1.8V with a controlled slope ($t_2 = t_1 + 1.5 \times T$). T is 64 times the internal oscillator period (approximately 25µs).
5) I/O pin is enabled ($t_3 = t_1 + 4T$) (they were previously pulled low).
6) The CLK signal is applied to the C3 contact (t_4).
7) RST is enabled ($t_5 = t_1 + 7T$).

To apply the clock to the card interface:

1) Set RSTIN high.
2) Set $\overline{CMDVCC}$ low.
3) Set RSTIN low between t_3 and t_5; CLK will now start.
4) RST stays low until t_5, then RST becomes the copy of RSTIN.
5) RSTIN has no further effect on CLK after t_5.

If the applied clock is not needed, set $\overline{CMDVCC}$ low with RSTIN low. In this case, CLK starts at t_3 (minimum 200ns after the transition on I/O, see Figure 4); after t_5, RSTIN can be set high to obtain an answer to request (ATR) from an inserted smart card. Do not perform activation with RSTIN held permanently high.

Active Mode

When the activation sequence is completed, the card interface is in active mode. The host microcontroller and the smart card exchange data on the I/O lines.

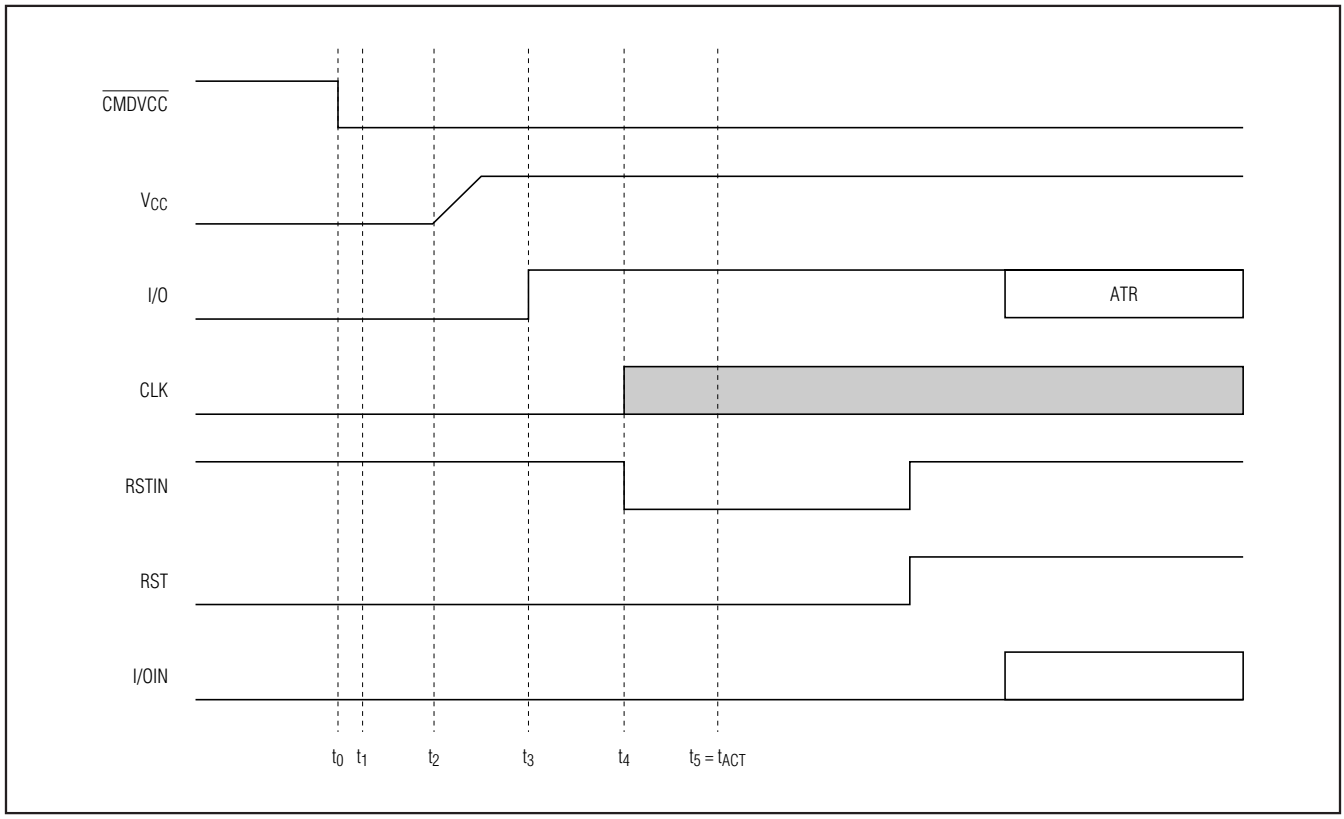


Figure 3. Activation Sequence Using RSTIN and $\overline{CMDVCC}$

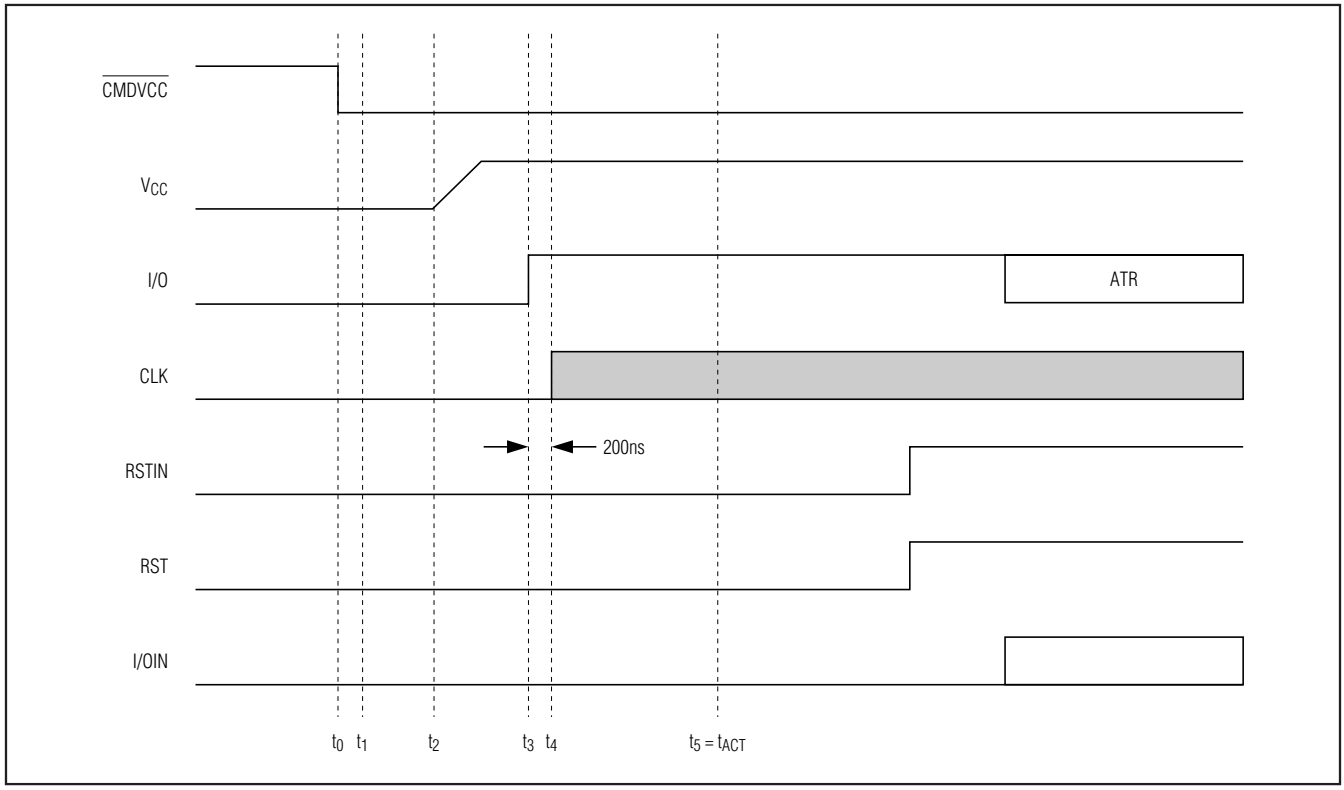


Figure 4. Activation Sequence at t_3

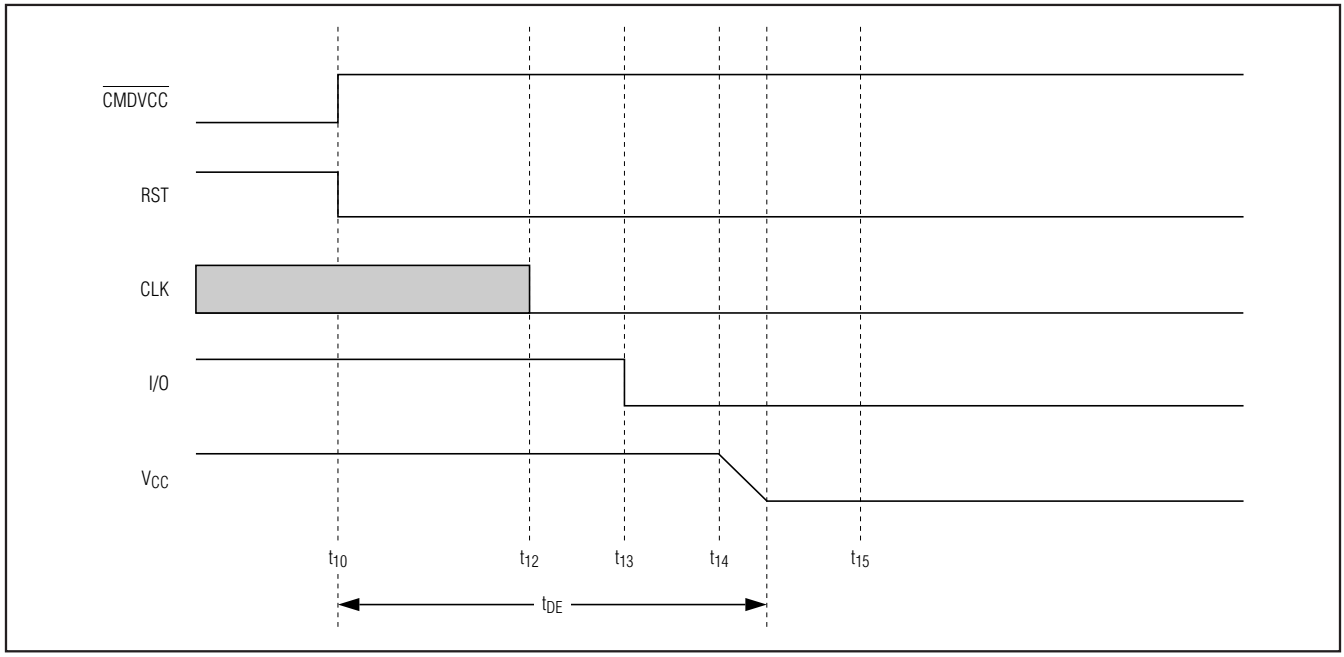


Figure 5. Deactivation Sequence

Smart Card Interface

Deactivation Sequence

When a session is completed, the host microcontroller sets the $\overline{CMDVCC}$ line high to execute an automatic deactivation sequence and returns the card interface to the inactive mode (Figure 5).

1) RST goes low (t_{10}).
2) CLK is held low ($t_{12} = t_{10} + 0.5 \times T$) where T is 64 times the period of the internal oscillator (approximately 25µs).
3) I/O pin is pulled low ($t_{13} = t_{10} + T$).
4) V_{CC} starts to fall ($t_{14} = t_{10} + 1.5 \times T$).
5) When V_{CC} reaches its inactive state, the deactivation sequence is complete (at t_{DE}).
6) All card contacts become low impedance to GND; I/OIN remains at V_{DD} (pulled up through an 11kΩ resistor).
7) The internal oscillator returns to its lower frequency.

Vcc Generator

The V_{CC} generator has a capacity to supply up to 80mA continuously at 5V, 65mA at 3V, and 30mA at 1.8V. An internal overload detector triggers at approximately 120mA. Current samples to the detector are filtered. This allows spurious current pulses (with a duration of a few µs) up to 200mA to be drawn without causing deactivation. The average current must stay below the specified maximum current value. To maintain V_{CC} voltage accuracy, a 100nF capacitor (with an ESR < 100mΩ) should be connected to CGND and placed near the V_{CC} pin, and a 100nF or 220nF capacitor (220nF is the best choice) with the same ESR should be connected to CGND and placed near the smart card reader's C1 contact.

Fault Detection

The following fault conditions are monitored:

- Short-circuit or high current on V_{CC}
- Removal of a card during a transaction
- V_{DD} dropping
- Card voltage generator operating out of the specified values (V_{DDA} too low or current consumption too high)
- Overheating

There are two different cases (Figure 6):

- **$\overline{CMDVCC}$ High Outside a Card Session.** Output $\overline{OFF}$ is low if a card is not in the card reader and high if a card is in the reader. The V_{DD} supply is monitored—a decrease in input voltage generates an internal power-on reset pulse but does not affect the $\overline{OFF}$ signal. Short-circuit and temperature detection is disabled because the card is not powered up.
- **$\overline{CMDVCC}$ Low Within a Card Session.** Output $\overline{OFF}$ goes low when a fault condition is detected, and an emergency deactivation is performed automatically (Figure 7). When the system controller resets $\overline{CMDVCC}$ to high, it may sense the $\overline{OFF}$ level again after completing the deactivation sequence. This distinguishes between a card extraction and a hardware problem ($\overline{OFF}$ goes high again if a card is present). Depending on the connector's card-present switch (normally closed or normally open) and the mechanical characteristics of the switch, bouncing can occur on the PRES signals at card insertion or withdrawal.

The DS8313/DS8314 have a debounce feature with an 8ms typical duration (Figure 6). When a card is inserted, output $\overline{OFF}$ goes high after the debounce time delay. When the card is extracted, an automatic deactivation sequence of the card is performed on the first true/false transition on PRES and output $\overline{OFF}$ goes low.

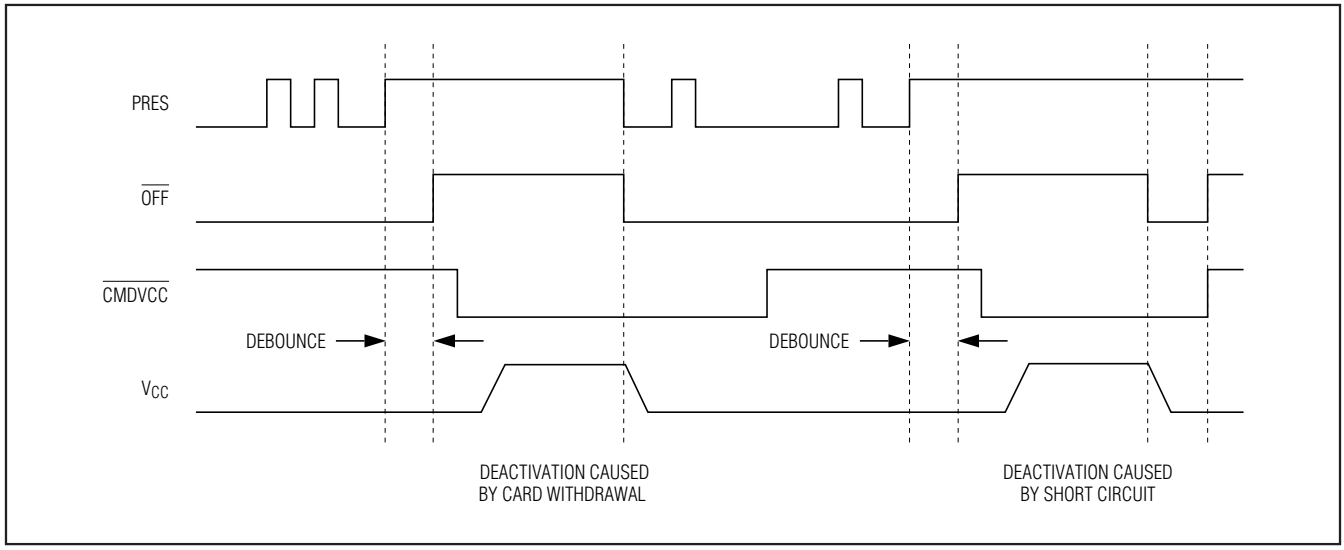


Figure 6. Behavior of PRES, $\overline{OFF}$, $\overline{CMDVCC}$, and V_{CC}

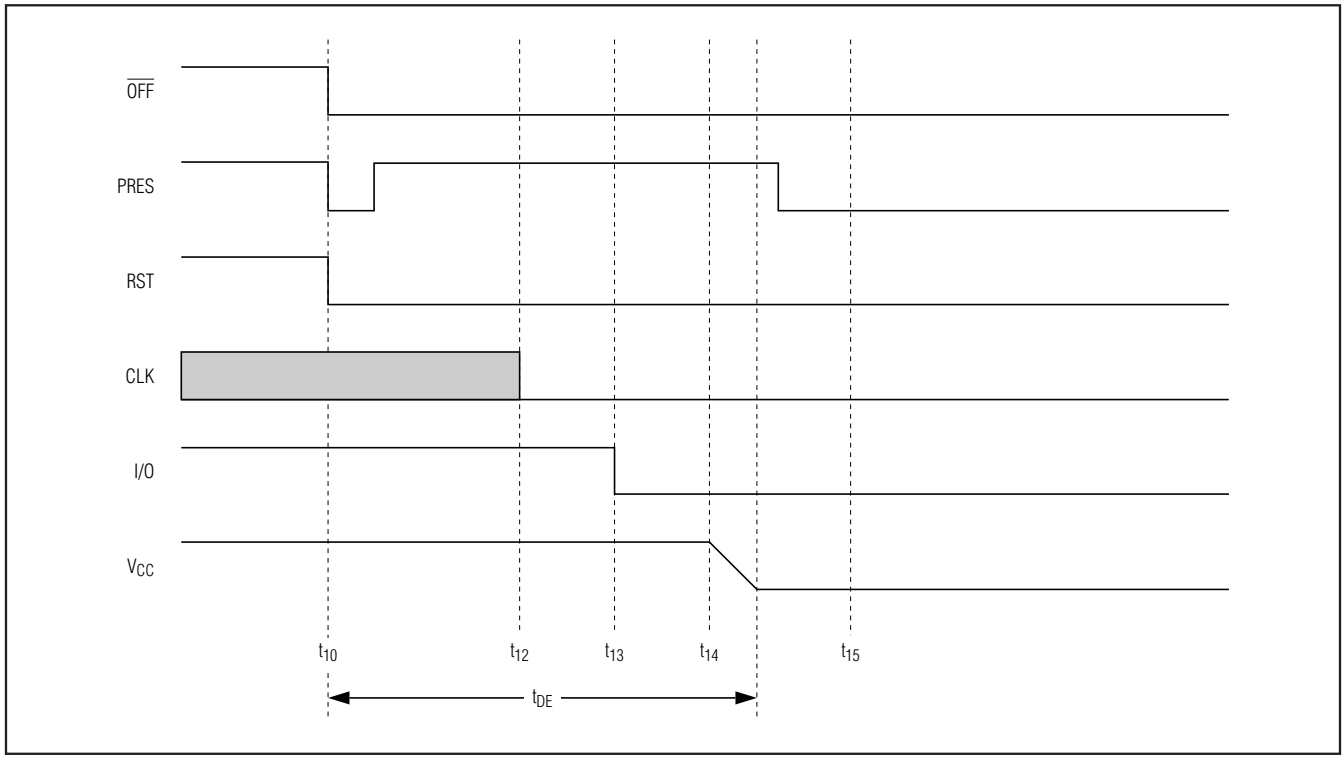


Figure 7. Emergency Deactivation Sequence (Card Extraction)

Smart Card Interface

Stop Mode (Low-Power Mode)

A low-power state, stop mode, can be entered by forcing the $\overline{CMDVCC}$, 5V/$\overline{3V}$, and 1_8V input pins to a logic-high state. Stop mode can only be entered when the smart card interface is inactive. In stop mode, all internal analog circuits are disabled. The $\overline{OFF}$ pin follows the status of the PRES pin. To exit stop mode, change the state of one or more of the three control pins to a logic-low. An internal 220µs (typ) power-up delay and the 8ms PRES debounce delay are in effect and $\overline{OFF}$ is asserted to allow the internal circuitry to stabilize. This prevents smart card access from occurring after leaving the stop mode. Figure 8 shows the control sequence for entering and exiting stop mode. Note that an in-progress deactivation sequence always finishes before the DS8313/DS8314 enter low-power stop mode.

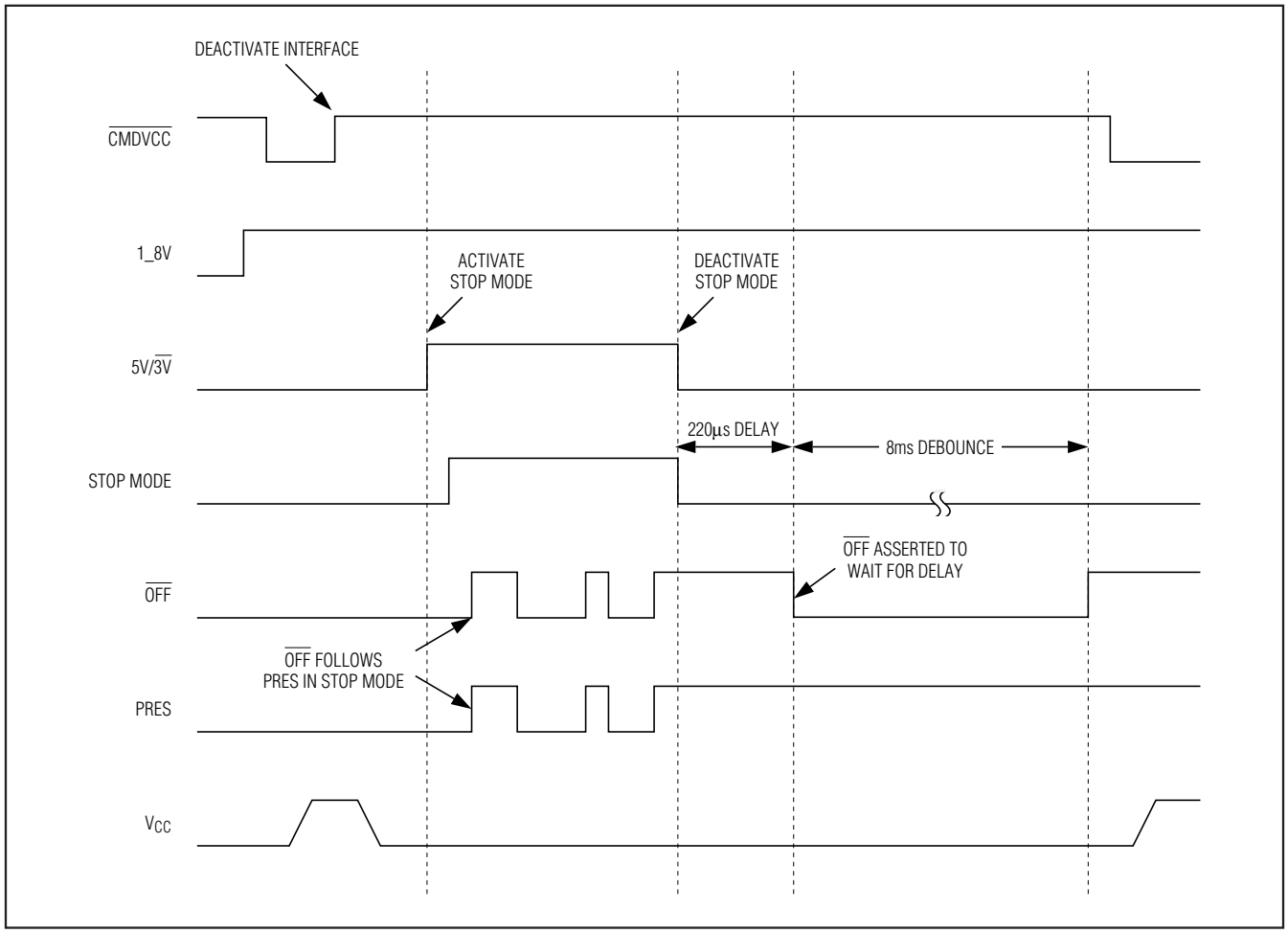


Figure 8. Stop-Mode Sequence

Smart Card Power Select

The DS8313/DS8314 support three smart card V_{CC} voltages: 1.8V, 3V, and 5V. The power select is controlled by the 1_8V and 5V/$\overline{3V}$ signals as shown in Table 3. The 1_8V signal has priority over 5V/$\overline{3V}$. When 1_8V is asserted high, 1.8V is applied to V_{CC} when the smart card is active. When 1_8V is deasserted, 5V/$\overline{3V}$ dictates V_{CC} power range. V_{CC} is 5V if 5V/$\overline{3V}$ is asserted to a logic-high state, and V_{CC} is 3V if 5V/$\overline{3V}$ is pulled to a logic-low state. Care must be exercised when switching from one V_{CC} power selection to the other. If both 1_8V and 5V/$\overline{3V}$ are high with $\overline{CMDVCC}$ high at the same time, the DS8313/DS8314 enter stop mode. To avoid accidental entry into stop mode, the state of 1_8V and 5V/$\overline{3V}$ must not be changed simultaneously. A minimum delay of 100ns should be observed between changing the states of 1_8V and 5V/$\overline{3V}$. See Figure 9 for the recommended sequence of changing the V_{CC} range.

Table 3. V_{CC} Select and Operation Mode

1_8V	5V/$\overline{3V}$	$\overline{CMDVCC}$	V_{CC} SELECT (V)	CARD INTERFACE STATUS
0	0	0	3	Activated
0	0	1	3	Inactivated
0	1	0	5	Activated
0	1	1	5	Inactivated
1	0	0	1.8	Activated
1	0	1	1.8	Inactivated
1	1	0	1.8	Reserved (Activated)
1	1	1	1.8	Not Applicable—Stop Mode

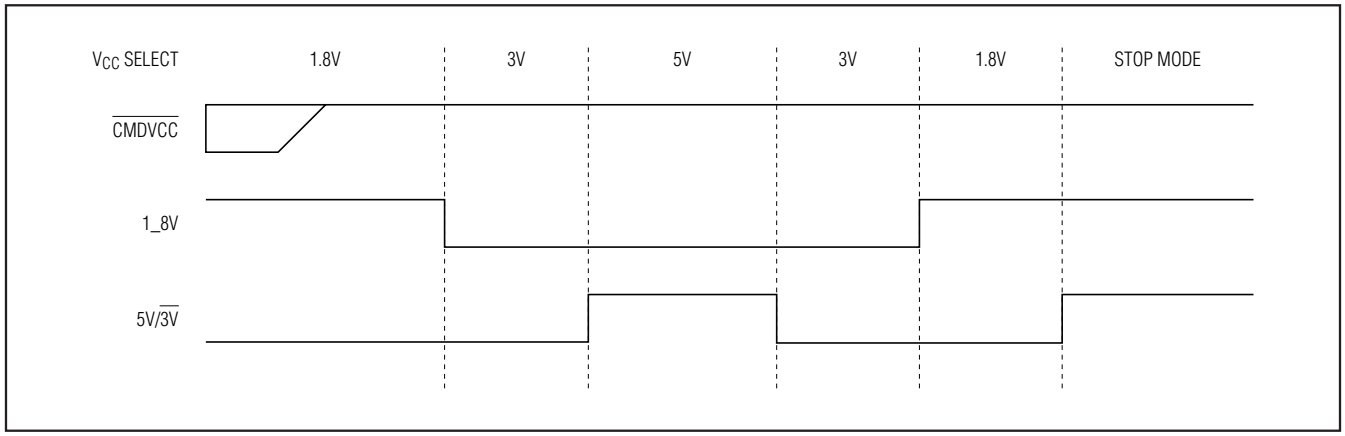


Figure 9. Smart Card Power Select

Smart Card Interface

Applications Information

Performance can be affected by the layout of the application. For example, an additional cross-capacitance of 1pF between card reader contacts C2 (RST) and C3 (CLK) or C2 (RST) and C7 (I/O) can cause contact C2 to be polluted with high-frequency noise from C3 (or C7). In this case, include a 100pF capacitor between contacts C2 and CGND.

Application recommendations include the following:

- Ensure there is ample ground area around the DS8313/DS8314 and the connector; place the DS8313/DS8314 very near to the connector; decouple the V_{DD} and V_{DDA} lines separately. These lines are best positioned under the connector.
- The device and the host microcontroller must use the same V_{DD} supply. Pins CLKDIV1, CLKDIV2, $\overline{RSTIN}$, PRES, I/OIN, 5V/$\overline{3V}$, 1_8V, $\overline{CMDVCC}$, and $\overline{OFF}$ are referenced to V_{DD}; if pin XTAL1 is to be driven by an external clock, also reference this pin to V_{DD}.
- Trace C3 (CLK) should be placed as far as possible from the other traces.
- The trace connecting CGND to C5 (GND) should be straight (the two capacitors on C1 (V_{CC}) should be connected to this ground trace).
- Avoid ground loops between CGND and GND.
- Decouple V_{DDA} and V_{DD} separately. If two supplies are the same in the application, they should be connected in a star on the main trace

With all these layout precautions, noise should be kept to an acceptable level and jitter on C3 (CLK) should be less than 100ps. Reference layouts are available on request.

Technical Support

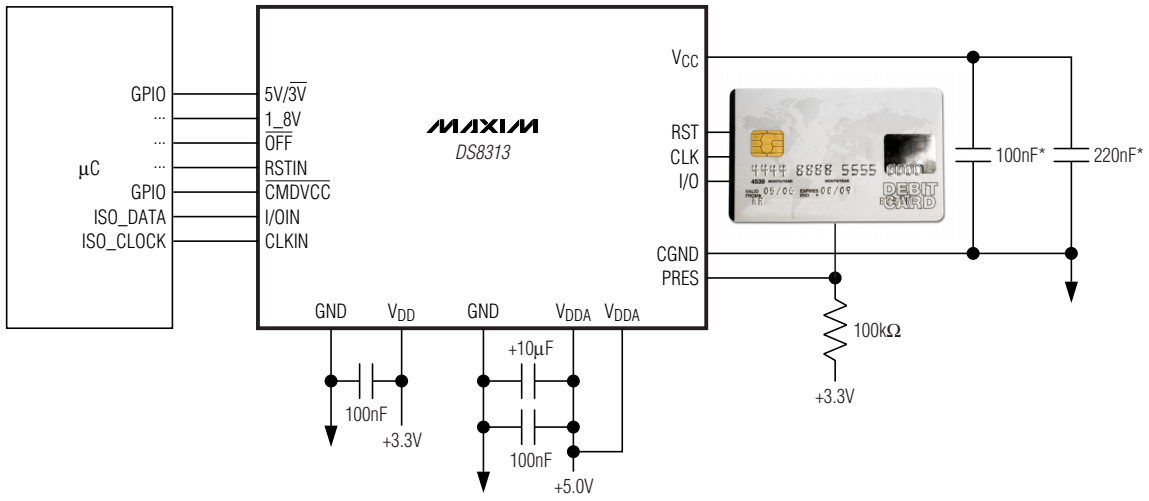
For technical support, go to **https://support.maxim-ic.com/micro**.

Selector Guide

PART	LOW STOP-MODE POWER	LOW ACTIVE-MODE POWER	PRES POLARITY	V_{DDA} INPUTS	PIN-PACKAGE
DS8313-RRX+	Yes	Yes	Positive	2	28 SO
DS8313L-RRX+*	Yes	Yes	Negative	2	28 SO
DS8314-RRX+*	Yes	Yes	Positive	1	28 SO
DS8314L-RRX+*	Yes	Yes	Negative	1	28 SO

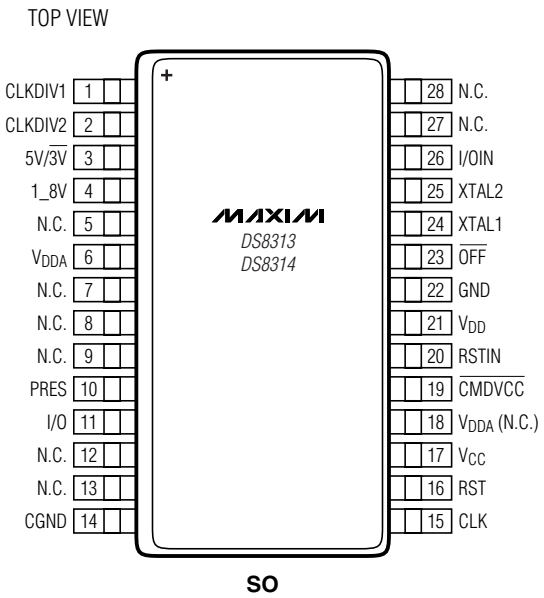
Note: *Contact the factory for availability of other variants and package options.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*

Typical Application Circuit



*PLACE A 100nF CAPACITOR CLOSE TO DS8313 AND PLACE A 220nF CAPACITOR CLOSE TO CARD CONTACT.

Pin Configuration



() INDICATES DS8314 ONLY.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 SO	W28+1	21-0042

Smart Card Interface

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/09	Initial release.	—
1	5/09	Removed the TSSOP package variant from the *General Description*, *Ordering Information*, *Selector Guide*, and *Package Information* sections.	1, 16, 17
		Changed “(IEC)” in the *Features* section to “(HBM)” for the “±8kV (min) ESD (HBM) Protection on Card Interfaces” bullet.	1

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