

Fractional-N Phase-Locked Loop Surface Mount Module

Applications

- Fixed Wireless
- Satellite Communications
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Application Notes

- AN-107: Manual Soldering Technique
- AN-202: Programming Z-COMM PLLs

Performance Specifications

	Min	Typ	Max	Units
Frequency	2000		2300	MHz
Phase Noise @ 10 kHz offset (1 Hz BW)		-90		dBc/Hz
Harmonic Suppression (2nd)		-20		dBc
Spurious Suppression		-65		dBc
Power Output	0	5	10	dBm
Load Impedance		50		Ω
Step Size		1000		kHz
Phase Detector Frequency		2500		kHz
Settling Time		100		mS
Charge Pump Output Current		1250		μ A
Operating Temperature Range	-40		85	$^{\circ}$ C
Package Style		PLL-24S1		

Power Supply Requirements

	Min	Typ	Max	Units
Supply Voltage 1: PLL (Vcc, nom)		5		Vdc
Supply Voltage 2: VCO (Vcc, nom)		15		Vdc
Supply Current 1: PLL (Icc, typ)		23		mA
Supply Current 2: VCO (Icc, typ)		25		mA

Reference Oscillator Signal

	Min	Typ	Max	Units
Frequency		10		MHz
Phase Noise @1 kHz Offset		-145		dBc/Hz

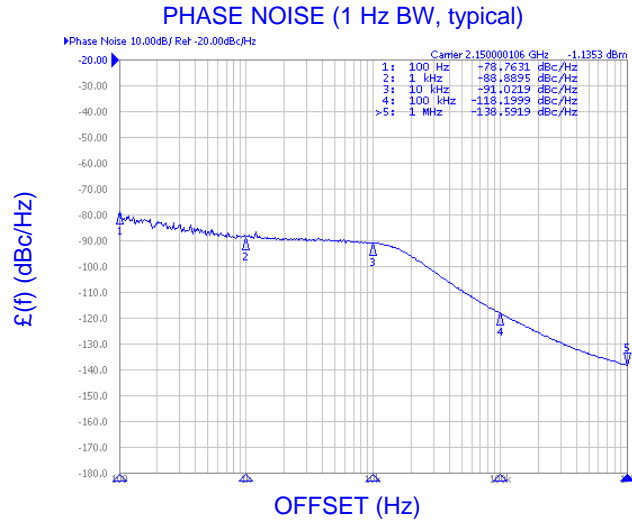
Additional Notes

Reference Oscillator Signal: $10\text{ MHz} < f_{\text{osc}} < 250\text{ MHz}$. Frequency Synthesizer: Analog Devices - ADF4156.
Smaller step sizes are possible with smaller PDF.

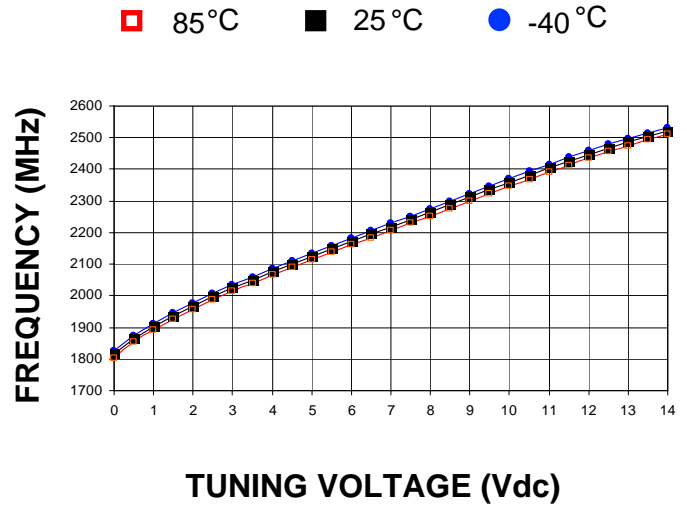
LFSuffix = RoHS Compliant. All specifications are subject to change without notice.

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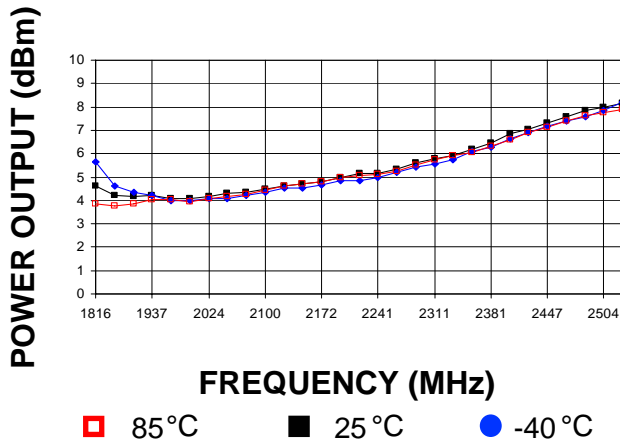
Phase Noise, typ.



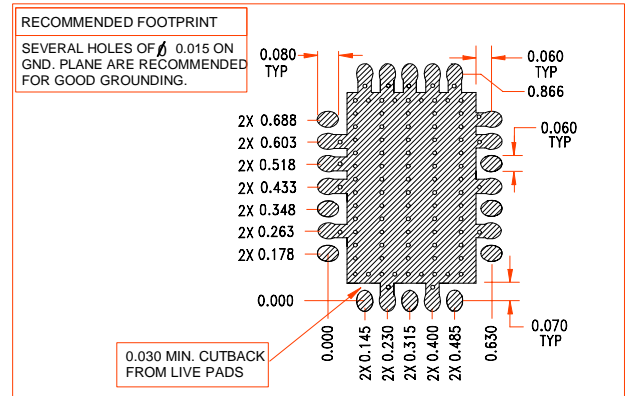
Tuning Curve, typ.



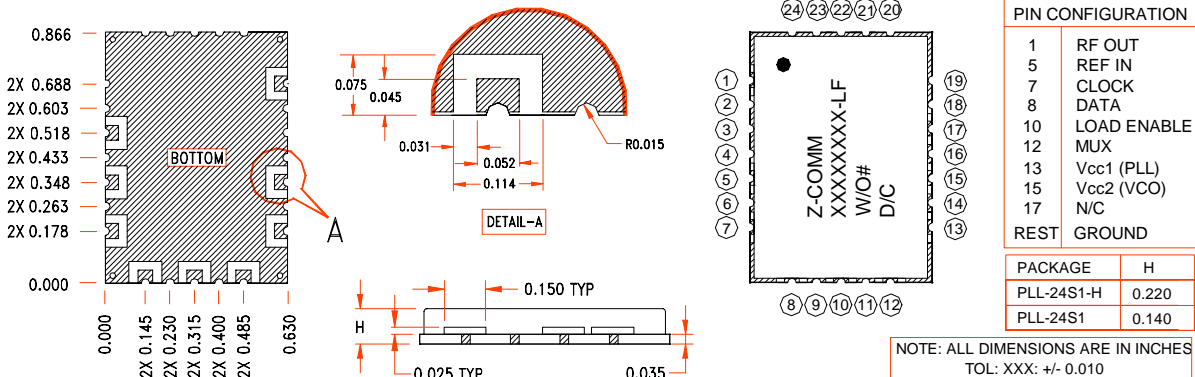
Power Curve, typ.



Footprint



Physical Dimensions



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