

## Diagonal 4.5mm (Type 1/4) Progressive Scan CCD Image Sensor with Square Pixel for B/W Cameras

### Description

The ICX098AL is a diagonal 4.5mm (Type 1/4) interline CCD solid-state image sensor with a square pixel array which supports VGA format. Progressive scan allows all pixels signals to be output independently within approximately 1/30 second. Also, the adoption of monitoring mode supports 60 frame/s. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without a mechanical shutter. Further, high sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip is suitable for applications such as second-dimensional bar-code reader, PC input cameras, etc.

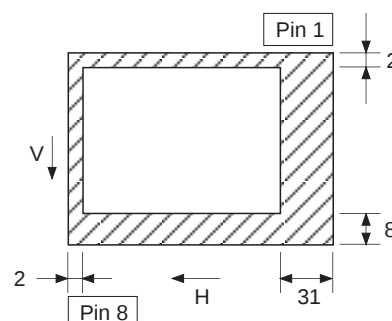
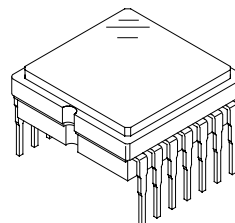
### Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High horizontal and vertical resolution (both approx. 480TV-lines) still image without a mechanical shutter.
- Supports monitoring mode
- Square pixel
- Supports VGA format
- Horizontal drive frequency: 12.27MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- High resolution, high sensitivity, low dark current
- Continuous variable-speed shutter
- Low smear
- Excellent antiblooming characteristics
- Horizontal register: 3.3V drive
- 14-pin high precision plastic package (enables dual-surface standard)

### Device Structure

- Interline CCD image sensor
- Image size: Diagonal 4.5mm (Type 1/4)
- Number of effective pixels: 659 (H) × 494 (V) approx. 330K pixels
- Total number of pixels: 692 (H) × 504 (V) approx. 350K pixels
- Chip size: 4.60mm (H) × 3.97mm (V)
- Unit cell size: 5.6μm (H) × 5.6μm (V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 31 pixels  
Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 16  
Vertical 5
- Substrate material: Silicon

14 pin DIP (Plastic)

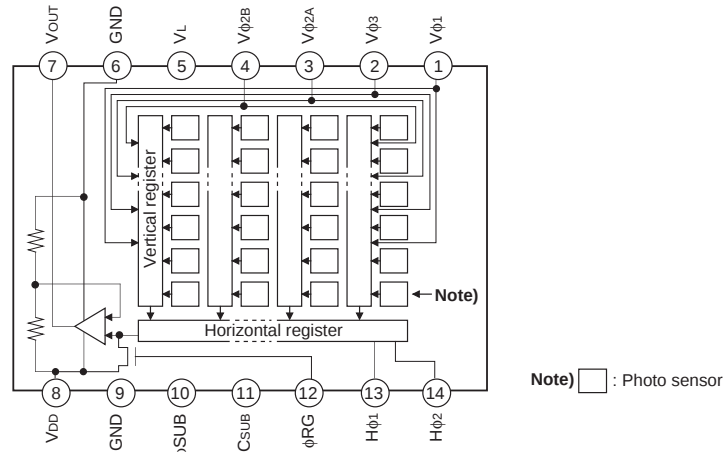


Optical black position  
(Top View)

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## Block Diagram and Pin Configuration

(Top View)



## Pin Description

| Pin No. | Symbol           | Description                      | Pin No. | Symbol           | Description                        |
|---------|------------------|----------------------------------|---------|------------------|------------------------------------|
| 1       | V $\phi$ 1       | Vertical register transfer clock | 8       | V <sub>DD</sub>  | Supply voltage                     |
| 2       | V $\phi$ 3       | Vertical register transfer clock | 9       | GND              | GND                                |
| 3       | V $\phi$ 2A      | Vertical register transfer clock | 10      | $\phi$ SUB       | Substrate clock                    |
| 4       | V $\phi$ 2B      | Vertical register transfer clock | 11      | C <sub>SUB</sub> | Substrate bias <sup>*1</sup>       |
| 5       | V <sub>L</sub>   | Protective transistor bias       | 12      | $\phi$ RG        | Reset gate clock                   |
| 6       | GND              | GND                              | 13      | H $\phi$ 1       | Horizontal register transfer clock |
| 7       | V <sub>OUT</sub> | Signal output                    | 14      | H $\phi$ 2       | Horizontal register transfer clock |

<sup>\*1</sup> DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1 $\mu$ F.

## Absolute Maximum Ratings

| Item                     |                                                                        | Ratings     | Unit | Remarks       |
|--------------------------|------------------------------------------------------------------------|-------------|------|---------------|
| Against $\phi$ SUB       | V <sub>DD</sub> , V <sub>OUT</sub> , $\phi$ RG – $\phi$ SUB            | –40 to +10  | V    |               |
|                          | V $\phi$ 2A, V $\phi$ 2B – $\phi$ SUB                                  | –50 to +15  | V    |               |
|                          | V $\phi$ 1, V $\phi$ 3, V <sub>L</sub> – $\phi$ SUB                    | –50 to +0.3 | V    |               |
|                          | H $\phi$ 1, H $\phi$ 2, GND – $\phi$ SUB                               | –40 to +0.3 | V    |               |
|                          | C <sub>SUB</sub> – $\phi$ SUB                                          | –25 to      | V    |               |
| Against GND              | V <sub>DD</sub> , V <sub>OUT</sub> , $\phi$ RG, C <sub>SUB</sub> – GND | –0.3 to +18 | V    |               |
|                          | V $\phi$ 1, V $\phi$ 2A, V $\phi$ 2B, V $\phi$ 3 – GND                 | –10 to +18  | V    |               |
|                          | H $\phi$ 1, H $\phi$ 2 – GND                                           | –10 to +5   | V    |               |
| Against V <sub>L</sub>   | V $\phi$ 2A, V $\phi$ 2B – V <sub>L</sub>                              | –0.3 to +28 | V    |               |
|                          | V $\phi$ 1, V $\phi$ 3, H $\phi$ 1, H $\phi$ 2, GND – V <sub>L</sub>   | –0.3 to +15 | V    |               |
| Between input clock pins | Voltage difference between vertical clock input pins                   | to +15      | V    | <sup>*2</sup> |
|                          | H $\phi$ 1 – H $\phi$ 2                                                | –5 to +5    | V    |               |
|                          | H $\phi$ 1, H $\phi$ 2 – V $\phi$ 3                                    | –13 to +13  | V    |               |
| Storage temperature      |                                                                        | –30 to +80  | °C   |               |
| Operating temperature    |                                                                        | –10 to +60  | °C   |               |

<sup>\*2</sup> +24V (Max.) when clock width < 10 $\mu$ s, clock duty factor < 0.1%.

**Bias Conditions**

| Item                       | Symbol           | Min.  | Typ. | Max.  | Unit | Remarks |
|----------------------------|------------------|-------|------|-------|------|---------|
| Supply voltage             | V <sub>DD</sub>  | 14.55 | 15.0 | 15.45 | V    |         |
| Protective transistor bias | V <sub>L</sub>   | *1    |      |       |      |         |
| Substrate clock            | φ <sub>SUB</sub> | *2    |      |       |      |         |
| Reset gate clock           | φ <sub>RG</sub>  | *2    |      |       |      |         |

\*1 V<sub>L</sub> setting is the V<sub>VL</sub> voltage of the vertical transfer clock waveform, or the same power supply as the V<sub>L</sub> power supply for the V driver should be used.

\*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

**DC Characteristics**

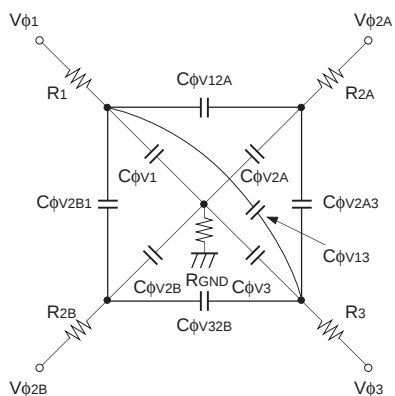
| Item           | Symbol          | Min. | Typ. | Max. | Unit | Remarks |
|----------------|-----------------|------|------|------|------|---------|
| Supply current | I <sub>DD</sub> |      | 6.0  |      | mA   |         |

**Clock Voltage Conditions**

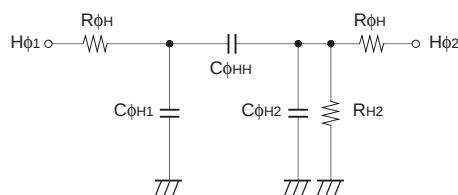
| Item                              | Symbol                                                                         | Min.  | Typ. | Max.  | Unit | Waveform diagram | Remarks                                                    |
|-----------------------------------|--------------------------------------------------------------------------------|-------|------|-------|------|------------------|------------------------------------------------------------|
| Readout clock voltage             | V <sub>VT</sub>                                                                | 14.55 | 15.0 | 15.45 | V    | 1                |                                                            |
| Vertical transfer clock voltage   | V <sub>VH02A</sub>                                                             | -0.05 | 0    | 0.05  | V    | 2                | V <sub>VH</sub> = V <sub>VH02A</sub>                       |
|                                   | V <sub>VH1</sub> , V <sub>VH2A</sub> ,<br>V <sub>VH2B</sub> , V <sub>VH3</sub> | -0.2  | 0    | 0.05  | V    | 2                |                                                            |
|                                   | V <sub>VL1</sub> , V <sub>VL2A</sub> ,<br>V <sub>VL2B</sub> , V <sub>VL3</sub> | -5.8  | -5.5 | -5.2  | V    | 2                | V <sub>VL</sub> = (V <sub>VL1</sub> + V <sub>VL3</sub> )/2 |
|                                   | V <sub>φ1</sub> , V <sub>φ2A</sub> ,<br>V <sub>φ2B</sub> , V <sub>φ3</sub>     | 5.2   | 5.5  | 5.8   | V    | 2                |                                                            |
|                                   | V <sub>VL1</sub> - V <sub>VL3</sub>                                            |       |      | 0.1   | V    | 2                |                                                            |
|                                   | V <sub>VHH</sub>                                                               |       |      | 0.3   | V    | 2                | High-level coupling                                        |
|                                   | V <sub>VHL</sub>                                                               |       |      | 1.0   | V    | 2                | High-level coupling                                        |
|                                   | V <sub>VLH</sub>                                                               |       |      | 0.5   | V    | 2                | Low-level coupling                                         |
|                                   | V <sub>VLL</sub>                                                               |       |      | 0.5   | V    | 2                | Low-level coupling                                         |
| Horizontal transfer clock voltage | V <sub>φH</sub>                                                                | 3.0   | 3.3  | 5.25  | V    | 3                |                                                            |
|                                   | V <sub>HL</sub>                                                                | -0.05 | 0    | 0.05  | V    | 3                |                                                            |
| Reset gate clock voltage          | V <sub>φRG</sub>                                                               | 3.0   | 3.3  | 5.5   | V    | 4                |                                                            |
|                                   | V <sub>RGLH</sub> - V <sub>RGLL</sub>                                          |       |      | 0.4   | V    | 4                | Low-level coupling                                         |
|                                   | V <sub>RGL</sub> - V <sub>RGLm</sub>                                           |       |      | 0.5   | V    | 4                | Low-level coupling                                         |
| Substrate clock voltage           | V <sub>φSUB</sub>                                                              | 19.75 | 20.5 | 21.25 | V    | 5                |                                                            |

## Clock Equivalent Circuit Constant

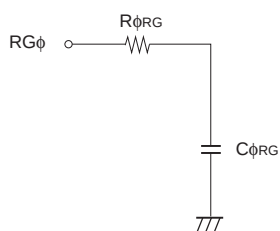
| Item                                                  | Symbol                   | Min. | Typ. | Max. | Unit       | Remarks |
|-------------------------------------------------------|--------------------------|------|------|------|------------|---------|
| Capacitance between vertical transfer clock and GND   | $C\phi V1$               |      | 1200 |      | pF         |         |
|                                                       | $C\phi V2A, C\phi V2B$   |      | 470  |      | pF         |         |
|                                                       | $C\phi V3$               |      | 2200 |      | pF         |         |
| Capacitance between vertical transfer clocks          | $C\phi V12A, C\phi V2B1$ |      | 470  |      | pF         |         |
|                                                       | $C\phi V2A3, C\phi V32B$ |      | 390  |      | pF         |         |
|                                                       | $C\phi V13$              |      | 10   |      | pF         |         |
| Capacitance between horizontal transfer clock and GND | $C\phi H1, C\phi H2$     |      | 22   |      | pF         |         |
| Capacitance between horizontal transfer clocks        | $C\phi HH$               |      | 68   |      | pF         |         |
| Capacitance between reset gate clock and GND          | $C\phi RG$               |      | 3    |      | pF         |         |
| Capacitance between substrate clock and GND           | $C\phi SUB$              |      | 220  |      | pF         |         |
|                                                       |                          |      |      |      |            |         |
|                                                       |                          |      |      |      |            |         |
| Vertical transfer clock series resistor               | $R1$                     |      | 20   |      | $\Omega$   |         |
|                                                       | $R2A, R2B$               |      | 43   |      | $\Omega$   |         |
|                                                       | $R3$                     |      | 36   |      | $\Omega$   |         |
| Vertical transfer clock ground resistor               | $R_{GND}$                |      | 43   |      | $\Omega$   |         |
| Horizontal transfer clock series resistor             | $R\phi H$                |      | 12   |      | $\Omega$   |         |
| Horizontal transfer clock ground resistor             | $R_{H2}$                 |      | 30   |      | k $\Omega$ |         |
| Reset gate clock series resistor                      | $R\phi RG$               |      | 62   |      | $\Omega$   |         |



Vertical transfer clock equivalent circuit



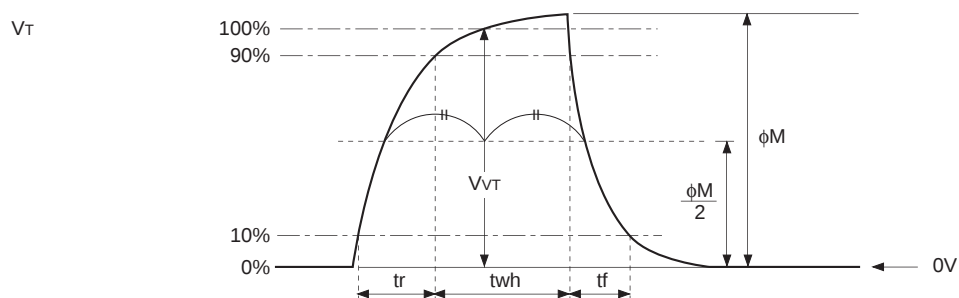
Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit

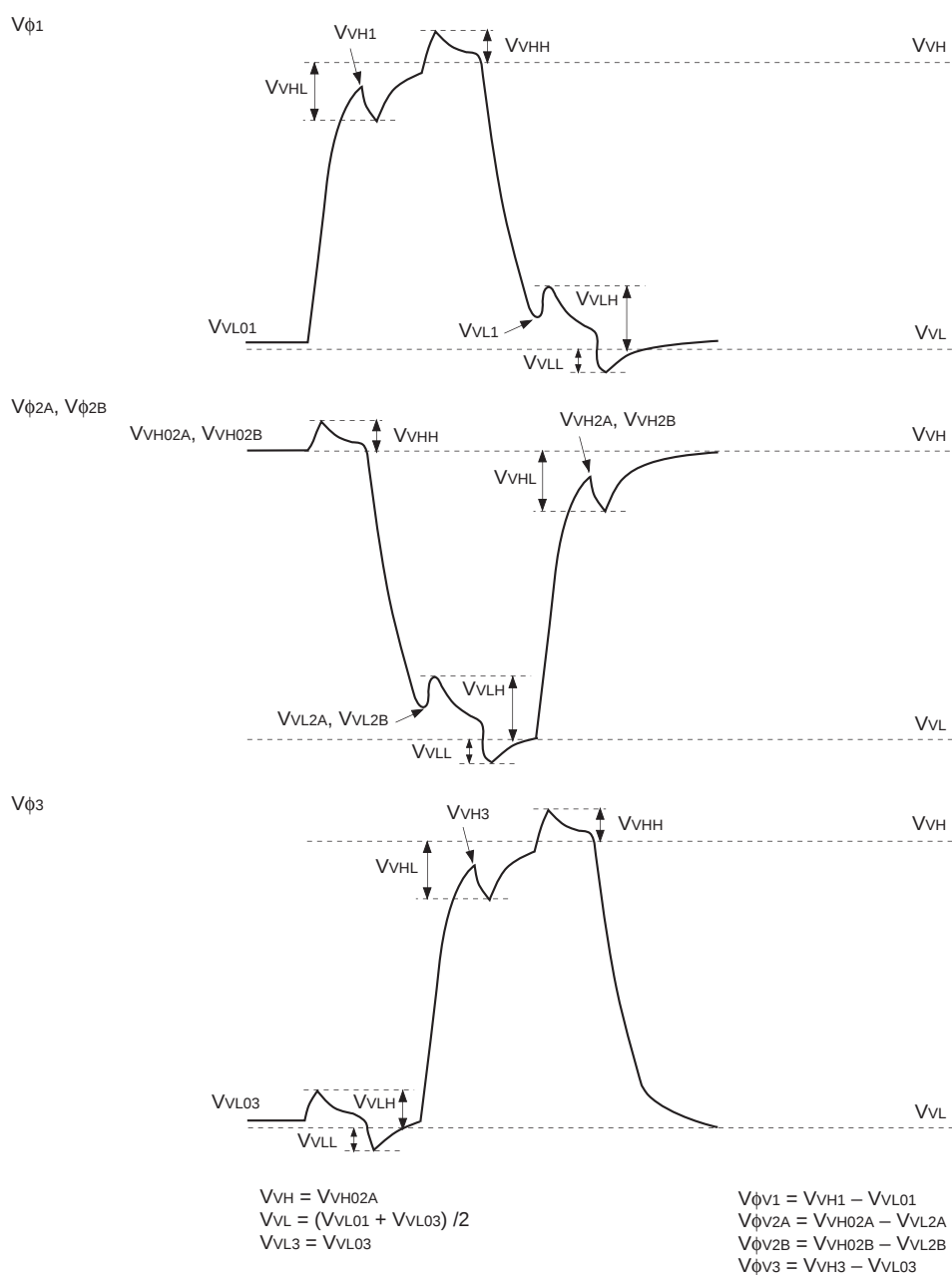
## Drive Clock Waveform Conditions

### (1) Readout clock waveform

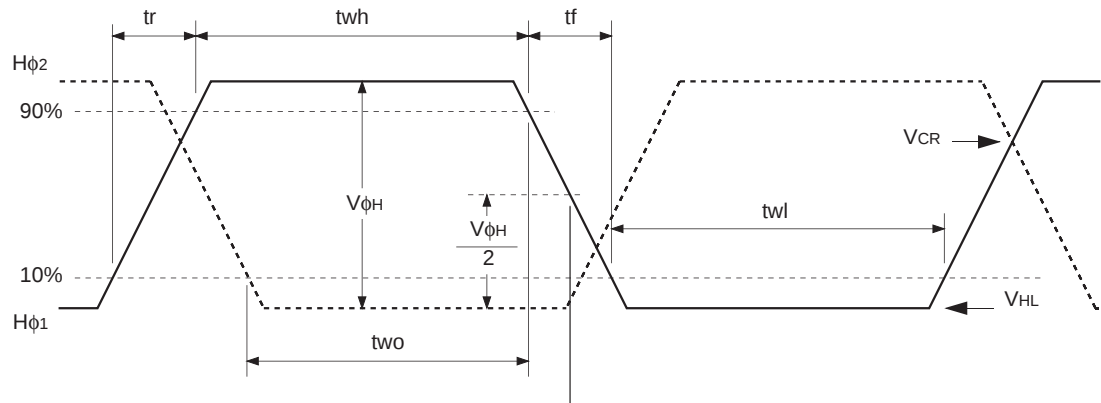


Note) Readout clock is used by composing vertical transfer clocks  $V\phi_{2A}$  and  $V\phi_{2B}$ .

### (2) Vertical transfer clock waveform

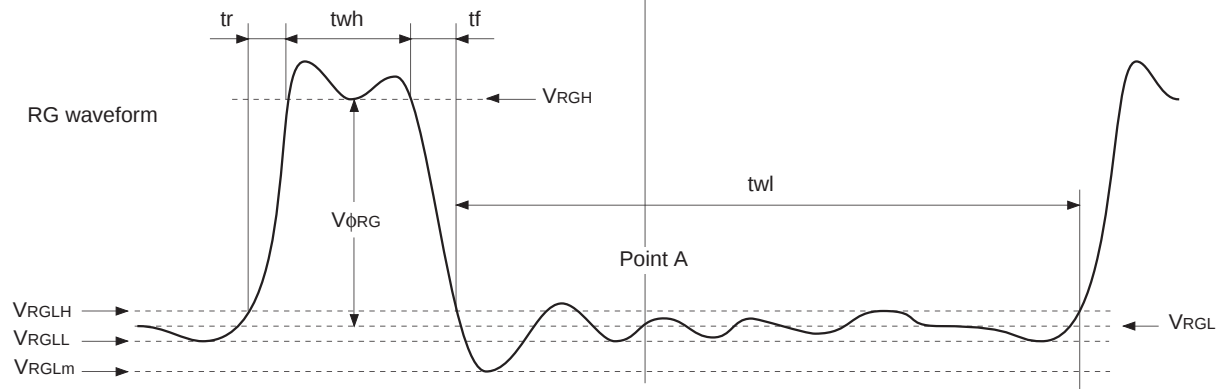


### (3) Horizontal transfer clock waveform



Cross-point voltage for the  $H\phi_1$  rising side of the horizontal transfer clocks  $H\phi_1$  and  $H\phi_2$  waveforms is  $V_{CR}$ . The overlap period for  $t_{wh}$  and  $t_{wl}$  of horizontal transfer clocks  $H\phi_1$  and  $H\phi_2$  is  $two$ .

### (4) Reset gate clock waveform



$V_{RGLH}$  is the maximum value and  $V_{RGLL}$  is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition,  $V_{RGL}$  is the average value of  $V_{RGLH}$  and  $V_{RGLL}$ .

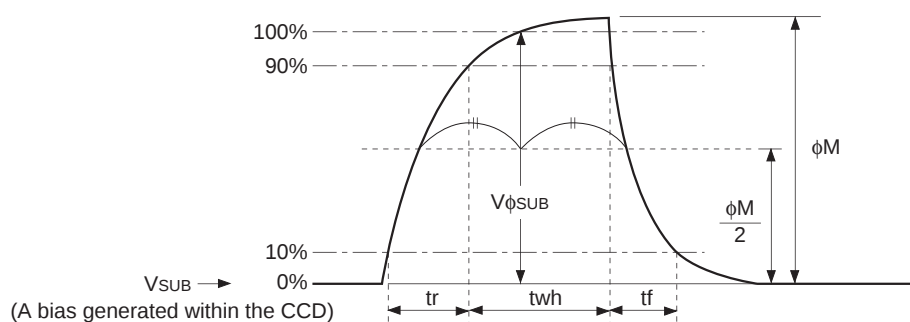
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming  $V_{RGH}$  is the minimum value during the interval  $t_{wh}$ , then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is  $V_{RGLm}$ .

### (5) Substrate clock waveform



## Clock Switching Characteristics

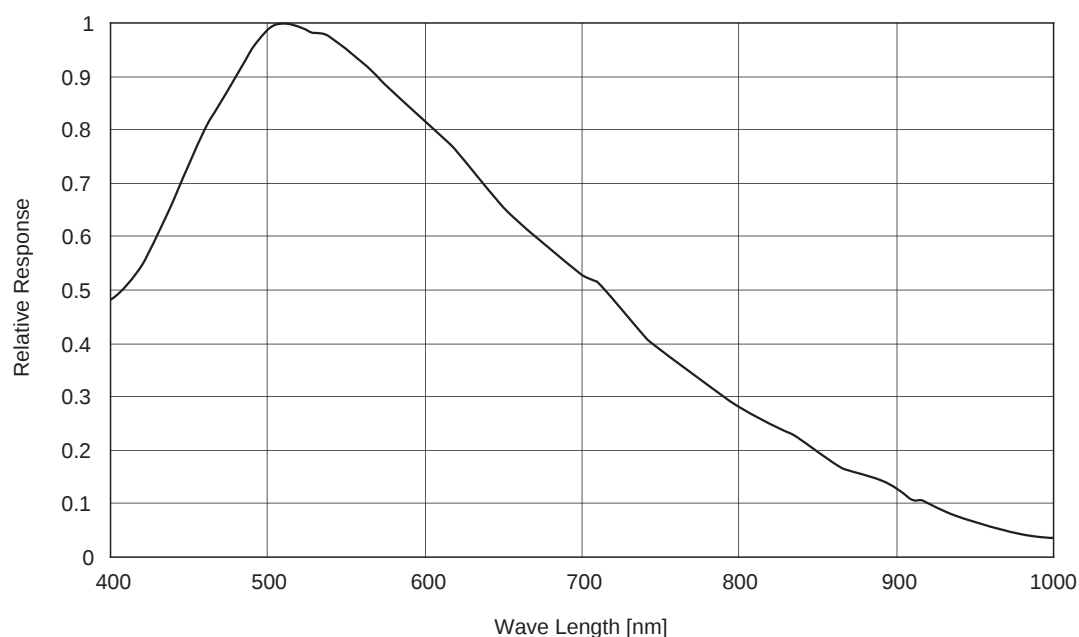
| Item                      |                                   | Symbol                                                                  | twh  |      |      | twl  |      |      | tr   |      |      | tf   |      |      | Unit | Remarks             |
|---------------------------|-----------------------------------|-------------------------------------------------------------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|---------------------|
|                           |                                   |                                                                         | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. |      |                     |
| Readout clock             |                                   | V <sub>T</sub>                                                          | 2.3  | 2.5  |      |      |      |      |      | 0.5  |      |      | 0.5  |      | μs   | During readout      |
| Vertical transfer clock   |                                   | V <sub>φ1</sub> , V <sub>φ2A</sub> , V <sub>φ2B</sub> , V <sub>φ3</sub> |      |      |      |      |      |      |      |      |      | 15   |      | 350  | ns   | *1                  |
| Horizontal transfer clock | During imaging                    | H <sub>φ1</sub>                                                         | 25.5 | 30.5 |      | 28   | 33   |      |      | 9    | 16.5 |      | 9    | 16.5 | ns   | *2                  |
|                           |                                   | H <sub>φ2</sub>                                                         | 28   | 33   |      | 25.5 | 30.5 |      |      | 9    | 14   |      | 9    | 14   |      |                     |
|                           | During parallel-serial conversion | H <sub>φ1</sub>                                                         |      |      |      |      |      |      |      | 0.01 |      |      | 0.01 |      | μs   |                     |
|                           |                                   | H <sub>φ2</sub>                                                         |      |      |      |      |      |      |      | 0.01 |      |      | 0.01 |      |      |                     |
| Reset gate clock          |                                   | φ <sub>RG</sub>                                                         | 11   | 12   |      |      | 63.5 |      |      | 3    |      |      | 3    |      | ns   |                     |
| Substrate clock           |                                   | φ <sub>SUB</sub>                                                        | 1.5  | 1.8  |      |      |      |      |      |      | 0.5  |      |      | 0.5  | μs   | During drain charge |

\*1 When vertical transfer clock driver CXD1267AN is used.

\*2  $t_f \geq t_r - 2\text{ns}$ , and the cross-point voltage ( $V_{CR}$ ) for the  $H_{\phi 1}$  rising side of the  $H_{\phi 1}$  and  $H_{\phi 2}$  waveforms must be at least  $V_{\phi H}/2$  [V].

| Item                      | Symbol                   | two  |      |      | Unit | Remarks |
|---------------------------|--------------------------|------|------|------|------|---------|
|                           |                          | Min. | Typ. | Max. |      |         |
| Horizontal transfer clock | $H_{\phi 1}, H_{\phi 2}$ | 21.5 | 25.5 |      | ns   |         |

## Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

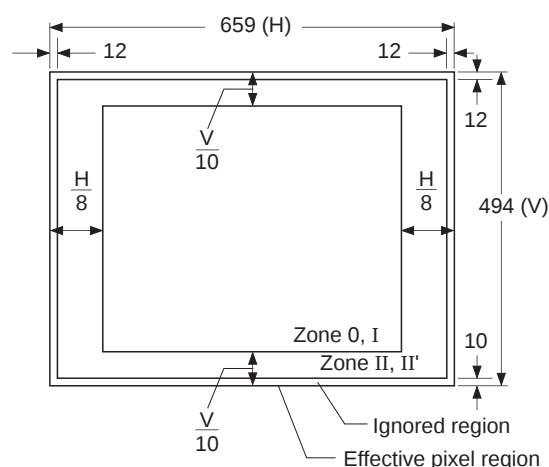


# Image Sensor Characteristics

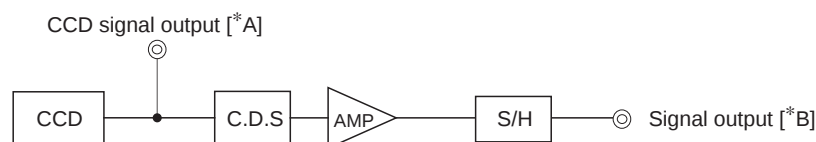
(Ta = 25°C)

| Item                 | Symbol       | Min. | Typ.  | Max.   | Unit | Measurement method | Remarks                 |
|----------------------|--------------|------|-------|--------|------|--------------------|-------------------------|
| Sensitivity          | S            | 480  | 600   |        | mV   | 1                  | 1/30s accumulation mode |
| Saturation signal    | Vsat         | 500  |       |        | mV   | 2                  | Ta = 60°C               |
| Smear                | Sm           |      | 0.001 | 0.0025 | %    | 3                  | 1/30s accumulation mode |
| Video signal shading | SH           |      |       | 20     | %    | 4                  | Zone 0 and I            |
|                      |              |      |       | 25     | %    | 4                  | Zone 0 to II'           |
| Dark signal          | Vdt          |      |       | 4      | mV   | 5                  | Ta = 60°C               |
| Dark signal shading  | $\Delta Vdt$ |      |       | 1      | mV   | 6                  | Ta = 60°C               |
| Lag                  | Lag          |      |       | 0.5    | %    | 7                  |                         |

## Zone Definition of Video Signal Shading



## Measurement System

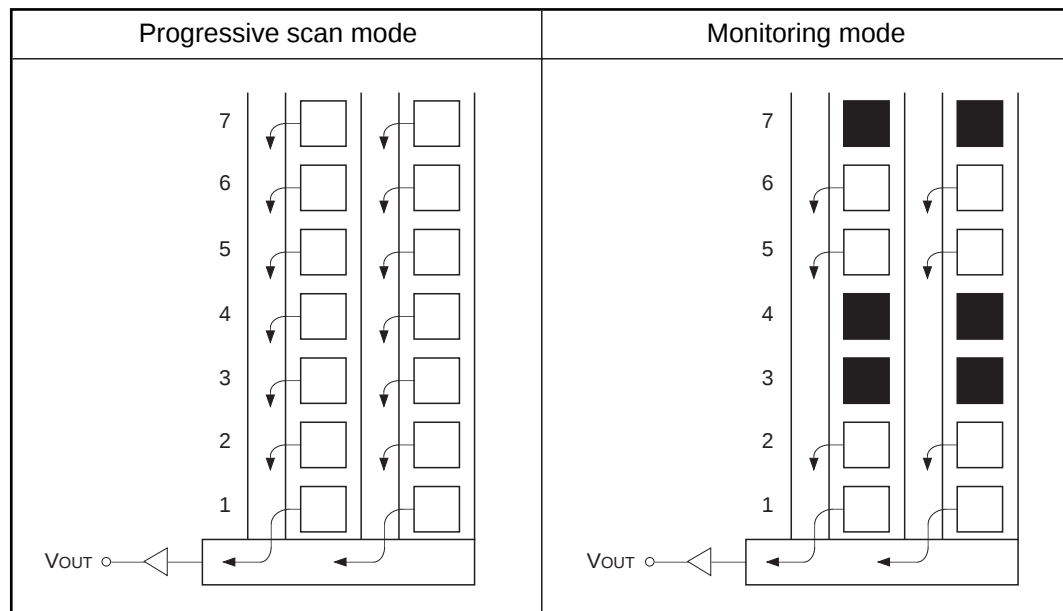


**Note)** Adjust the amplifier gain so that the gain between [\*A] and [\*B] equals 1.

## Image Sensor Characteristics Measurement Method

### ◎ Readout modes

The diagram below shows the output methods for the following two readout modes.



**Note)** Blacked out portions in the diagram indicate pixels which are not read out.

#### 1. Progressive scan mode

In this mode, all pixel signals are output in non-interlace format in 1/30s.

The vertical resolution is approximately 480TV-lines and all pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

#### 2. Monitoring mode

The signals for all effective areas are output in approximately 1/60s by repeating readout pixels and non-readout pixels every two lines. The vertical resolution is approximately 240TV-lines.

This readout mode emphasizes processing speed over vertical resolution.

## © Measurement conditions

- 1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
- 2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value measured at point [\*B] of the measurement system.

## © Definition of standard imaging conditions

- 1) Standard imaging condition I:  
Use a pattern box (luminance : 706cd/m<sup>2</sup>, color temperature of 3200K halogen source) as a subject. (pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.
- 2) Standard imaging condition II:  
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

### 1. Sensitivity

Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100s, measure the signal output (Vs) at the center of the screen, and substitute the value into the following formula.

$$S = V_s \times \frac{100}{30} \text{ [mV]}$$

### 2. Saturation signal

Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 150mV, measure the minimum value of the signal output.

### 3. Smear

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of the signal output, 150mV. Then after the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) of the signal output and substitute the value into the following formula.

$$S_m = \frac{V_{sm}}{150} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [%]} \text{ (1/10V method conversion value)}$$

### 4. Video signal shading

Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 150mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (V_{max} - V_{min}) / 150 \times 100 \text{ [%]}$$

### 5. Dark signal

Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

## 6. Dark signal shading

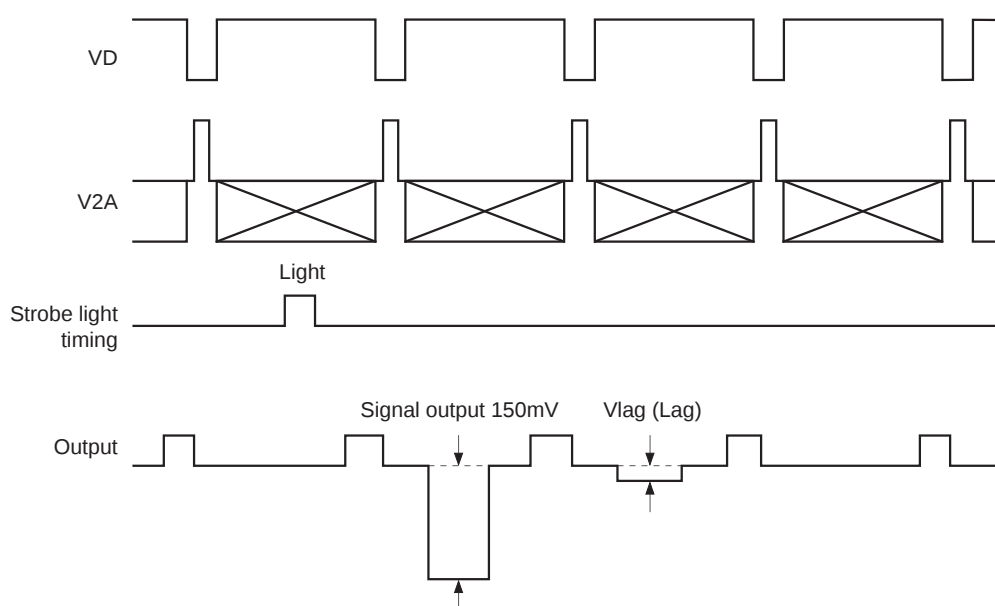
After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

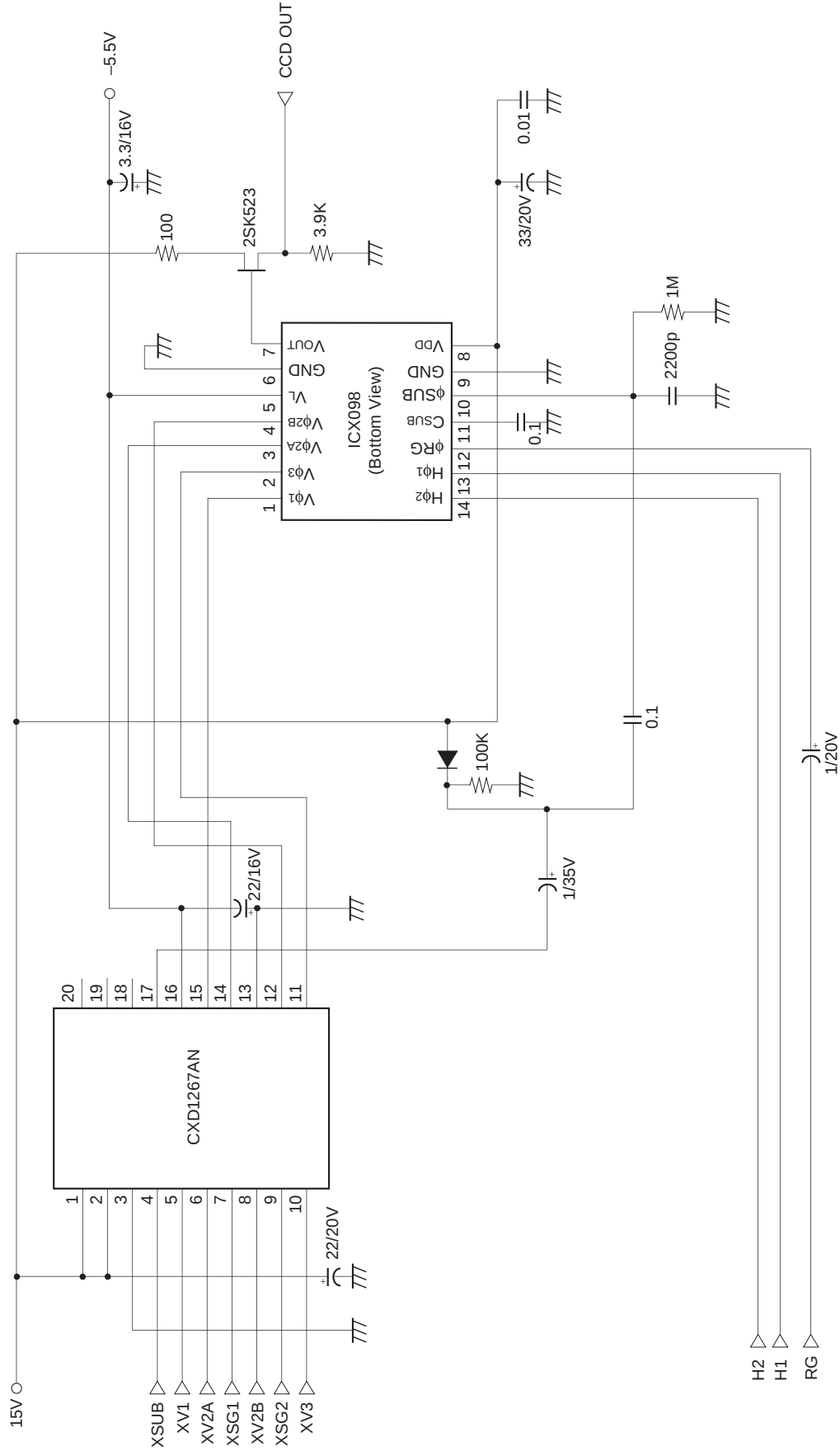
## 7. Lag

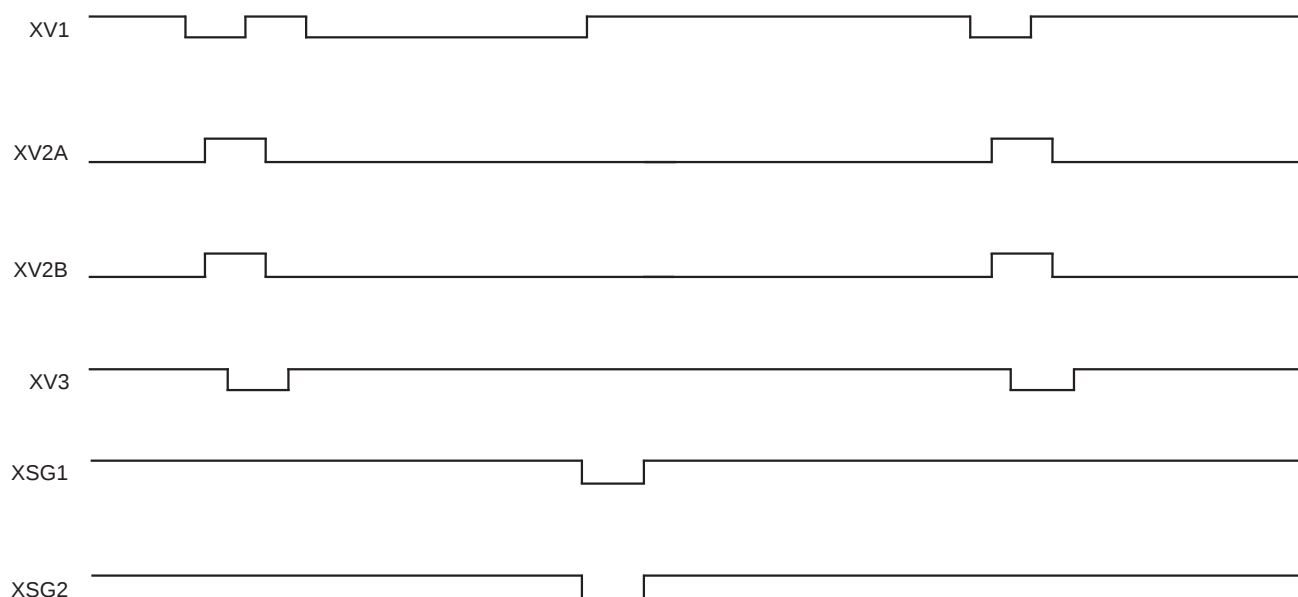
Adjust the signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

$$\text{Lag} = (Vlag/150) \times 100 \text{ [\%]}$$

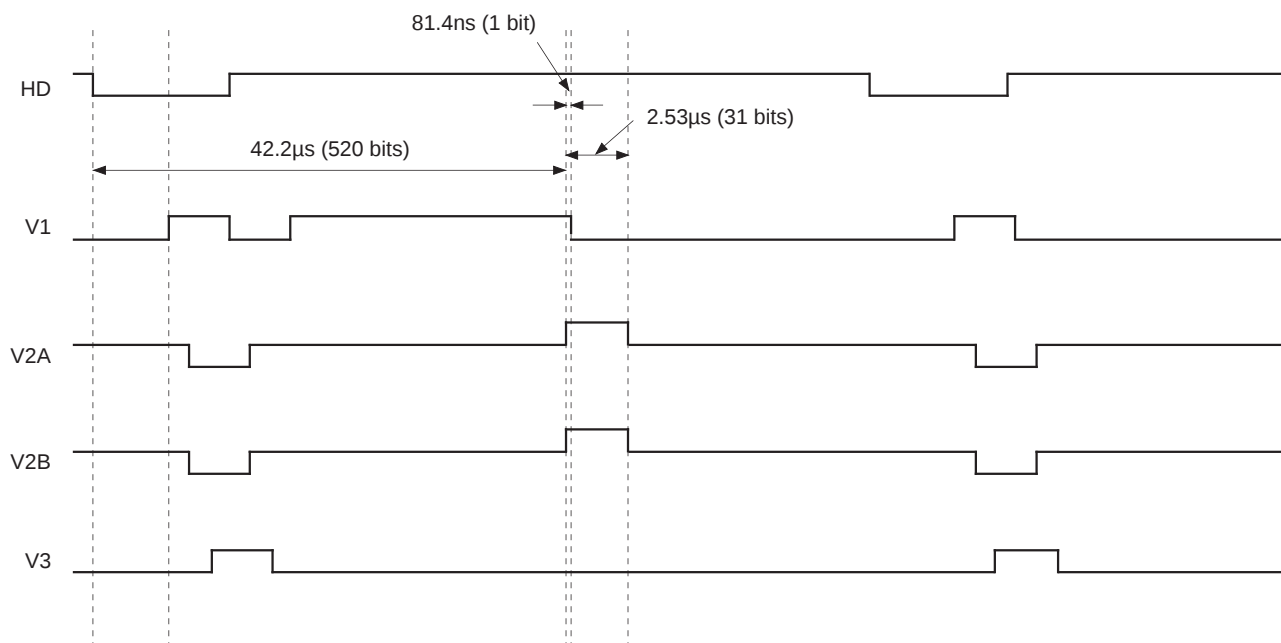


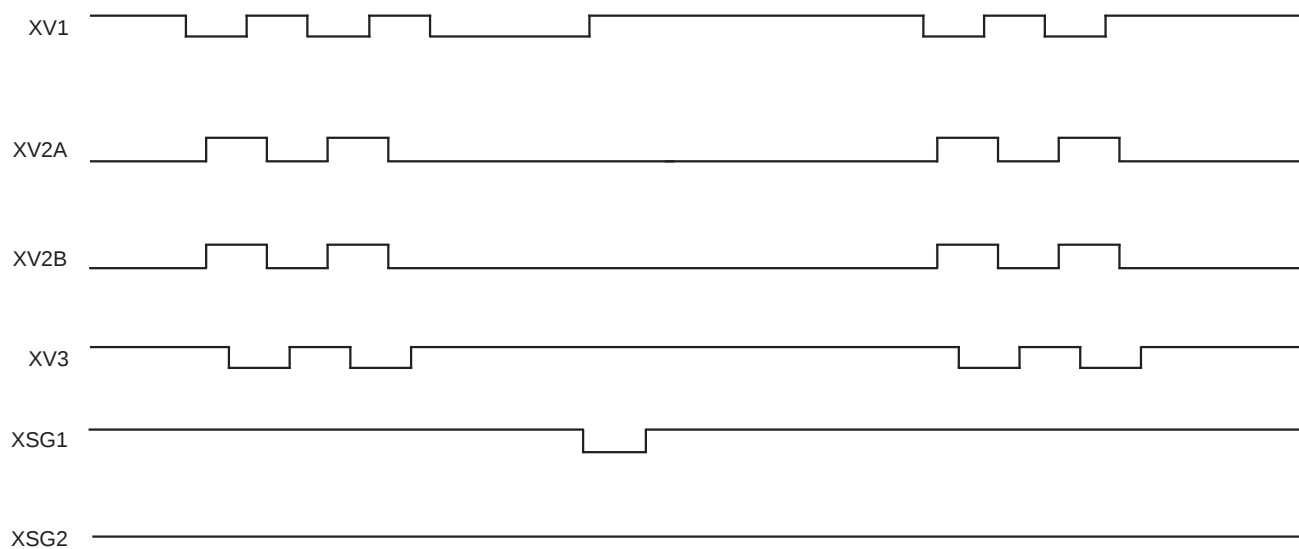
Drive Circuit



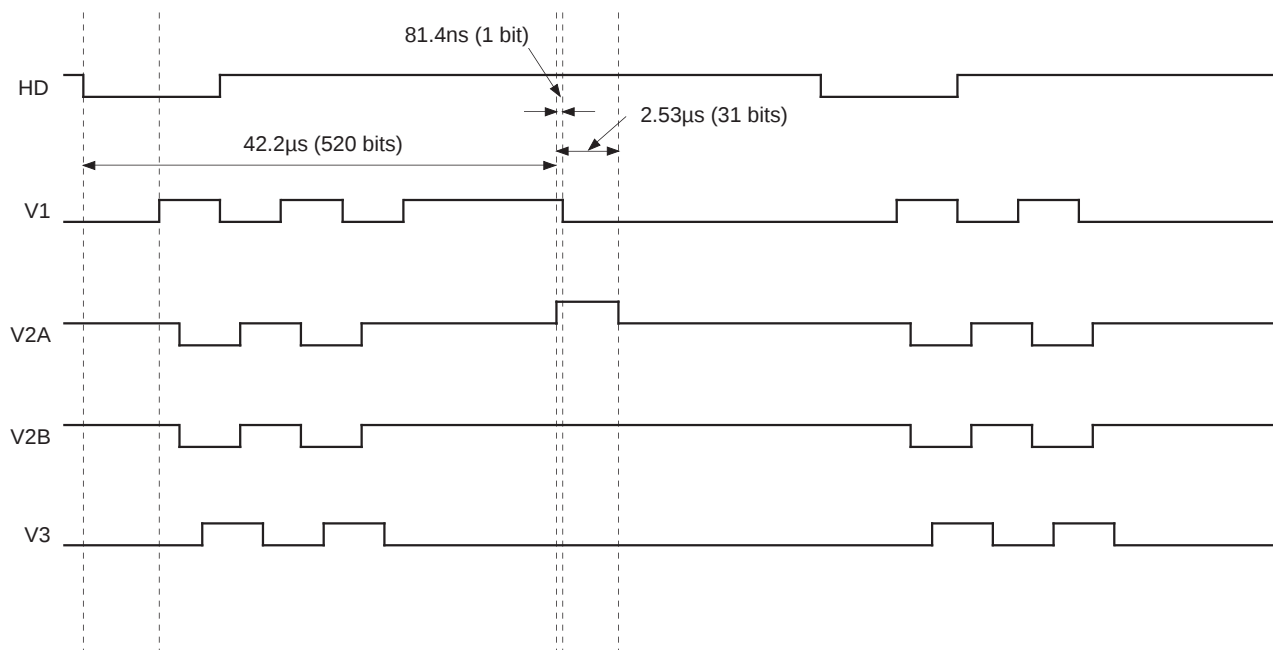
**Sensor Readout Clock Timing Chart      Progressive Scan Mode**

Sensor readout clocks XSG1 and XSG2 are used by composing XV2A and XV2B.

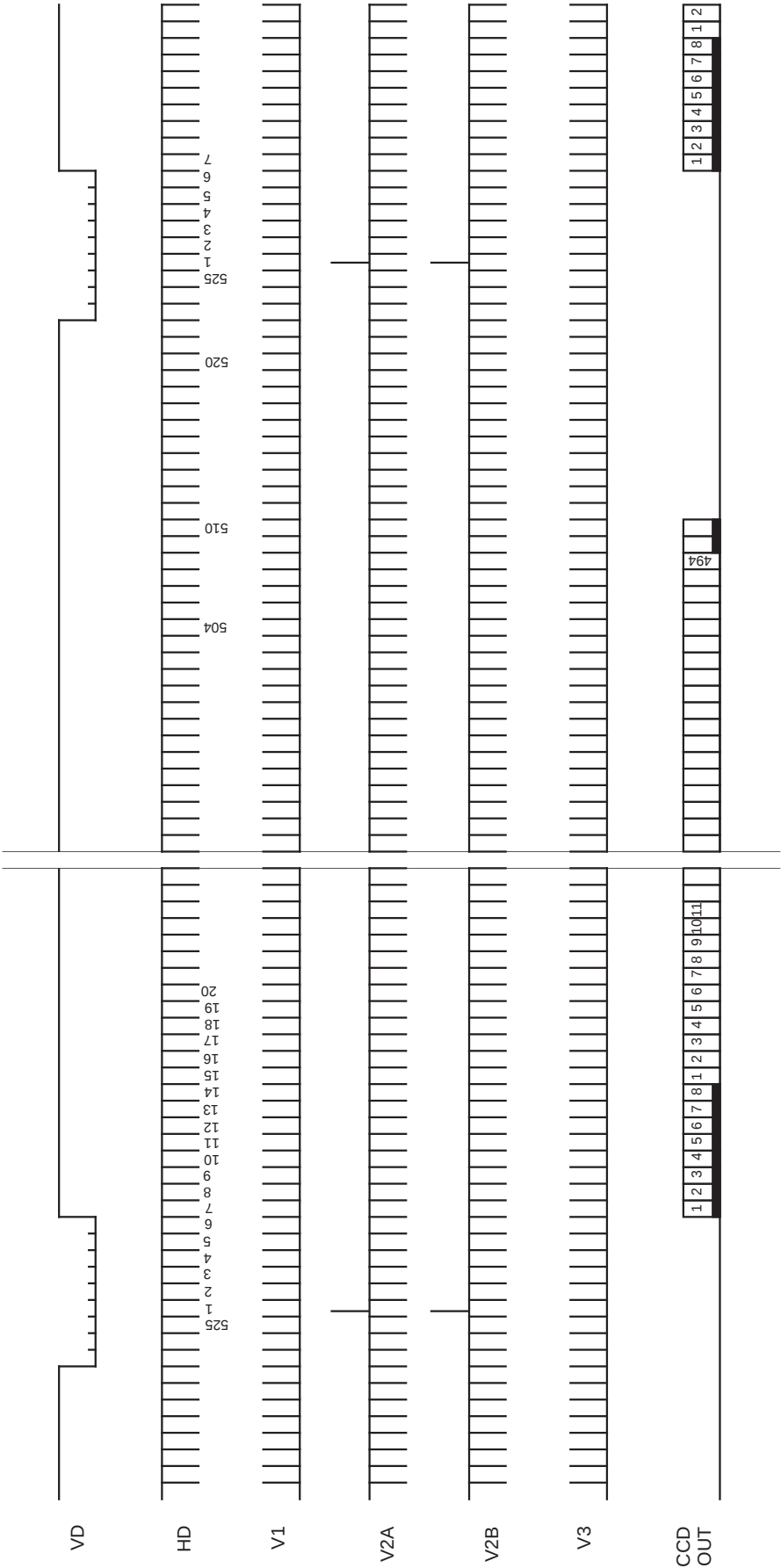


**Sensor Readout Clock Timing Chart      Monitoring Mode**

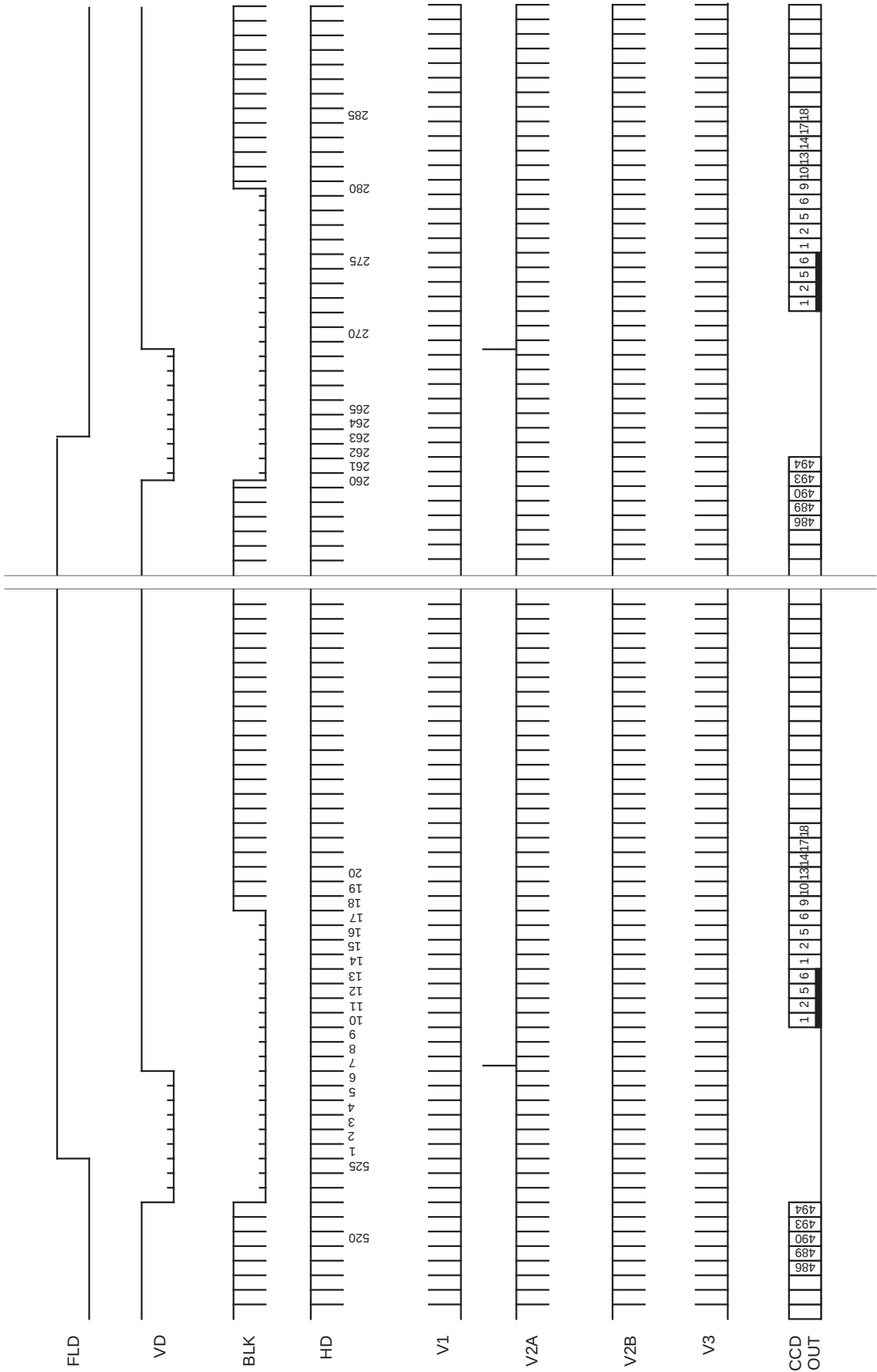
Sensor readout clock XSG1 is used by composing XV2A.



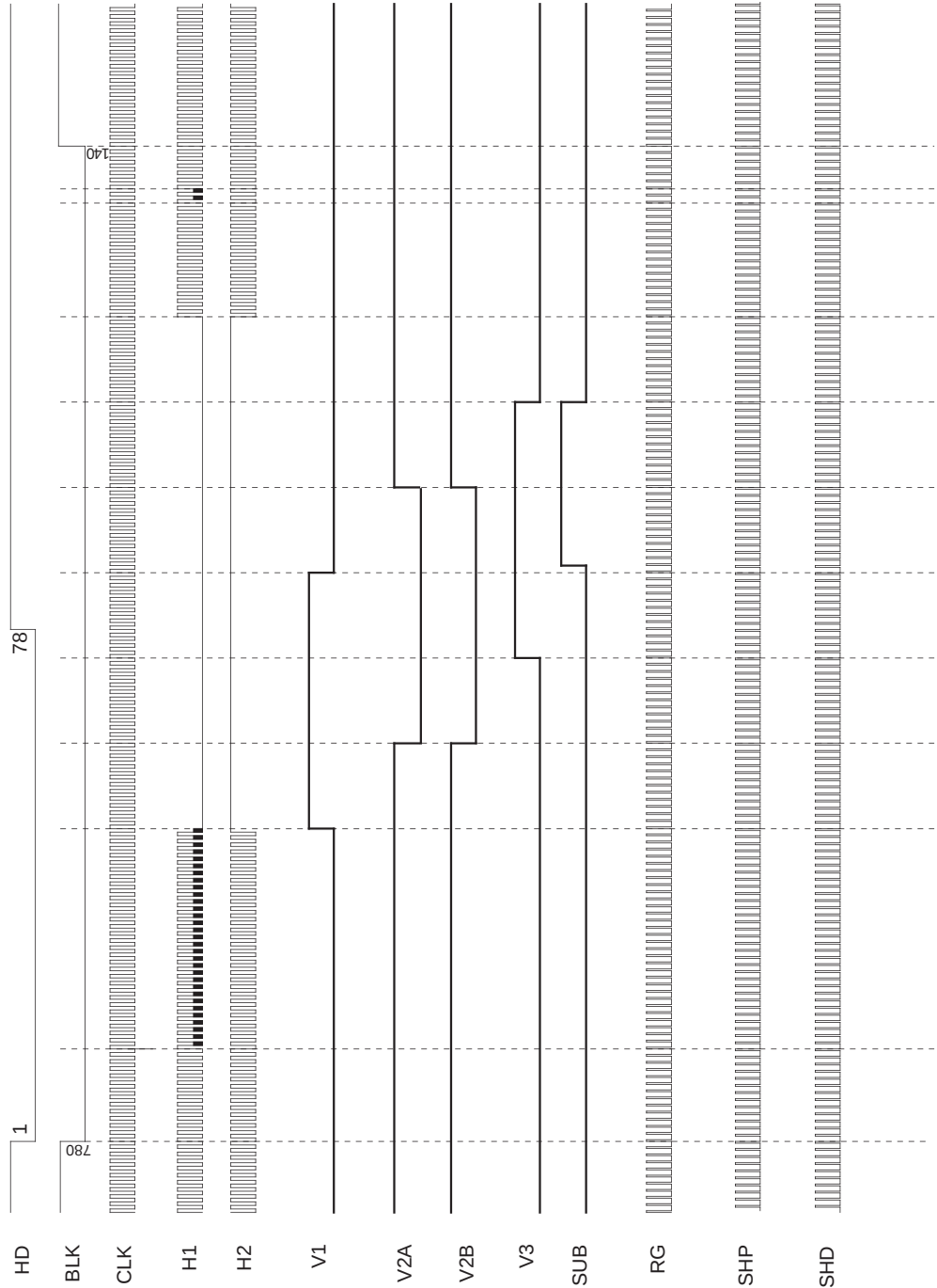
Drive Timing Chart (Vertical Sync)      Progressive Scan Mode



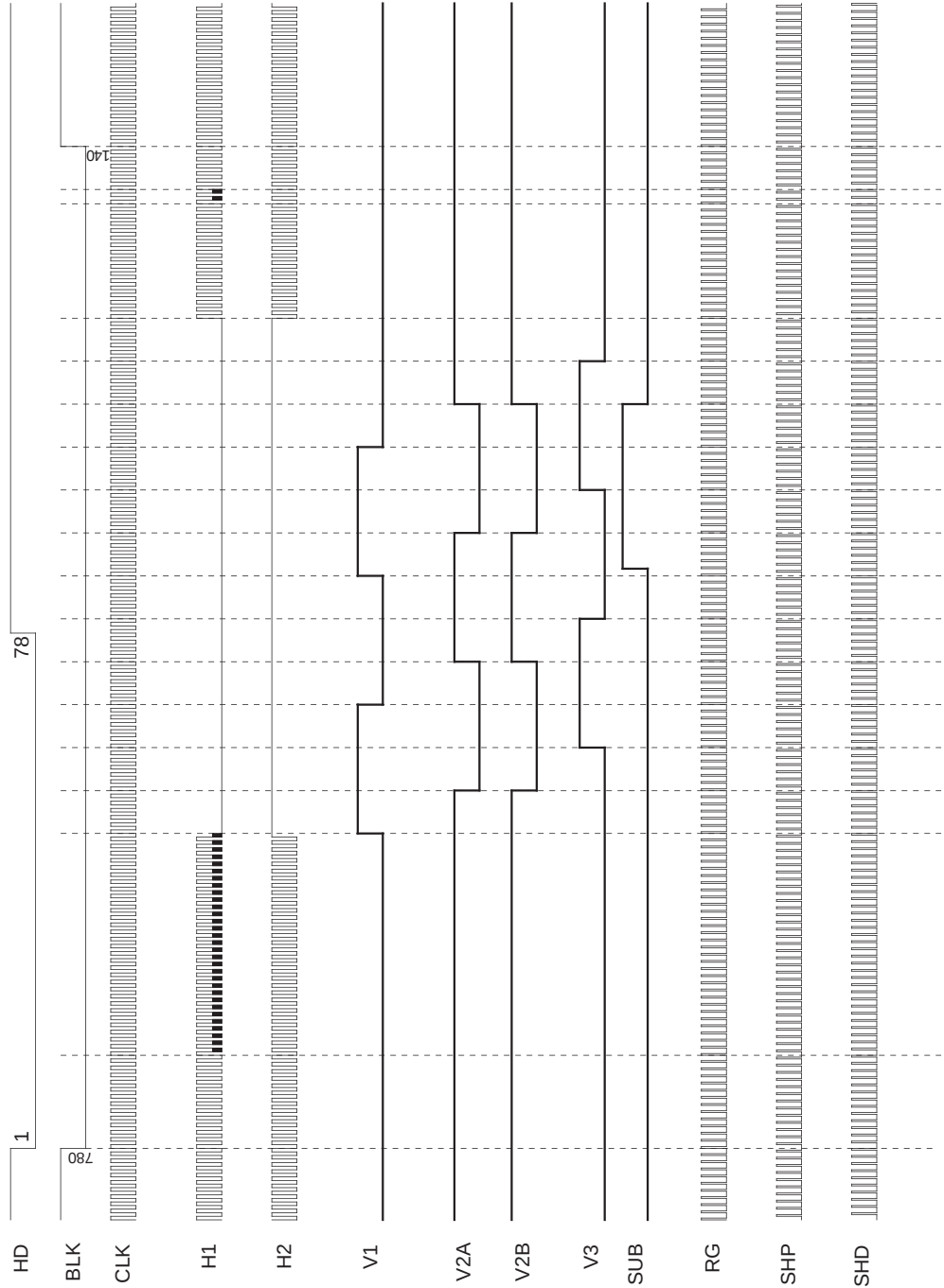
Drive Timing Chart (Vertical Sync)      Monitoring Mode



Drive Timing Chart (Horizontal Sync)      Progressive Scan Mode



Drive Timing Chart (Horizontal Sync)      Monitoring Mode



## Notes on Handling

### 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material.  
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

### 2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

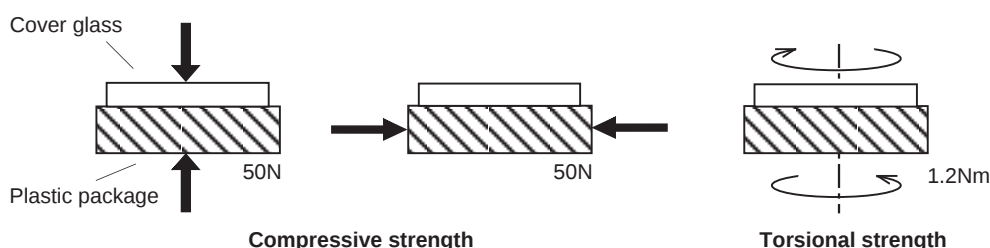
### 3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

- a) Perform all assembly operations in a clean room (class 1000 or less).
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

### 4) Installing (attaching)

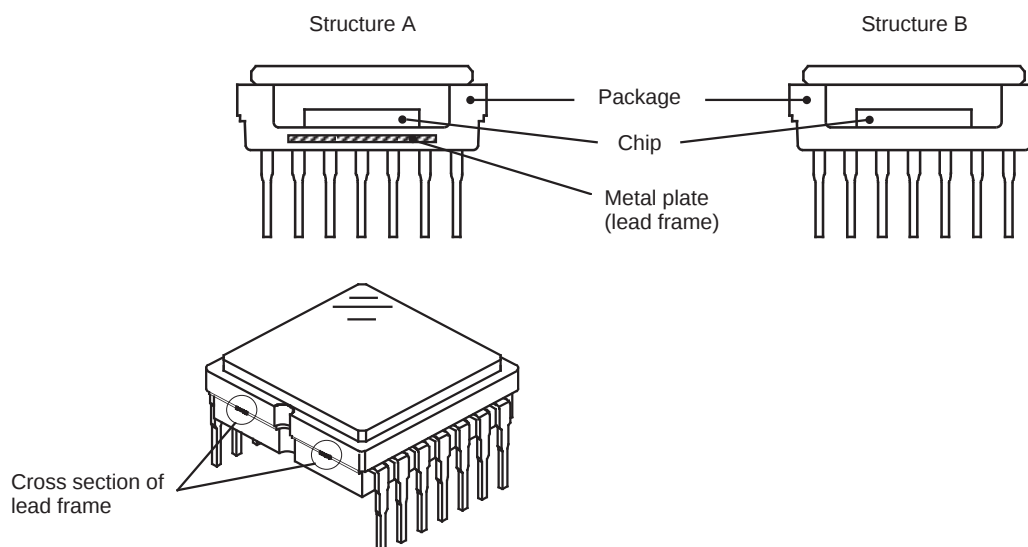
- a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



- b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
- c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
- d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
- e) If the lead bend repeatedly and the metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
- f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

#### 5) Others

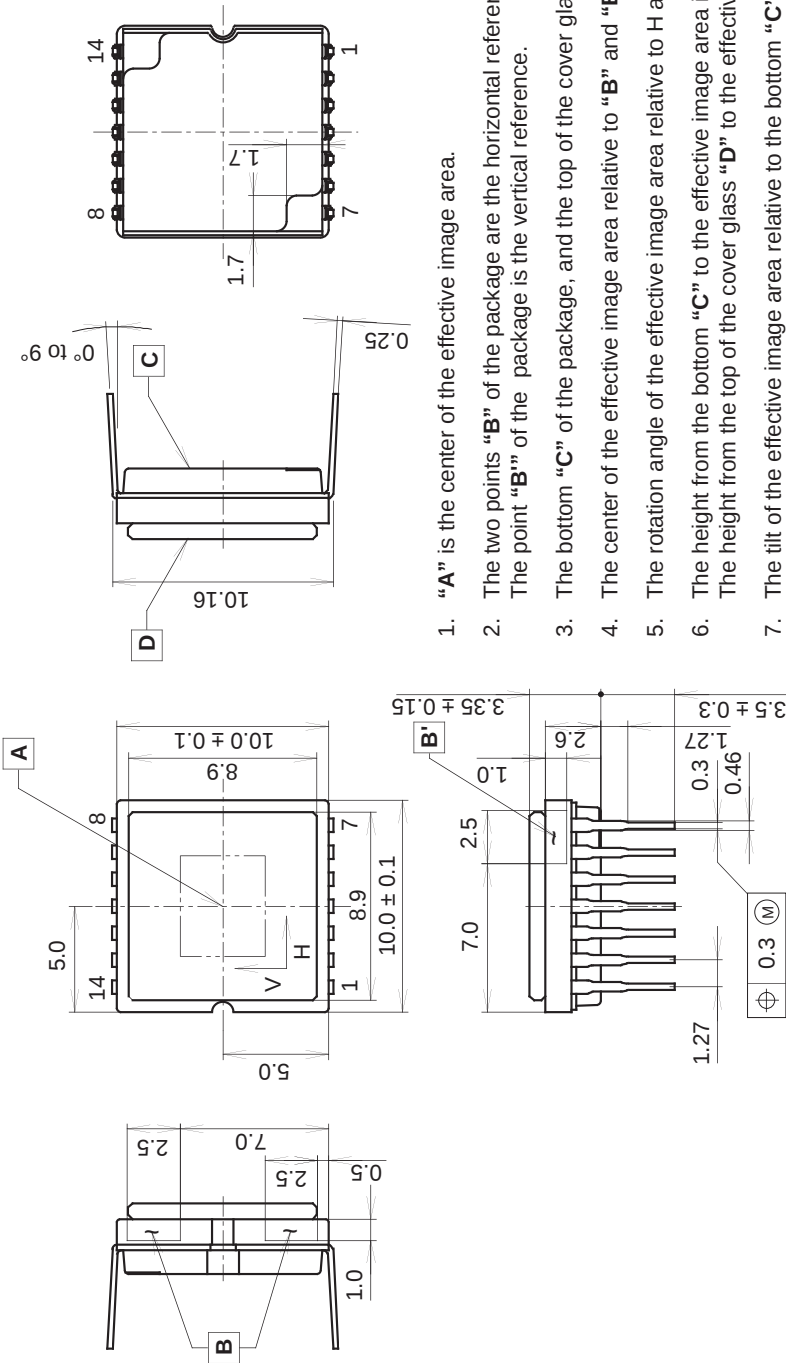
- a) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.
- b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- c) The brown stain may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
- d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline      Unit: mm

14 pin DIP (400mil)



1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference.  
The point "B" of the package is the vertical reference.
3. The bottom "C" of the package, and the top of the cover glass "D" are the height reference.
4. The center of the effective image area relative to "B" and "B" is (H, V) = (5.0, 5.0) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom "C" to the effective image area is 1.41 ± 0.10mm.  
The height from the top of the cover glass "D" to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom "C" is less than 25μm.  
The tilt of the effective image area relative to the top "D" of the cover glass is less than 25μm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.

PACKAGE STRUCTURE

|                  |              |
|------------------|--------------|
| PACKAGE MATERIAL | Plastic      |
| LEAD TREATMENT   | GOLD PLATING |
| LEAD MATERIAL    | 42 ALLOY     |
| PACKAGE WEIGHT   | 0.6g         |