ACT-S128K32 High Speed 4 Megabit SRAM Multichip Module

AEROFLEX CIRCUIT TECHNOLOGY
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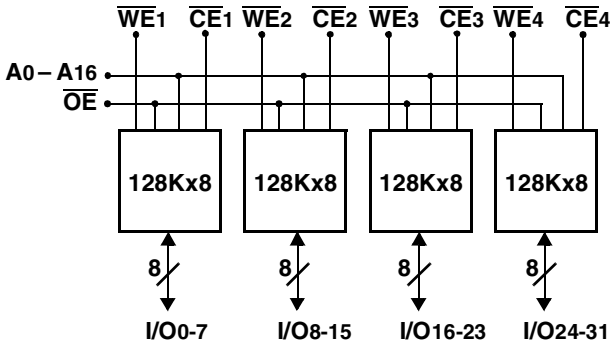
Features

- 4 Low Power CMOS 128K x 8 SRAMs in one MCM
- Overall configuration as 128K x 32
- Input and Output TTL Compatible
- 17, 20, 25, 35, 45 & 55ns Access Times, 15ns Available by Special Order
- Full Military (-55°C to +125°C) Temperature Range
- +5V Power Supply
- Choice of 7 Hermetically sealed Co-fired Packages:
  - 68–Lead, Low Profile CQFP (F1), 1.56"SQ x .140"max
  - 68–Lead, Dual-Cavity CQFP (F2), .88"SQ x .20"max (.18"max thickness available, contact factory for details) *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 68–Lead, Single-Cavity CQFP (F18), .94"SQ x .140"max *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
  - 66–Lead, PGA-Type (P2,P6 with/without shoulders), 1.185"SQ x .245"max
  - 66–Lead, PGA-Type (P7,P3 with/without shoulders), 1.08"SQ x .160"max
- Internal Decoupling Capacitors
- DESC SMD# 5962–93187 Released (P2,P3,P6,P7)
  5962–95595 Released (F1,F2,F18)

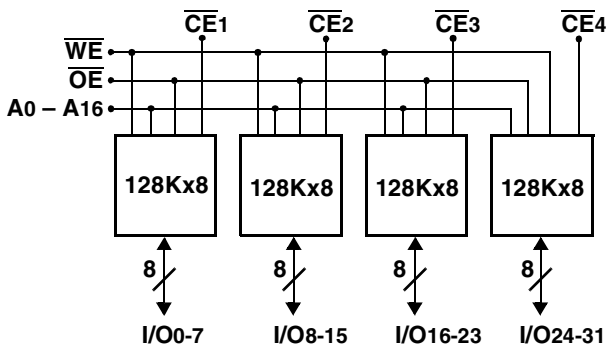
Block Diagram – PGA Type Package(P2,P7) & CQFP(F2,F18)



Pin Description

I/O0-31	Data I/O
A0–16	Address Inputs
WE1–4	Write Enables
CE1–4	Chip Enables
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

Block Diagram – CQFP(F1)



Pin Description

I/O0-31	Data I/O
A0–16	Address Inputs
WE	Write Enable
CE1–4	Chip Enables
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

General Description

The ACT–S128K32 is a High Speed 4 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range, military, space, or high reliability mass memory and fast cache applications.

The MCM can be organized as a 128K x 32 bits, 256K x 16 bits or 512k x 8 bits device and is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and output enable ($\overline{OE}$) are both low. Access time grades of 17ns, 20ns, 25ns, 35ns, 45ns and 55ns maximum are standard.

The +5 Volt power supply version is standard and the +3.3 Volt low power model is available (See ACT-S128K32V data sheet).

The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment. DESC Standard Military Drawing (SMD) part numbers are released and available.

The ACT-S128K32 is manufactured in Aeroflex's 80,000ft^2 MIL-PRF-38534 certified facility in Plainview, N.Y.

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Case Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Package Power Dissipation		
	F1, P2/P6, P3/P7 Packages	4.4	W
	F2,F18 Package	3.3	W
$Ø_{J-C}$	Hottest Die, Max Thermal Resistance - Junction to Case		
	F1, P2/P6, P3/P7 Packages	2.0	°C/W
	F2,F18 Package	8.0	°C/W
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Truth Table

Mode	CE	OE	WE	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

Capacitance

(f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C_{AD}	A_0 – A_{16} Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{WE}	CQFP(F1) Package	50	pF
	PGA(P2,P3,P6,P7) and CQFP(F2,F18) Packages	20	pF
C_{CE}	Chip Enable Capacitance	20	pF
$C_{I/O}$	I/O_0 – I/O_{31} Capacitance	20	pF

Capacitance is guaranteed by design but not tested.

DC Characteristics

(4.5Vdc≤ V_{CC} ≤ 5.5Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	–017 & –020		–025 & –035		–045 & –055		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = 0 or V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = 0 or V_{CC}		10		10		10	µA
Operating Supply Current 32 Bit Mode	I_{CC}x32	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz, V_{CC} = Max, CMOS Compatible		600		600		600	mA

DC Characteristics (Continued)

(4.5Vdc≤ V_{CC} ≤ 5.5Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	–017 & –020		–025 & –035		–045 & –055		Units
			Min	Max	Min	Max	Min	Max	
Standby Current	I_{SB}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5 MHz, V_{CC} = Max, CMOS Compatible		80		60		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA, V_{CC} = Min	2.4		2.4		2.4		V

AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_C = -55°C to +125°C)

Read Cycle

Parameter	Sym	–017		–020		–025		–035		–045		–055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		35		45		55		ns
Address Access Time	t_{AA}		17		20		25		35		45		55	ns
Chip Enable Access Time	t_{ACE}		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		ns
Output Enable to Output Valid	t_{OE}		9		12		15		20		25		30	ns
Chip Enable to Output in Low Z*	t_{CLZ}	3		3		3		3		3		3		ns
Output Enable to Output in Low Z*	t_{OLZ}	0		0		0		0		0		0		ns
Chip Deselect to Output in High Z*	t_{CHZ}		12		12		12		15		20		20	ns
Output Disable to Output in High Z*	t_{OHZ}		10		11		12		15		20		20	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Sym	–017		–020		–025		–035		–045		–055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		35		45		55		ns
Chip Enable to End of Write	t_{CW}	12		15		20		25		30		40		ns
Address Valid to End of Write	t_{AW}	12		15		20		25		30		40		ns
Data Valid to End of Write	t_{DW}	10		12		15		18		20		20		ns
Write Pulse Width	t_{WP}	13		15		20		25		30		40		ns
Address Setup Time	t_{AS}	0		0		0		0		0		0		ns
Output Active from End of Write *	t_{OW}	3		3		3		4		4		4		ns
Write to Output in High Z *	t_{WHZ}		10		10		10		15		15		15	ns
Data Hold from Write Time	t_{DH}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		0		0		ns

* Parameters guaranteed by design but not tested

Data Retention Electrical Characteristics (Special Order Only)

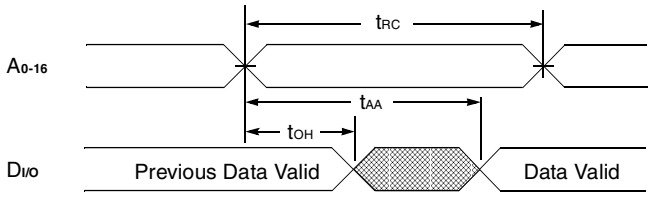
(T_C = -55°C to +125°C)

Parameter	Sym	Test Conditions	All Speeds		Units
			Min	Max	
V_{CC} for Data Retention	V_{DR}	$\overline{CE}$ ≥ V_{CC} – 0.2V	2	5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V, 17-55ns		11.6	mA

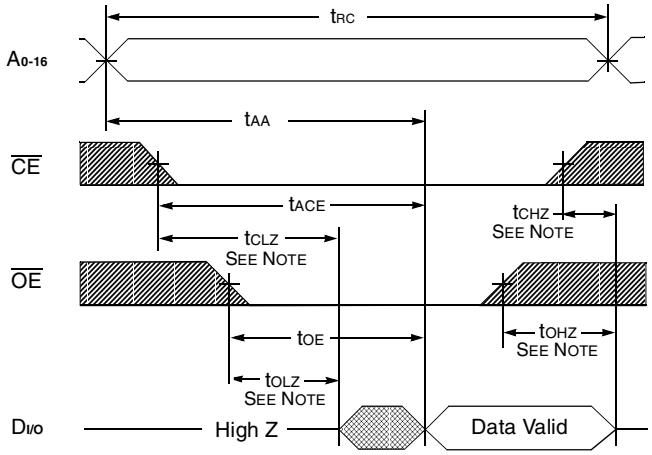
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



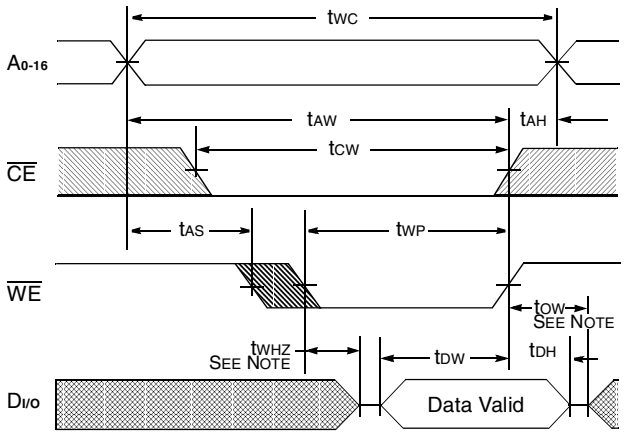
Read Cycle 2 ($\overline{WE}$ = V_{IH})



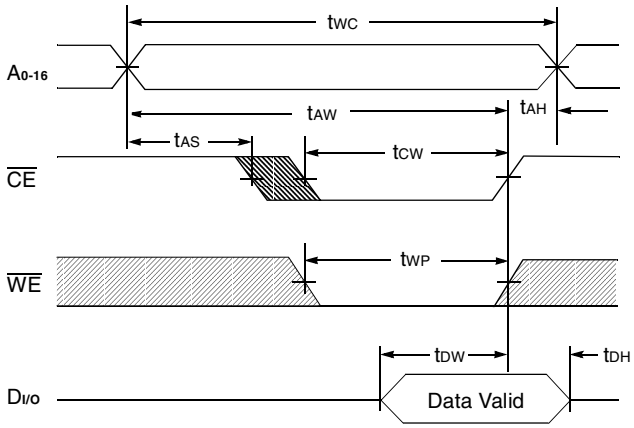
Note: Guaranteed by design, but not tested.

Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE}$ = V_{IL})

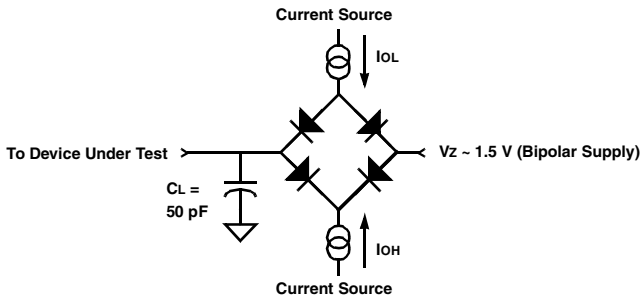


Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE}$ = V_{IH})



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V
Output Lead Capacitance	50	pF

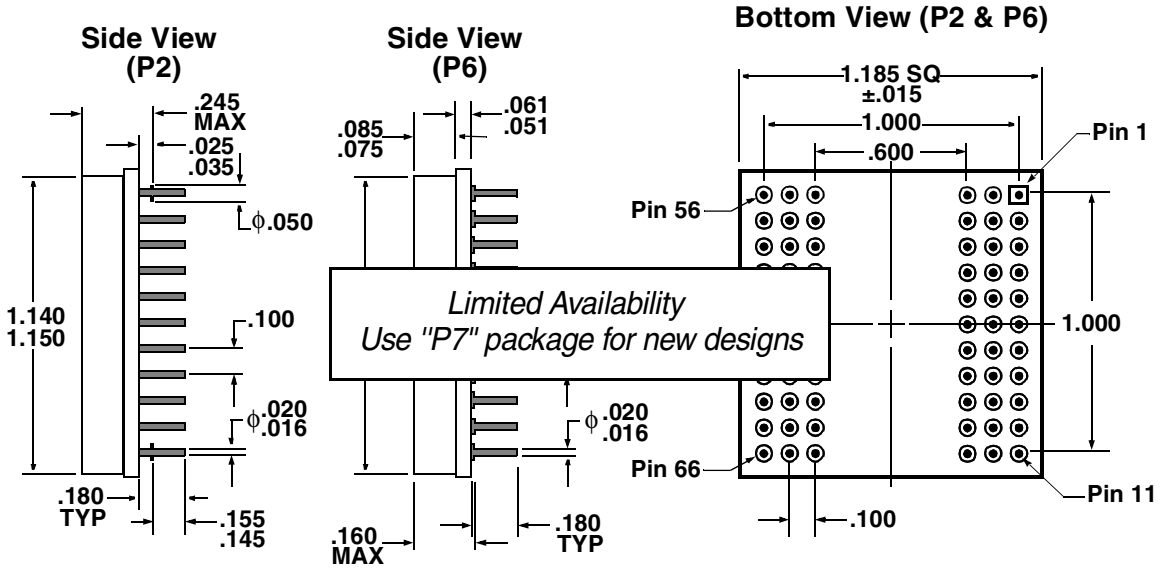
Notes:
1) V_Z is programmable from -2V to +7V. 2) I_{OL} and I_{OH} programmable from 0 to 16 mA. 3) Tester Impedance $Z_O = 75\Omega$. 4) V_Z is typically the midpoint of V_{OH} and V_{OL}. 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

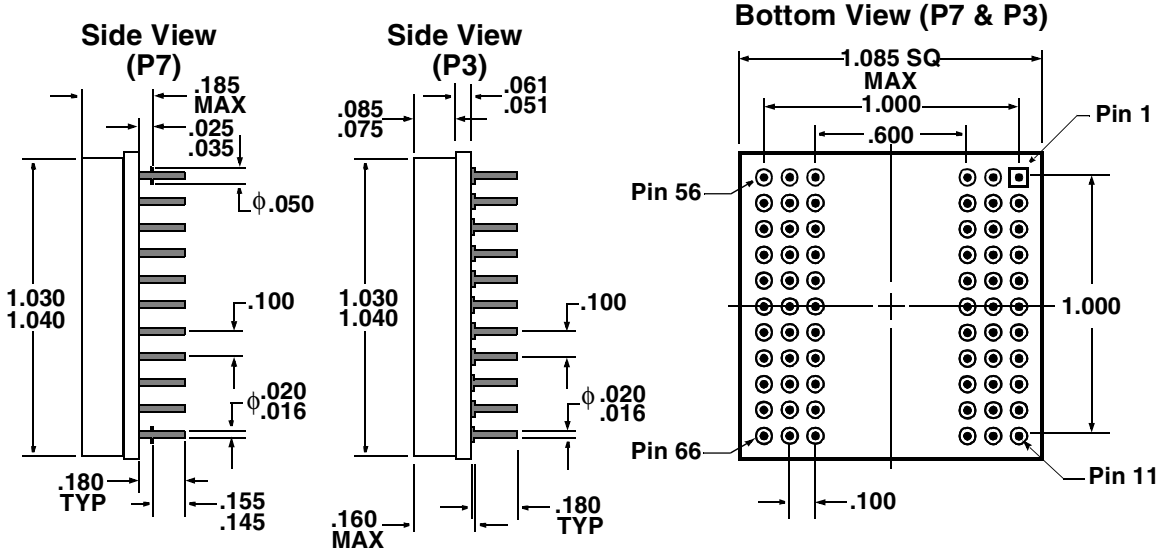
66 Pins — PGA-Type													
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O_8	11	I/O_2	21	NC	31	I/O_6	41	A_9	51	A_5	61	A_1
2	I/O_9	12	$\overline{WE}_2$	22	I/O_3	32	I/O_5	42	I/O_{16}	52	$\overline{WE}_3$	62	A_2
3	I/O_{10}	13	$\overline{CE}_2$	23	I/O_{15}	33	I/O_4	43	I/O_{17}	53	$\overline{CE}_3$	63	I/O_{23}
4	A_{13}	14	GND	24	I/O_{14}	34	I/O_{24}	44	I/O_{18}	54	GND	64	I/O_{22}
5	A_{14}	15	I/O_{11}	25	I/O_{13}	35	I/O_{25}	45	V_{CC}	55	I/O_{19}	65	I/O_{21}
6	A_{15}	16	A_{10}	26	I/O_{12}	36	I/O_{26}	46	$\overline{CE}_4$	56	I/O_{31}	66	I/O_{20}
7	A_{16}	17	A_{11}	27	OE	37	A_6	47	$\overline{WE}_4$	57	I/O_{30}		
8	NC	18	A_{12}	28	NC	38	A_7	48	I/O_{27}	58	I/O_{29}		
9	I/O_0	19	Vcc	29	$\overline{WE}_1$	39	NC	49	A_3	59	I/O_{28}		
10	I/O_1	20	$\overline{CE}_1$	30	I/O_7	40	A_8	50	A_4	60	A_0		

Note: Pins 8, 21, 28, & 39 normally not connected, and can be connected to ground by specifing pinout Option "C".

"P2" — 1.185" SQ PGA Type Package Standard (with shoulders on Pins 1, 11, 56 & 66)
"P6" — 1.185" SQ PGA Type Special Order Package (without shoulders)



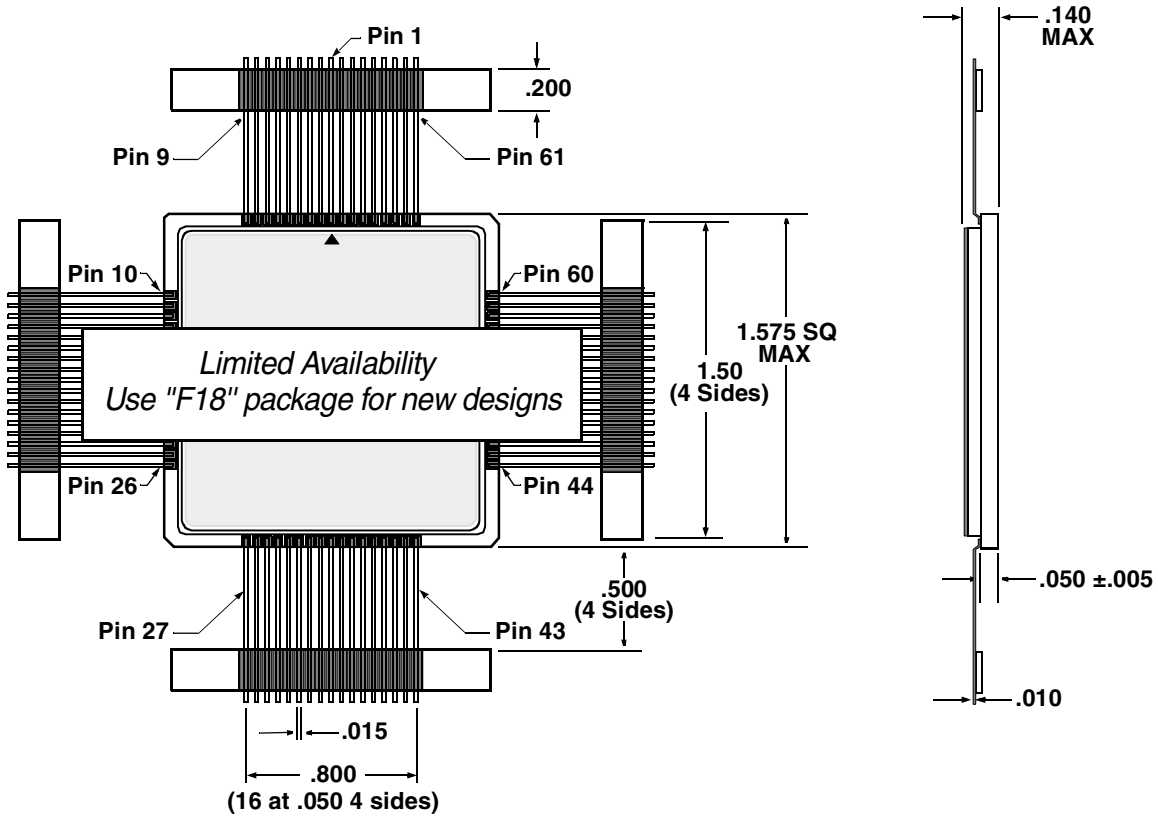
"P7" — 1.08" SQ PGA Type Package Standard (with shoulders on Pins 1, 11, 56 & 66)
"P3" — 1.08" SQ PGA Type Special Order Package (without shoulders)



Pin Numbers & Functions

68 Pins — CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_1$	19	I/O_8	36	$\overline{CE}_4$	53	I/O_{23}
3	A_5	20	I/O_9	37	NC	54	I/O_{22}
4	A_4	21	I/O_{10}	38	NC	55	I/O_{21}
5	A_3	22	I/O_{11}	39	NC	56	I/O_{20}
6	A_2	23	I/O_{12}	40	NC	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}$
17	I/O_7	34	$\overline{CE}_2$	51	I/O_{24}	68	$\overline{CE}_3$

Package Outline — CQFP "F1"



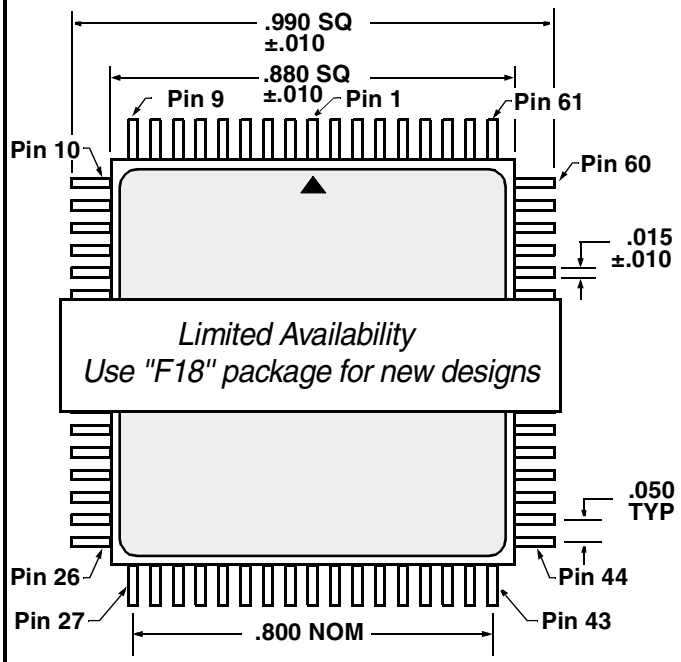
All dimensions in inches

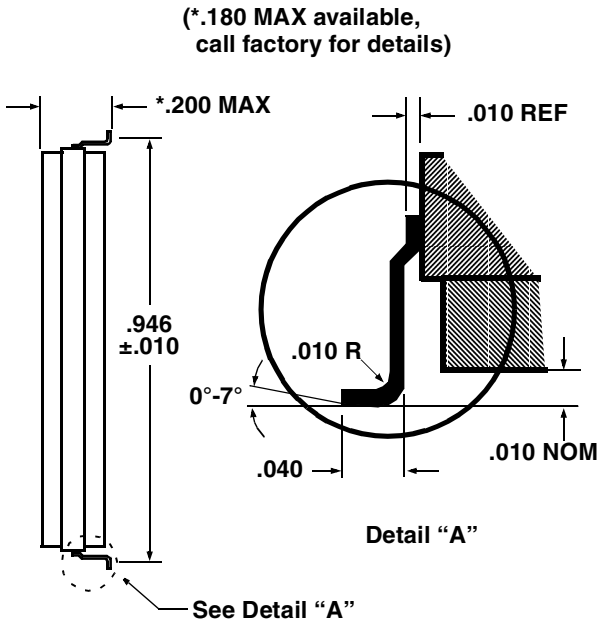
Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	NC	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}1$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Package Outline "F2" — Dual-Cavity CQFP

Top View





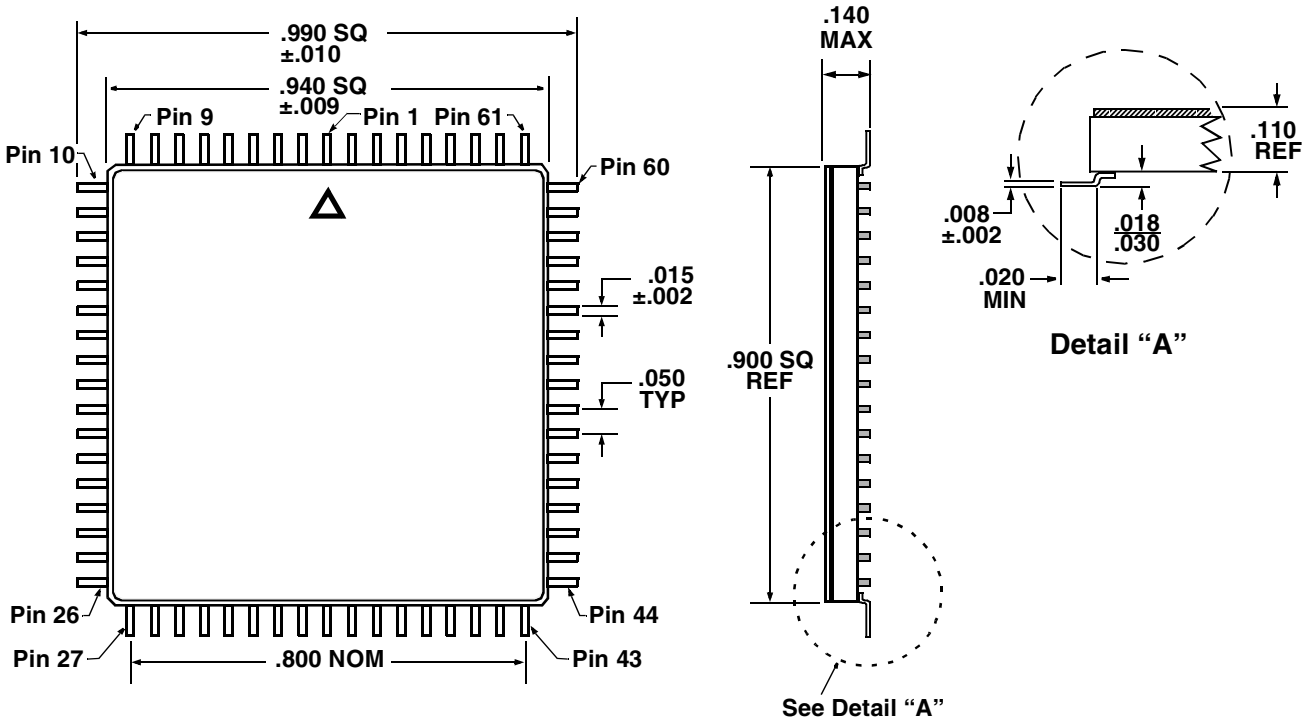
All dimensions in inches

Note: Metallic lids and walls – both sides

Pin Numbers & Functions

68 Pins — Single-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	NC	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$\overline{WE}_2$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	$\overline{WE}_3$	56	I/O_{20}
6	A_2	23	I/O_{12}	40	$\overline{WE}_4$	57	I/O_{19}
7	A_1	24	I/O_{13}	41	NC	58	I/O_{18}
8	A_0	25	I/O_{14}	42	NC	59	I/O_{17}
9	NC	26	I/O_{15}	43	NC	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}_1$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Package Outline — CQFP Single Cavity "F18"

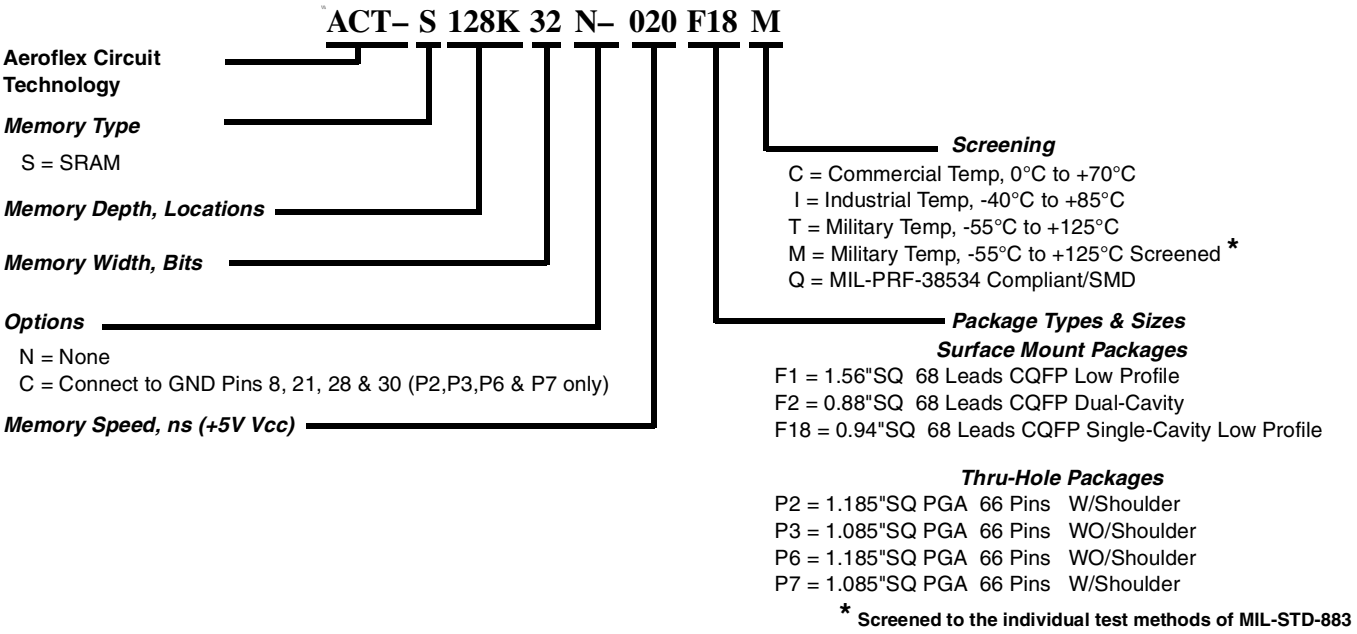


All dimensions in inches

DESC Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT–S128K32N–017F1Q	5962–9559510HYX	17ns	1.56"sq CQFP
ACT–S128K32N–020F1Q	5962–9559509HYX	20ns	1.56"sq CQFP
ACT–S128K32N–025F1Q	5962–9559508HYX	25ns	1.56"sq CQFP
ACT–S128K32N–035F1Q	5962–9559507HYX	35ns	1.56"sq CQFP
ACT–S128K32N–045F1Q	5962–9559506HYX	45ns	1.56"sq CQFP
ACT–S128K32N–055F1Q	5962–9559505HYX	55ns	1.56"sq CQFP
ACT–S128K32N–017F2Q	5962–9559510HMX	17ns	.88"sq CQFP
ACT–S128K32N–020F2Q	5962–9559509HMX	20ns	.88"sq CQFP
ACT–S128K32N–025F2Q	5962–9559508HMX	25ns	.88"sq CQFP
ACT–S128K32N–035F2Q	5962–9559507HMX	35ns	.88"sq CQFP
ACT–S128K32N–045F2Q	5962–9559506HMX	45ns	.88"sq CQFP
ACT–S128K32N–055F2Q	5962–9559505HMX	55ns	.88"sq CQFP
ACT–S128K32N–017F2Q	5962–9559510HZX	17ns	.88"sq CQFP
ACT–S128K32N–020F2Q	5962–9559509HZX	20ns	.88"sq CQFP
ACT–S128K32N–025F2Q	5962–9559508HZX	25ns	.88"sq CQFP
ACT–S128K32N–035F2Q	5962–9559507HZX	35ns	.88"sq CQFP
ACT–S128K32N–045F2Q	5962–9559506HZX	45ns	.88"sq CQFP
ACT–S128K32N–055F2Q	5962–9559505HZX	55ns	.88"sq CQFP
ACT–S128K32N–017F18Q	5962–9559510H9X	17ns	.94"sq CQFP
ACT–S128K32N–020F18Q	5962–9559509H9X	20ns	.94"sq CQFP
ACT–S128K32N–025F18Q	5962–9559508H9X	25ns	.94"sq CQFP
ACT–S128K32N–035F18Q	5962–9559507H9X	35ns	.94"sq CQFP
ACT–S128K32N–045F18Q	5962–9559506H9X	45ns	.94"sq CQFP
ACT–S128K32N–055F18Q	5962–9559505H9X	55ns	.94"sq CQFP
ACT–S128K32N–017P2Q	5962–9318710HTX	17ns	1.185"sq PGA-Type
ACT–S128K32N–020P2Q	5962–9318709HTX	20ns	1.185"sq PGA-Type
ACT–S128K32N–025P2Q	5962–9318708HTX	25ns	1.185"sq PGA-Type
ACT–S128K32N–035P2Q	5962–9318707HTX	35ns	1.185"sq PGA-Type
ACT–S128K32N–045P2Q	5962–9318706HTX	45ns	1.185"sq PGA-Type
ACT–S128K32N–055P2Q	5962–9318705HTX	55ns	1.185"sq PGA-Type
ACT–S128K32C–017P2Q	5962–9318710HTX	17ns	1.185"sq PGA-Type
ACT–S128K32C–020P2Q	5962–9318709HTX	20ns	1.185"sq PGA-Type
ACT–S128K32C–025P2Q	5962–9318708HTX	25ns	1.185"sq PGA-Type
ACT–S128K32C–035P2Q	5962–9318707HTX	35ns	1.185"sq PGA-Type
ACT–S128K32C–045P2Q	5962–9318706HTX	45ns	1.185"sq PGA-Type
ACT–S128K32C–055P2Q	5962–9318705HTX	55ns	1.185"sq PGA-Type
ACT–S128K32N–017P7Q	5962–9318710H4X	17ns	1.085"sq PGA-Type
ACT–S128K32N–020P7Q	5962–9318709H4X	20ns	1.085"sq PGA-Type
ACT–S128K32N–025P7Q	5962–9318708H4X	25ns	1.085"sq PGA-Type
ACT–S128K32N–035P7Q	5962–9318707H4X	35ns	1.085"sq PGA-Type
ACT–S128K32N–045P7Q	5962–9318706H4X	45ns	1.085"sq PGA-Type
ACT–S128K32N–055P7Q	5962–9318705H4X	55ns	1.085"sq PGA-Type
ACT–S128K32C–017P7Q	5962–9318710H5X	17ns	1.085"sq PGA-Type
ACT–S128K32C–020P7Q	5962–9318709H5X	20ns	1.085"sq PGA-Type
ACT–S128K32C–025P7Q	5962–9318708H5X	25ns	1.085"sq PGA-Type
ACT–S128K32C–035P7Q	5962–9318707H5X	35ns	1.085"sq PGA-Type
ACT–S128K32C–045P7Q	5962–9318706H5X	45ns	1.085"sq PGA-Type
ACT–S128K32C–055P7Q	5962–9318705H5X	55ns	1.085"sq PGA-Type

Part Number Breakdown



* **Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice

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