TEXAS INSTRUMENTS

ISO7720, ISO7721

SLLSEP3A – NOVEMBER 2016 – REVISED DECEMBER 2016

ISO772x High Speed, Robust EMC Reinforced Dual-Channel Digital Isolators

1 Features

- Signaling Rate: Up to 100 Mbps
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V Level Translation
- Default Output *High* and *Low* Options
- Wide Temperature Range: –55°C to +125°C
- Low Power Consumption, Typical 1.7 mA per Channel at 1 Mbps
- Low Propagation Delay: 11 ns Typical (5-V Supplies)
- High CMTI: ±100 kV/µs Typical
- Robust Electromagnetic Compatibility (EMC)
  - System-Level ESD, EFT, and Surge Immunity
  - Low Emissions
- Isolation Barrier Life: >40 Years
- Wide-SOIC (DW-16) and Narrow-SOIC (D-8) Package Options
- Safety and Regulatory Approvals:
  - VDE Reinforced Insulation according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - 5000 V_{RMS} (DW) and 3000 V_{RMS} (D) Isolation Rating per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
  - TUV Certification according to EN 60950-1 and EN 61010-1
  - VDE, UL, CSA, and TUV Certifications for DW Package Complete; All Other Certifications Planned

2 Applications

- Industrial Automation
- Hybrid Electric Vehicles
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment

3 Description

The ISO772x devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. The ISO7720 device has both channels in the same direction while the ISO7721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See the *Device Functional Modes* section for further details.

Used in conjunction with isolated power supplies, these devices help prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO772x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO772x family of devices is available in 16-pin SOIC wide-body (DW) and 8-pin SOIC narrow-body (D) packages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7720, ISO7721 ISO7721F, ISO7721F	SOIC (D)	4.90 mm × 3.91 mm
	SOIC (DW)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic
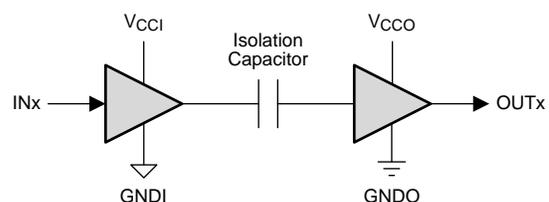
Copyright © 2016, Texas Instruments Incorporated

V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2016) to Revision A   **Page**

- Changed *Feature* From: IEC 60950-1, IEC 60601-1 and IEC 61010-1 End Equipment Standards To: IEC 60950-1 and IEC 60601-1 End Equipment Standards 1
- Added Climatic category to the *Insulation Specifications* 6
- Changed the CSA column of *Regulatory Information* 7
- Changed DW package) To: (DW-16) in the TUV column of *Regulatory Information* 7
- Changed t_{ie} TYP value From: 1.5 To 1 in *Switching Characteristics—5-V Supply* 12
- Changed t_{ie} TYP value From: 1.5 To 1 in *Switching Characteristics—3.3-V Supply* 12
- Changed t_{ie} TYP value From: 1.5 To 1 in *Switching Characteristics—2.5-V Supply* 12

Product Folder Links: *ISO7720 ISO7721*

5 Pin Configuration and Functions

ISO7720 DW Package
16-Pin SOIC
Top View
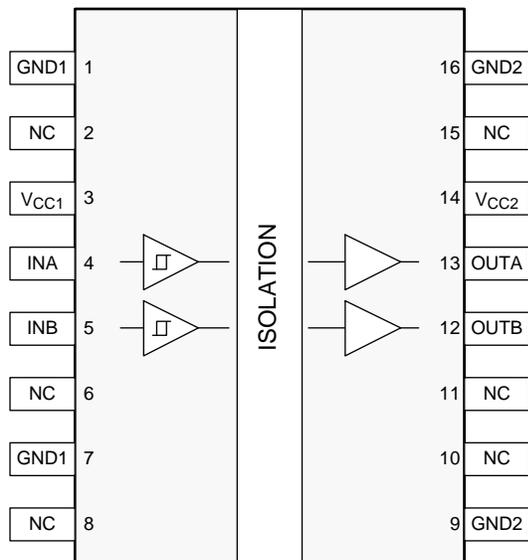
ISO7721 DW Package
16-Pin SOIC
Top View
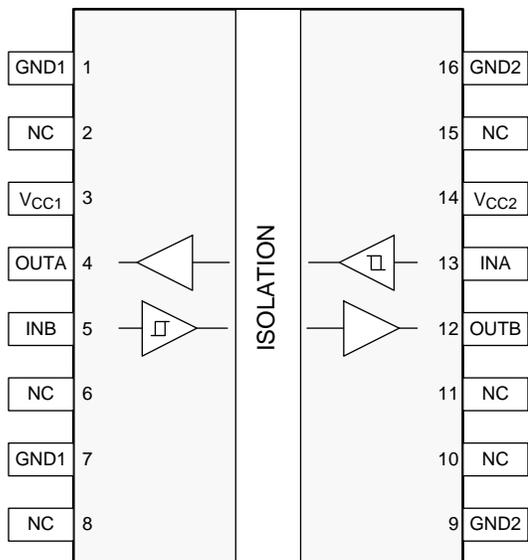
ISO7720 D Package
8-Pin SOIC
Top View
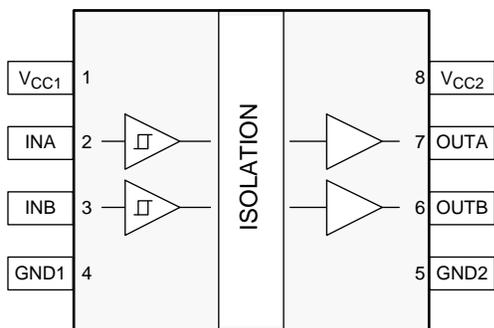
ISO7721 D Package
8-Pin SOIC
Top View
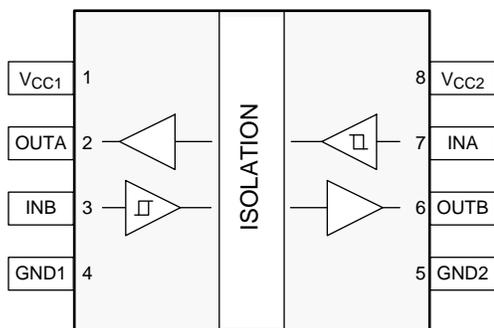
Pin Functions

PIN					I/O	DESCRIPTION
NAME	**DW PACKAGE**		**D PACKAGE**			
	ISO7720	**ISO7721**	**ISO7720**	**ISO7721**		
GND1	1, 7	1, 7	4	4	—	Ground connection for V_{CC1}
GND2	9	9	5	5	—	Ground connection for V_{CC2}
	16	16				
INA	4	13	2	7	I	Input, channel A
INB	5	5	3	3	I	Input, channel B
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	—	—	—	Not connected
OUTA	13	4	7	2	O	Output, channel A
OUTB	12	12	6	6	O	Output, channel B
V_{CC1}	3	3	1	1	—	Power supply, V_{CC1}
V_{CC2}	14	14	8	8	—	Power supply, V_{CC2}

Submit Documentation Feedback   3

Product Folder Links: *ISO7720 ISO7721*

6 Specifications

6.1 Absolute Maximum Ratings

See [1].

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage[2]	−0.5	6	V
V	Voltage at INx, OUTx	−0.5	V_{CC} + 0.5[3]	V
I_O	Output current	−15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	V_{CCO}[1] = 5 V	−4			mA
		V_{CCO} = 3.3 V	−2			
		V_{CCO} = 2.5 V	−1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI}[1]		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}	V
DR	Signaling rate		0		100	Mbps
T_A	Ambient temperature		−55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

Product Folder Links: *ISO7720 ISO7721*

6.4 Thermal Information

	THERMAL METRIC[1]	ISO772x		UNIT
		DW (SOIC)	D (SOIC)	
		16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	137.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.6	54.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	71.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32.3	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.2	70.7	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power Rating

PARAMETER		TEST CONDITIONS	VALUE	UNIT
ISO7720				
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave	100	mW
P_{D1}	Maximum power dissipation by side-1		20	mW
P_{D2}	Maximum power dissipation by side-2		80	mW
ISO7721				
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, input a 50 MHz 50% duty cycle square wave	100	mW
P_{D1}	Maximum power dissipation by side-1		50	mW
P_{D2}	Maximum power dissipation by side-2		50	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE DW-16	VALUE D-8	UNIT
CLR	External clearance [1]	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage [1]	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	> 600	> 600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–IV	I–III	
		Rated mains voltage ≤ 600 V_{RMS}	I–IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	n/a	
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 [2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	637	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) test	1000	450	V_{RMS}
		DC voltage	1414	637	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM} t = 60 s (qualification) t = 1 s (100% production)	8000	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage [3]	Test method per IEC 60065, 1.2/50 μs waveform, V_{TEST} = 1.6 × V_{IOSM} (qualification)	8000	5000	V_{PK}
q_{pd}	Apparent charge [4]	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output [5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	~0.5	pF
R_{IO}	Isolation resistance [5]	V_{IO} = 500 V, T_A = 25°C	>10^{12}	>10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	>10^{11}	>10^{11}	
		V_{IO} = 500 V at T_S = 150°C	>10^{9}	>10^{9}	
	Pollution degree		2	2	
	Climatic category		55/125/21	5/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	V_{TEST} = V_{ISO}, t = 60 s(qualification); V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

Product Folder Links: *ISO7720 ISO7721*

6.7 Regulatory Information

DW package devices certified according to VDE, CSA, UL, and TUV; All other certifications are planned.

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced Insulation Maximum transient isolation voltage, 8000 V_{PK} (DW-16) and 4242 V_{PK} (D-8); Maximum repetitive peak isolation voltage, 1414 V_{PK} (DW-16) and 637 V_{PK} (D-8); Maximum surge isolation voltage, 8000 V_{PK} (DW-16) and 5000 V_{PK} (D-8)	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed., 800 V_{RMS} (DW-16) and 400 V_{RMS} (D-8) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} (DW-16) max working voltage	**DW-16:** Single protection, 5000 V_{RMS}; **D-8:** Single protection, 3000 V_{RMS}	**DW-16:** Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage; **D-8:** Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW-16) 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 V_{RMS} (DW-16)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certification planned	Client ID number: 77311

Product Folder Links: *ISO7720 ISO7721*

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 86.5 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			263	mA
		$R_{\theta JA}$ = 86.5 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			401	
		$R_{\theta JA}$ = 86.5 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			525	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 86.5 °C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1445	mW
T_S	Maximum safety temperature				150	°C
D-8 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 137.7 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 3			165	mA
		$R_{\theta JA}$ = 137.7 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 3			252	
		$R_{\theta JA}$ = 137.7 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 3			330	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 137.7 °C/W, T_J = 150°C, T_A = 25°C, see Figure 4			908	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information is that of a device installed on a High-K test board for leaded surface mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

Product Folder Links: *ISO7720 ISO7721*

6.9 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V $\pm$ 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA; see Figure 13	$V_{CCO}{}^{(1)} - 0.4$	4.8		V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA; see Figure 13		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input threshold voltage		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}{}^{(1)}$ at INx			10	µA
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx	−10			µA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V, VCM = 1200 V; see Figure 15	40	100		kV/µs
C_I	Input Capacitance$^{(2)}$	$V_I = V_{CC}/ 2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, $V_{CC} = 5$ V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V $\pm$ 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720							
Supply current - DC signal		$V_I = V_{CCI}$ (ISO7720), $V_I = 0$ V (ISO7720 with F suffix)	I_{CC1}		0.8	1.1	mA
			I_{CC2}		1.1	1.7	
		$V_I = 0$ V (ISO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)	I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	1.9	
Supply current - AC signal		All channels switching with square wave clock input; $C_L = 15$ pF	1 Mbps — I_{CC1}		1.8	2.7	
			1 Mbps — I_{CC2}		1.3	1.9	
			10 Mbps — I_{CC1}		1.9	2.7	
			10 Mbps — I_{CC2}		2.2	3	
			100 Mbps — I_{CC1}		2.5	3.2	
			100 Mbps — I_{CC2}		11.6	14	
ISO7721							
Supply current - DC signal		$V_I = V_{CCI}$ (ISO7721), $V_I = 0$ V (ISO7721 with F suffix)	I_{CC1}, I_{CC2}		1	1.6	mA
		$V_I = 0$ V (ISO7721), $V_I = V_{CCI}$ (ISO7721 with F suffix)	I_{CC1}, I_{CC2}		2.2	3.2	
Supply current - AC signal		All channels switching with square wave clock input; $C_L = 15$ pF	1 Mbps — I_{CC1}, I_{CC2}		1.7	2.4	
			10 Mbps — I_{CC1}, I_{CC2}		2.2	3	
			100 Mbps — I_{CC1}, I_{CC2}		7.3	9	

Product Folder Links: ISO7720 ISO7721

6.11 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3$ V ± 10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA; see Figure 13	V_{CCO}[(1)] $- 0.3$	3.2		V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA; see Figure 13		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$[(1)] at INx			10	µA
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx	−10			µA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V, VCM = 1200 V; see Figure 15	40	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3$ V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720), $V_I = 0$ V (ISO7720 with F suffix)		I_{CC1}		0.8	1.1	mA
			I_{CC2}		1.1	1.7	
	$V_I = 0$ V (ISO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	1.9	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15$ pF	1 Mbps	I_{CC1}		1.8	2.7	
			I_{CC2}		1.2	1.9	
		10 Mbps	I_{CC1}		1.9	2.7	
			I_{CC2}		1.9	2.6	
		100 Mbps	I_{CC1}		2.2	3.1	
			I_{CC2}		8.6	11	
ISO7721							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721), $V_I = 0$ V (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		1	1.6	mA
	$V_I = 0$ V (ISO7721), $V_I = V_{CCI}$ (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.2	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15$ pF	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.4	
		10 Mbps	I_{CC1}, I_{CC2}		2	2.8	
		100 Mbps	I_{CC1}, I_{CC2}		5.6	7	

Product Folder Links: *ISO7720 ISO7721*

6.13 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5$ V ± 10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA; see Figure 13	$V_{CCO}^{(1)} - 0.2$	2.45		V
V_{OL}	Low-level output voltage	$I_{OL} = 1$ mA; see Figure 13		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0$ V at INx	−10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V, VCM = 1200 V; see Figure 15	40	100		kV/μs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5$ V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720), $V_I = 0$ V (ISO7720 with F suffix)		I_{CC1}		0.8	1.1	mA
			I_{CC2}		1.1	1.7	
	$V_I = 0$ V (ISO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)		I_{CC1}		2.9	4.2	
			I_{CC2}		1.2	1.9	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15$ pF	1 Mbps	I_{CC1}		1.8	2.7	
			I_{CC2}		1.3	1.9	
		10 Mbps	I_{CC1}		1.9	2.7	
			I_{CC2}		1.7	2.4	
		100 Mbps	I_{CC1}		2.2	3	
			I_{CC2}		6.8	9	
ISO7721							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721), $V_I = 0$ V (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		1	1.6	mA
	$V_I = 0$ V (ISO7721), $V_I = V_{CCI}$ (ISO7721 with F suffix)		I_{CC1}, I_{CC2}		2.2	3.2	
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15$ pF	1 Mbps	I_{CC1}, I_{CC2}		1.6	2.4	mA
		10 Mbps	I_{CC1}, I_{CC2}		1.9	2.7	
		100 Mbps	I_{CC1}, I_{CC2}		4.6	6	

6.15 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5$ V ± 10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	6	11	16	ns
PWD	Pulse width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time[2]	Same direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time[3]				4.5	ns
t_r	Output signal rise time	See Figure 13		1.8	3.9	ns
t_f	Output signal fall time			1.9	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3$ V ± 10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	6	11	16	ns
PWD	Pulse width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time[2]	Same direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time[3]				4.5	ns
t_r	Output signal rise time	See Figure 13		0.7	3	ns
t_f	Output signal fall time			0.7	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
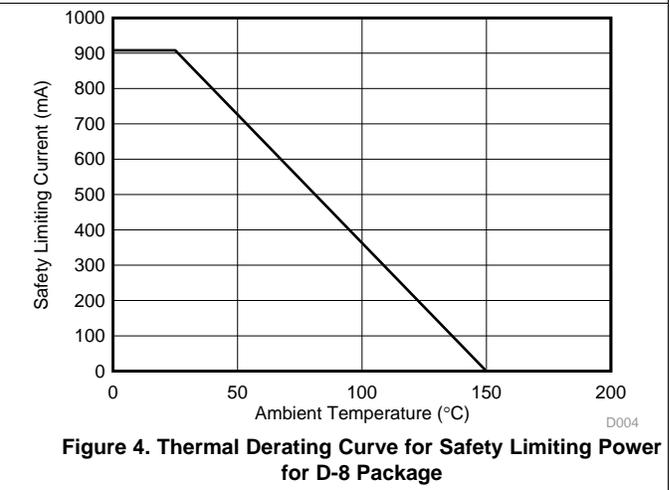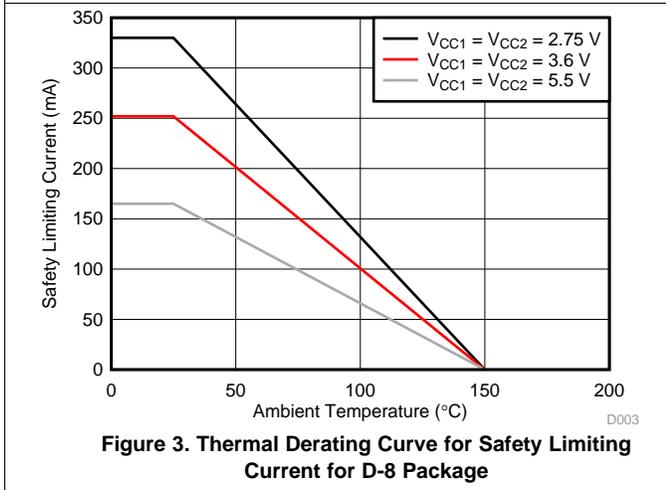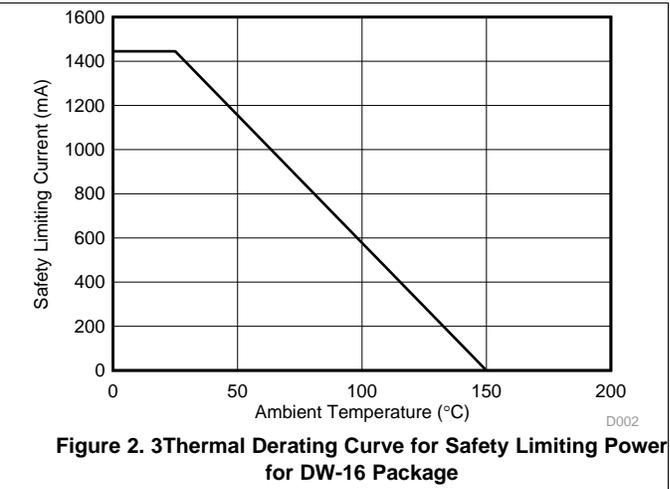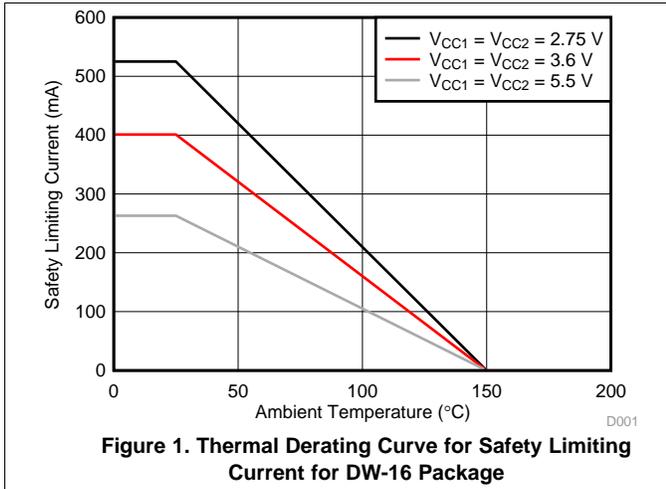
6.17 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5$ V ± 10% (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 13	7.5	12	18.5	ns
PWD	Pulse width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time[2]	Same direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time[3]				4.6	ns
t_r	Output signal rise time	See Figure 13		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 14		0.1	0.3	μs
t_{ie}	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

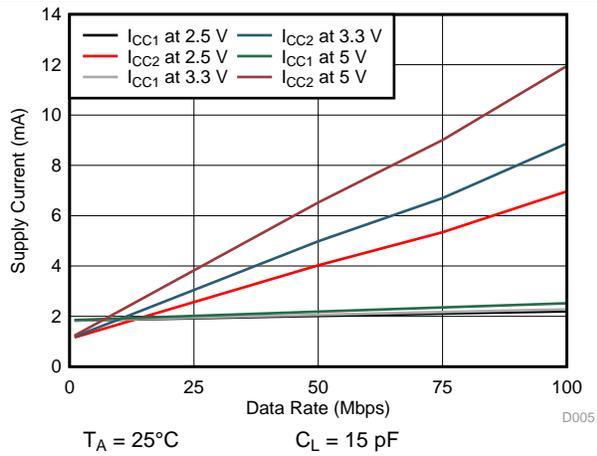## 6.18 Safety and Insulation Characteristics Curves

Figure 1. Thermal Derating Curve for Safety Limiting
Current for DW-16 Package

Figure 2. 3Thermal Derating Curve for Safety Limiting Power
for DW-16 Package

Figure 3. Thermal Derating Curve for Safety Limiting
Current for D-8 Package

Figure 4. Thermal Derating Curve for Safety Limiting Power
for D-8 Package

6.19 Typical Characteristics

Figure 5. ISO7720 Supply Current vs Data Rate (With 15-pF Load)
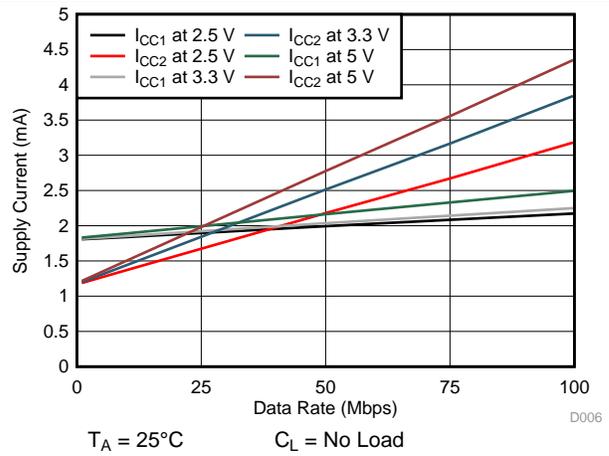
Figure 6. ISO7720 Supply Current vs Data Rate (With No Load)
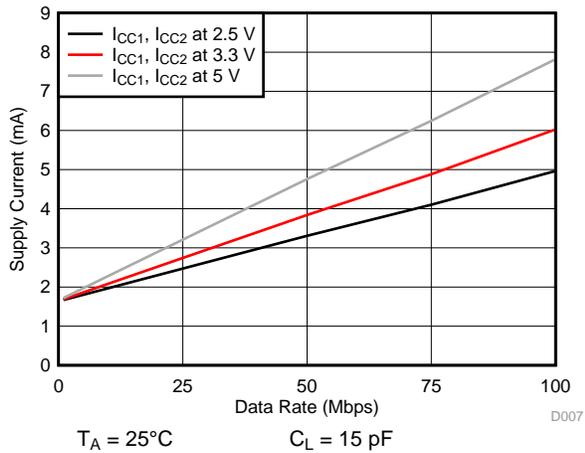
Figure 7. ISO7721 Supply Current vs Data Rate (With 15-pF Load)
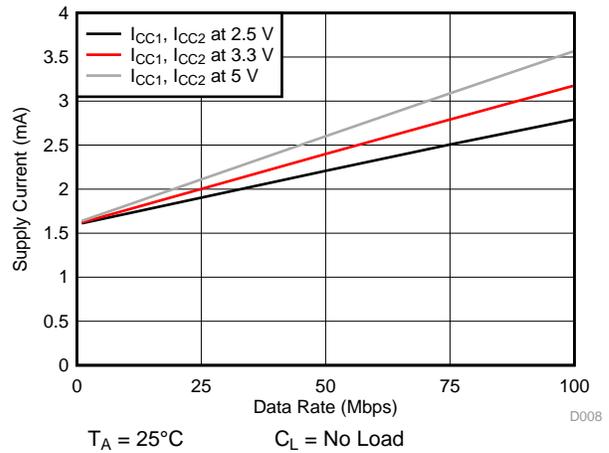
Figure 8. ISO7721 Supply Current vs Data Rate (With No Load)
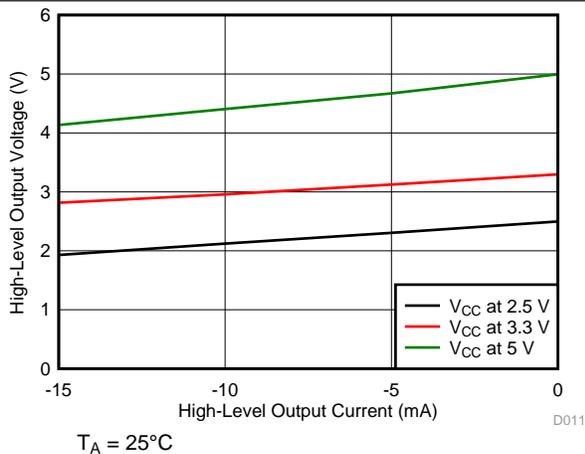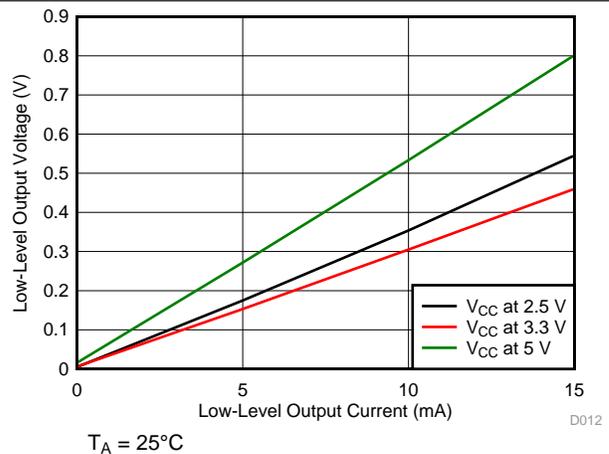

Figure 9. High-Level Output Voltage vs High-level Output Current

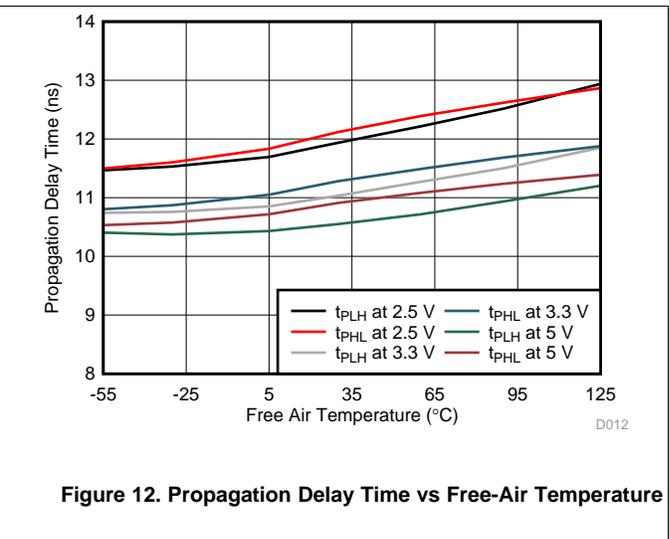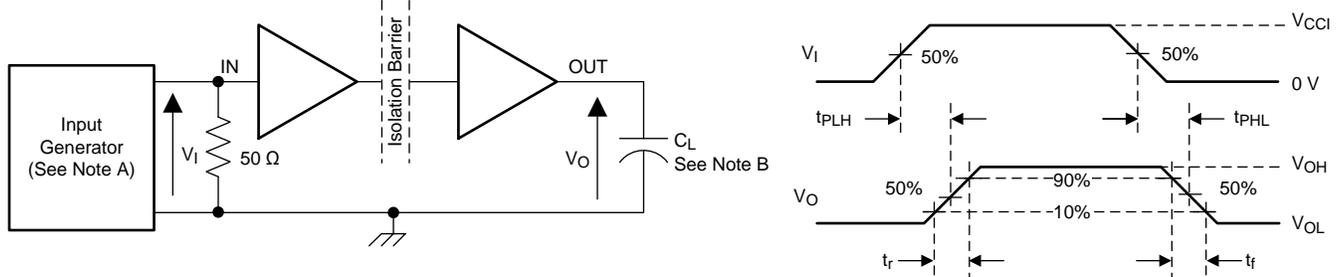**Figure 10. Low-Level Output Voltage vs Low-Level Output Current**

Typical Characteristics (continued)

Figure 11. Power Supply Undervoltage Threshold vs Free-Air Temperature

**Figure 12. Propagation Delay Time vs Free-Air Temperature**
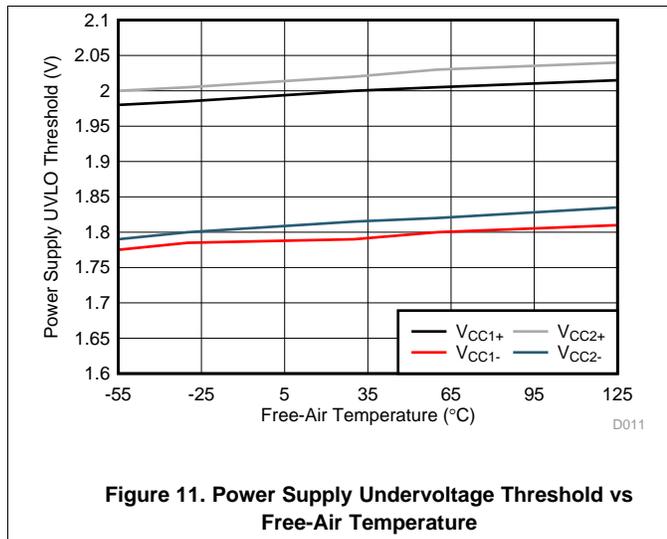
7 Parameter Measurement Information

Copyright © 2016, Texas Instruments Incorporated

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
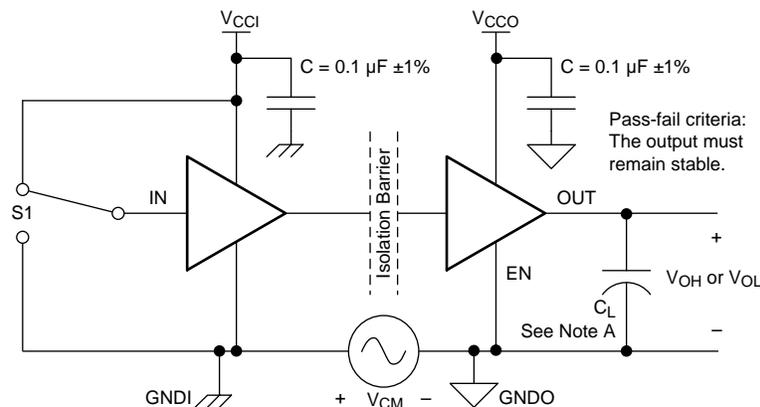
Figure 13. Switching Characteristics Test Circuit and Voltage Waveforms
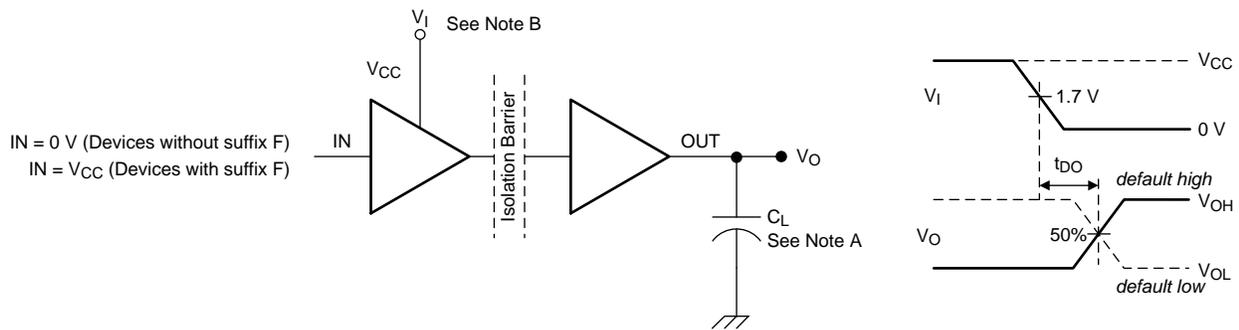
Copyright © 2016, Texas Instruments Incorporated

A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 14. Default Output Delay Time Test Circuit and Voltage Waveforms

Copyright © 2016, Texas Instruments Incorporated

A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 15. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO772x family of devices has an ON-OFF Keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 16, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram
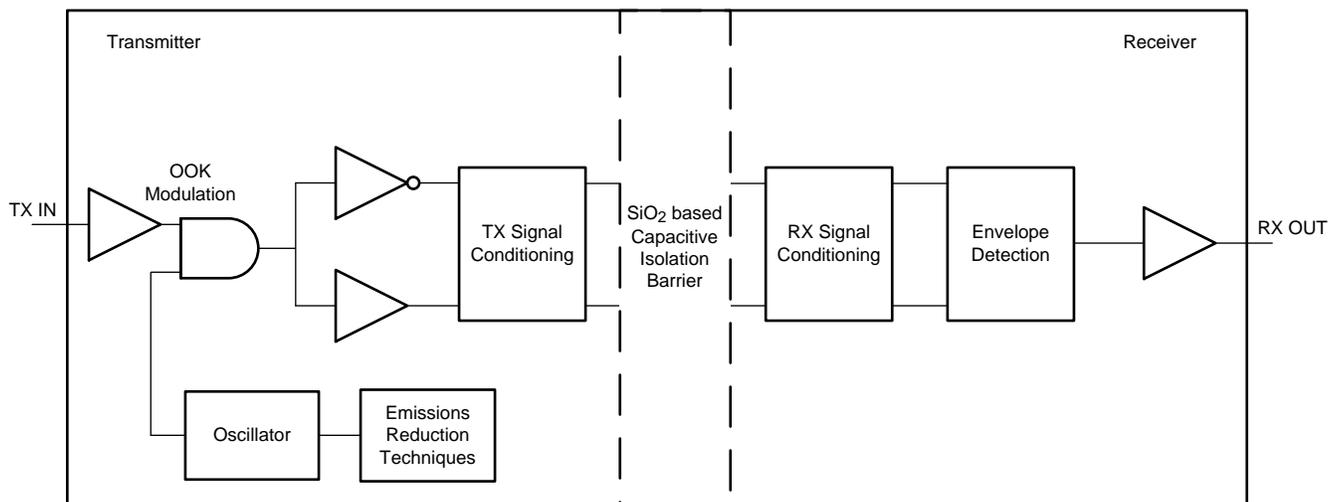
Copyright © 2016, Texas Instruments Incorporated

Figure 16. Conceptual Block Diagram of a Digital Capacitive Isolator

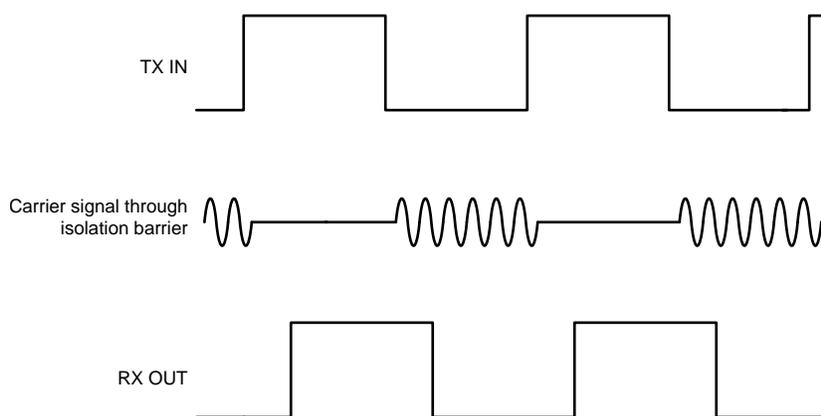Figure 17 shows a conceptual detail of how the ON/OFF keying scheme works.

Figure 17. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISO772x family of devices is available in two channel configurations and default output state options to enable a variety of application uses. Table 1 lists the device features of the ISO772x.

Table 1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION[1]
ISO7720	100 Mbps	2 Forward, 0 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7720F	100 Mbps	2 Forward, 0 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7721	100 Mbps	1 Forward, 1 Reverse	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}
ISO7721F	100 Mbps	1 Forward, 1 Reverse	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				D-8	3000 V_{RMS} / 4242 V_{PK}

(1) See the *Regulatory Information* section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO772x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

Product Folder Links: *ISO7720 ISO7721*

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO772x .

Table 2. Function Table[1]

V_{CCI}	V_{CCO}	INPUT (INx)[2]	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to the default high logic state. Default is *High* for ISO772x and *Low* for ISO772x with F suffix.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO772x and *Low* for ISO772x with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined[3]. When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up ($V_{CC} \geq 2.25$ V); PD = Powered down ($V_{CC} \leq 1.7$ V); X = Irrelevant; H = High level; L = Low level

(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.

(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics
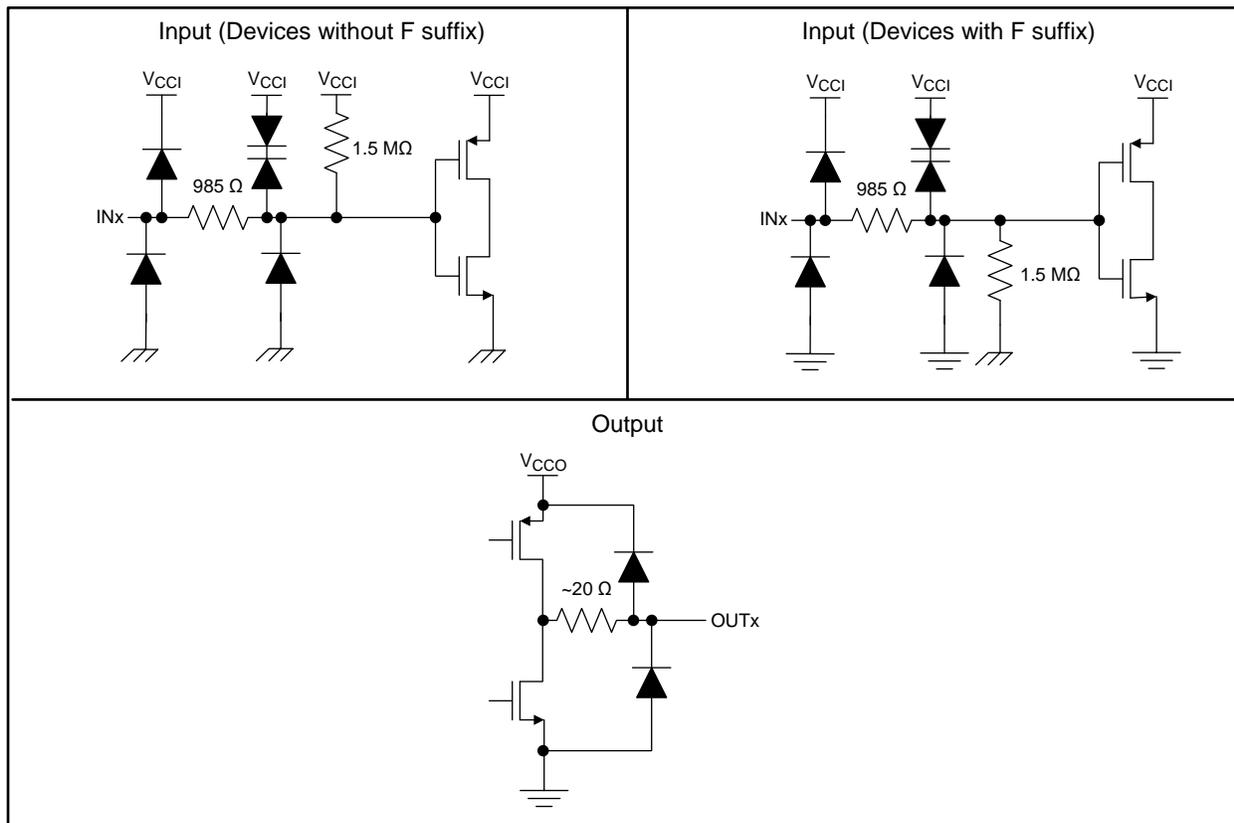
Copyright © 2016, Texas Instruments Incorporated

Figure 18. Device I/O Schematics

9 Applications and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO772x devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7721 device can be used with Texas Instruments' mixed signal microcontroller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-mA to 20-mA current loop.
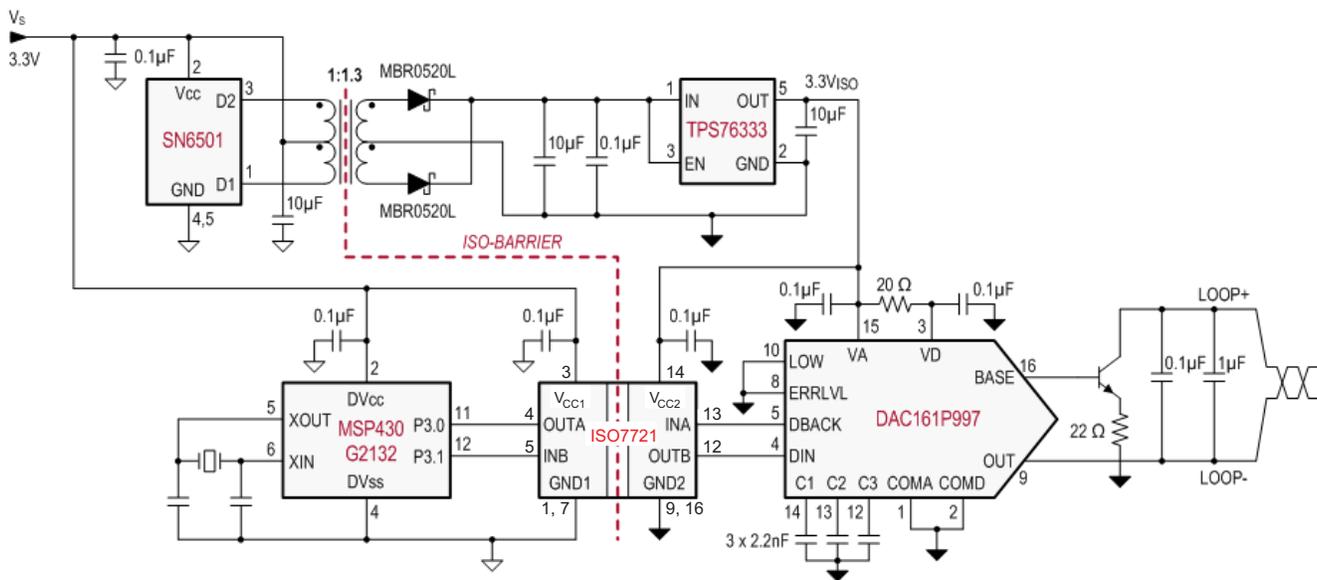
Copyright © 2016, Texas Instruments Incorporated

Figure 19. Isolated 4-mA to 20-mA Current Loop

9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO772x devices only require two external bypass capacitors to operate.
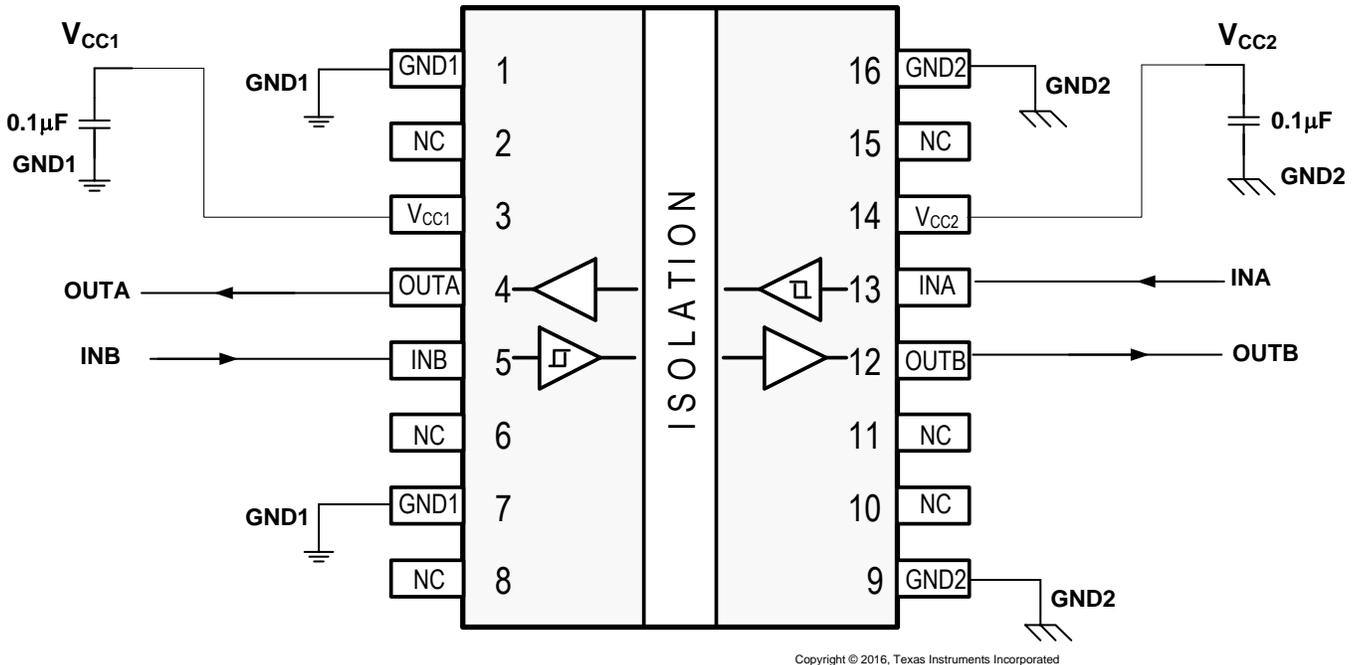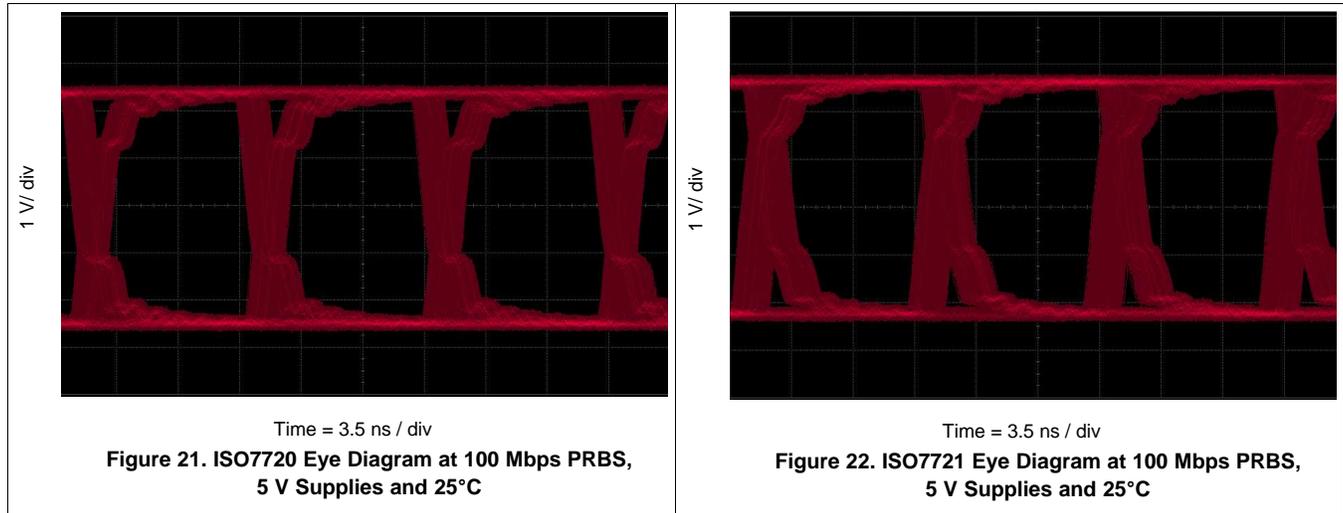

Copyright © 2016, Texas Instruments Incorporated

Figure 20. Typical ISO7721 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO772x family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.

Time = 3.5 ns / div

Figure 21. ISO7720 Eye Diagram at 100 Mbps PRBS, 5 V Supplies and 25°C

Time = 3.5 ns / div

Figure 22. ISO7721 Eye Diagram at 100 Mbps PRBS, 5 V Supplies and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in the SN6501 data sheet (SLLSEA0) or SN6505A data sheet (SLLSEP9).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 23). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the application note, *Digital Isolator Design Guide* (SLLA284).

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.
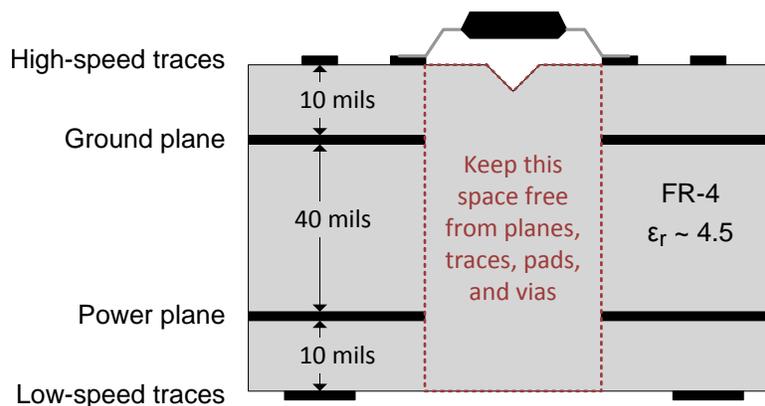
11.2 Layout Example

Figure 23. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:
- *DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops*, SNAS515
- *Isolation Glossary*, SLLA353
- MSP430G2132 *Mixed Signal Microcontroller*, SLAS723
- *SN6501 Transformer Driver for Isolated Power Supplies*, SLLSEA0
- TPS76333 *Low-Power 150-mA Low-Dropout Linear Regulators*, SLVS181

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7720	Click here	Click here	Click here	Click here	Click here
ISO7721	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC

4221445/B 04/2014
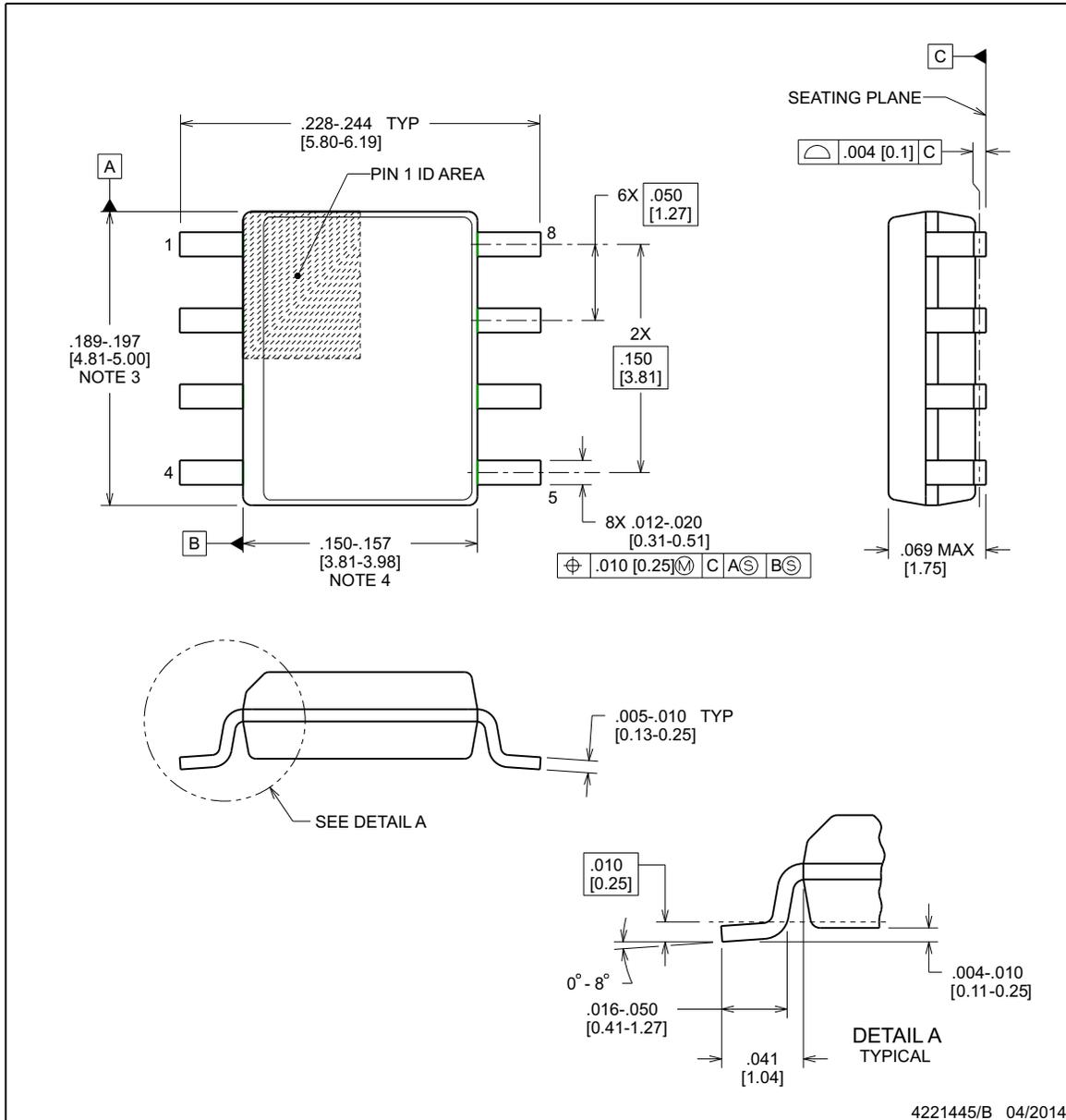
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

Submit Documentation Feedback   25

Product Folder Links: *ISO7720 ISO7721*

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height
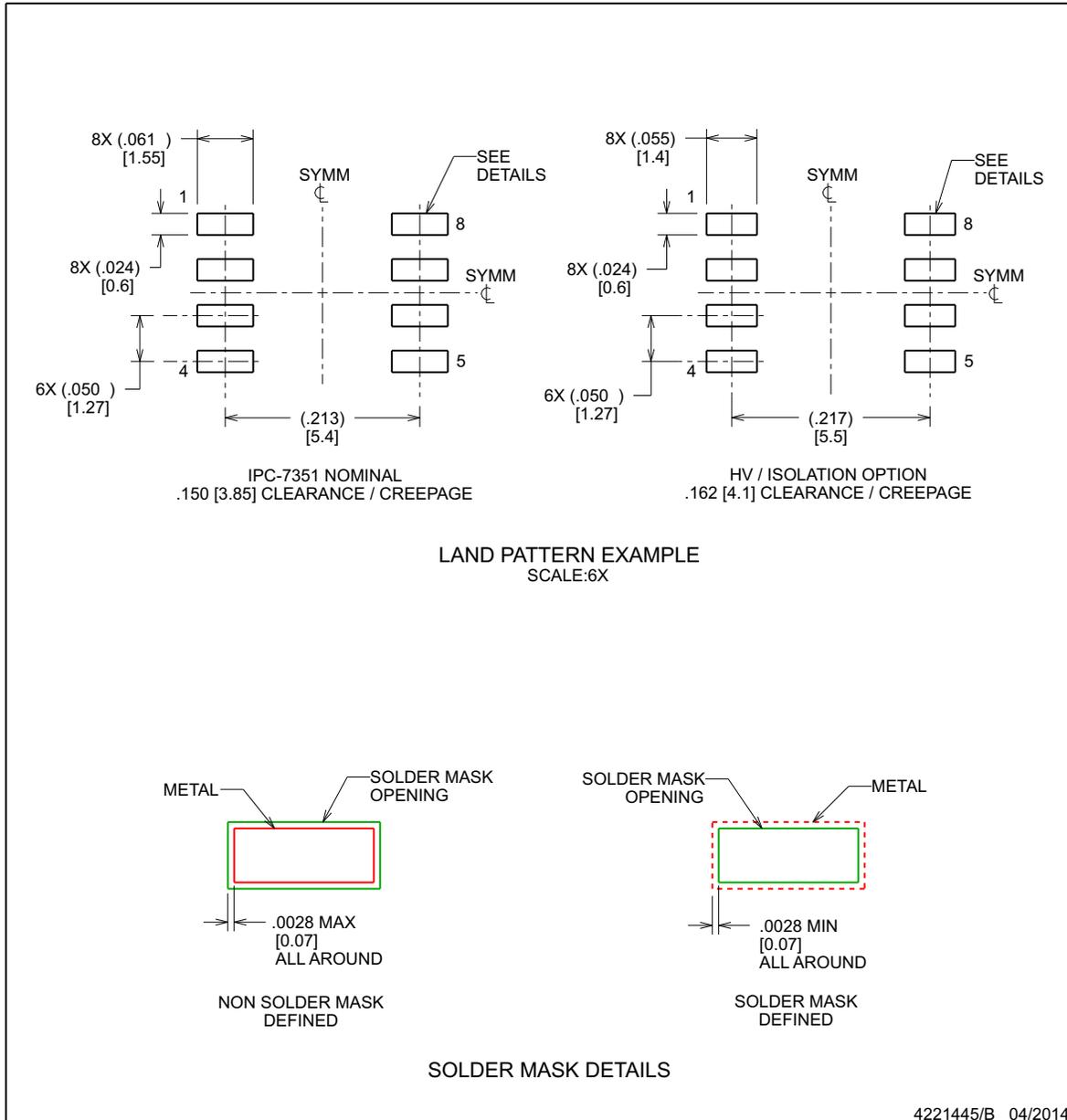
SOIC

8X (.061)
[1.55]

SYMM

SEE DETAILS

8X (.024)
[0.6]

SYMM

6X (.050)
[1.27]

(.213)
[5.4]

IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

8X (.055)
[1.4]

SYMM

SEE DETAILS

8X (.024)
[0.6]

SYMM

6X (.050)
[1.27]

(.217)
[5.5]

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
SCALE:6X

METAL

SOLDER MASK
OPENING

.0028 MAX
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
OPENING

METAL

.0028 MIN
[0.07]
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/B   04/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Product Folder Links: *ISO7720 ISO7721*

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SOIC

IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/B 04/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Product Folder Links: *ISO7720 ISO7721*

TEXAS
INSTRUMENTS

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC

10.63 / 9.97 TYP

PIN 1 ID AREA

14X 1.27

2X 8.89

16X 0.51 / 0.31

10.5 / 10.1 NOTE 3

7.6 / 7.4 NOTE 4

⊕ 0.25Ⓜ C AⓈ BⓈ

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

(1.4)

0.3 / 0.1

DETAIL A
TYPICAL

4221009/B 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

Product Folder Links: *ISO7720 ISO7721*

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height
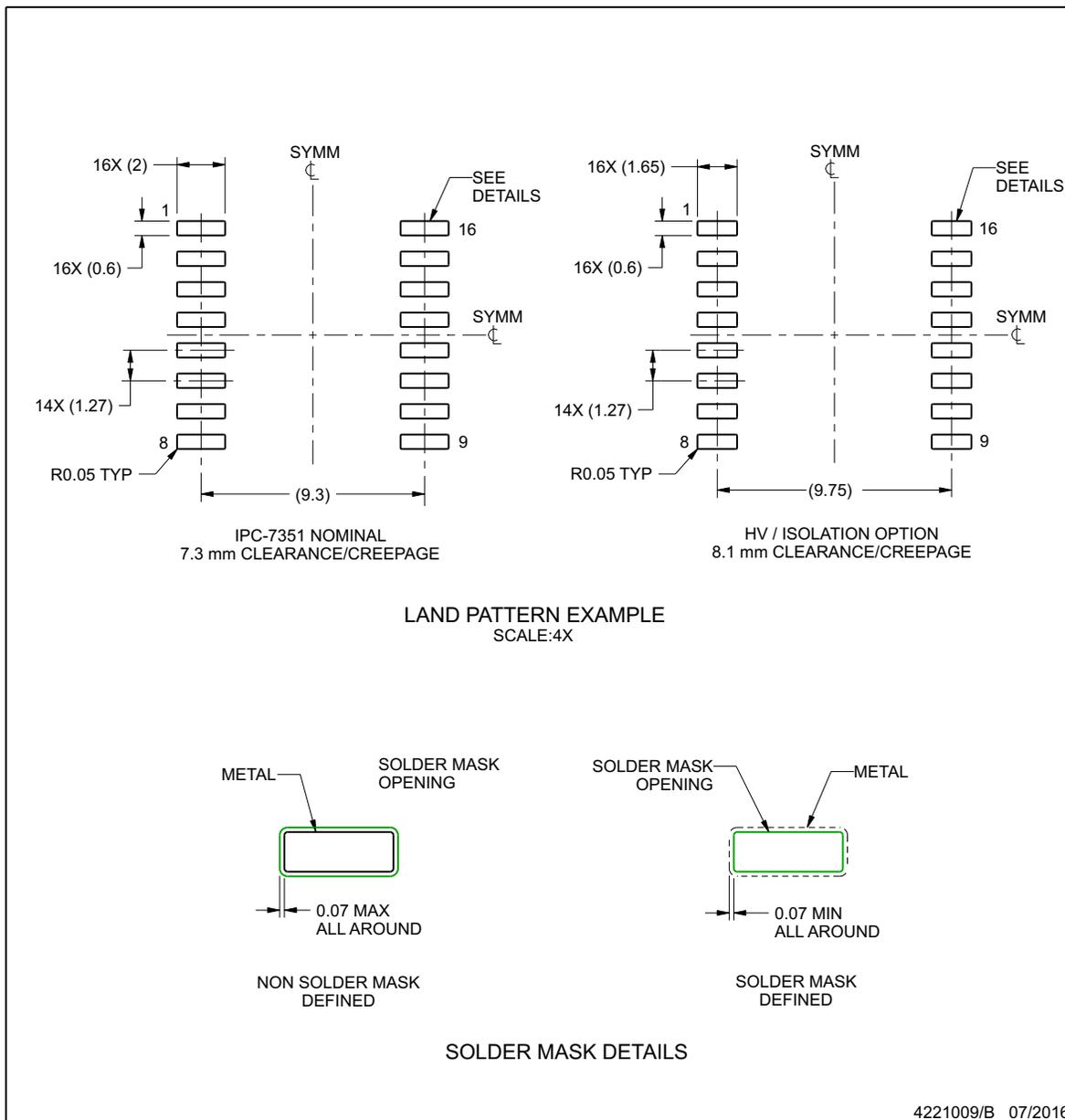
SOIC

LAND PATTERN EXAMPLE
SCALE:4X

IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER MASK DETAILS

NON SOLDER MASK DEFINED
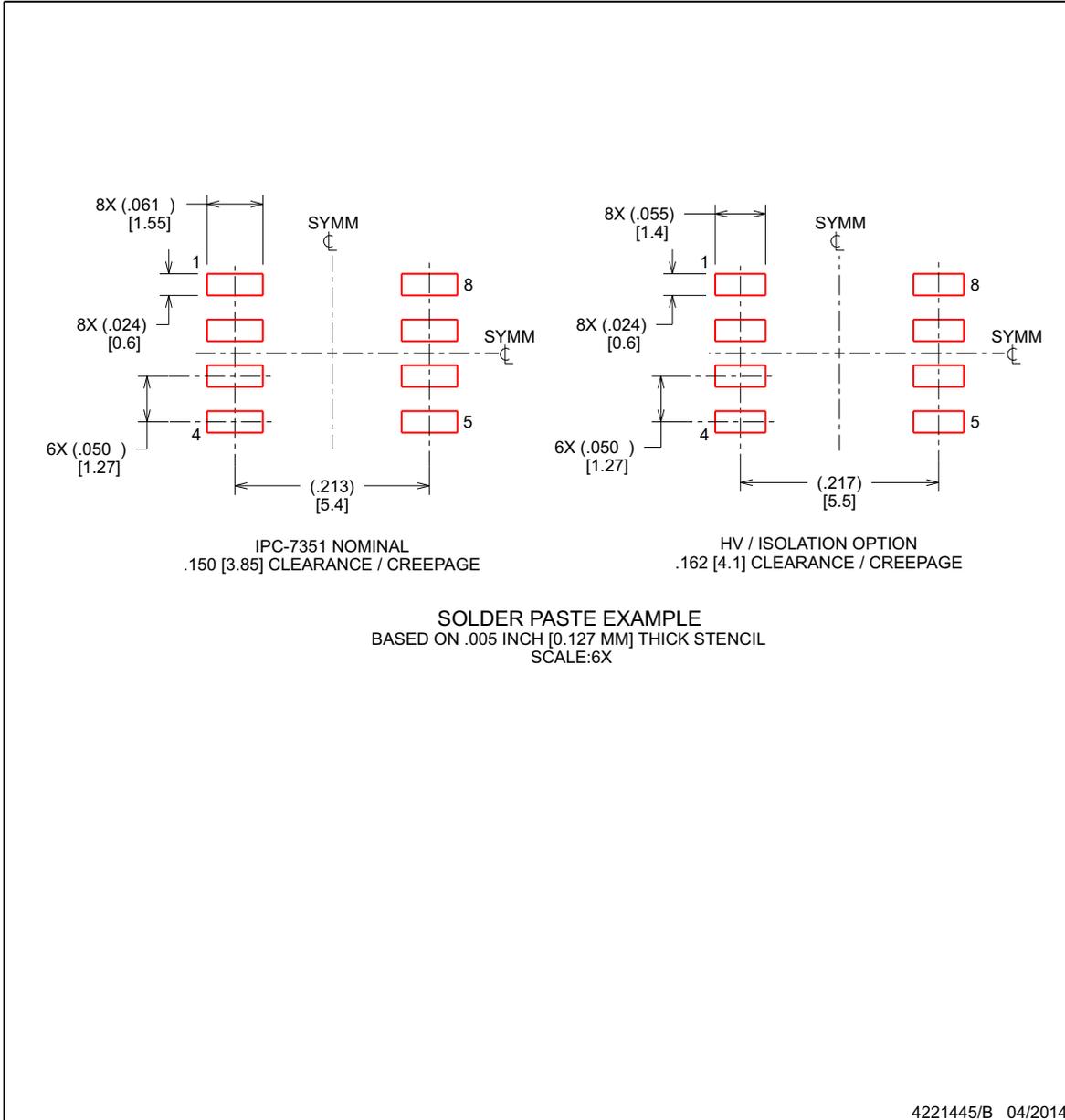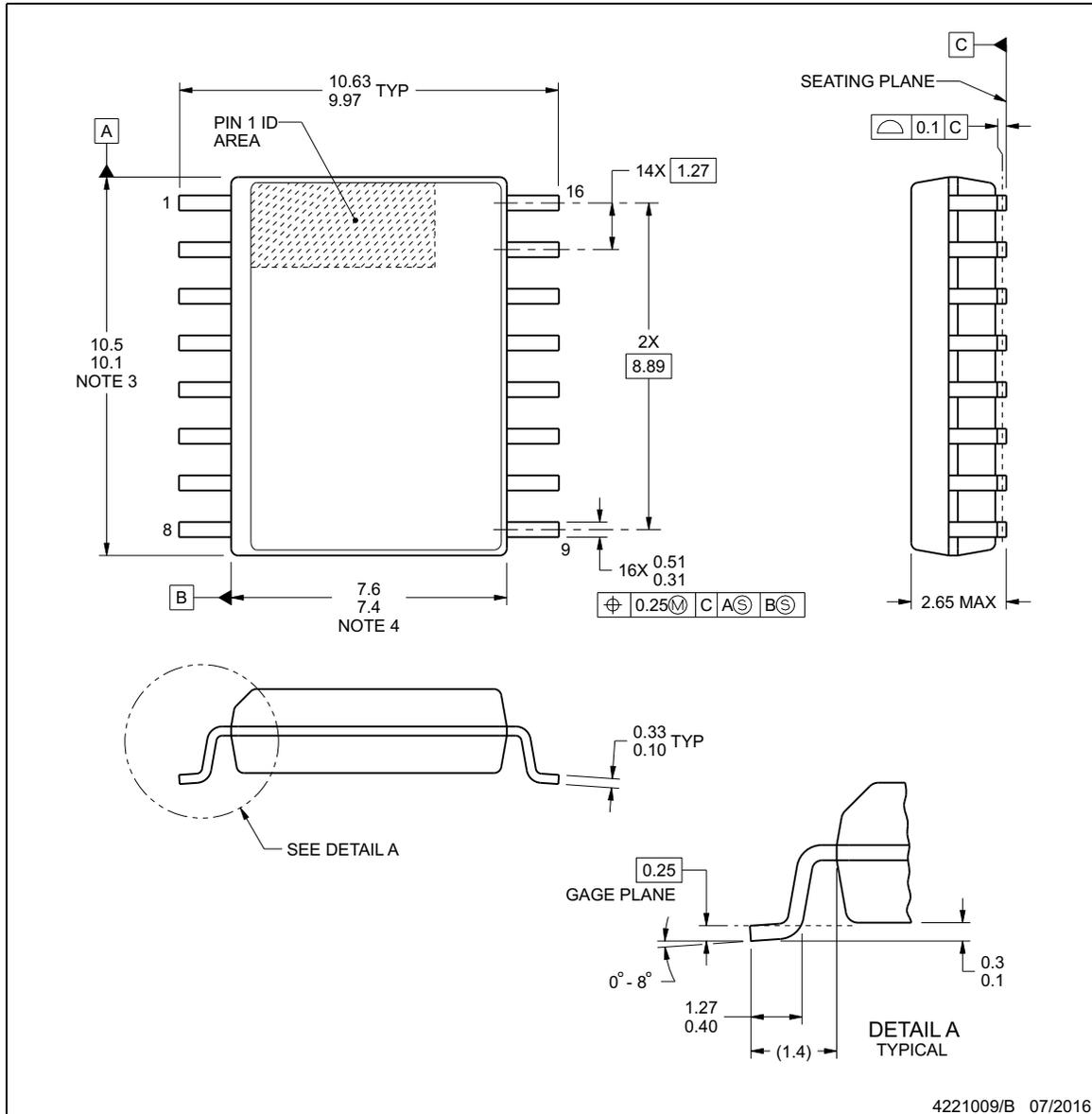
SOLDER MASK DEFINED

4221009/B   07/2016

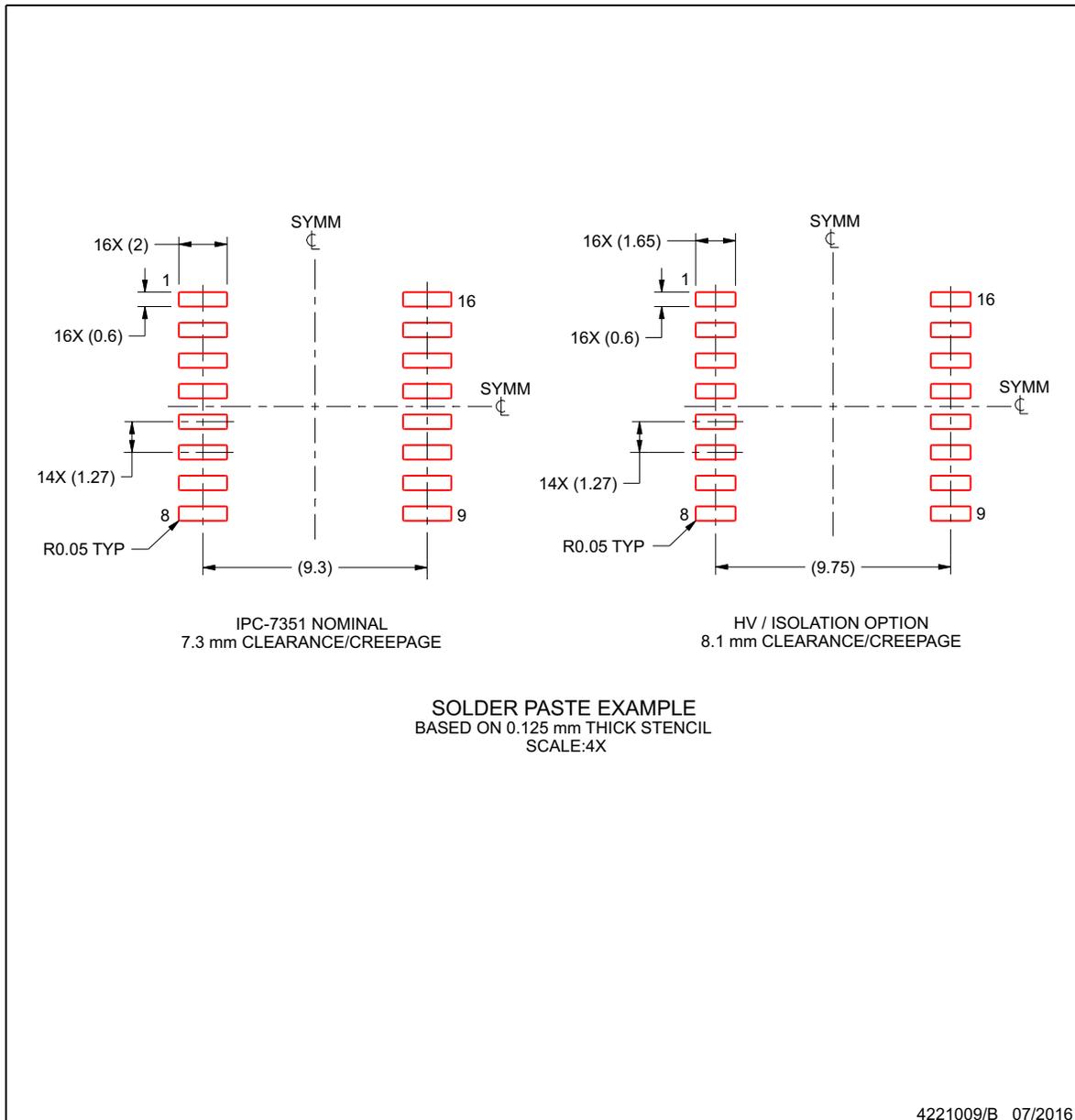NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Submit Documentation Feedback   29

Product Folder Links: ISO7720 ISO7721

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC

IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B   07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Product Folder Links: *ISO7720 ISO7721*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7720D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-55 to 125	7720	
ISO7720DR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
ISO7720DW	PREVIEW	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	
ISO7720DWR	PREVIEW	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	
ISO7720FD	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-55 to 125	7720F	
ISO7720FDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
ISO7720FDW	PREVIEW	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	
ISO7720FDWR	PREVIEW	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	
ISO7721D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-55 to 125	7721	
ISO7721DR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
ISO7721DW	PREVIEW	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	
ISO7721DWR	PREVIEW	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	
ISO7721FD	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-55 to 125	7721F	
ISO7721FDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI	-55 to 125		
ISO7721FDW	PREVIEW	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	
ISO7721FDWR	PREVIEW	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		