Six-Input Channel Analog Front End

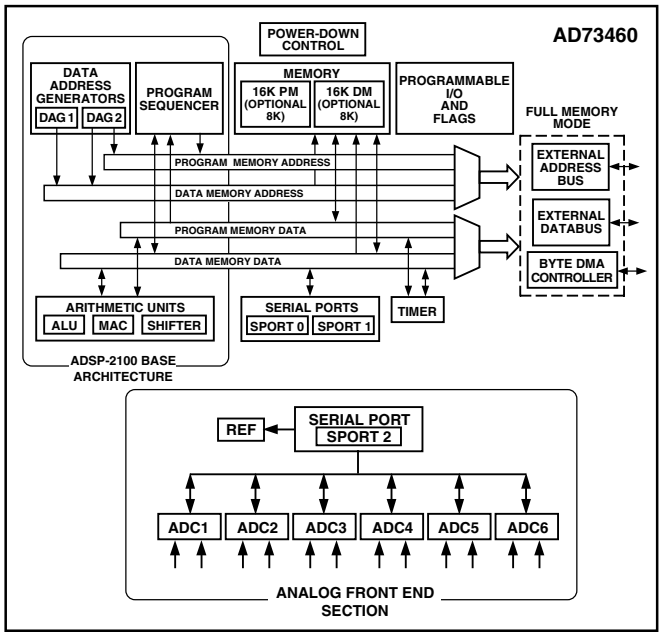
AD73460

FEATURES

AFE PERFORMANCE
- 6 16-Bit A/D Converters
- Programmable Input Sample Rate
- Simultaneous Sampling
- 72 dB SNR
- 64 kS/s Maximum Sample Rate
- –80 dB Crosstalk
- Low Group Delay (25 μs Typ per ADC Channel)
- Programmable Input Gain
- Single Supply Operation
- On-Chip Reference

DSP PERFORMANCE
- 19 ns Instruction Cycle Time @ 3.3 V, 52 MIPS Sustained Performance
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- 3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Multifunction Instructions
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 400 Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD73460 is a six-input channel analog front end processor for general-purpose applications including industrial power metering or multichannel analog inputs. It features six 16-bit A/D conversion channels, each of which provides 72 dB signal-to-noise ratio over a dc-to-2 kHz signal bandwidth. Each channel also features a programmable input gain amplifier (PGA) with gain settings in eight stages from 0 dB to 38 dB.

The AD73460 is particularly suitable for industrial power metering since each channel samples synchronously, ensuring that there is no (phase) delay between the conversions. The AD73460 also features low group delay conversions on all channels.

An on-chip reference voltage of 1.25 V is included. The sampling rate of the device is programmable with separate settings offering 64 kHz, 32 kHz, 16 kHz, and 8 kHz sampling rates (from a master clock of 16.384 MHz), while the serial port (SPORT2) allows easy expansion of the number of input channels by cascading an extra AFE external to the AD73460.

The AD73460's DSP engine combines the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The AD73460-80 integrates 80K bytes of on-chip memory configured as 16K words (24-bit) of program RAM and 16K (16-bit) of data RAM. The AD73460-40 integrates 40K bytes of on-chip memory configured as 8K words (24-bit) of program RAM and 8K (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The AD73460 is available in a 119-ball PBGA package.

REV. A

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SPECIFICATIONS

(AVDD = 3.0 V to 3.6 V; DVDD = 3.0 V to 3.6 V; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, f_{SCLK} = 8.192 MHz, f_S = 8 kHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	AD73460B Min	Typ	Max	Unit	Test Conditions/Comments[1]
REFERENCE					
REFCAP					
Absolute Voltage, V_{REFCAP}	1.125	1.25	1.375	V	
REFCAP TC		50		ppm/°C	0.1 µF Capacitor Required from REFCAP to AGND2
REFOUT					
Typical Output Impedance		130		Ω	
Absolute Voltage, V_{REFOUT}	1.125	1.25	1.375	V	Unloaded
Minimum Load Resistance	1			kΩ	
Maximum Load Capacitance			100	pF	
ADC SPECIFICATIONS					
Maximum Input Range at VIN[2, 3]		1.644		V p-p	Measured Differentially
		–2.85		dBm	
Nominal Reference Level at VIN		1.1413		V p-p	Measured Differentially
(0 dBm0)		–6.02		dBm	
Absolute Gain					
PGA = 0 dB	–1.2		+0.6	dB	1.0 kHz
Signal to (Noise + Distortion)					
PGA = 0 dB		71		dB	0 Hz to 4 kHz; f_S = 8 kHz; f_{IN} = 60 Hz
PGA = 0 dB	70	72		dB	0 Hz to 2 kHz; f_S = 8 kHz; f_{IN} = 60 Hz
Total Harmonic Distortion					
PGA = 0 dB		–77	–72	dB	
Intermodulation Distortion		–76		dB	PGA = 0 dB
Idle Channel Noise		–70		dB	PGA = 0 dB
Crosstalk ADC-to-ADC		–83		dB	ADC1 Input at Idle ADC2 to ADC6 Input Signal: 1.0 kHz
		–95		dB	ADC1 Input at Idle ADC2 to ADC6 Input Signal: 60 Hz
DC Offset	–30	+10	+45	mV	PGA = 0 dB
Power Supply Rejection		–55		dB	Input Signal Level at AVDD and DVDD Pins 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	64 kHz Output Sample Rate
		50		µs	32 kHz Output Sample Rate
		95		µs	16 kHz Output Sample Rate
		190		µs	8 kHz Output Sample Rate
Input Resistance at VIN[2, 4]		25		kΩ[6]	DMCLK = 16.384 MHz
Phase Mismatch		0.15		Degrees	f_{IN} = 1 kHz
		0.01		Degrees	f_{IN} = 60 Hz
FREQUENCY RESPONSE					
(ADC)[7] Typical Output					
Frequency (Normalized to f_S)					
0		0		dB	
0.03125		–0.1		dB	
0.0625		–0.25		dB	
0.125		–0.6		dB	
0.1875		–1.4		dB	
0.25		–2.8		dB	
0.3125		–4.5		dB	
0.375		–7.0		dB	
0.4375		–9.5		dB	
> 0.5		< –12.5		dB	

AD73460–SPECIFICATIONS

(AVDD = 3.0 V to 3.6 V; DVDD = 3.0 V to 3.6 V; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, f_{SAMP} = 64 kHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	AD73460B Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
V_{INH}, Input High Voltage	V_{DD} – 0.8		V_{DD}	V	
V_{INL}, Input Low Voltage	0		0.8	V	
I_{IH}, Input Current			10	μA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	V_{DD} – 0.4		V_{DD}	V	|IOUT| ≤ 100 μA
V_{OL}, Output Low Voltage	0		0.4	V	|IOUT| ≤ 100 μA
Three-State Leakage Current	–10		+10	μA	
POWER SUPPLIES					
AVDD1, AVDD2	3.0		3.6	V	
DVDD	3.0		3.6	V	
I_{DD}[8]					See Table I

NOTES

[1]Operating temperature range is as follows: –40°C to +85°C. Therefore, T_{MIN} = –40°C and T_{MAX} = +85°C.

[2]Test conditions: Input PGA set for 0 dB gain (unless otherwise noted).

[3]At input to sigma-delta modulator of ADC.

[4]Guaranteed by design.

[5]Overall group delay will be affected by the sample rate and the external digital filtering.

[6]The ADC's input impedance is inversely proportional to DMCLK and is approximated by: (4×10^{11})/DMCLK.

[7]Frequency response of ADC measured with input at audio reference level (the input level that produces an output level of –10 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.

[8]Test Conditions: no load on digital inputs, analog inputs ac-coupled to ground.

Specifications subject to change without notice.

Table I. AFE Section Current Summary (AVDD = DVDD = 3.3 V)

Conditions	Total Current (Max)	SE	MCLK ON	Comments
REFCAP Only On	1.0	0	No	REFOUT Disabled
REFCAP and REFOUT Only On	4.5	0	No	
All Sections On	26.5	1	Yes	REFOUT Enabled
All Sections Off	1.5	0	Yes	MCLK Active Levels Equal to 0 V and DVDD
All Sections Off	0.1	0	No	Digital Inputs Static and Equal to 0 V or DVDD

The above values are in mA. MCLK = 16.384 MHz; SCLK = 16.384 MHz.

SPECIFICATIONS (AVDD = 3.0 V to 3.6 V; DVDD = 3.0 V to 3.6 V; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, f_{SAMP} = 64 kHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter		Test Conditions	Min	Typ	Max	Unit
DSP SECTION						
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min			0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4			V
		@ V_{DD} = min, I_{OH} = –100 μA[6]	V_{DD} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max, V_{IN} = V_{DD} max			10	μA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max, V_{IN} = 0 V			10	μA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = V_{DD} max[8]			10	μA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V[8]			10	μA
I_{DD}	Supply Current (Idle)[9]	@ V_{DD} = 3.3 V				
		t_{CK} = 19 ns[10]		14		mA
		t_{CK} = 25 ns[10]		12		mA
		t_{CK} = 30 ns[10]		10		mA
I_{DD}	Supply Current (Dynamic)[11]	@ V_{DD} = 3.3 V, T_{AMB} = 25°C				
		t_{CK} = 19 ns[10]		54		mA
		t_{CK} = 25 ns[10]		43		mA
		t_{CK} = 30 ns[10]		37		mA
C_I	Input Pin Capacitance[3, 6, 12]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

NOTES

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PWDACK}}$, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all AD73460 outputs are CMOS compatible and will drive to V_{DD} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.

[8]0 V on $\overline{\text{BR}}$.

[9]Idle refers to AD73460 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[11]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.

[12]Applies to PBGA package type.

[13]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

AD73460
TIMING CHARACTERISTICS–AFE SECTION*

(AVDD = 3 V to 3.6 V; DVDD = 3 V to 3.6 V; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_A = –40°C to +85°C	Unit	Description
Clock Signals			See Figure 1
t_1	61	ns min	AMCLK Period
t_2	24.4	ns min	AMCLK Width High
t_3	24.4	ns min	AMCLK Width Low
Serial Port			See Figures 3 and 4
t_4	t_1	ns min	SCLK Period (SCLK = AMCLK)
t_5	$0.4 \times t_1$	ns min	SCLK Width High
t_6	$0.4 \times t_1$	ns min	SCLK Width Low
t_7	20	ns min	SDI/SDIFS Setup Before SCLK Low
t_8	0	ns min	SDI/SDIFS Hold After SCLK Low
t_9	10	ns max	SDOFS Delay from SCLK High
t_{10}	10	ns max	SDOFS Hold After SCLK High
t_{11}	10	ns max	SDO Hold After SCLK High
t_{12}	10	ns max	SDO Delay from SCLK High
t_{13}	30	ns max	SCLK Delay from AMCLK

*For details of the DSP section timing, please refer to the ADSP-2185L data sheet and the *ADSP-2100 Family User's Manual,* Third Edition.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

AVDD, DVDD to GND . . . . . –0.3 V to +4.6 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to AVDD + 0.3 V
Operating Temperature Range
  Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –20°C to +125°C
Maximum Junction Temperature . . . . . 150°C
PBGA, θ_{JA} Thermal Impedance . . . . . 25°C/W
Reflow Soldering
  Maximum Temperature . . . . . 225°C
  Time at Maximum Temperature . . . . . 15 sec

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD73460BB-80	–40°C to +85°C	119-Ball Plastic Grid Array	B-119
AD73460BB-40	–40°C to +85°C	119-Ball Plastic Grid Array	B-119

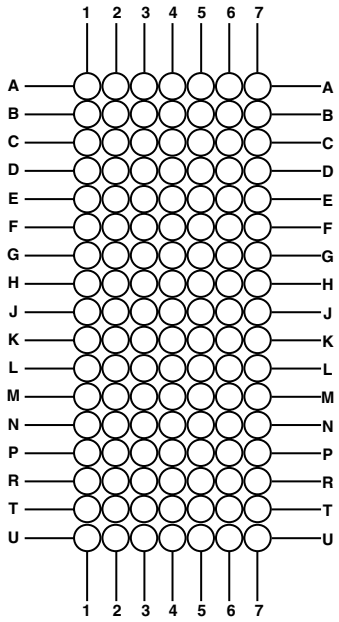
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD73460 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PBGA BALL CONFIGURATIONS

PBGA Number	Ball Name	PBGA Number	Ball Name	PBGA Number	Ball Name	PBGA Number	Ball Name
A1	$\overline{\text{IRQE}}$/*PF4*	E3	RFS0	J5	D22	N7	D13
A2	$\overline{\text{DMS}}$	E4	A3/IAD2	J6	D21	P1	$\overline{\text{EBR}}$
A3	VDD(INT)	E5	A2/IAD1	J7	D20	P2	D0/IAD13
A4	CLKIN	E6	A1/IAD0	K1	$\overline{\text{ELOUT}}$	P3	DVDD
A5	A11/IAD10	E7	A0	K2	ELIN	P4	DGND
A6	A7/IAD6	F1	DR0	K3	$\overline{\text{EINT}}$	P5	$\overline{\text{ARESET}}$
A7	A4/IAD3	F2	SCLK0	K4	D19	P6	SCLK2
B1	$\overline{\text{IRQL0}}$/*PF5*	F3	DT1	K5	D18	P7	MCLK
B2	$\overline{\text{PMS}}$	F4	$\overline{\text{PWDACK}}$	K6	D17	R1	SDO
B3	$\overline{\text{WR}}$	F5	$\overline{\text{BGH}}$	K7	D16	R2	SDOFS
B4	XTAL	F6	Mode A/*PF0*	L1	$\overline{\text{BG}}$	R3	SDIFS
B5	A12/IAD11	F7	Mode B/*PF1*	L2	D3/$\overline{\text{IACK}}$	R4	SDI
B6	A8/IAD7	G1	TFS1	L3	D5/IAL	R5	SE
B7	A5/IAD4	G2	RFS1	L4	D8	R6	REFCAP
C1	$\overline{\text{IRQL1}}$/*PF6*	G3	DR1	L5	D9	R7	REFOUT
C2	$\overline{\text{IOMS}}$	G4	GND	L6	D12	T1	VINN2
C3	$\overline{\text{RD}}$	G5	$\overline{\text{PWD}}$	L7	D15	T2	VINP2
C4	VDD(EXT)	G6	VDD(EXT)	M1	$\overline{\text{EBG}}$	T3	VINN1
C5	A13/IAD12	G7	Mode C/*PF2*	M2	D2/IAD15	T4	VINP1
C6	A9/IAD8	H1	SCLK1	M3	D4/$\overline{\text{IS}}$	T5	VINN3
C7	GND	H2	$\overline{\text{ERESET}}$	M4	D7/$\overline{\text{IWR}}$	T6	VINP3
D1	$\overline{\text{IRQ2}}$/*PF7*	H3	$\overline{\text{RESET}}$	M5	VDD(EXT)	T7	VINN4
D2	$\overline{\text{CMS}}$	H4	PF3	M6	D11	U1	AGND
D3	$\overline{\text{BMS}}$	H5	FL0	M7	D14	U2	AVDD
D4	CLKOUT	H6	FL1	N1	$\overline{\text{BR}}$	U3	VINP6
D5	GND	H7	FL2	N2	D1/IAD14	U4	VINN6
D6	A10/IAD9	J1	$\overline{\text{EMS}}$	N3	VDD(INT)	U5	VINP5
D7	A6/IAD5	J2	EE	N4	D6/$\overline{\text{IRD}}$	U6	VINN5
E1	DT0	J3	ECLK	N5	GND	U7	VINP4
E2	TFS0	J4	D23	N6	D10		

PBGA BALL CONFIGURATION



PIN FUNCTION DESCRIPTIONS[1]

Mnemonic	Function
VINP1	Analog Input to the Positive Terminal of Input Channel 1
VINN1	Analog Input to the Negative Terminal of Input Channel 1
VINP2	Analog Input to the Positive Terminal of Input Channel 2
VINN2	Analog Input to the Negative Terminal of Input Channel 2
VINP3	Analog Input to the Positive Terminal of Input Channel 3
VINN3	Analog Input to the Negative Terminal of Input Channel 3
VINP4	Analog Input to the Positive Terminal of Input Channel 4
VINN4	Analog Input to the Negative Terminal of Input Channel 4
VINP5	Analog Input to the Positive Terminal of Input Channel 5
VINN5	Analog Input to the Negative Terminal of Input Channel 5
VINP6	Analog Input to the Positive Terminal of Input Channel 6
VINN6	Analog Input to the Negative Terminal of Input Channel 6
REFOUT	Buffered Reference Output, which has a nominal value of 1.25 V
REFCAP	A bypass capacitor to AGND2 of 0.1 μF is required for the on-chip reference. The capacitor should be fixed to this pin. This pin can be overdriven by an external reference if required.
AVDD	Analog Power Supply Connection
AGND	Analog Ground/Substrate Connection
DGND	Digital Ground/Substrate Connection
DVDD	Digital Power Supply Connection
$\overline{\text{ARESET}}$	Active Low Reset Signal. This input resets the analog front end of the AD73460, resetting the control registers and clearing the digital circuitry.
SCLK2	Output Serial Clock whose Rate Determines the Serial Transfer Rate to/from the AFE. It is used to clock data or control information to and from the serial port (SPORT2). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number—this integer number being the product of the external master clock rate divider and the serial clock rate divider.
MCLK	Master Clock Input of the Analog Front End. MCLK is driven from an external clock signal.
SDO	Serial Data Output of the AD73460. Both data and control information may be output on this pin and are clocked on the positive edge of SCLK2. SDO is in three-state when no information is being transmitted and when SE is low.
SDOFS	Framing Signal Output for SDO Serial Transfers. The frame sync is one bit wide and is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK2. SDOFS is in three-state when SE is low.
SDIFS	Framing Signal Input for SDI Serial Transfers. The frame sync is one bit wide and is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK2 and is ignored when SE is low.
SDI	Serial Data Input of the AD73460. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK2. SDI is ignored when SE is low.
SE	SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK2 is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low); however, the timing counters and other internal registers are at their reset values.
$\overline{\text{RESET}}$	(Input) Processor Reset Input
$\overline{\text{BR}}$	(Input) Bus Request Input
$\overline{\text{BG}}$	(Output) Bus Grant Output
$\overline{\text{BGH}}$	(Output) Bus Grant Hung Output
$\overline{\text{DMS}}$	(Output) Data Memory Select Output
$\overline{\text{PMS}}$	(Output) Program Memory Select Output
$\overline{\text{IOMS}}$	(Output) Memory Select Output
$\overline{\text{BMS}}$	(Output) Byte Memory Select Output
$\overline{\text{CMS}}$	(Output) Combined Memory Select Output
$\overline{\text{RD}}$	(Output) Memory Read Enable Output

PIN FUNCTION DESCRIPTIONS[1] (continued)

Mnemonic	Function
$\overline{WR}$	(Output) Memory Write Enable Output
$\overline{IRQ2}$/	(Input) Edge- or Level-Sensitive Interrupt
PF7	(Input/Output) Request.[2] Programmable I/O Pin
$\overline{IRQL0}$/	(Input) Level-Sensitive Interrupt Requests[2]
PF6	(Input/Output) Programmable I/O Pin
$\overline{IRQL1}$/	(Input) Level-Sensitive Interrupt Requests[2]
PF5	(Input/Output) Programmable I/O Pin
$\overline{IRQE}$/	(Input) Edge-Sensitive Interrupt Requests[2]
PF4	(Input/Output) Programmable I/O Pin
Mode D/	(Input) Mode Select Input—Checked Only During RESET
PF3	(Input/Output) Programmable I/O Pin During Normal Operation
Mode C/	(Input) Mode Select Input—Checked Only During RESET
PF2	(Input/Output) Programmable I/O Pin During Normal Operation
Mode B/	(Input) Mode Select Input—Checked Only During RESET
PF1	(Input/Output) Programmable I/O Pin During Normal Operation
Mode A/	(Input) Mode Select Input—Checked Only During RESET
PF0	(Input/Output) Programmable I/O Pin During Normal Operation
CLKIN, XTAL	(Inputs) Clock or Quartz Crystal Input
CLKOUT	(Output) Processor Clock Output
SPORT0	(Inputs/Outputs) Serial Port I/O Pins
SPORT1	(Inputs/Outputs) Serial Port I/O Pins
$\overline{IRQ1}$:0	(Inputs) Edge- or Level-Sensitive Interrupts,
FI	(Input) Flag In[3]
FO	(Output) Flag Out[3]
$\overline{PWD}$	(Input) Power-Down Control Input
$\overline{PWDACK}$	(Output) Power-Down Control Output
FL0, FL1, FL2	(Outputs) Output Flags
A13 to A0	(Output) Address Output Pins for Program, Data, Byte, and I/O Space
D23 to D0	(Input/Output) Data I/O Pins for Program, Data, Byte, and I/O Space
VDD and GND	Power and Ground
EZ-ICE Port	(Inputs/Outputs) For Emulation Use
$\overline{ERESET}$	
$\overline{EMS}$	
EE	
ECLK	
$\overline{ELOUT}$	
ELIN	
$\overline{EINT}$	
$\overline{EBR}$	
$\overline{EBG}$	

NOTES
[1]Refer to the ADSP-2185L data sheet for a detailed description of the DSP pins.
[2]Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.
[3]SPORT configuration determined by the DSP System Control Register. Software configurable.

ARCHITECTURE OVERVIEW

The AD73460 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The AD73460 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

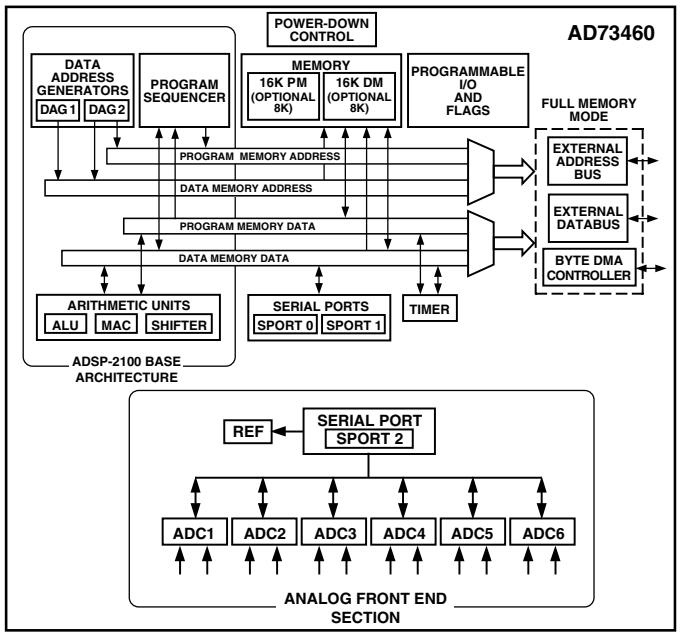


Figure 1. Functional Block Diagram

Figure 1 is an overall block diagram of the AD73460. The processor section contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the AD73460 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two databuses (PMD and DMD) share a single external databus. Byte memory space and I/O memory space also share the external buses.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The AD73460 can respond to 11 interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master RESET signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

ANALOG FRONT END

The analog front end (AFE) of the AD73460 is configured as a separate block that is normally connected to either SPORT0 or SPORT1 of the DSP section. As it is not hardwired to either SPORT, users have total flexibility in how they wish to allocate system resources to support the AFE. It is also possible to further expand the number of analog input channels connected to the SPORT by cascading an AD73360 device external to the AD73460.

The AFE is configured as six input channels. It comprises six independent encoder channels, each featuring signal conditioning, programmable gain amplifier, sigma-delta A/D converter, and decimator sections. Each of these sections is described in further detail later in this data sheet. All channels share a common internal reference whose nominal value is 1.25 V. Figure 2 shows a block diagram of the AFE section of the AD73460. It shows six input channels along with a common reference. Communication to all channels is handled by the SPORT2 block, which interfaces to either SPORT0 or SPORT1 of the DSP section.

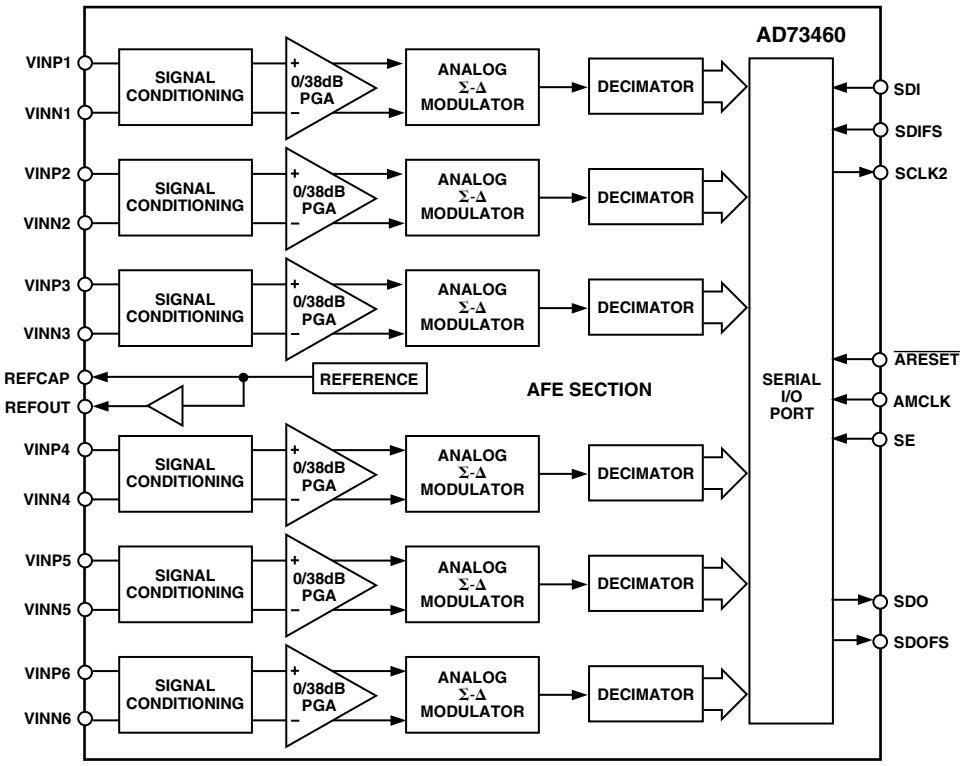


Figure 2. Functional Block Diagram of Analog Front End

FUNCTIONAL DESCRIPTION—AFE

Encoder Channel

Each encoder channel consists of a signal conditioner, a switched capacitor PGA, and a sigma-delta analog-to-digital converter (ADC). An on-board digital filter, which forms part of the sigma-delta ADC, also performs critical system-level filtering. Due to the high level of oversampling, the input antialias requirements are reduced such that a simple single pole RC stage is sufficient to give adequate attenuation in the band of interest.

Signal Conditioner

Each analog channel has an independent signal conditioning block. This allows the analog input to be configured by the user depending on whether differential or single-ended mode is used.

Programmable Gain Amplifier

Each encoder section's analog front end comprises a Switched Capacitor PGA that also forms part of the sigma-delta modulator. The SC sampling frequency is DMCLK/8. The PGA, whose programmable gain settings are shown in Table II, may be used to increase the signal level applied to the ADC from low output sources such as microphones, and can be used to avoid placing external amplifiers in the circuit. The input signal level to the sigma-delta modulator should not exceed the maximum input voltage permitted.

The PGA gain is set by bits IGS0, IGS1, and IGS2 in control Registers D, E, and F.

Table II. PGA Settings for the Encoder Channel

IxGS2	IxGS1	IxGS0	Gain (dB)
0	0	0	0
0	0	1	6
0	1	0	12
0	1	1	18
1	0	0	20
1	0	1	26
1	1	0	32
1	1	1	38

ADC

Each channel has its own ADC consisting of an analog sigma-delta modulator and a digital antialiasing decimation filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a DMCLK/8 rate. This bit stream, representing the analog input signal, is input to the antialiasing decimation filter. The decimation filter reduces the sample rate and increases the resolution.

Analog Sigma-Delta Modulator

The AD73460 input channels employ a sigma-delta conversion technique, which provides a high resolution 16-bit output with system filtering being implemented on-chip.

Sigma-delta converters employ a technique known as oversampling, where the sampling rate is many times the highest frequency of interest. In the case of the AD73460, the initial sampling rate of the sigma-delta modulator is DMCLK/8. The main effect of oversampling is that the quantization noise is spread over a very wide bandwidth, up to $f_S/2$ = DMCLK/16 (Figure 3a). This means that the noise in the band of interest is much reduced. Another complementary feature of sigma-delta converters is the use of a technique called noise-shaping. This technique has the effect of pushing the noise from the band of interest to an out-of-band position (Figure 3b). The combination of these techniques, followed by the application of a digital filter, reduces the noise in-band sufficiently to ensure good dynamic performance from the part (Figure 3c).

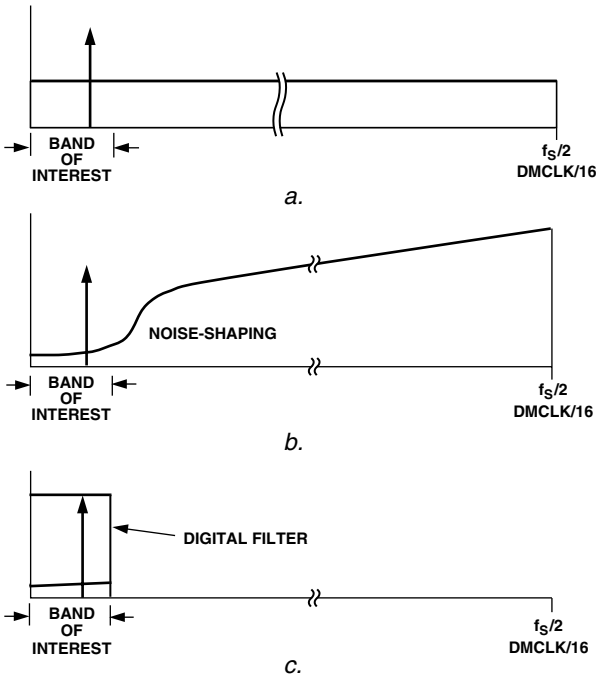


Figure 3. Sigma-Delta Noise Reduction

Figure 4 shows the various stages of filtering that are employed in a typical AD73460 application. In Figure 4a we see the transfer function of the external analog antialias filter. Even though it is a single RC pole, its cutoff frequency is sufficiently far away from the initial sampling frequency (DMCLK/8) that it takes care of any signals that could be aliased by the sampling frequency. This also shows the major difference between the initial oversampling rate and the bandwidth of interest. In Figure 4b, the signal and noise-shaping responses of the sigma-delta modulator are shown. The signal response provides further rejection of any high frequency signals while the noise-shaping will push the inherent quantization noise to an out-of-band position. The detail of Figure 4c shows the response of the digital decimation filter (sinc-cubed response) with nulls every multiple of DMCLK/256, which is the decimation filter update rate. The final detail in Figure 4d shows the application of a final antialias filter in the DSP engine. This has the advantage of being implemented according to the user's requirements and available MIPS. The filtering in Figures 4a through 4c is implemented in the AD73460.

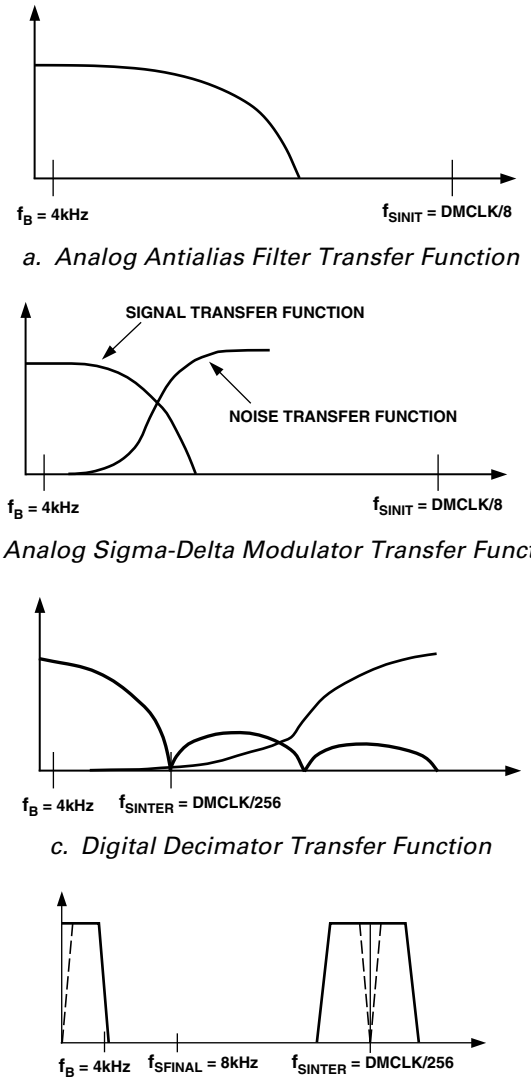


Figure 4. DC Frequency Responses

Decimation Filter

The digital filter used in the AD73460 carries out two important functions. Firstly, it removes the out-of-band quantization noise, which is shaped by the analog modulator, and secondly, it decimates the high frequency bit stream to a lower rate 15-bit word. The antialiasing decimation filter is a sinc-cubed digital filter that reduces the sampling rate from DMCLK/8 to DMCLK/256, and increases the resolution from a single bit to 15 bits. Its Z transform is given as: $[(1–Z^{–32})/(1–Z^{–1})]^3$. This ensures a minimal group delay of 25 µs.

ADC Coding

The ADC coding scheme is in two's complement format (see Figure 5). The output words are formed by the decimation filter, which grows the word length from the single-bit output of the sigma-delta modulator to a 15-bit word, which is the final output of the ADC block. In 16-bit Data Mode, this value is left shifted with the LSB being set to 0. For input values equal to or greater than positive full scale however, the output word is set at 0x7FFF, which has the LSB set to 1. In mixed Control/Data Mode, the resolution is fixed at 15 bits, with the MSB of the 16-bit transfer being used as a flag bit to indicate either control or data in the frame.

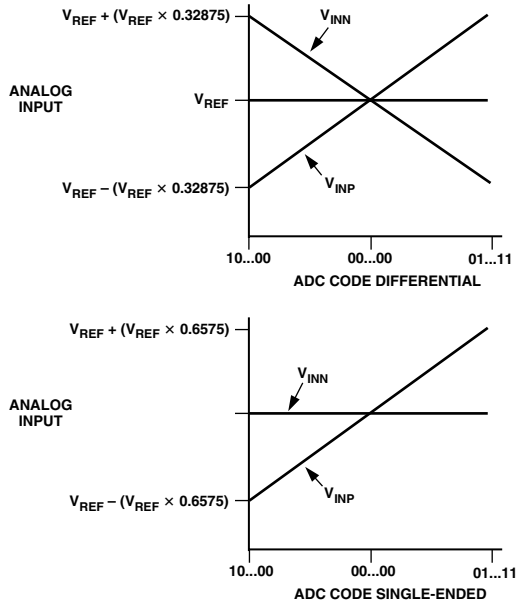


Figure 5. ADC Transfer Function

Voltage Reference

The AD73460 contains an internal band gap reference that provides a low noise, temperature-compensated reference to the ADCs. The reference has a nominal value of 1.25 V and is available on the REFCAP pin. A buffered version of the reference is available on the REFOUT pin and can be used to bias external analog circuitry if required. The reference output (REFOUT) can be enabled by setting the RU bit (CRC:6) in Control Register C. It is possible to overdrive the internal reference by connecting an external reference to the REFCAP pin. This may be required when a different value of reference or better temperature coefficient is required. The current sink and source capabilities of the REFCAP pin must be taken into consideration when overdriving the reference. When a lower value of external reference is required, it must have sufficient current sink capability to override the current source capabilities of the REFCAP pin. When a higher value of external reference is required, it can usually be connected directly to the REFCAP pin as the pin can typically only sink 0.25 mA before its value changes. Figure 6 shows a plot of REFCAP voltage versus current. Note that the negative values indicate that the external reference is sinking current to provide the required reference voltage.

AFE Serial Port (SPORT2)

The AFE section communicates with DSP via the bidirectional synchronous serial port (SPORT2), which interfaces to either SPORT0 or SPORT1 of the DSP section. SPORT2 is used to transmit and receive digital data and control information. An additional external AFE can be cascaded to the internal AFE (up to a limit of seven) to provide additional input channels if required.

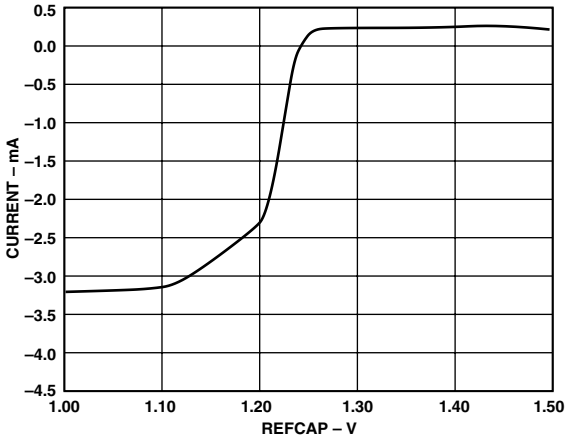


Figure 6. REFCAP Voltage vs. Current

In both transmit and receive modes, data is transferred at the serial clock (SCLK2) rate with the MSB being transferred first. Communication between the AFE section and DSP section must always be initiated by the AFE section (AFE is in master mode, DSP is in slave mode). This ensures that there is no collision between input data and output samples.

SPORT2 Overview

SPORT2 is a flexible, full-duplex, synchronous serial port whose protocol has been designed to allow an additional AFE to be connected in cascade to the DSP section. It has a very flexible architecture that can be configured by programming two of the internal control registers in each AFE block. SPORT2 has three distinct modes of operation: Control Mode, Data Mode, and Mixed Control/Data Mode.

NOTE: As each AFE has its own SPORT section, the register settings in each must be programmed. The registers that control SPORT and sample rate operation (CRA and CRB) must be programmed with the same values to ensure correct operation.

In Control Mode (CRA:0 = 0), the device's internal configuration can be programmed by writing to the eight internal control registers. In this mode, control information can be written to or read from the AFE. In Data Mode (CRA:0 = 1), any information that is sent to the AFE is ignored, while the encoder section (ADC) data is read from the device. In this mode, only ADC data is read from the device. Mixed mode (CRA:0 = 1 and CRA:1 = 1) allows the user to send control information and receive either control information or ADC data. This is achieved by using the MSB of the 16-bit frame as a flag bit. Mixed mode reduces the resolution to 15 bits with the MSB being used to indicate whether the information in the 16-bit frame is control information or ADC data.

SPORT2 features a single 16-bit serial register that is used for both input and output data transfers. As the input and output data must share the same register, some precautions must be observed. The primary precaution is that no information must be written to SPORT2 without reference to an output sample event, which is when the serial register will be overwritten with the latest ADC sample word. Once SPORT2 starts to output the latest ADC word, it is safe for the DSP to write new control

words to the AFE. In certain configurations, data can be written to the device to coincide with the output sample being shifted out of the serial register—see section on interfacing devices. The serial clock rate (CRB:2–3) defines how many 16-bit words can be written to a device before the next output sample event will happen.

The SPORT2 block diagram, shown in Figure 7, details the blocks associated with AFE including the eight control registers (A–H), external AMCLK to internal DMCLK divider and serial clock divider. The divider rates are controlled by the setting of Control Register B. The AFE features a master clock divider that allows users the flexibility of dividing externally available high frequency DSP clocks to generate a lower frequency master clock internally in the AFE, which may be more suitable for either serial transfer or sampling rate requirements. The master clock divider has five divider options (÷1 default condition, ÷2, ÷3, ÷4, ÷5) that are set by loading the master clock divider field in Register B with the appropriate code (see Table VIII). Once the internal device master clock (DMCLK) has been set using the master clock divider, the sample rate and serial clock settings are derived from DMCLK.

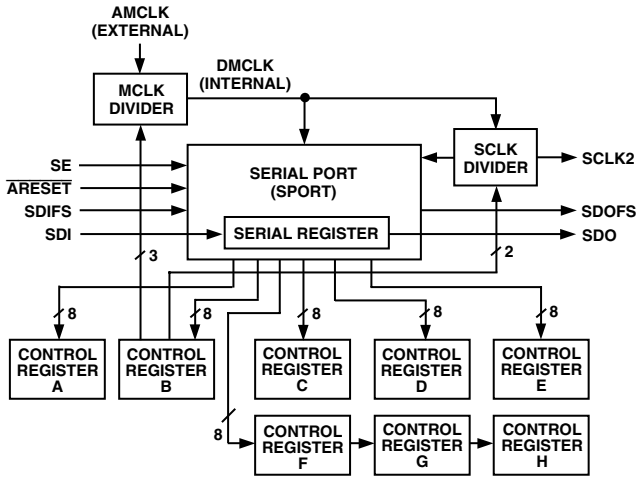


Figure 7. SPORT Block Diagram

SPORT2 can work at four different serial clock (SCLK) rates: chosen from DMCLK, DMCLK/2, DMCLK/4, or DMCLK/8, where DMCLK is the internal or device master clock resulting from the external or pin master clock being divided by the master clock divider. Care should be taken when selecting Master Clock, Serial Clock, and Sample Rate divider settings to ensure that there is sufficient time to read all the data from the AFE before the next sample interval.

SPORT Register Maps

There are eight control registers for the AFE, each eight bits wide. Table VI shows the control register map for the AFE. The first two control registers, CRA and CRB, are reserved for controlling SPORT2. They hold settings for parameters such as bit rate, internal master clock rate, and device count. If multiple AFEs are cascaded, registers CRA and CRB on both devices must be programmed with the same setting to ensure correct operation. The other six registers, CRC through CRH, are used to hold control settings for the Reference, Power Control, ADC channel, and PGA sections of the device. It is not necessary that the contents of CRC through CRH on each AFE are similar. Control registers are written to on the negative edge of SCLK2.

Master Clock Divider

The AFE features a programmable master clock divider that allows the user to reduce an externally available master clock, at pin AMCLK, by one of the ratios 1, 2, 3, 4, or 5 to produce an internal master clock signal (DMCLK) that is used to calculate the sampling and serial clock rates. The master clock divider is programmable by setting CRB:4–6. Table III shows the division ratio corresponding to the various bit settings. The default divider ratio is divide-by-one.

Table III. DMCLK (Internal) Rate Divider Settings

MCD2	MCD1	MCD0	DMCLK Rate
0	0	0	AMCLK
0	0	1	AMCLK/2
0	1	0	AMCLK/3
0	1	1	AMCLK/4
1	0	0	AMCLK/5
1	0	1	AMCLK
1	1	0	AMCLK
1	1	1	AMCLK

Serial Clock Rate Divider

The AFE features a programmable serial clock divider that allows users to match the serial clock (SCLK2) rate of the data to that of the DSP. The maximum SCLK2 rate available is DMCLK and the other available rates are: DMCLK/2, DMCLK/4 and DMCLK/8. The slowest rate (DMCLK/8) is the default SCLK2 rate. The serial clock divider is programmable by setting bits CRB:2–3. Table IV shows the serial clock rate corresponding to the various bit settings.

Table IV. SCLK Rate Divider Settings

SCD1	SCD0	SCLK2 Rate
0	0	DMCLK/8
0	1	DMCLK/4
1	0	DMCLK/2
1	1	DMCLK

Decimation Rate Divider

The AFE features a programmable decimation rate divider that allows users flexibility in matching the AFE's ADC sample rates to the needs of the DSP software. The maximum sample rate available is DMCLK/256, and the other available rates are DMCLK/512, DMCLK/1024, and DMCLK/2048. The slowest rate (DMCLK/2048) is the default sample rate. The sample rate divider is programmable by setting bits CRB:0–1. Table V shows the sample rate corresponding to the various bit settings.

Table V. Decimation Rate Divider Settings

DR1	DR0	Sample Rate
0	0	DMCLK/2048
0	1	DMCLK/1024
1	0	DMCLK/512
1	1	DMCLK/256

Table VI. Control Register Map

Address (Binary)	Name	Description	Type	Width	Reset Setting (Hex)
000	CRA	Control Register A	R/$\overline{W}$	8	0x00
001	CRB	Control Register B	R/$\overline{W}$	8	0x00
010	CRC	Control Register C	R/$\overline{W}$	8	0x00
011	CRD	Control Register D	R/$\overline{W}$	8	0x00
100	CRE	Control Register E	R/$\overline{W}$	8	0x00
101	CRF	Control Register F	R/$\overline{W}$	8	0x00
110	CRG	Control Register G	R/$\overline{W}$	8	0x00
111	CRH	Control Register H	R/$\overline{W}$	8	0x00

Table VII. Control Word Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C/$\overline{D}$	R/$\overline{W}$	DEVICE ADDRESS			REGISTER ADDRESS			REGISTER DATA							

Control	Frame	Description
Bit 15	CONTROL/$\overline{DATA}$	When set high, it signifies a control word in Program or Mixed Program/Data Modes. When set low, it signifies an invalid control word in Program Mode.
Bit 14	READ/$\overline{WRITE}$	When set low, it tells the device that the data field is to be written to the register selected by the register field setting provided the address field is zero. When set high, it tells the device that the selected register is to be written to the data field in the serial register and that the new control word is to be output from the device via the serial output.
Bits 13–11	DEVICE ADDRESS	This 3-bit field holds the address information. Only when this field is zero is a device selected. If the address is not zero, it is decremented and the control word is passed out of the device via the serial output.
Bits 10–8	REGISTER ADDRESS	This 3-bit field is used to select one of the eight control registers on the AD73460.
Bits 7–0	REGISTER DATA	This 8-bit field holds the data that is to be written to or read from the selected register provided the address field is zero.

CONTROL REGISTER A

Table VIII. Control Register A Description

7	6	5	4	3	2	1	0
$\overline{RESET}$	DC2	DC1	DC0	SLB	RES	MM	DATA/$\overline{PGM}$

Bit	Name	Description
0	DATA/$\overline{PGM}$	Operating Mode (0 = Program; 1 = Data Mode)
1	MM	Mixed Mode (0 = OFF; 1 = Enabled)
2	Reserved	Must Be Programmed to Zero (0)
3	SLB	SPORT Loop-Back Mode (0 = OFF; 1 = Enabled)
4	DC0	Device Count (Bit 0)
5	DC1	Device Count (Bit 1)
6	DC2	Device Count (Bit 2)
7	$\overline{RESET}$	Software Reset (0 = OFF; 1 = Initiates Reset)

Table IX. Control Register B Description

CONTROL REGISTER B

7	6	5	4	3	2	1	0
CEE	MCD2	MCD1	MCD0	SCD1	SCD0	DR1	DR0

Bit	Name	Description
0	DR0	Decimation Rate (Bit 0)
1	DR1	Decimation Rate (Bit 1)
2	SCD0	Serial Clock Divider (Bit 0)
3	SCD1	Serial Clock Divider (Bit 1)
4	MCD0	Master Clock Divider (Bit 0)
5	MCD1	Master Clock Divider (Bit 1)
6	MCD2	Master Clock Divider (Bit 2)
7	CEE	Control Echo Enable (0 = OFF; 1 = Enabled)

Table X. Control Register C Description

CONTROL REGISTER C

7	6	5	4	3	2	1	0
RES	RU	PUREF	RES	RES	RES	RES	GPU

Bit	Name	Description
0	GPU	Global Power-Up Device (0 = Power Down; 1 = Power Up)
1	Reserved	Must Be Programmed to Zero (0)
2	Reserved	Must Be Programmed to Zero (0)
3	Reserved	Must Be Programmed to Zero (0)
4	Reserved	Must Be Programmed to Zero (0)
5	PUREF	REF Power (0 = Power Down; 1 = Power Up)
6	RU	REFOUT Use (0 = Disable REFOUT; 1 = Enable REFOUT)
7	Reserved	Must Be Programmed to Zero (0)

Table XI. Control Register D Description

CONTROL REGISTER D

7	6	5	4	3	2	1	0
PUI2	I2GS2	I2GS1	I2GS0	PUI1	I1GS2	I1GS1	I1GS0

Bit	Name	Description
0	I1GS0	ADC1: Input Gain Select (Bit 0)
1	I1GS1	ADC1: Input Gain Select (Bit 1)
2	I1GS2	ADC1: Input Gain Select (Bit 2)
3	PUI1	Power Control (ADC1): 1 = ON, 0 = OFF
4	I2GS0	ADC2: Input Gain Select (Bit 0)
5	I2GS1	ADC2: Input Gain Select (Bit 1)
6	I2GS2	ADC2: Input Gain Select (Bit 2)
7	PUI2	Power Control (ADC2): 1 = ON, 0 = OFF

Table XII. Control Register E Description

CONTROL REGISTER E

7	6	5	4	3	2	1	0
PUI4	**I4GS2**	**I4GS1**	**I4GS0**	**PUI3**	**I3GS2**	**I3GS1**	**I3GS0**

Bit	Name	Description
0	I3GS0	ADC3: Input Gain Select (Bit 0)
1	I3GS1	ADC3: Input Gain Select (Bit 1)
2	I3GS2	ADC3: Input Gain Select (Bit 2)
3	PUI3	Power Control (ADC3): 1 = ON, 0 = OFF
4	I4GS0	ADC4: Input Gain Select (Bit 0)
5	I4GS1	ADC4: Input Gain Select (Bit 1)
6	I4GS2	ADC4: Input Gain Select (Bit 2)
7	PUI4	Power Control (ADC4): 1 = ON, 0 = OFF

Table XIII. Control Register F Description

CONTROL REGISTER F

7	6	5	4	3	2	1	0
PUI6	**I6GS2**	**I6GS1**	**I6GS0**	**PUI5**	**I5GS2**	**I5GS1**	**I5GS0**

Bit	Name	Description
0	I5GS0	ADC5: Input Gain Select (Bit 0)
1	I5GS1	ADC5: Input Gain Select (Bit 1)
2	I5GS2	ADC5: Input Gain Select (Bit 2)
3	PUI5	Power Control (ADC5): 1 = ON, 0 = OFF
4	I6GS0	ADC6: Input Gain Select (Bit 0)
5	I6GS1	ADC6: Input Gain Select (Bit 1)
6	I6GS2	ADC6: Input Gain Select (Bit 2)
7	PUI6	Power Control (ADC6): 1 = ON, 0 = OFF

Table XIV. Control Register G Description

CONTROL REGISTER G

7	6	5	4	3	2	1	0
SEEN	**RMOD**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**

Bit	Name	Description
0	CH1	Channel 1 Select
1	CH2	Channel 2 Select
2	CH3	Channel 3 Select
3	CH4	Channel 4 Select
4	CH5	Channel 5 Select
5	CH6	Channel 6 Select
6	RMOD	Reset Analog Modulator
7	SEEN	Enable Single-Ended Input Mode

Table XV. Control Register H Description

CONTROL REGISTER H

7	6	5	4	3	2	1	0
INV	TME	CH6	CH5	CH4	CH3	CH2	CH1

Bit	Name	Description
0	CH1	Channel 1 Select
1	CH2	Channel 2 Select
2	CH3	Channel 3 Select
3	CH4	Channel 4 Select
4	CH5	Channel 5 Select
5	CH6	Channel 6 Select
6	TME	Test Mode Enable
7	INV	Enable Invert Channel Mode

OPERATION

Resetting the AFE

The $\overline{\text{ARESET}}$ pin resets all the control registers. All the AFE registers are reset to zero, indicating that the default SCLK2 rate (DMCLK/8) and sample rate (DMCLK/2048) are at a minimum. As well as resetting the control registers of the AFE using the $\overline{\text{ARESET}}$ pin, the device can be reset using the $\overline{\text{RESET}}$ bit (CRA:7) in Control Register A. Both hardware and software resets require four DMCLK cycles. On reset, DATA/$\overline{\text{PGM}}$ (CRA:0) is set to 0 (default condition), thus enabling Control Mode. The reset conditions ensure that the device must be programmed to the correct settings after power-up or reset. Following a reset, the SDOFS will be asserted approximately 2070 master (AMCLK) cycles after $\overline{\text{ARESET}}$ goes high. The data that is output following the reset and during Control Mode is random and contains no valid information until either data or mixed mode is set.

Power Management

The individual functional blocks of the AFE can be enabled separately by programming the power control register CRC. (The Power Management functions of the DSP section are separate and will be referred to later.) It allows certain sections to be powered down if not required, which adds to the device's flexibility in that the user need not incur the penalty of having to provide power for a certain section if it is not necessary to their design. The power control registers provide individual control settings for the major functional blocks on each analog front end unit and also a global override that allows all sections to be powered up/down by setting/clearing the bit. Using this method the user could, for example, individually enable a certain section, such as the reference (CRC:5), and disable all others. The global power-up (CRC:0) can be used to enable all sections, but if power-down is required using the global control, the reference will still be enabled; in this case, because its individual bit is set. Refer to Table VI for details of the settings of CRC. CRD–CRF can be used to control the power status of individual channels, allowing multiple channels to be powered down if required.

Operating Modes

Three operating modes are available on the AFE. They are Control (Program) Mode, Data Mode, and Mixed Control/Data Mode. The device configuration—register settings—can be changed only in Program and Mixed Program/Data Modes. In all modes, transfers of information to or from the device occur in 16-bit packets. Therefore the DSP engine's SPORT will be programmed for 16-bit transfers.

Control Mode

In Control Mode, CRA:0 = 0, the user writes to the control registers to set up the device for desired operation—SPORT2 operation, cascade length, power management, input/output gain, and so on. In this mode, the 16-bit information packet sent to the device by the DSP is interpreted as a control word whose format is shown in Table VII. In this mode, the user must address the device to be programmed using the address field of the control word. This field is read by the device and if it is zero (000 bin), the device recognizes the word as being addressed to it. If the address field is not zero, it is then decremented and the control word is passed out of the device—either to the next device in a cascade or back to the DSP. This 3-bit address format allows the user to uniquely address any device in a cascade. If the AFE is used in a standalone configuration connected to the DSP, the device address corresponds to 0.

Following reset, when the SE pin is enabled, the AFE responds by raising the SDOFS pin to indicate that an output sample event has occurred. Control words can be written to the device to coincide with the data being sent out of SPORT2, as shown in Figure 9 (Directly Coupled), or they can lag the output words by a time interval that should not exceed the sample interval (Indirectly Coupled). Refer to the Digital Interface section for more information. After reset, output frame sync pulses will occur at a slower default sample rate, which is DMCLK/2048, until Control Register B is programmed, after which the SDOFS will be pulsed at the selected rate. While the AFE is in Control Mode, the data output by the device is random and should not be interpreted as ADC data.

Data Mode

Once the device has been configured by programming the correct settings to the various control registers, the device may exit Program Mode and enter Data Mode. This is done by programming the DATA/$\overline{\text{PGM}}$ (CRA:0) bit to 1 and MM (CRA:1) to 0. Once the device is in Data Mode, the input data is ignored. When the device is in normal Data Mode (i.e., mixed mode disabled), it must receive a hardware reset to reprogram any of the control register settings.

Mixed Program/Data Mode

This mode allows the user to send control words to the device while receiving ADC words. This permits adaptive control of the device whereby control of the input gains can be affected by reprogramming the control registers. The standard data frame remains 16 bits, but now the MSB is used as a flag bit to indicate that the remaining 15 bits of the frame represent control information. Mixed mode is enabled by setting the MM bit (CRA:1) to 1 and the DATA/$\overline{\text{PGM}}$ bit (CRA:0) to 1. In the case where control setting changes will be required during normal operation, this mode allows the ability to load control information with the slight inconvenience of formatting the data. Note that the output samples from the ADC will also have the MSB set to zero to indicate it is a data-word.

Channel Selection

The ADC channels of the AD73460 can be powered up or down individually by programming the PUIx bit of registers CRD to CRF. If the AD73460 is being used in Mixed Data/Control Mode, individual channels may be powered up or down as the program requires. In Data Mode, the number of channels selected while the AD73460 was in Program Mode is fixed and cannot be altered without resetting and reprogramming the AD73460. In all cases, ADC Channel 1 must be powered up as the frame sync pulse generated by this channel defines the start of a new sample interval.

INTERFACING

The AFE section SPORT (SPORT2) can be interfaced to either SPORT0 or SPORT1 of the DSP section. Both serial input and output data use an accompanying frame synchronization signal that is active high one clock cycle before the start of the 16-bit word or during the last bit of the previous word if transmission is continuous. The serial clock (SCLK) is an output from the AFE and is used to define the serial transfer rate to the DSP's Tx and Rx ports. Two primary configurations can be used: the first is shown in Figure 8 where the DSP's Tx data, Tx frame sync, Rx data and Rx frame sync are connected to the AD73460's SDI, SDIFS, SDO, and SDOFS, respectively. This configuration, referred to as indirectly coupled or nonframe sync loop-back, has the effect of decoupling the transmission of input data from the receipt of output data. When programming the DSP serial port for this configuration, it is necessary to set the Rx frame sync as an input to the DSP and the Tx frame sync as an output generated by the DSP. This configuration is most useful when operating in mixed mode, as the DSP has the ability to decide how many words can be sent to the AFE(s). This means that full control can be implemented over the device configuration in a given sample interval. The second configuration (shown in Figure 9) has the DSP's Tx data and Rx data connected to the AFE's SDI and SDO, respectively, while the DSP's Tx and Rx frame syncs are connected to the AD73460's SDIFS and SDOFS. In this configuration, referred to as directly coupled or frame sync loop-back, the frame sync signals are connected together and the input data to the AFE is forced to be synchronous with the output data from the AFE. The DSP must be programmed so that both the Tx and Rx frame syncs are inputs as the AFE's SDOFS will be input to both. This configuration guarantees that input and output events occur simultaneously and is the simplest configuration for operation in normal Data Mode. Note that when programming the AFE in this configuration it is advisable to preload the transmit register with the first control word to be sent before the AFE is taken out of reset. This ensures that this word will be transmitted to coincide with the first output word from the device(s).

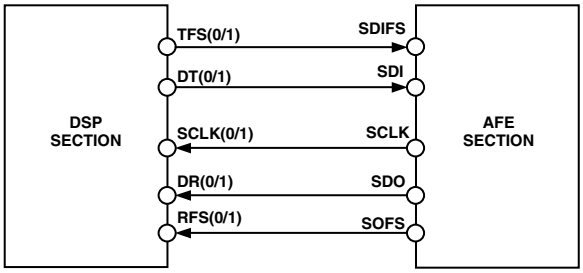


Figure 8. Indirectly Coupled or Nonframe Sync Loop-Back Configuration

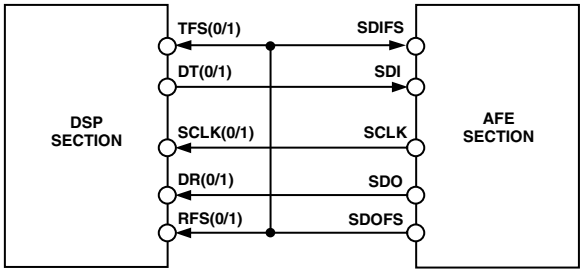


Figure 9. Directly Coupled or Frame Sync Loop-Back Configuration

Cascade Operation

The AD73460 has been designed to support cascading of an external AFE from either SPORT0 or SPORT1. The SPORT2 interface protocol has been designed so that device addressing is built into the packet of information sent to the device. This allows the cascade to be formed with no extra hardware overhead for control signals or addressing. A cascade can be formed in either of the two modes previously discussed.

There may be some restrictions in cascade operation due to the number of devices configured in the cascade and the serial clock rate chosen. The formula below gives an indication of whether the combination of sample rate, serial clock, and number of devices can be successfully cascaded. This assumes a directly coupled frame sync arrangement as shown in Figure 9 and does not take any interrupt latency into account.

$$\frac{1}{f_S} \geq \frac{6 \times [((Device\ Count - 1) \times 16) + 17]}{SCLK}$$

When using the indirectly coupled frame sync configuration in cascaded operation, it is necessary to be aware of the restrictions in sending control word data to all devices in the cascade. The user should ensure that there is sufficient time for all the control words to be sent between reading the last ADC sample and the start of the next sample period.

In Cascade Mode, both devices must know the number of devices in the cascade to be able to output data at the correct time. Control Register A contains a 3-bit field (DC0–2) that is programmed by the DSP during the programming phase. The default condition is that the field contains 000b, which is equivalent to a single device in cascade (see Table XVI). However, for cascade operation this field must contain a binary value that is one less than the number of devices in the cascade. With a cascade, each device takes a turn to send an ADC result to the DSP. For example, in a cascade of two devices the data will be output as Device 2-Channel 1, Device 1-Channel 1, Device 2-Channel 2, Device 1-Channel 2 and so on. When the first device in the cascade has transmitted its channel data, there is an additional SCLK period during which the last device asserts its SDOFS as it begins its transmission of the next channel. This will not cause a problem for most DSPs as they count clock edges after a frame sync and therefore the extra bit will be ignored.

When two devices are connected in cascade, there are also restrictions concerning which ADC channels can be powered up. In all cases the cascaded devices must all have the same channels powered up (i.e., for a cascade requiring Channels 1 and 2 on Device 1 and Channel 5 on Device 2, Channels 1, 2, and 5 must be powered up on both devices to ensure correct operation).

Table XVI. Device Count Settings

DC2	DC1	DC0	Cascade Length
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

FUNCTIONAL DESCRIPTION—DSP

The AD73460 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The AD73460 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 10 is an overall block diagram of the AD73460. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the AD73460 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data

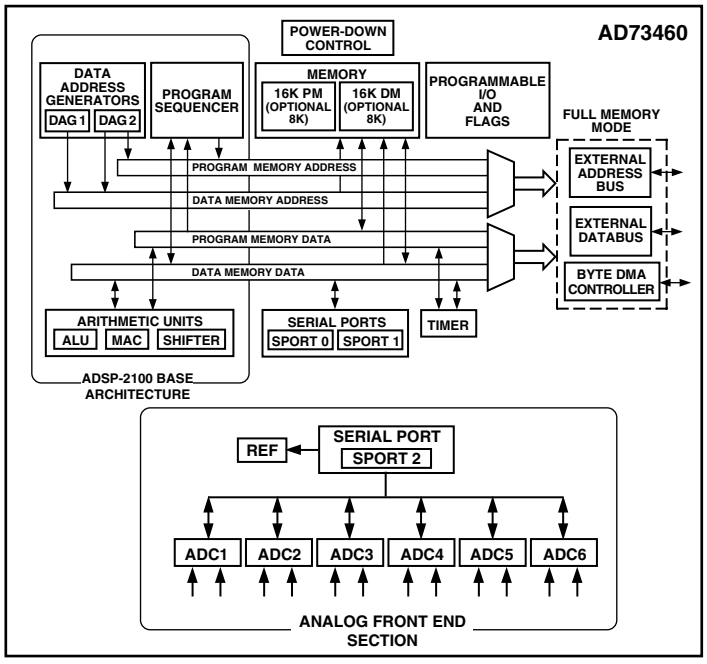


Figure 10. Functional Block Diagram

(indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the AD73460 to fetch two operands in a single cycle, one from program memory and one from data memory. The AD73460 can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and databus for external memory connection, the AD73460 may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals (BR, BGH, and BG). One execution mode (Go Mode) allows the AD73460 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The AD73460 can respond to 11 interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master $\overline{\text{RESET}}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The AD73460 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, there are eight flags that are programmable as inputs or outputs and three flags that are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycle, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The AD73460 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the AD73460 SPORTs. For additional information on Serial Ports, refer to the *ADSP-2100 Family User's Manual*, Third Edition.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data-word lengths from 3 bits to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data-word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data-word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24- or 32-word, time-division multiplexed, serial bit stream.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

DSP SECTION PIN DESCRIPTIONS

The AD73460 is available in a 119-ball PBGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt, and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{\text{RESET}}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics. See Pin Function Descriptions.

Memory Interface Pins

The AD73460 processor can be used in one of two modes, Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running. See tables for Full Memory Mode Pins and Host Mode Pins for descriptions.

Full Memory Mode Pins (Mode C = 0)

Pin Name(s)	# of Pins	Input/ Output	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory addresses)

Host Mode Pins (Mode C = 1)

Pin Name(s)	# of Pins	Input/ Output	Function
IAD15:0	16	I/O	IDMA Port Address/Databus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte access
D23:8	16	I/O	Data I/O Pins for Program, Data Byte, and I/O spaces
$\overline{IWR}$	1	I	IDMA Write Enable
$\overline{IRD}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{IS}$	1	I	IDMA Select
$\overline{IACK}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Source

In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{CMS}$, $\overline{PMS}$, $\overline{DMS}$, and $\overline{IOMS}$ signals

Terminating Unused Pins

The following table shows the recommendations for terminating unused pins.

Pin Terminations

Pin Name	I/O Three-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float
A13:1 or	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD12:0	I/O (Z)	Hi-Z	$\overline{IS}$	Float
A0	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D23:8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IWR}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2:0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15:13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float

Pin Terminations (continued)

Pin Name	I/O Three-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL1}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL0}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQE}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	O		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/$\overline{FL1}$	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	O		High or Low
DT1/FO	O	O		Float
EE	I	I		
$\overline{EBR}$	I	I		
$\overline{EBG}$	O	O		
$\overline{ERESET}$	I	I		
$\overline{EMS}$	O	O		
$\overline{EINT}$	I	I		
ECLK	I	I		
ELIN	I	I		
$\overline{ELOUT}$	O	O		

NOTES

*Hi-Z = High Impedance.

1. If the CLKOUT pin is not used, turn it OFF.
2. If the Interrupt/Programmable Flag pins are not used, there are two options:
   Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive).
   Option 2: Program the unused pins as OUTPUTS, set them to 1, and let them float.
3. All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, RESET, and PF3:0 are not included in the table because these pins must be used.

Interrupts

The interrupt controller allows the processor to respond to the 11 possible interrupts and $\overline{\text{RESET}}$ with minimum overhead. The AD73460 provides four dedicated external interrupt input pins, $\overline{\text{IRQ2}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQE}}$. In addition, SPORT1 may be reconfigured for $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, FLAG_IN, and FLAG_OUT, for a total of six external interrupts. The AD73460 also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table XVII.

Table XVII. Interrupt Priority and Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)
$\overline{\text{RESET}}$ (or Power-Up with PUCR = 1)	0000 (*Highest Priority*)
Power-Down (Nonmaskable)	002C
$\overline{\text{IRQ2}}$	0004
$\overline{\text{IRQL1}}$	0008
$\overline{\text{IRQL0}}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{\text{IRQE}}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0024
Timer	0028 (*Lowest Priority*)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The AD73460 masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level-sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;
DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The AD73460 has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The AD73460 processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, Third Edition, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 400 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the 400 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 CLKIN cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 400 CLKIN cycle startup.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt can also be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin can also be used to terminate power-down.
- Power-down acknowledge pin indicates when the processor has entered power-down.

Idle

When the AD73460 is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle Mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The *IDLE* instruction on the AD73460 slows the processor's internal clock signal, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction. The format of the instruction is

IDLE (n);

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard *IDLE* instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by *n*, the clock divisor. When an enabled interrupt is received, the AD73460 will remain in the idle state for up to a maximum of *n* processor cycles (*n* = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a rate faster than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of *n* processor cycles).

SYSTEM INTERFACE

Figure 11 shows a typical basic system configuration with the AD73460, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode selectable). Programmable wait state generation allows the processor to easily connect to slow peripheral devices. The AD73460 also provides four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external databus, but limits addressing to a single address bit (A0). Additional system peripherals can be added in this mode through the use of external hardware to generate and latch address signals.

Clock Signals

The AD73460 can be clocked by either a crystal or a TTL compatible clock signal.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual,* Third Edition, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

The AD73460 uses an input clock with a frequency equal to half the instruction rate; a 26.00 MHz input clock yields a 19 ns processor cycle (which is equivalent to 52 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the AD73460 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 12. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLK0DIS bit in the SPORT0 Autobuffer Control Register.

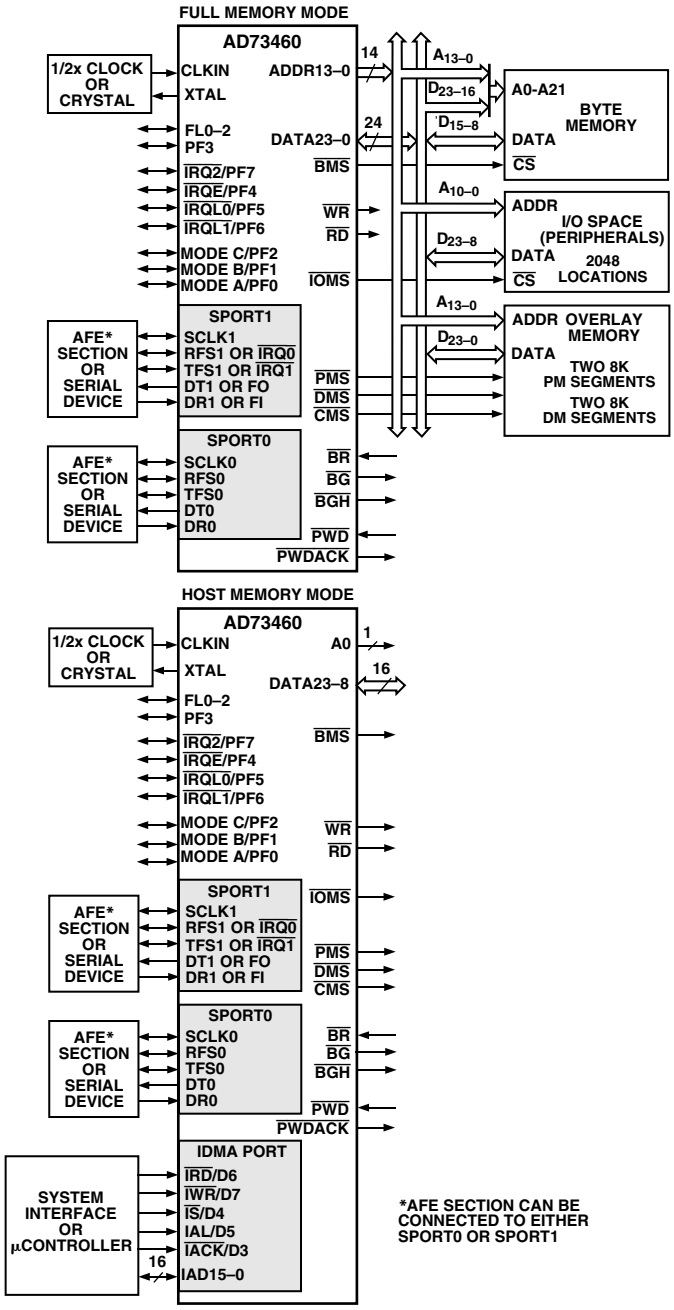


Figure 11. Basic System Configuration

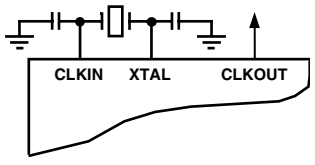


Figure 12. External Crystal Connections

Table XVIII. Modes of Operation[1]

MODE C[2]	MODE B[3]	MODE A[4]	Booting Method
0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[5]
0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. **(REQUIRES ADDITIONAL HARDWARE.)**
1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode.[5]

NOTES
[1]All mode pins are recognized while $\overline{\text{RESET}}$ is active (low).
[2]When Mode C = 0, Full Memory enabled. When Mode C = 1, Host Memory Mode enabled.
[3]When Mode B = 0, Auto Booting enabled. When Mode B = 1, no Auto Booting.
[4]When Mode A = 0, BDMA enabled. When Mode A = 1, IDMA enabled.
[5]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ signal initiates a master reset of the AD73460. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence, the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulsewidth specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, an external Schmitt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

MODES OF OPERATION

Table XVIII summarizes the AD73460 memory modes.

Setting Memory Mode

Memory Mode selection for the AD73460 is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 100 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's RESET signal such that it only drives the PF2 pin when RESET is active (low). When RESET is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level and not oscillate should the three-state driver's level hover around the logic switching point.

MEMORY ARCHITECTURE

The AD73460 provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to the following figures and tables for PM and DM memory allocations in the AD73460.

PROGRAM MEMORY

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The AD73460-80 has 16K words of Program Memory RAM on-chip (the AD73460-40 has 8K words of Program Memory RAM on-chip), and the capability of accessing up to two 8K external memory overlay spaces using the external databus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted databus that is only 16 bits wide.

Table XIX. PMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

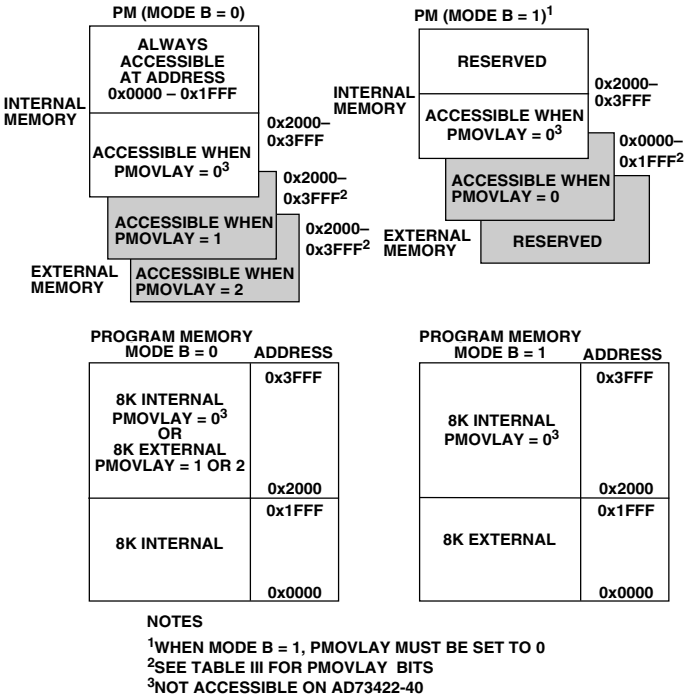


Figure 13. Program Memory Map

DATA MEMORY

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The AD73460-80 has 16K words on Data Memory RAM on-chip (the AD73460-40 has 8K words on Data Memory RAM on-chip), consisting of 16,352 user-accessible locations in the case of the AD73460-80 (8,160 user-accessible locations in the case of the AD73460-40) and 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external databus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

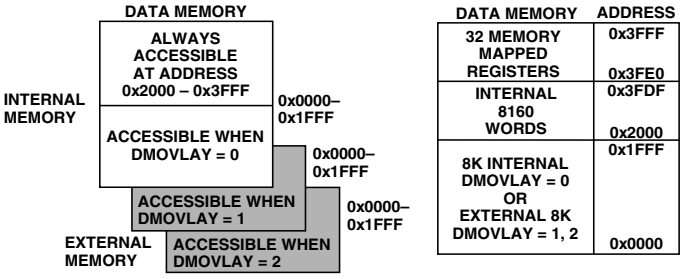


Figure 14. Data Memory Map

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). The DMOVLAY bits are defined in Table XX.

Table XX. DMOVLAY Bits

DMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

I/O Space (Full Memory Mode)

The AD73460 supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit-wide data. The lower 11 bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0-3, that specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table XXI.

Table XXI. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

Composite Memory Select ($\overline{\text{CMS}}$)

The AD73460 has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$), but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory; use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{CMS}$ pin functions like the other memory select signals, with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{CMS}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{BMS}$ bit.

Boot Memory Select ($\overline{BMS}$) Disable

The AD73460 also allows the user to boot the processor from one external memory space while using a different external memory space for BDMA transfers during normal operation. $\overline{CMS}$ can be used to select the first external memory space for BDMA transfers and $\overline{BMS}$ to select the second external memory space for booting. The $\overline{BMS}$ signal can be disabled by setting Bit 3 of the System Control Register to 1. The System Control Register is illustrated in Figure 15.

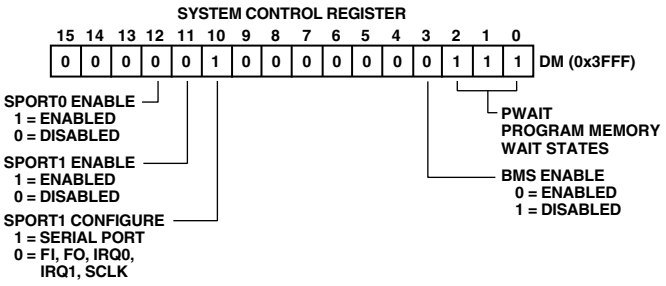


Figure 15. System Control Register

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The BDMA Control Register is shown in Figure 16. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the AD73460 supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32-megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

Byte Memory DMA (BDMA, Full Memory Mode)

The Byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally, and steals only one DSP cycle per 8-, 16-, or 24-bit word transferred.

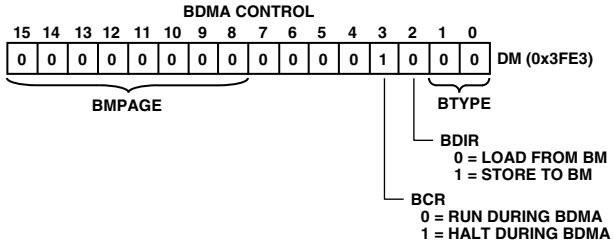


Figure 16. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table XXII shows the data formats supported by the BDMA circuit.

Table XXII. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer, so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value, the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether or not the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and the AD73460. The port is used to access the on-chip program memory and data memory of the

DSP with only one DSP cycle per word overhead. The IDMA port cannot be used, however, to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers.

   IAD[15] must be set to 0.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and databus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to while the AD73460 is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location; the destination type specifies whether it is a DM or PM access. The falling edge of the address latch signal latches this value into the IDMAA register.

Once the address is stored, data can either be read from or written to the AD73460's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the AD73460 that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the AD73460 to write the address onto the IAD0–14 bus into the IDMA Control Register. If IAD[15] is set to 0, IDMA latches the address. The IDMAA register, shown below, is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. The IDMA OVLAY register is memory mapped at address DM (0x3FE7). See Figure 17 for more information on IDMA and DMA memory maps.

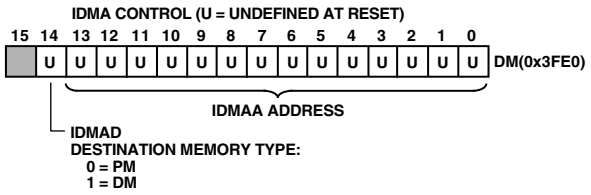


Figure 17. IDMA Control/OVLAY Registers

Bootstrap Loading (Booting)

The AD73460 has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting after reset is controlled by the Mode A, B, and C configuration bits.

When the mode pins specify BDMA booting, the AD73460 initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family Development Software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the AD73460. The only memory address bit provided by the processor is A0.

IDMA Port Booting

The AD73460 can also boot programs through its Internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the AD73460 boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

Bus Request and Bus Grant (Full Memory Mode)

The AD73460 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request (BR) signal. If the AD73460 is not performing an external memory access, it responds to the active BR input in the following processor cycle by:

- three-stating the data and address buses and the $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ output drivers,
- asserting the bus grant ($\overline{\text{BG}}$) signal, and
- halting program execution.

If Go Mode is enabled, the AD73460 will not halt program execution until it encounters an instruction that requires an external memory access.

If the AD73460 is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when the AD73460 is ready to execute an instruction, but is stopped because the external bus is already granted to another device. The other device can release the bus by deasserting the bus request. Once the bus is released, the AD73460 deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

Flag I/O Pins

The AD73460 has eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the AD73460's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the AD73460 has five fixed-mode flags, FLAG_IN, FLAG_OUT, FL0, FL1, and FL2. FL0–FL2 are dedicated output flags. FLAG_IN and FLAG_OUT are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The AD73460 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the AD73460's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

DESIGNING AN EZ-ICE COMPATIBLE SYSTEM

The AD73460 has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug. See the ADSP-2100 Family EZ-Tools data sheet for complete information on ICE products.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If you are using a passive method of maintaining mode information (as discussed in Setting Memory Modes) then it does not matter that the mode information is latched by an emulator reset. However, if you are using the $\overline{RESET}$ pin as a method of setting the value of the mode pins, then you have to take into consideration the effects of an emulator reset.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 18. This circuit forces the value located on the Mode A pin to logic high; regardless if it latched via the $\overline{RESET}$ or $\overline{ERESET}$ pin.

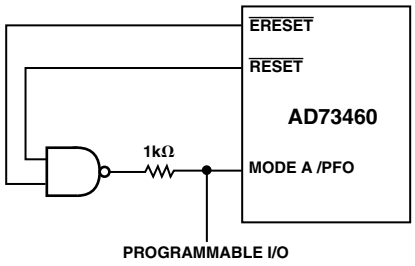


Figure 18. Mode A Pin/EZ-ICE Circuit

The ICE-Port interface consists of the following AD73460 pins:

$\overline{EBR}$	$\overline{EBG}$	$\overline{ERESET}$
$\overline{EMS}$	$\overline{EINT}$	ECLK
ELIN	$\overline{ELOUT}$	EE

These AD73460 pins must be connected *only* to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the AD73460 and the connector must be kept as short as possible, no longer than three inches.

The following pins are also used by the EZ-ICE:

$\overline{BR}$	$\overline{BG}$
$\overline{RESET}$	GND

The EZ-ICE uses the EE (emulator enable) signal to take control of the AD73460 in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The BG output is three-stated. These signals do not need to be jumper-isolated in your system. The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The ribbon cable is 10 inches in length with one end fixed to the EZ-ICE. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe
The EZ-ICE connector (a standard pin strip header) is shown in Figure 19. This connector must be added to the target board design in order to use the EZ-ICE. Be sure to allow enough room in the system to fit the EZ-ICE probe onto the 14-pin connector.

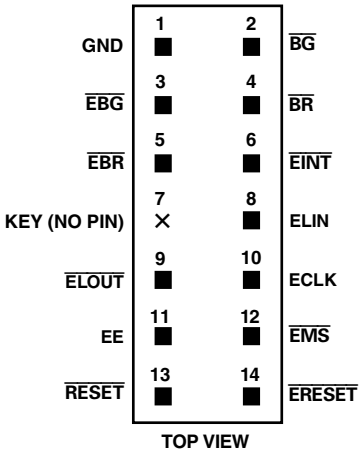


Figure 19. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15-inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface
For the target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM, and CM
Design Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst-case device timing requirements and switching characteristics as specified in the DSP's data sheet. The performance of the EZ-ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If the target does not meet the worst-case chip specification for memory access parameters, user may not be able to emulate the circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, it may create a problem manufacturing the system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the AD73460 ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, and $\overline{\text{IOMS}}$) used in the target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at the user's option when the EZ-ICE is not being used.

Target System Interface Signals
When the EZ-ICE board is installed, the performance on some system signals changes. Design the system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{RESET}}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{BR}}$ signal.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus *only* if bus grant ($\overline{\text{BG}}$) is asserted by the EZ-ICE board's DSP.

ANALOG FRONT END (AFE) INTERFACING

The AFE section of the AD73460 features six input channels, each with 16-bit linear resolution. Connectivity to the AFE section from the DSP is uncommitted, thus allowing the user the flexibility of connecting in the mode or configuration of their choice. This section will detail several configurations—with no extra AFE channels configured and with an extra AFE section configured (using an external AD73360 AFE).

DSP SPORT TO AFE INTERFACING

The SCLK, SDO, SDOFS, SDI, and SDIFS must be connected to the SCLK, DR, RFS, DT, and TFS pins of the DSP respectively. The SE pin may be controlled from a parallel output pin or flag pin such as FL0–2 or, where SPORT power-down is not required, it can be permanently strapped high using a suitable pull-up resistor. For consistent performance, the SE pin should be synchronized to the rising edge of the AMCLK using a circuit similar to that of Figure 23. The $\overline{\text{ARESET}}$ pin may be connected to the system hardware reset structure or it may also be controlled using a dedicated control line. In the event of tying it to the global system reset, it is necessary to operate the device in mixed mode, which allows a software reset. Otherwise there is no convenient way of resetting the device.

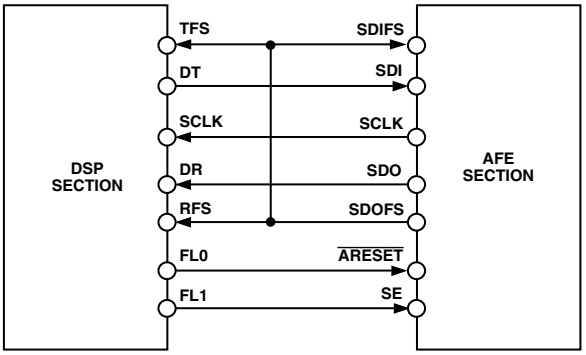


Figure 20. DSP to AD73460 AFE Connection

CASCADE OPERATION

Where it is required to configure an extra analog input channel to the existing six channels on the AD73460, it is possible to cascade six more channels (using external AD73360 AFEs) by using the scheme described in Figure 22. It is necessary however to ensure that the timing of the SE and $\overline{\text{ARESET}}$ signals is synchronized at each device in the cascade. A simple D-type flip-flop is sufficient to synchronize each signal to the master clock AMCLK as shown in Figure 21.

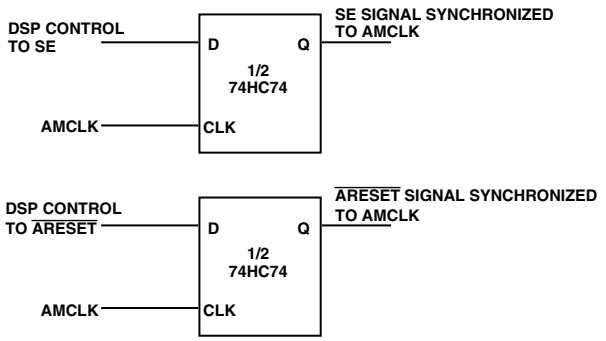


Figure 21. SE and $\overline{\text{ARESET}}$ Sync Circuit for Cascaded Operation

There may be some restrictions in cascade operation due to the number of devices configured in the cascade and the serial clock rate chosen. The formula below gives an indication of whether the combination of sample rate and serial clock can be successfully cascaded. This assumes a directly coupled frame sync arrangement as shown in Figure 20 and does not take any interrupt latency into account.

$$\frac{1}{f_S} \geq \frac{6 \times [((Device\ Count - 1) \times 16) + 17]}{SCLK}$$

When using the indirectly coupled frame sync configuration in cascaded operation, it is necessary to be aware of the restrictions in sending control word data to all devices in the cascade. The user should ensure that there is sufficient time for all the control words to be sent between reading the last ADC sample and the start of the next sample period.

Connection of a cascade, as shown in Figure 22, is no more complicated than connecting a single device. Instead of connecting the SDO and SDOFS to the DSP's Rx port, these are now daisy-chained to the SDI and SDIFS of the next device in the cascade. The SDO and SDOFS of the final device in the cascade are connected to the DSP's Rx port to complete the cascade. SE and $\overline{\text{ARESET}}$ on all devices are fed from the signals that were synchronized with the AMCLK using the circuit of Figure 21. The SCLK from only one device needs to be connected to the DSP's SCLK input(s) as both devices will be running at the same SCLK frequency and phase.

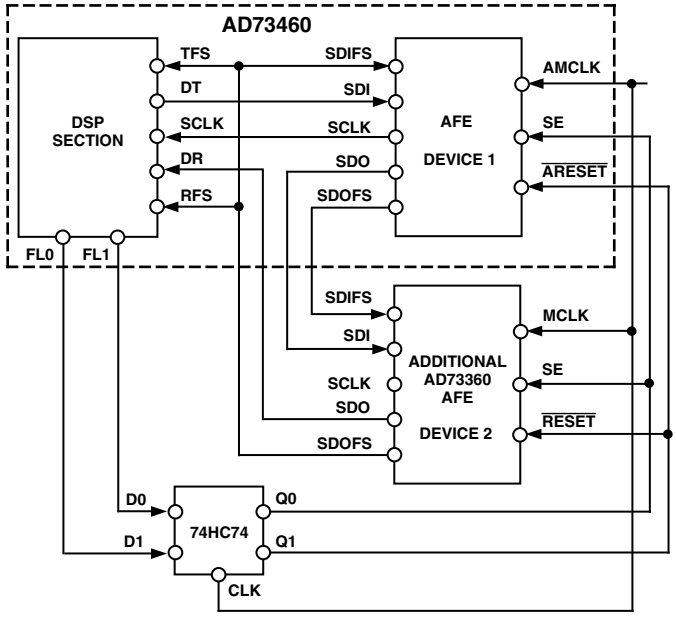


Figure 22. Connection of an AD73360 Cascaded to the AD73460

Interfacing to the AFE's Analog Inputs

The AD73460 features six signal conditioning inputs. Each signal conditioning block allows the AD73460 to be used with either a single-ended or differential signal. The applied signal can also be inverted internally by the AD73460 if required. The analog input signal to the AD73460 can be dc-coupled, provided that the dc bias level of the input signal is the same as the internal reference level (REFOUT). Figure 23 shows the recommended differential input circuit for the AD73460. The circuit of Figure 23 implements first-order low-pass filters with a 3 dB point at 34 kHz; these are the only filters that must be implemented external to the AD73460 to prevent aliasing of the sampled signal. Since the ADC uses a highly oversampled approach that transfers the bulk of the antialiasing filtering into the digital domain, the off-chip antialiasing filter need only be of a low order. It is recommended that for optimum performance, the capacitors used for the antialiasing filter be of high quality dielectric (NPO).

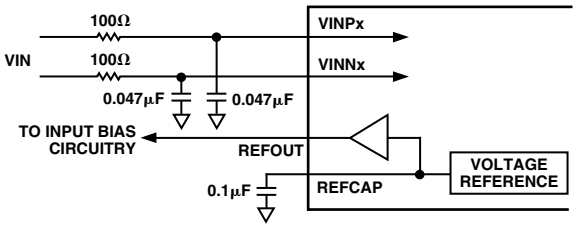


Figure 23. Example Circuit for Differential Input (DC Coupling)

Figure 24 details the dc-coupled input circuits for single-ended operation respectively.

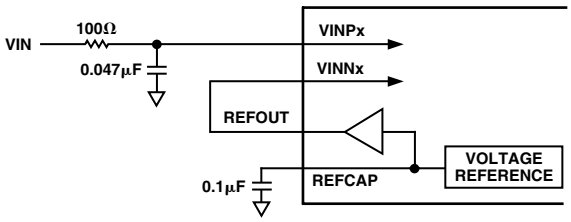


Figure 24. Example Circuit for Single-Ended Input (DC Coupling)

Digital Interface

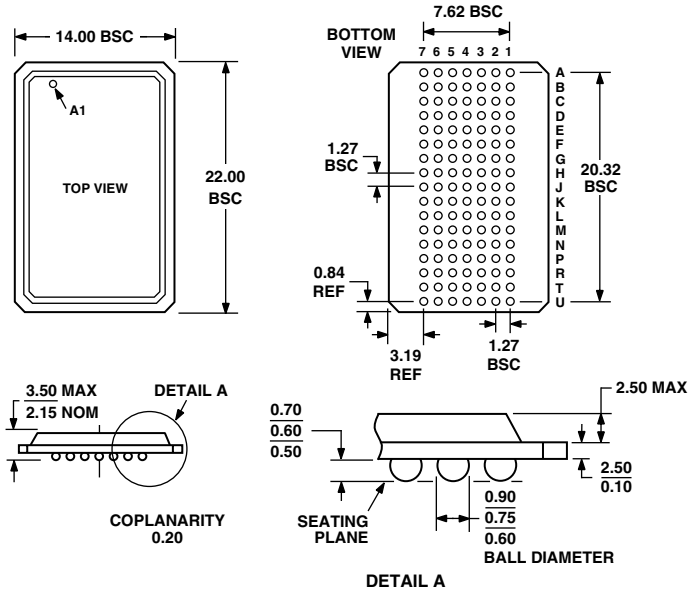
As there are a number of variations of sample rate and clock speeds that can be used with the AD73460 in a particular application, it is important to select the best combination to achieve the desired performance. High speed serial clocks will read the data from the AD73460 in a shorter time, giving more time for processing at the expense of injecting some digital noise into the circuit. Digital noise can also be reduced by connecting resistors (typ <50 Ω) in series with the digital input and output lines. The noise can be minimized by good grounding and layout. Typically the best performance is achieved by selecting the slowest sample rate and SCLK frequency for the required application, as this will produce the least amount of digital noise.

C01040–0–10/02(A)

OUTLINE DIMENSIONS

119-Lead Chip Scale Ball Grid Array (PBGA)
(B-119)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-028AA

Revision History

Location	Page
10/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to Note 1 of SPECIFICATIONS	4
Edits to TIMING CHARACTERISTICS	6
Edits to ABSOLUTE MAXIMUM RATINGS	6
Edits to ORDERING GUIDE	6
Updated OUTLINE DIMENSIONS	32

PRINTED IN U.S.A.