

# BLS6G2731-120; BLS6G2731S-120

LDMOS S-band radar power transistor

Rev. 01 — 14 November 2008

Product data sheet

## 1. Product profile

### 1.1 General description

120 W LDMOS power transistor intended for radar applications in the 2.7 GHz to 3.1 GHz range.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ ;  $I_{Dq} = 100\text{ mA}$ ; in a class-AB production test circuit.

Mode of operation	f (GHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)	t <sub>r</sub> (ns)	t <sub>f</sub> (ns)
pulsed RF	2.7 to 3.1	32	120	13.5	48	20	6

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

### 1.2 Features

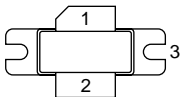
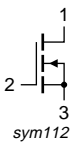
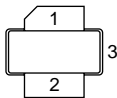
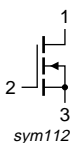
- Typical pulsed RF performance at a frequency of 2.7 GHz to 3.1 GHz, a supply voltage of 32 V, an  $I_{Dq}$  of 100 mA, a  $t_p$  of 100  $\mu\text{s}$  with  $\delta$  of 10 %:
  - ◆ Output power = 120 W
  - ◆ Power gain = 13.5 dB
  - ◆ Efficiency = 48 %
- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2.7 GHz to 3.1 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

## 1.3 Applications

- S-band power amplifiers for radar applications in the 2.7 GHz to 3.1 GHz frequency range

## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
<b>BLS6G2731-120 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source		
<b>BLS6G2731S-120 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source		

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BLS6G2731-120	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLS6G2731S-120	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
$V_{DS}$	drain-source voltage	-	60	V
$V_{GS}$	gate-source voltage	-0.5	+13	V
$I_D$	drain current	-	33	A
$T_{stg}$	storage temperature	-65	+150	°C
$T_j$	junction temperature	-	225	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	$T_{case} = 85\text{ °C}; P_L = 120\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.23	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.28	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.32	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.33	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.6\text{ mA}$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 180\text{ mA}$	1.4	1.8	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	4.2	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	27	33	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	450	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 9\text{ A}$	8.1	13	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 6.3\text{ A}$	-	0.085	0.135	$\Omega$

## 7. Application information

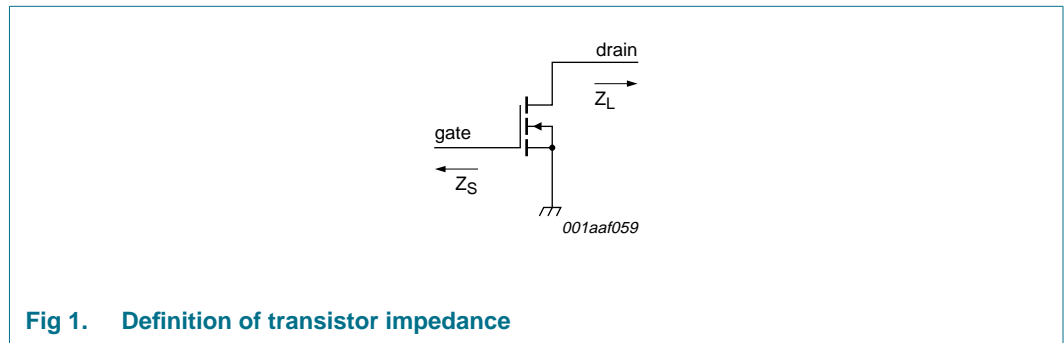
**Table 7. Application information**

Mode of operation: pulsed RF;  $t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$ ; RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_L$	output power		-	120	-	W
$V_{CC}$	supply voltage	$P_L = 120\text{ W}$	-	-	32	V
$G_p$	power gain	$P_L = 120\text{ W}$	12	13.5	-	dB
$RL_{in}$	input return loss	$P_L = 120\text{ W}$	-	7	-	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		-	130	-	W
$\eta_D$	drain efficiency	$P_L = 120\text{ W}$	40	48	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 120\text{ W}$	-	0	0.5	dB
$t_r$	rise time	$P_L = 120\text{ W}$	-	20	50	ns
$t_f$	fall time	$P_L = 120\text{ W}$	-	6	50	ns

**Table 8. Typical impedance**

<b>f</b> <b>GHz</b>	<b>Z<sub>S</sub></b> <b>Ω</b>	<b>Z<sub>L</sub></b> <b>Ω</b>
2.7	3.4 – j7.2	4.6 – j4.4
2.8	3.8 – j5.9	3.8 – j4.6
2.9	4.7 – j4.8	3.0 – j4.6
3.0	6.3 – j4.1	2.3 – j4.3
3.1	8.8 – j4.9	1.8 – j3.9

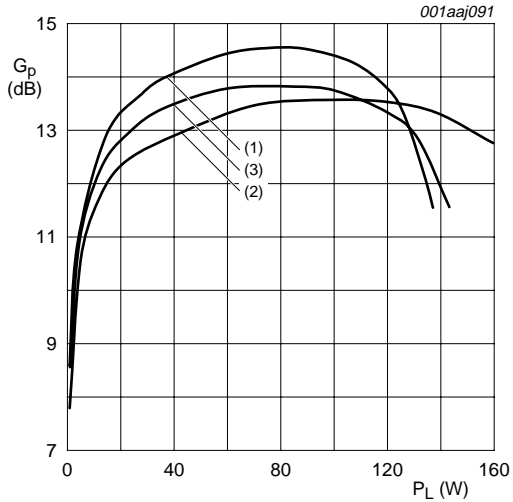


**Fig 1. Definition of transistor impedance**

## 7.1 Ruggedness in class-AB operation

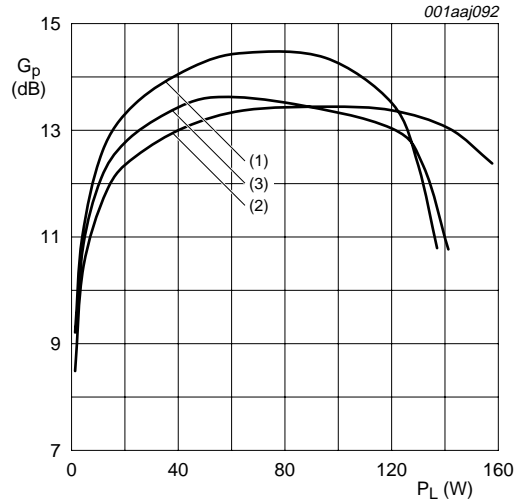
The BLS6G2731-120 and BLS6G2731S-120 are capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions:  $V_{DS} = 32 \text{ V}$ ;  $I_{Dq} = 100 \text{ mA}$ ;  $P_L = 120 \text{ W}$ ;  $t_p = 100 \text{ } \mu\text{s}$ ;  $\delta = 10 \text{ \%}$ .

**7.2 Graphs**



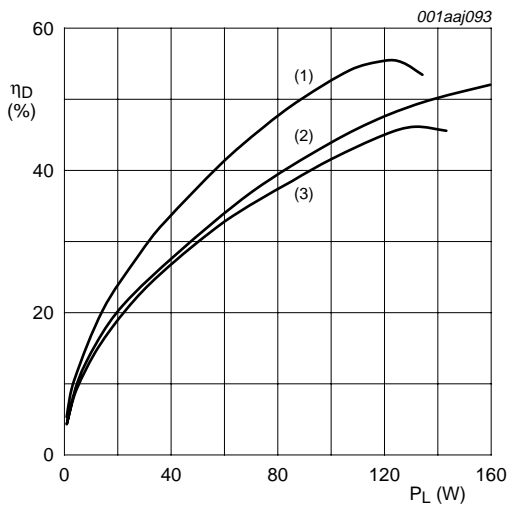
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.9\text{ GHz}$   
 (3)  $f = 3.1\text{ GHz}$

**Fig 2. Power gain as a function of load power; typical values**



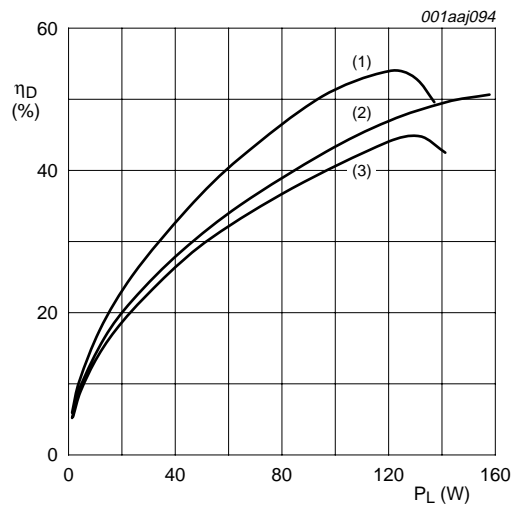
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$ .  
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.9\text{ GHz}$   
 (3)  $f = 3.1\text{ GHz}$

**Fig 3. Power gain as a function of load power; typical values**



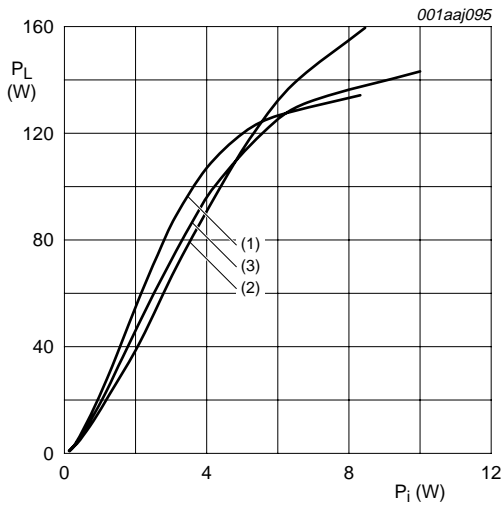
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.9\text{ GHz}$   
 (3)  $f = 3.1\text{ GHz}$

**Fig 4. Drain efficiency as a function of load power; typical values**



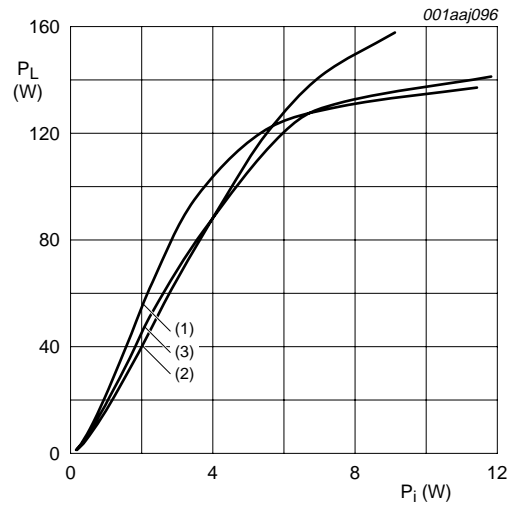
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$ .  
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.9\text{ GHz}$   
 (3)  $f = 3.1\text{ GHz}$

**Fig 5. Drain efficiency as a function of load power; typical values**



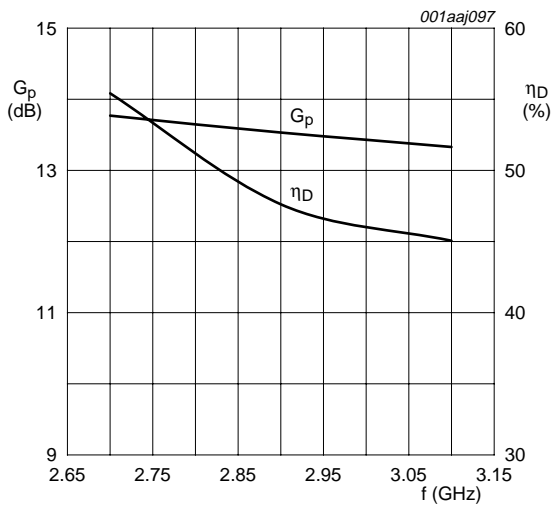
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .  
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.9\text{ GHz}$   
 (3)  $f = 3.1\text{ GHz}$

**Fig 6. Load power as a function of input power; typical values**



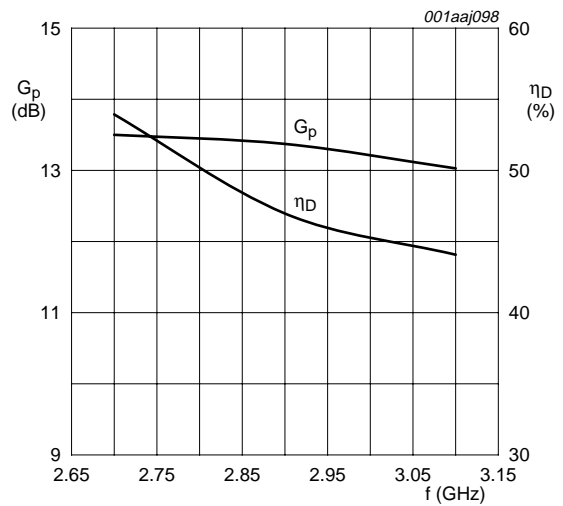
$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$ .  
 (1)  $f = 2.7\text{ GHz}$   
 (2)  $f = 2.9\text{ GHz}$   
 (3)  $f = 3.1\text{ GHz}$

**Fig 7. Load power as a function of input power; typical values**



$P_L = 120\text{ W}; V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

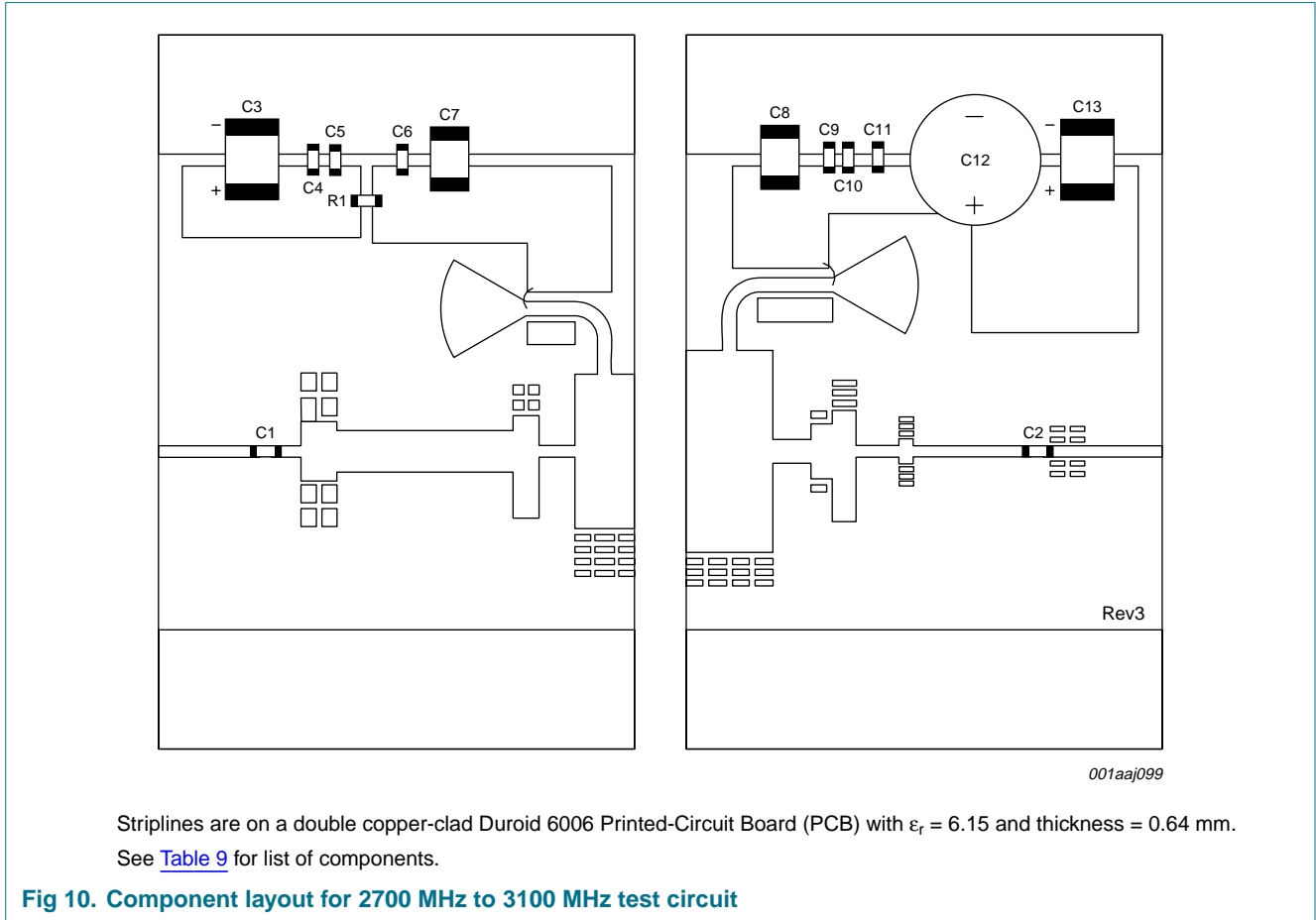
**Fig 8. Power gain and drain efficiency as function of frequency; typical values**



$P_L = 120\text{ W}; V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$ .

**Fig 9. Power gain and drain efficiency as function of frequency; typical values**

**8. Test information**



**Table 9. List of components**

See [Figure 10](#).

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	24 pF	ATC 100A or equivalent
C3	multilayer ceramic chip capacitor	47 $\mu$ F; 20 V	
C4, C6, C9, C10	multilayer ceramic chip capacitor	33 pF	ATC 100A or equivalent
C5, C11	multilayer ceramic chip capacitor	1 nF	ATC 100A or equivalent
C7, C8	multilayer ceramic chip capacitor	100 pF	ATC 100B or equivalent
C12	electrolytic capacitor	47 $\mu$ F; 63 V	
C13	multilayer ceramic chip capacitor	10 $\mu$ F; 35 V	
R1	SMD resistor	56 $\Omega$	SMD 0603

**9. Package outline**

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

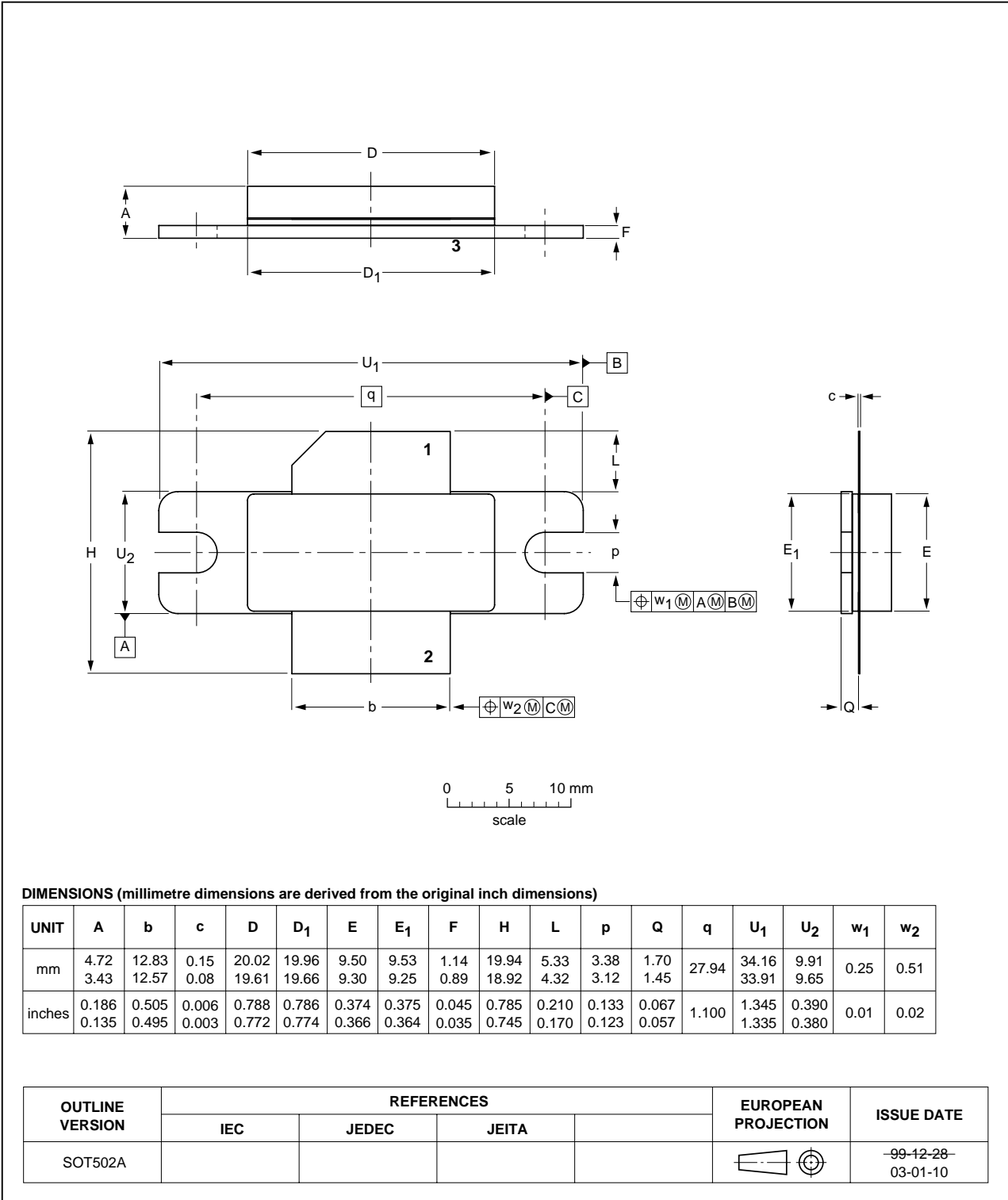


Fig 11. Package outline SOT502A



Earless flanged LDMOST ceramic package; 2 leads

SOT502B

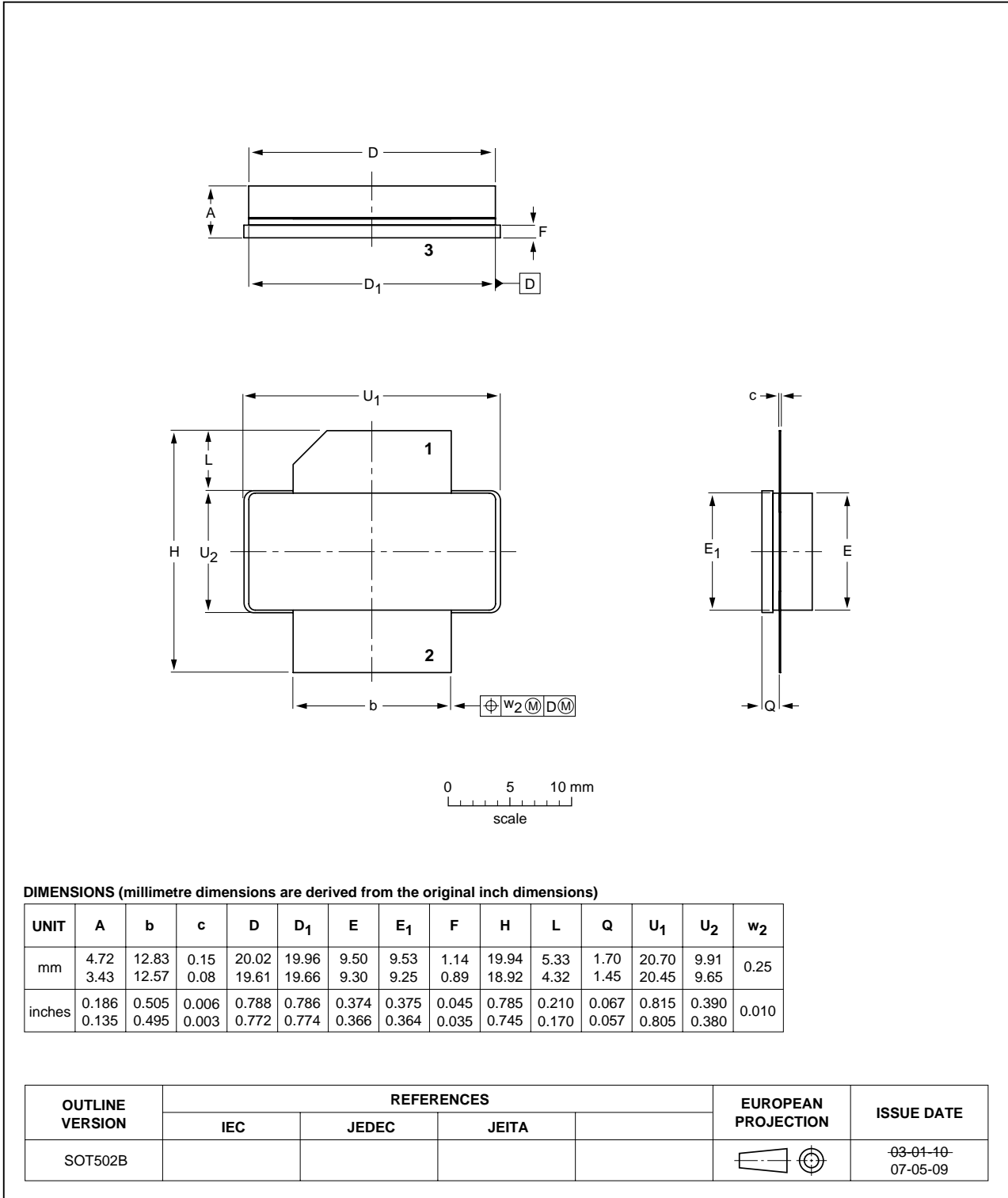


Fig 12. Package outline SOT502B

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
S-band	Short wave Band
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS6G2731-120_6G2731S-120_1	20081114	Product data sheet	-	-

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### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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