1Mx8 Static RAM CMOS, Module

FEATURES

- 1024Kx8 bit CMOS Static
- Random Access Memory
  - Access Times 70 thru 100ns
  - Data Retention Function (EDI8F81024LP)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- High Density Packaging
  - 36 Pin SIP, No. 62
- Single +5V (±10%) Supply Operation

*This product is subject to change without notice.

DESCRIPTION

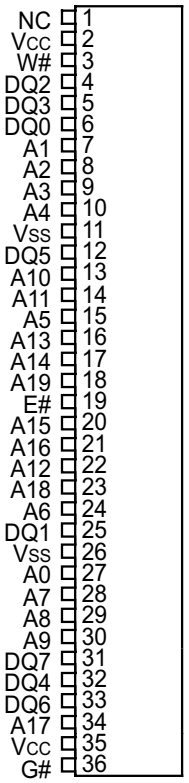
The EDI8F81024C is a 8Mb CMOS Static RAM based on eight 128Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

A version featuring Low Power with Data Retention (EDI8F81024LP) is also available.

The EDI8F81024C is offered in a double sided, 36 pin single-in-line Package (SIP). Surface mount SIP technology is a cost effective solution to very high packing density requirements.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8F81024C requires no clocks or refreshing for operation.

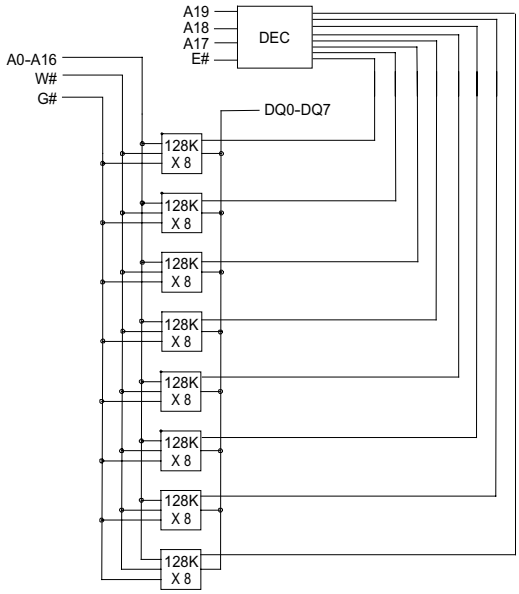
PIN CONFIGURATIONS AND BLOCK DIAGRAM



PIN OUT

PIN NAMES

AØ-A19	Address Inputs
E#	Chip Enable
W#	Write Enable
G#	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



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ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature T_A (Ambient) Commercial Industrial	 0°C to +70°C -40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	1 Watt
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 100pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	I_{CC1}	W#, E# = V_{IL}, II/O = 0mA, Min Cycle			80	130	mA
Standby (TTL) Power Supply Current	I_{CC2}	E# ≥ V_{IH}, V_{IN} ≤ V_{IL} or V_{IN} ≥ V_{IH}			40	90	mA
Full Standby Power Supply Current (CMOS)	I_{CC3}	E# ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	C LP		10 400	20 950	mA µA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		–	–	±10	µA
Output Leakage Current	I_{LO}	V I/O = 0V to V_{CC}		–	–	±10	µA
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		–	–	0.4	V

*Typical: T_A = 25°C, V_{CC} = 5.0V

TRUTH TABLE

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	HIGH Z	I_{CC2}/I_{CC3}
H	L	H	Output Deselect	HIGH Z	I_{CC1}
L	L	H	Read	D_{OUT}	I_{CC1}
X	L	L	Write	D_{IN}	I_{CC1}

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	58	pF
Capacitance (DQ Pins)	CD/Q	43	pF
Input (E#) Control Lines	CC	10	pF
Input (W#) Line (G#)	CW	60	pF

These parameters are sampled, not 100% tested.

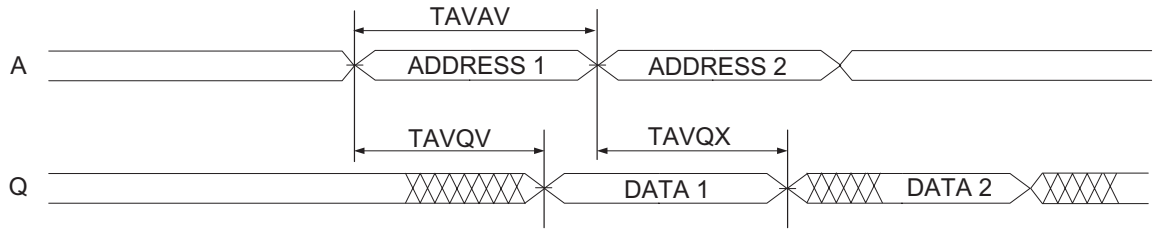
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AC CHARACTERISTICS READ CYCLE

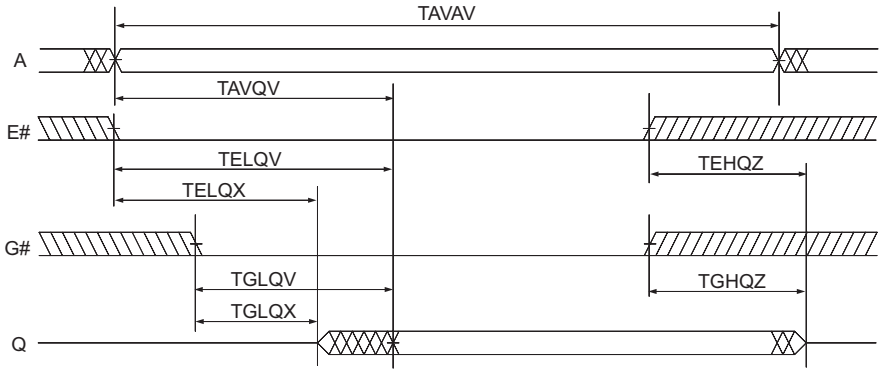
	Symbol		70ns		85ns		100ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	70		85		100		ns
Address Access Time	TAVQV	TAA		70		85		100	ns
Chip Enable Access	TELQV	TACS		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

READ CYCLE 1 - W# HIGH, G#, E# LOW



READ CYCLE 2 - W# HIGH



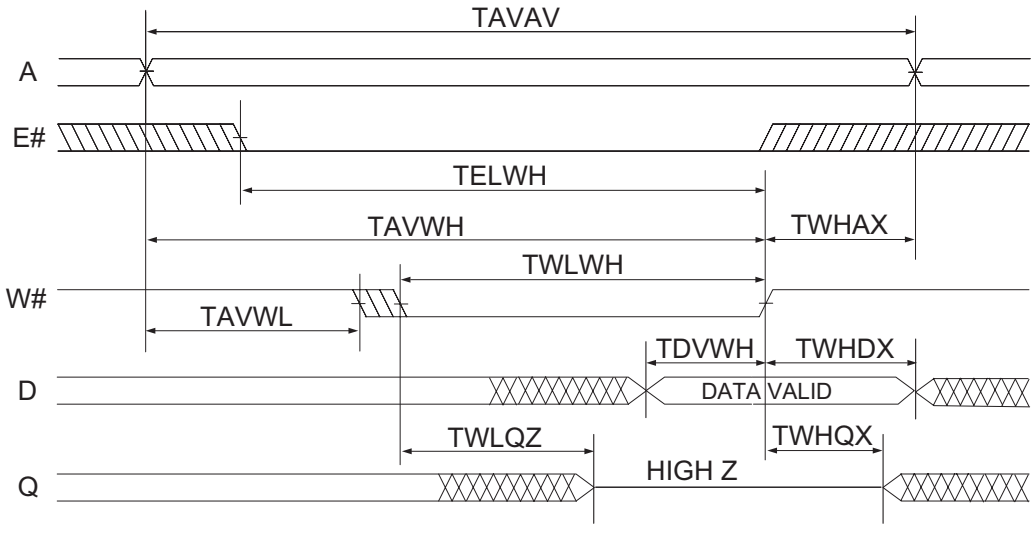
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AC CHARACTERISTICS WRITE CYCLE

	Symbol		70ns		85ns		100ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	70		85		100		ns
Chip Enable to End of Write	TELWH TELEH	TCW TCW	65 65		70 70		80 80		ns ns
Address Setup Time	TAVWL TAVEL	TAS TAS	0 0		0 0		0 0		ns ns
Address Valid to End of Write	TAVWH TAVEH	TAW TAW	65 65		70 70		80 80		ns ns
Write Pulse Width	TWLWH TWLEH	TWP TWP	65 65		70 70		80 80		ns ns
Write Recovery Time	TWHAX TEHAX	TWR TWR	0 0		0 0		0 0		ns ns
Data Hold Time	TWHDX TEHDX	TDH TDH	0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	35	0	40	ns
Data to Write Time	TDVWH TDVEH	TDW TDW	30 30		35 35		40 40		ns ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		ns

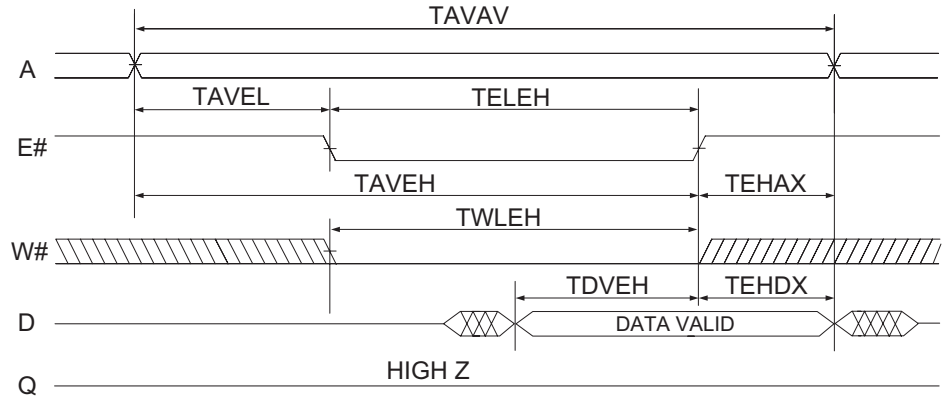
Note 1: Parameter guaranteed, but not tested.

WRITE CYCLE 1 - W# CONTROLLED



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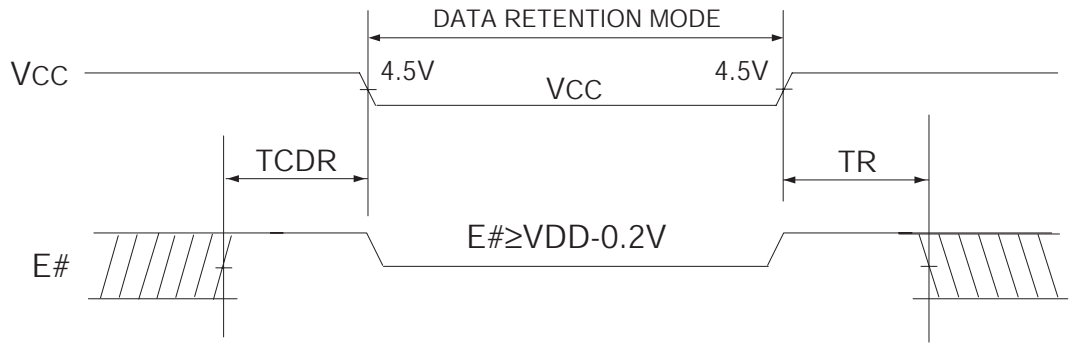
WRITE CYCLE 2 - E# CONTROLLED



Characteristic	Sym	Test Conditions	Vcc	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	V_{CC}	V_{CC} = 0.2V		2	–	–	–	V
Data Retention Quiescent Current	I_{CCDR}	E# ≥ V_{CC} -0.2V	2V	–	25	300	400	µA
		V_{IN} ≥ V_{CC} -0.2V	3V	–	50	450	550	µA
Chip Disable to Data Retention Time (1)	TCDR	or V_{IN} ≤ 0.2V		0	–	–	–	ns
Operation Recovery Time (1)	TR			TAVAV*	–	–	–	ns

Note 1: Parameter guaranteed, but not tested.
* Read Cycle Time

DATA RETENTION E# CONTROLLED



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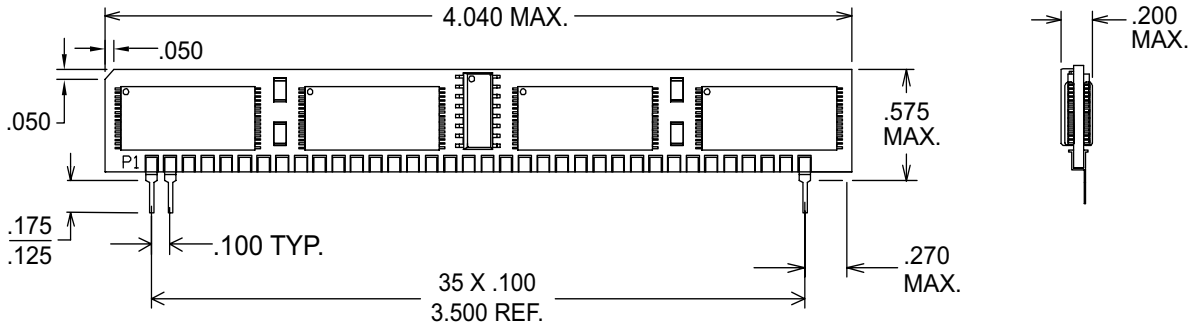
ORDERING INFORMATION

Standard Power	Low Power with Data Retention	Speed (ns)	Package No.
EDI8F81024C70BSC	EDI8F81024LP70BSC	70	62
EDI8F81024C85BSC	EDI8F81024LP85BSC	85	62
EDI8F81024C100BSC	EDI8F81024LP100BSC	100	62

Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I,
e.g. EDI8F81024C70BSC becomes EDI8F81024C70BSI.

PACKAGE DESCRIPTION

PACKAGE NO. 62: 36 PIN SINGLE-IN-LINE PACKAGE



ALL DIMENSIONS ARE IN INCHES