REF34xx 低漂移、低功耗、小型串联电压基准

1 特性

- 初始精度：±0.05%（最大值）
- 温度系数：6ppm/°C（最大值）
- 运行温度范围：−40°C 至 +125°C
- 输出电流：±10mA
- 低静态电流：95µA（最大值）
- 宽输入电压：12V
- 输出 1/f 噪声（0.1Hz 至 10Hz）：$5\mu V_{PP}/V$
- 出色的长期稳定性（30ppm/1000 小时）
- 小型 6 引脚 SOT-23 封装

2 应用

- 精密数据采集系统
- PLC 模拟 I/O 模块
- 现场发送器
- 便携式、电池供电类设备
- 工业仪表
- 测试设备
- 电源监控
- LCR 表

3 说明

REF34xx 器件是低温漂

(6 ppm/°C)、低功耗、高精度 CMOS 电压基准，具有 ±0.05% 初始精度、低运行电流以及小于 95µA 的功耗。该器件还提供 $5\mu V_{p-p}/V$ 的极低输出噪声，这使得它在用于噪声关键型系统中的高分辨率数据转换器时能够保持较高的信号完整性。REF34xx 采用小型 SOT-23 封装，具有更高的规格参数并且能够以引脚对引脚方式替代 MAX607x 和 ADR34xx。REF34xx 系列与大多数 ADC 和 DAC 兼容，如 ADS1287、ADUCM360、ADS1112。

该器件的低输出电压迟滞和低长期输出电压漂移进一步提高了稳定性和系统可靠性。此外， 器件的小尺寸和低运行电流 (95µA) 特性使其非常适合便携式和电池供电应用 应用中，低功耗是一个关键问题。

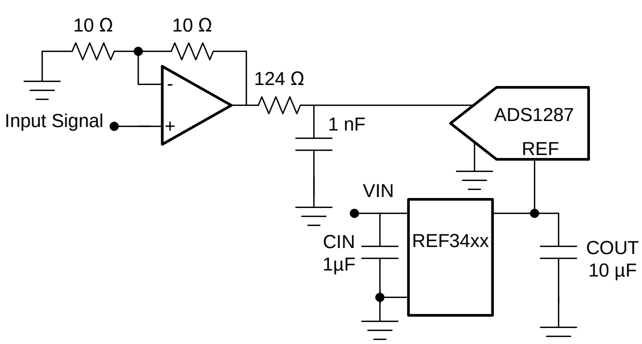
REF34xx 具有 −40°C 至 +125°C 的较宽额定温度范围。有关其他电压选项，请联系 TI 销售代表。

器件信息(1)

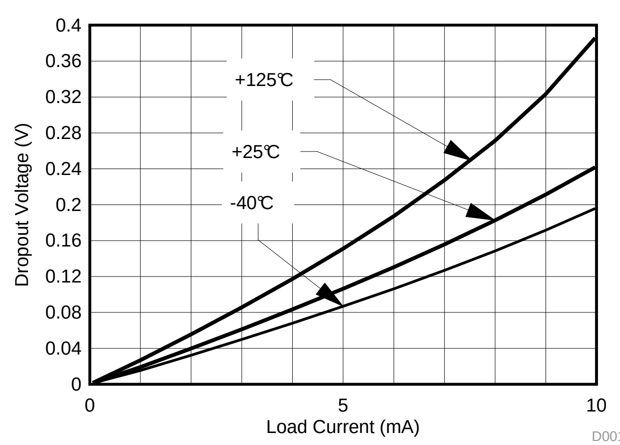
部件名称	封装	封装尺寸（标称值）
REF3425	SOT-23 (6)	2.90mm × 1.60mm
REF3430		
REF3433		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



过热时压降与电流负载间的关系



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2017) to Revision A **Page**

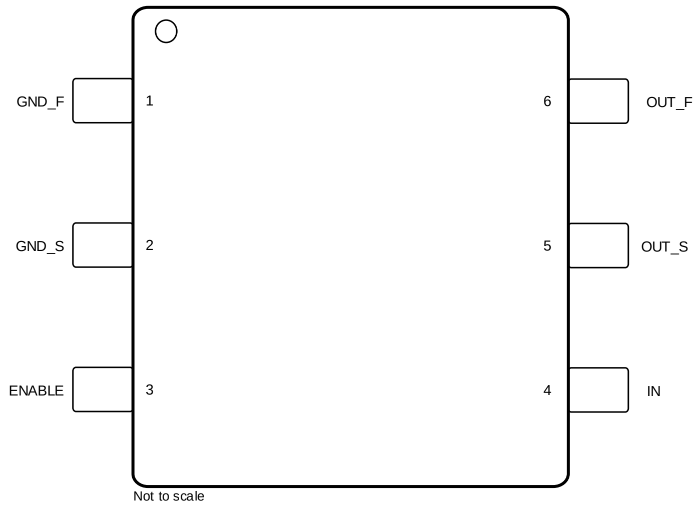
- 已添加 2 个新输出电压选项器件 REF3430 和 REF3433 的产品发布 ... 1

5 器件比较表

产品	V_{OUT}
REF3425	2.5V
REF3430	3V
REF3433	3.3V

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND_F	Ground	Ground force connection
2	GND_S	Ground	Ground sense connection
3	ENABLE	Input	Enable connection. Enables or disables the device.
4	IN	Power	Input supply voltage connection
5	OUT_S	Output	Reference voltage output sense connection
6	OUT_F	Output	Reference voltage output force connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	V_{REF} + 0.05	13	V
	EN	–0.3	IN + 0.3	
Output voltage	V_{REF}	–0.3	5.5	V
Output short circuit current			20	mA
Temperature	Operating, T_A (2)	–55	150	°C
	Storage T_{stg}	–65	170	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) By design, the device is guaranteed functional over the operating temperature of -55°C to 150°C.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Supply input voltage (I_L = 0 mA, T_A = 25°C)	V_{REF} + V_{DO} (1)		12	V
EN	Enable voltage	0		IN	V
I_L	Output current	–10		10	mA
T_A	Operating temperature	–40	25	125	°C

(1) Dropout voltage

7.4 Thermal Information

THERMAL METRIC (1)		REF34xx DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

At T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
	Output voltage accuracy	–40°C ≤ T_A ≤ 125°C			–0.05%		0.05%	
	Output voltage temperature coefficient(1)	–40°C ≤ T_A ≤ 125°C				2.5	6	ppm/°C
LINE AND LOAD REGULATION								
$\Delta V_{(O\Delta VIN)}$	Line regulation(2)	V_{IN} = 2.55 V to 12 V , T_A = 25°C				2		ppm/V
		V_{IN} = V_{REF} + V_{DO}(3) to 12 V, −40°C ≤ T_A ≤ 125°C					15	ppm/V
$\Delta V_{(O\Delta IL)}$	Load regulation(2)	I_L = 0 mA to 10 mA, V_{IN} = 3 V, T_A = 25°C	Sourcing			20		ppm/mA
		I_L = 0 mA to 10 mA, V_{IN} = 3 V, −40°C ≤ T_A ≤ 125°C	Sourcing				30	ppm/mA
		I_L = 0 mA to –10 mA, V_{IN} = V_{REF}+ V_{DO}(4), T_A = 25°C	Sinking	REF3425		40		ppm/mA
				REF3430		43		ppm/mA
				REF3433		48		ppm/mA
		I_L = 0 mA to –10 mA, V_{IN} = V_{REF}+ V_{DO}(4), −40°C ≤ T_A ≤ 125°C	Sinking	REF3425			70	ppm/mA
				REF3430			75	ppm/mA
				REF3433			84	ppm/mA
I_{SC}	Short-circuit current (Output shorted to ground)	V_{REF} = 0, T_A = 25°C				18	22	mA
NOISE								
e_n p-p	Output voltage noise(5)	*f* = 0.1 Hz to 10 Hz				5		µV p-p/V
		f = 10 Hz to 10 kHz				24		µV rms
e_n	Output voltage noise density	*f* = 1 kHz				0.25		ppm/√Hz
HYSTERESIS AND LONG TERM STABILITY								
	Long-term stability(6)	1000 hours				30		ppm
	Output voltage hysteresis(7)	T_A = 25°C to −40°C to 125°C to 25°C, Cycle 1				30		ppm
		T_A = 25°C to −40°C to 125°C to 25°C, Cycle 2				10		ppm
TURNON								
t_{ON}	Turnon time	0.1% of output voltage settling, C_L = 10 µF, REF34xx				2.5		ms
CAPACITIVE LOAD								
C_L	Stable output capacitor value	−40°C ≤ T_A ≤ 125°C			0.1		10	µF
OUTPUT VOLTAGE								
V_{REF}	Output voltage	REF3425				2.5		V
		REF3430				3		V
		REF3433				3.3		V

(1) Temperature drift is specified according to the box method. See *Feature Description* for more details.
(2) The ppm/V and ppm/mA in line and load regulation can be also expressed as µV/V and µV/mA.
(3) The dropout voltage in line regulation test condition is 50 mV.
(4) The dropout voltage in test condition is 500 mV.
(5) The peak-to-peak noise measurement procedure is explained in more detail in *Noise Performance*.
(6) Long-term stability measurement procedure is explained in more in detail in *Long-Term Stability*.
(7) The thermal hysteresis measurement procedure is explained in more detail in *Thermal Hysteresis*.

Electrical Characteristics (continued)

At T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{IN}	Input voltage			V_{REF} + V_{DO}		12	V
I_L	Output current capacity	V_{IN} = V_{REF} + V_{DO} (4) to 12 V	Sourcing	10			mA
		V_{IN} = V_{REF} + V_{DO} (4) to 12 V	Sinking	–10			
I_Q	Quiescent current	−40°C ≤ T_A ≤ 125°C	Active mode		72	95	µA
		−40°C ≤ T_A ≤ 125°C	Shutdown mode		2.5	3	
V_{DO}	Dropout voltage	I_L = 0 mA, T_A = 25°C			50		mV
		I_L = 0 mA, −40°C ≤ T_A ≤ +125°C				100	
		I_L = 10 mA, −40°C ≤ T_A ≤ +125°C				500	
V_{EN}	ENABLE pin voltage	Voltage reference in active mode (EN = 1)		1.6			V
		Voltage reference in shutdown mode (EN = 0)				0.5	
I_{EN}	ENABLE pin leakage current	V_{EN} = V_{IN}=12 V, −40°C ≤ T_A ≤ 125°C			1	2	µA

7.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

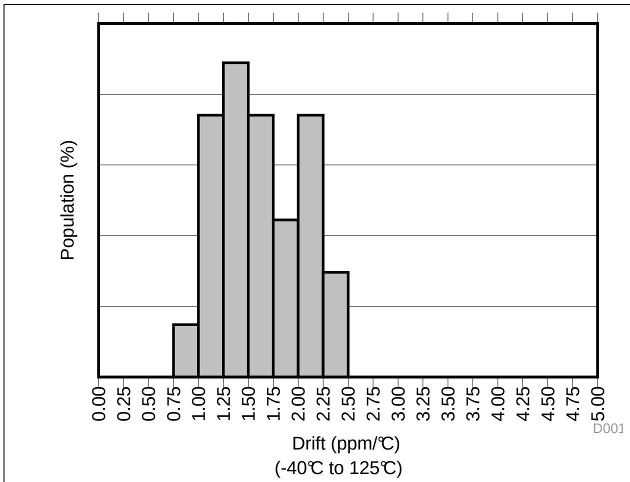


Figure 1. Temperature Drift

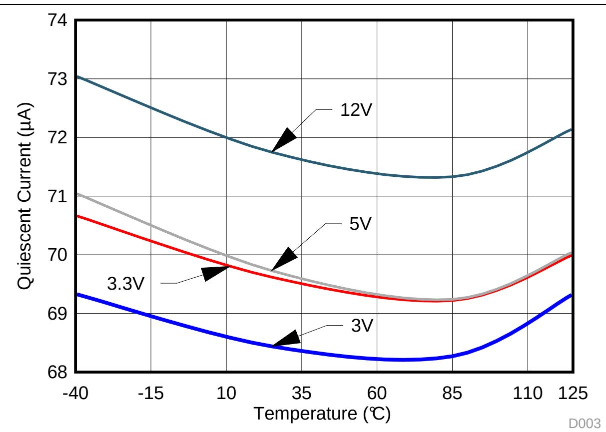


Figure 2. Vin vs Iq over Temperature

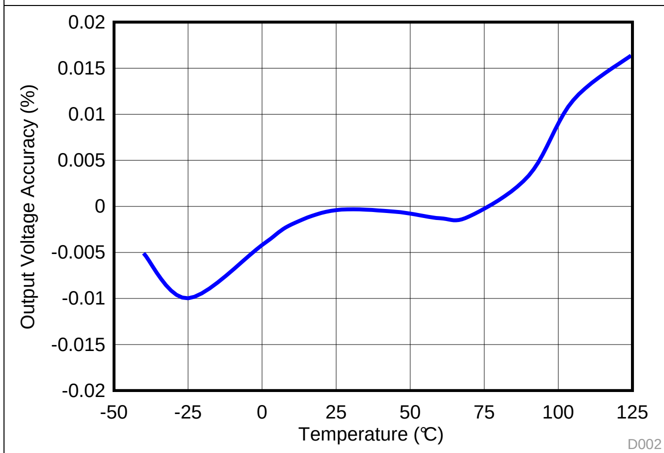


Figure 3. Output Voltage Accuracy vs Temperature

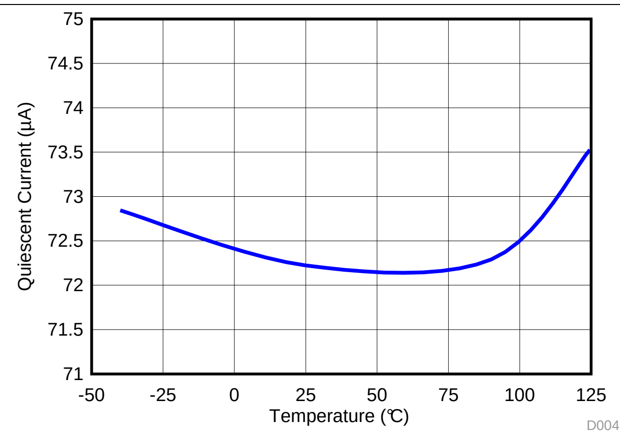


Figure 4. Quiescent Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

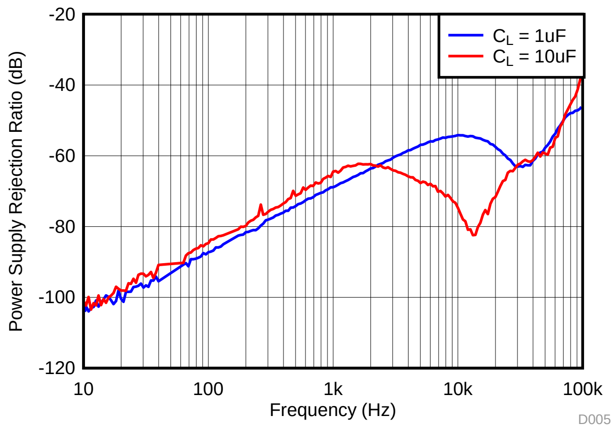


Figure 5. Power-Supply Rejection Ratio vs Frequency

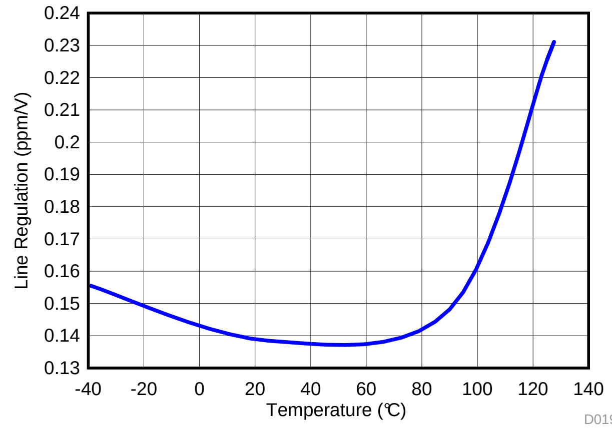


Figure 6. Line Regulation

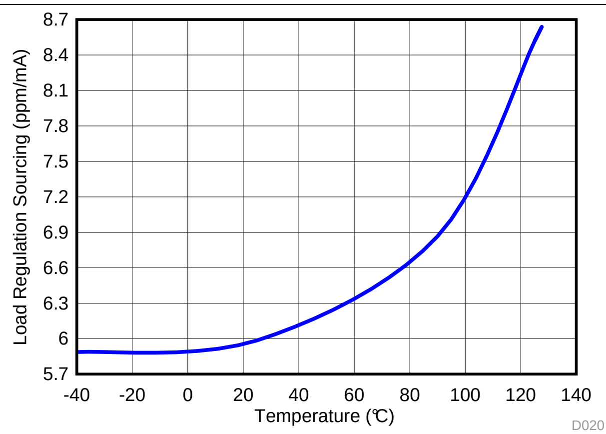


Figure 7. Load Regulation Sourcing

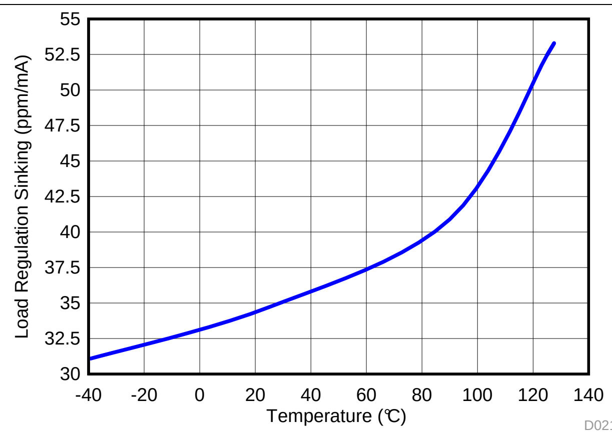


Figure 8. Load Regulation Sinking

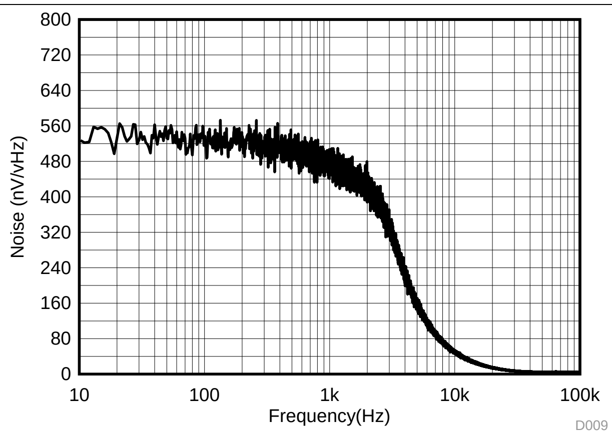


Figure 9. Noise Performance 10Hz to 10kHz

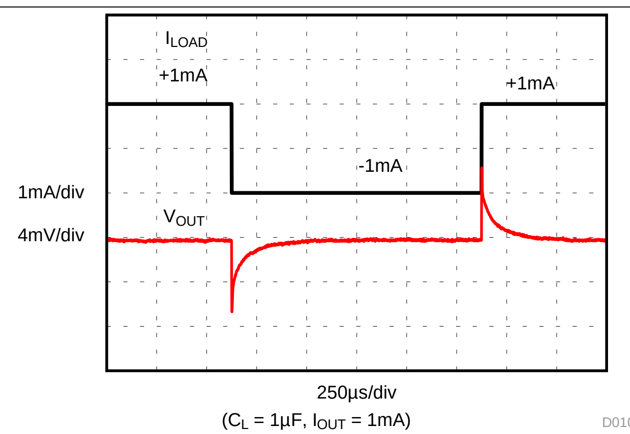


Figure 10. Load Transient

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

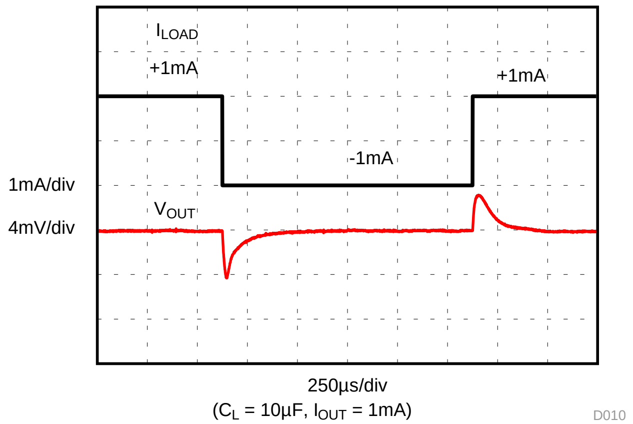


Figure 11. Load Transient

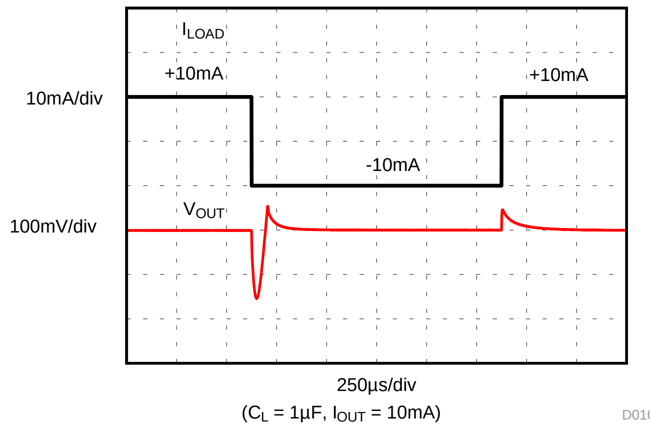


Figure 12. Load Transient

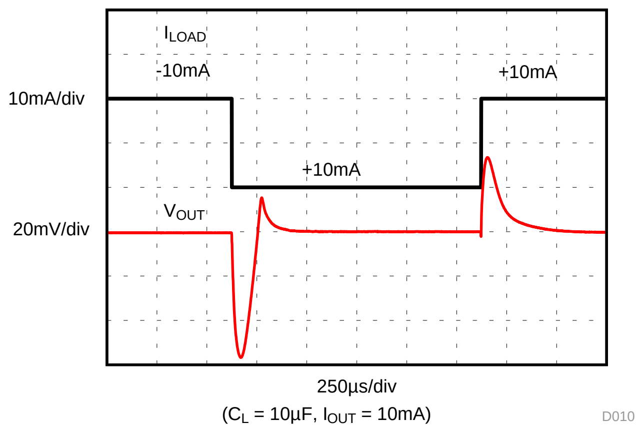


Figure 13. Load Transient

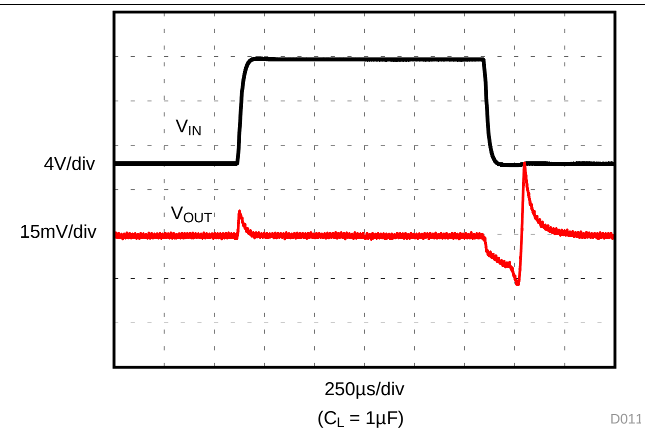


Figure 14. Line Transient

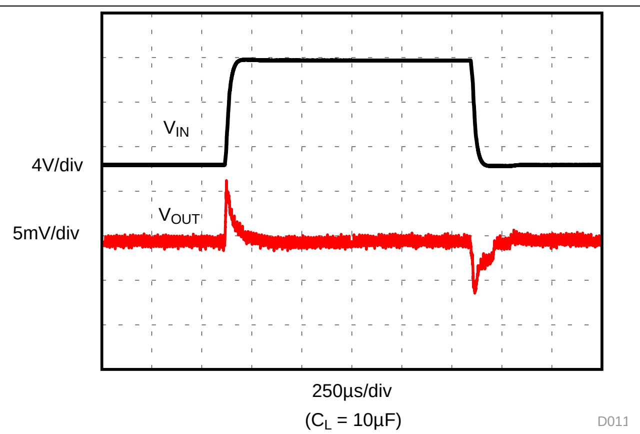


Figure 15. Line Transient

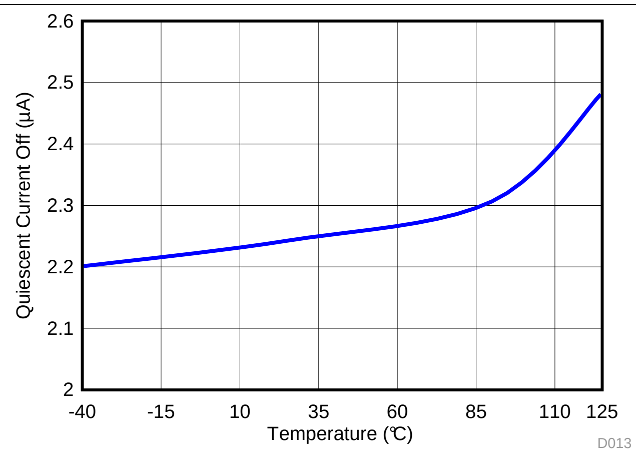


Figure 16. Quiescent Current Shutdown Mode

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 12 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

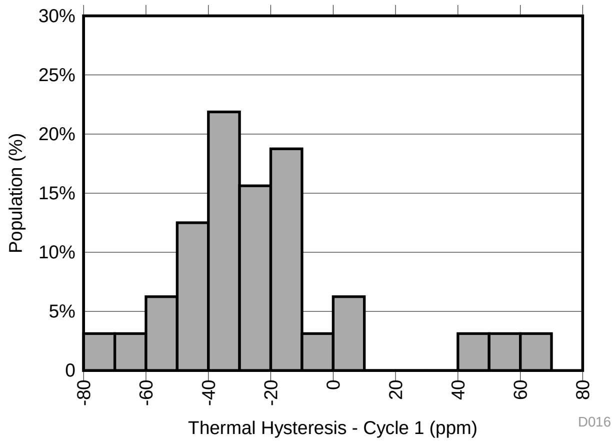


Figure 17. Thermal Hysteresis Distribution (Cycle 1)

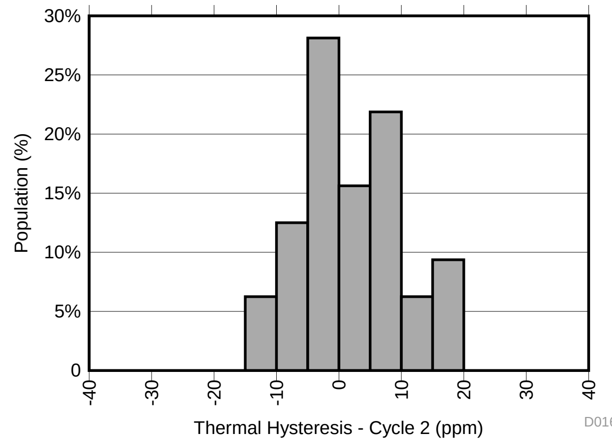
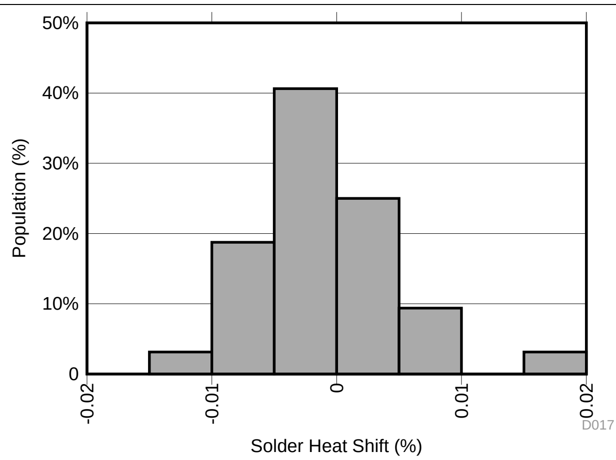


Figure 18. Thermal Hysteresis Distribution (Cycle 2)



Refer to *Solder Heat Shift* for more information

Figure 19. Solder Heat Shift Distribution

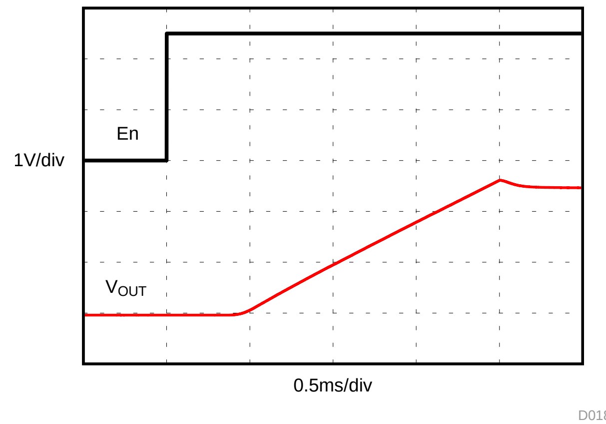


Figure 20. Turnon Time (Enable)

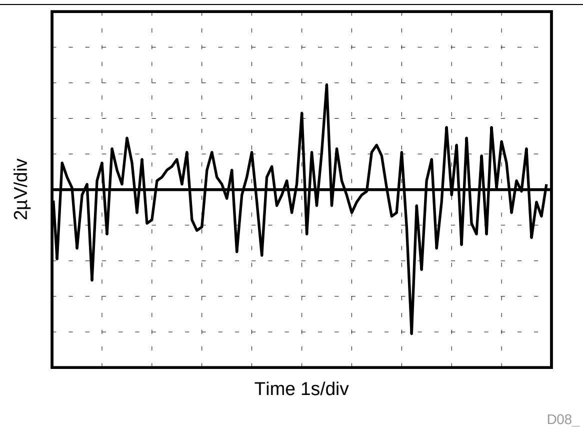


Figure 21. 0.1-Hz to 10-Hz Noise (V_{REF})

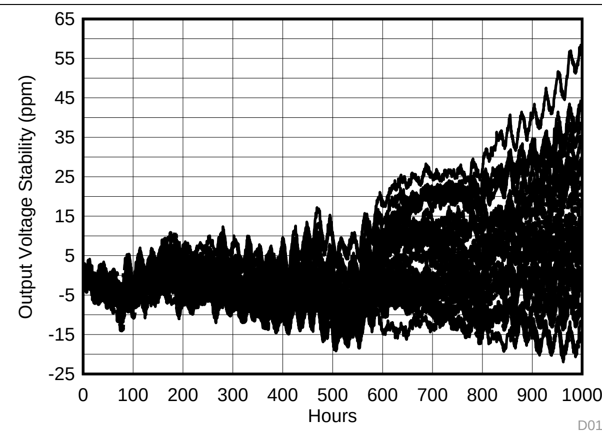


Figure 22. Long Term Stability - 1000 hours (V_{REF})

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF34xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on four printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 23. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm.

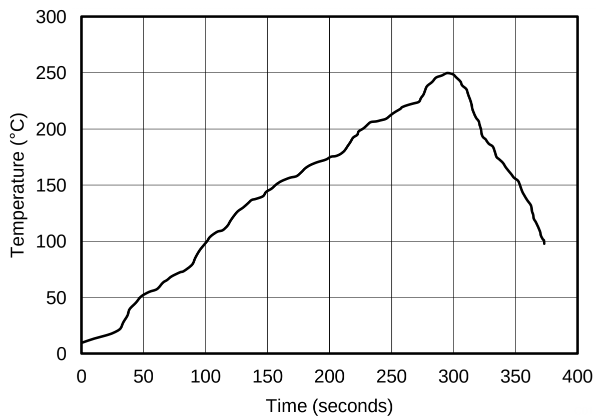


Figure 23. Reflow Profile

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in Figure 24. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the second pass to minimize its exposure to thermal stress.

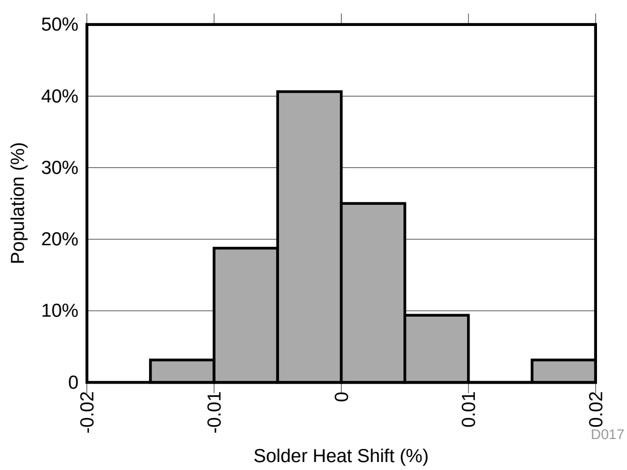


Figure 24. Solder Heat Shift Distribution, V_{REF} (%)

8.2 Long-Term Stability

One of the key parameters of the REF34xx references is long-term stability. Typical characteristic expressed as: curves shows the typical drift value for the REF34xx is 30 ppm from 0 to 1000 hours. This parameter is characterized by measuring 32 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 30 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time

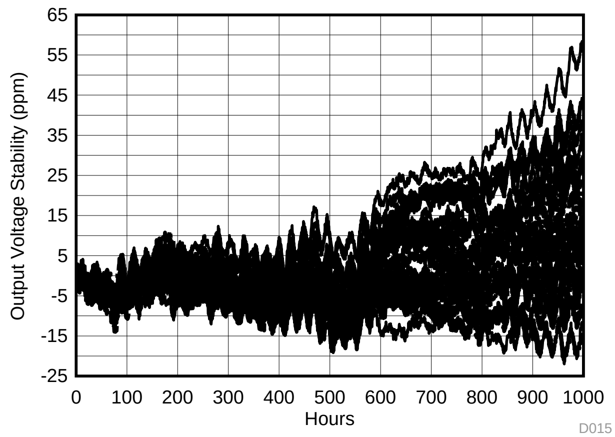


Figure 25. Long Term Stability - 1000 hours (V_{REF})

8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF34xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Hysteresis can be expressed by Equation 1:

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C. (1)

Typical thermal hysteresis distribution is as shown in Figure 26.

Thermal Hysteresis (continued)

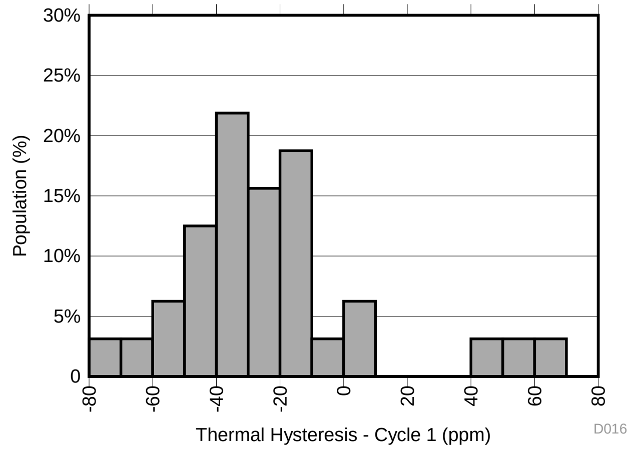


Figure 26. Thermal Hysteresis Distribution (V_{REF})

8.4 Power Dissipation

The REF34xx voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 2:

$$T_J = T_A + P_D \times R_{\theta JA}$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance (2)

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

8.5 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in Figure 27 . Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in Figure 27.

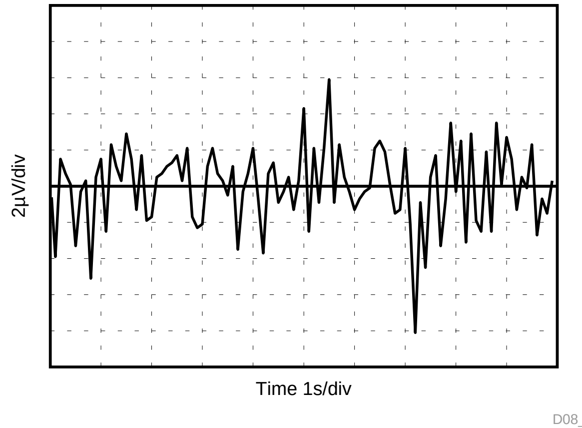


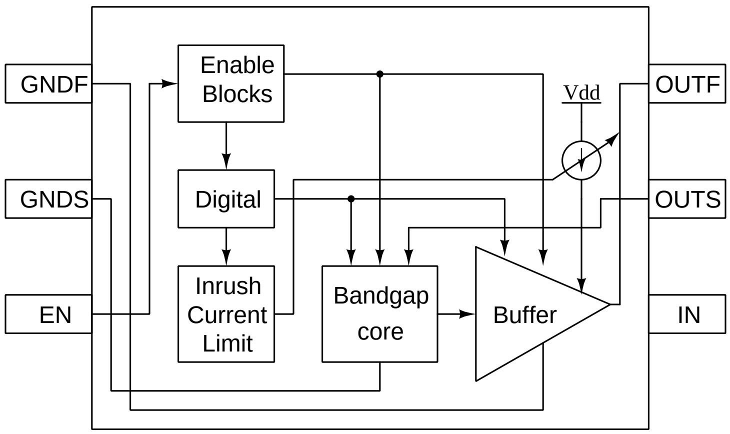
Figure 27. 0.1-Hz to 10-Hz Noise (V_{REF})

9 Detailed Description

9.1 Overview

The REF34xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The *Functional Block Diagram* is a simplified block diagram of the REF34xx showing basic band-gap topology.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Supply Voltage

The REF34xx family of references features an extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The REF34xx features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 72 µA, and the maximum quiescent current over temperature is just 95 µA. Supply voltages below the specified levels can cause the REF34xx to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

9.3.2 Low Temperature Drift

The REF34xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \times \text{Temperature Range}} \right) \times 10^6 \quad (3)$$

9.3.3 Load Current

The REF34xx family is specified to deliver a current load of ±10 mA per output. The V_{REF} output of the device are protected from short circuits by limiting the output short-circuit current to 18 mA. The device temperature increases according to Equation 4:

$$T_J = T_A + P_D \times R_{\theta JA}$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W) (4)

The REF34xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

9.4 Device Functional Modes

9.4.1 EN Pin

When the EN pin of the REF34xx is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF34xx can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 2 µA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the *Thermal Information* for logic high and logic low voltage levels.

9.4.2 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF34xx and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 28 shows the REF34xx used to provide a 2.5-V supply reference voltage. The low drift performance of the REF34xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

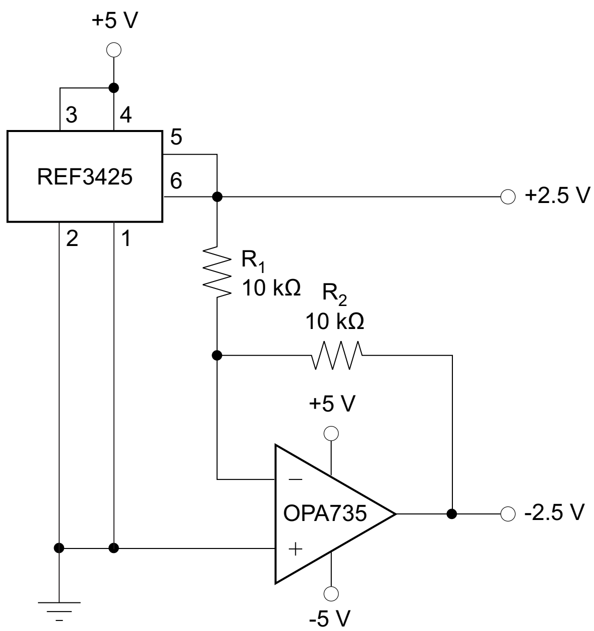


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Figure 28. REF34xx and OPA735 Create Positive and Negative Reference Voltages

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail. Basic applications includes positive/negative voltage reference and data acquisition systems. The table below shows the typical application of REF34xx and its companion ADC/DAC.

Table 1. Typical Applications and Companion ADC/DAC

Applications	ADC/DAC
PLC - DCS	DAC8881, ADS8332, ADS8568, ADS8317, ADS8588S, ADS1287
Display Test Equipment	ADS8332
Field Transmitters - Pressure	ADUCM360
Video Surveillance - Thermal Cameras	ADS7279
Medical Blood Glucose Meter	ADS1112

10.2 Typical Application: Basic Voltage Reference Connection

The circuit shown in Figure 29 shows the basic configuration for the REF34xx references. Connect bypass capacitors according to the guidelines in *Input and Output Capacitors*.

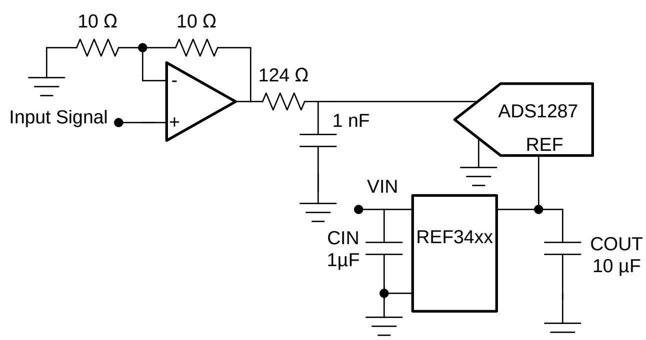

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Figure 29. Basic Reference Connection

10.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5 V
Output voltage V_{OUT}	2.5 V
REF34xx input capacitor	1 µF
REF34xx output capacitor	10 µF

10.2.2 Detailed Design Procedure

10.2.2.1 Input and Output Capacitors

A 1-µF to 10-µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1-µF ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 µF must be connected to the output to improve stability and help filter out high frequency noise. An additional 1-µF to 10-µF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the turnon time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1-µF ceramic capacitor in parallel to reduce overall ESR on the output.

10.2.2.2 4-Wire Kelvin Connections

Current flowing through a PCB trace produces an IR voltage drop, and with longer traces, this drop can reach several millivolts or more, introducing a considerable error into the output voltage of the reference. A 1-inch long, 5-millimeter wide trace of 1-ounce copper has a resistance of approximately 100 mΩ at room temperature; at a load current of 10 mA, this can introduce a full millivolt of error. In an ideal board layout, the reference must be mounted as close as possible to the load to minimize the length of the output traces, and, therefore, the error introduced by voltage drop. However, in applications where this is not possible or convenient, force and sense connections (sometimes referred to as Kelvin sensing connections) are provided as a means of minimizing the IR drop and improving accuracy.

Kelvin connections work by providing a set of high impedance voltage-sensing lines to the output and ground nodes. Because very little current flows through these connections, the IR drop across their traces is negligible, and the output and ground

It is always advantageous to use Kelvin connections whenever possible. However, in applications where the IR drop is negligible or an extra set of traces cannot be routed to the load, the force and sense pins for both V_{OUT} and GND can simply be tied together, and the device can be used in the same fashion as a normal 3-terminal reference (as shown in **Figure 26**).

10.2.2.3 V_{IN} Slew Rate Considerations

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage wave-form has both a rising and falling slew rate close to 6 V/ms.

10.2.2.4 Shutdown/Enable Feature

The REF34xx references can be switched to a low power shut-down mode when a voltage of 0.5 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 1.6 V or higher. During shutdown, the supply current drops to less than 2 µA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.5 V and 1.6 V because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly. If not using the shutdown feature, however, the ENABLE pin can simply be tied to the IN pin, and the reference remains operational continuously.

10.2.3 Application Curves

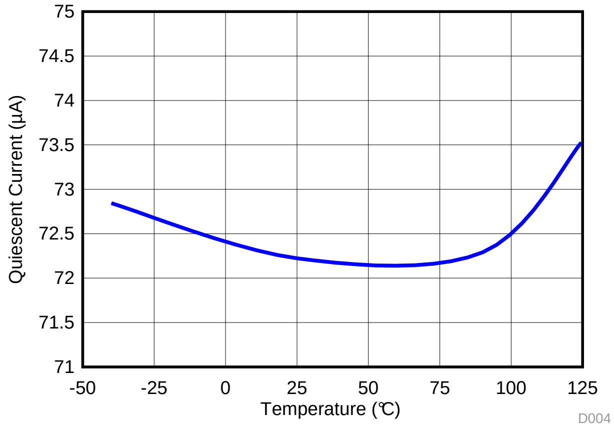

Figure 30. Quiescent Current vs Temperature

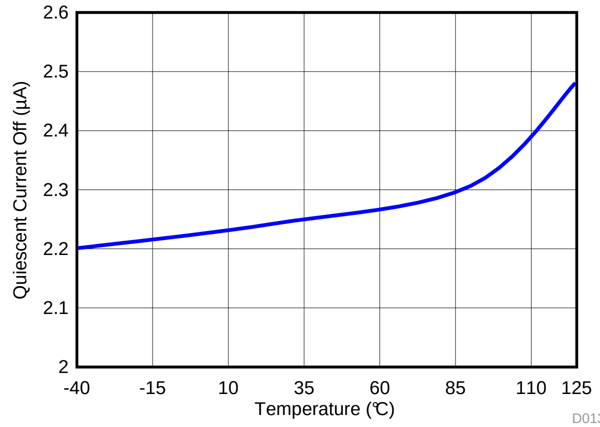

Figure 31. Quiescent Current Shutdown Mode

11 Power-Supply Recommendations

The REF34xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

12 Layout

12.1 Layout Guidelines

Figure 32 illustrates an example of a PCB layout for a data acquisition system using the REF34xx. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF} of the REF34xx.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

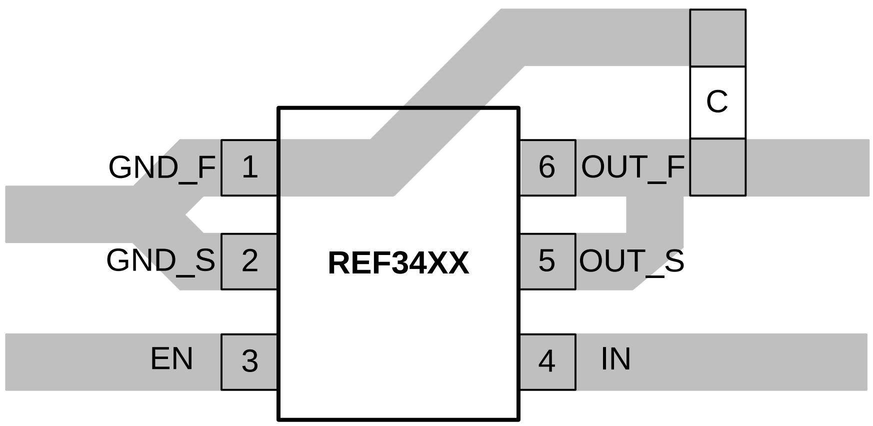

Figure 32. Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

如需相关文档，请参阅：

- *《INA21x 电压输出、低侧或高侧测量、双向、零漂移系列分流监控器》*
- *《低漂移双向单电源低侧电流感应参考设计》*

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13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF3425IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	-40 to 125	19ED	Samples
REF3430IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H6D	Samples
REF3433IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1H5D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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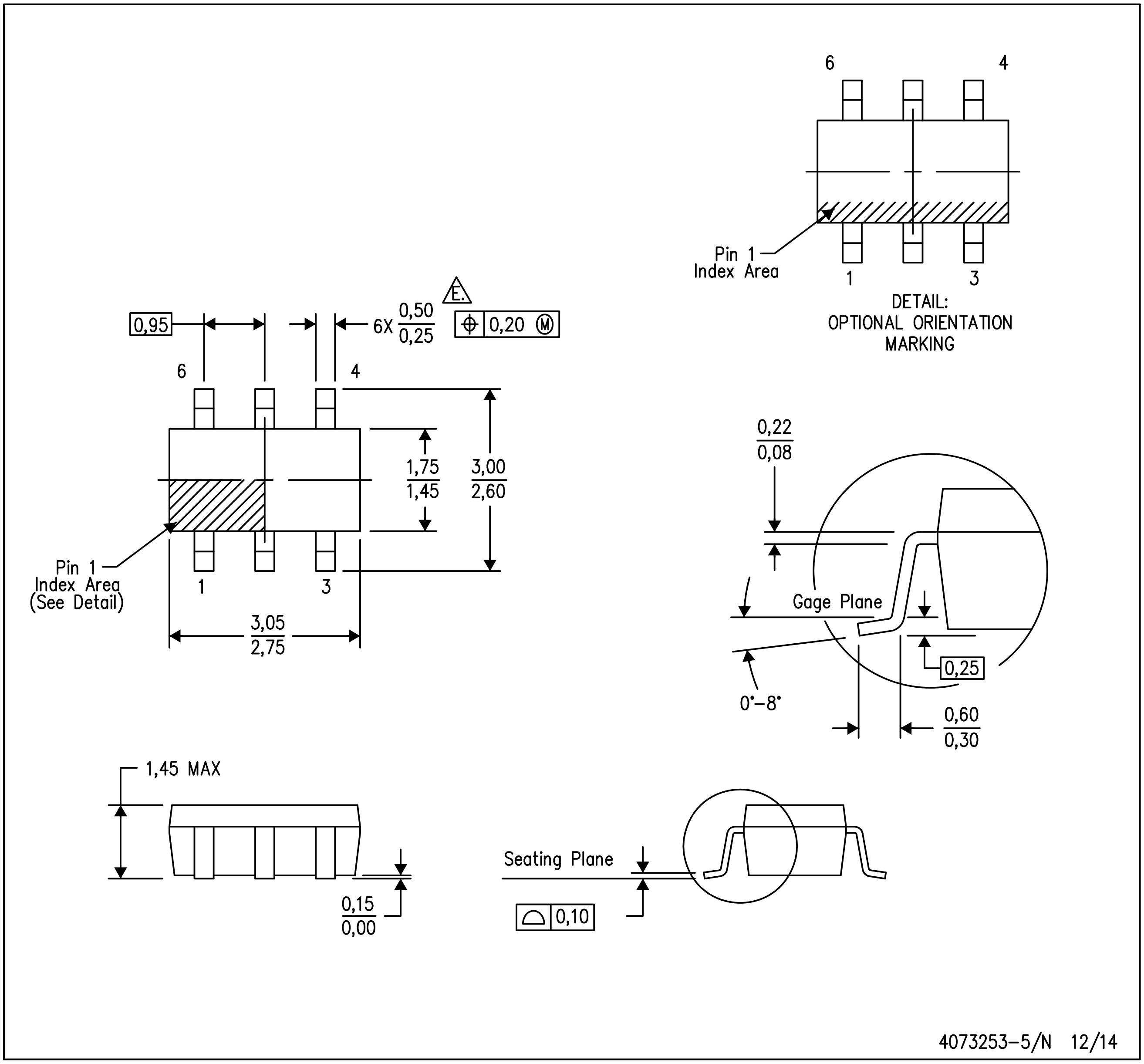
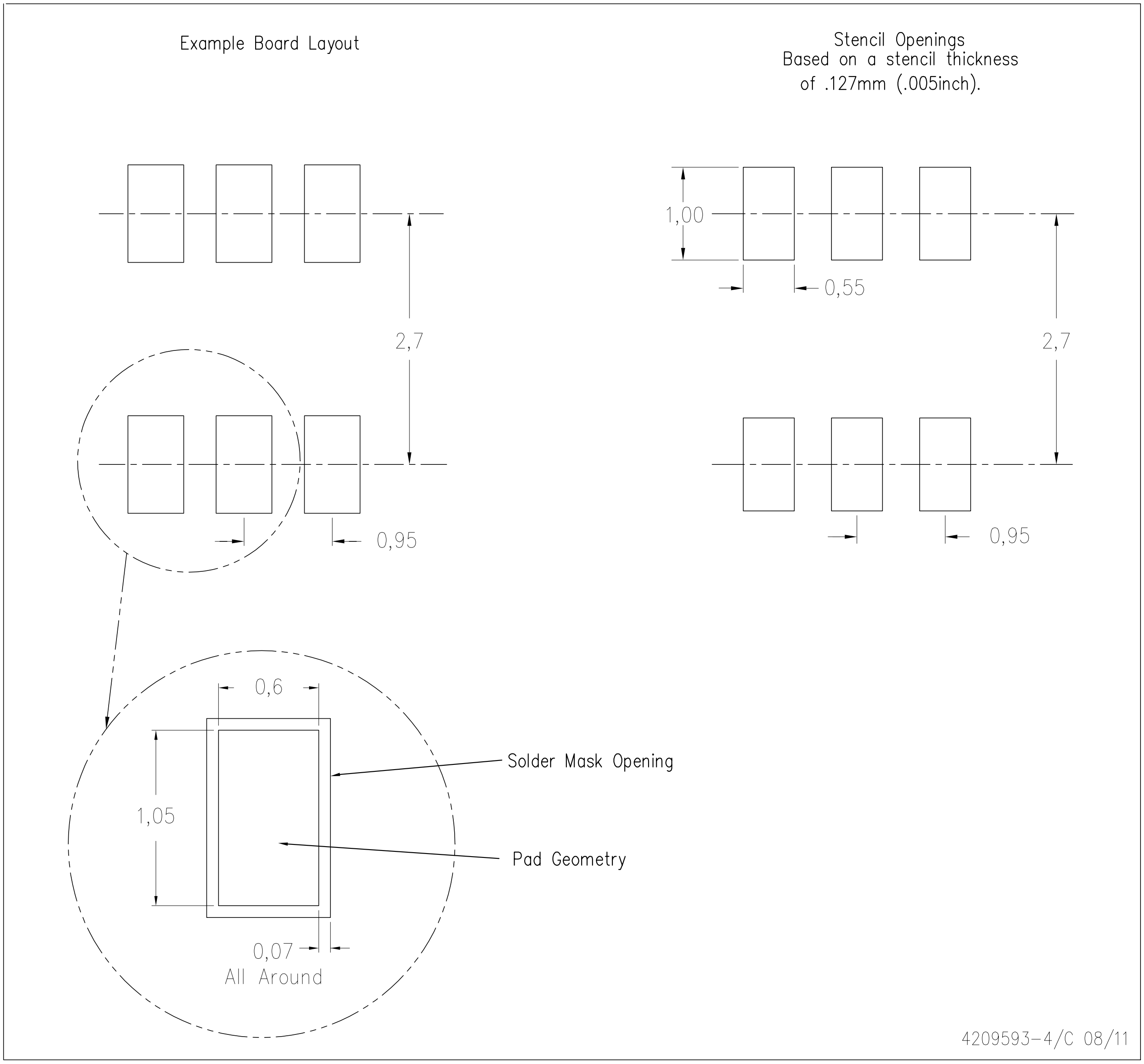


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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