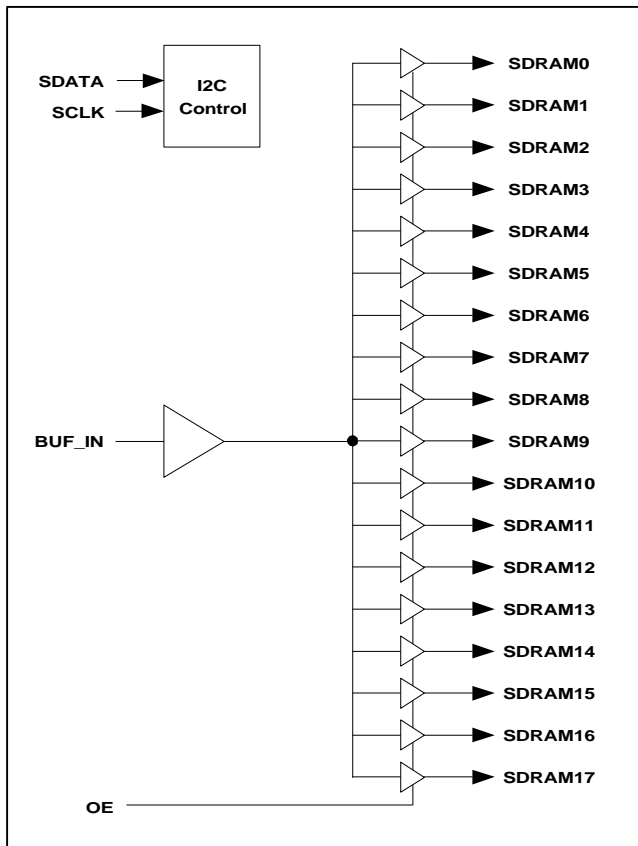


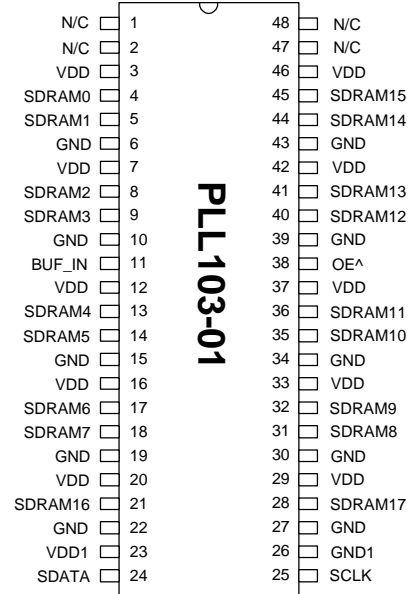
FEATURES

- Generate 18 copies of High-speed clock inputs.
- Supports up to four SDRAM DIMMS synchronous clocks.
- Supports 2-wire I2C serial bus interface with readback.
- 50% duty cycle with low jitter.
- Less than 5ns delay.
- Skew between any outputs is less than 250 ps.
- Tri-state pin for testing.
- Frequency up to 133 MHZ.
- 3.0V-3.7V Supply range.
- 48-pin SSOP package.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: ^: pull up

POWER GROUP

- VDD: SDRAM(0:17)
- VDD1: I2C Circuitry

GROUND GROUP

- GND: SDRAM(0:17)
- GND1: I2C Circuitry

KEY SPECIFICATIONS

- BUF_IN to SDRAM outputs Delay: 1 ~ 5 ns.
- Output Slew: ≥ 1.5 V/ns.
- Output Skew: ± 250 ps.
- Output Duty Cycle: $50\% \pm 5\%$.

PIN DESCRIPTIONS

| Name | Number | Type | Description |
|---------------|------------------------------|------|--|
| SDRAM (0:3) | 4,5,8,9 | O | SDRAM Byte0 Clock outputs. |
| SDRAM (4:7) | 13,14,17,18 | O | SDRAM Byte1 Clock outputs. |
| SDRAM (8:11) | 31,32,35,36 | O | SDRAM Byte2 Clock outputs. |
| SDRAM (12:15) | 40,41,44,45 | O | SDRAM Byte3 Clock outputs. |
| SDRAM (16:17) | 21,28 | O | SDRAM Byte4 Clock outputs. |
| OE | 38 | I | Tristates all outputs, active low. Has internal pull-up. |
| BUF_IN | 11 | I | Input for fanout buffers SDRAM (0:17). |
| SDATA | 24 | B | Serial data inputs for serial interface port. |
| SCLK | 25 | I | |
| VDD | 3,7,12,16,20,29,33,37,42,46 | P | 3.3V Power supply for SDRAM buffer. |
| VDD1 | 23 | P | 3.3V Power supply for I2C circuitry. |
| GND | 6,10,15,19,22,27,30,34,39,43 | P | Ground for SDRAM buffer. |
| GND1 | 26 | P | Power supply for I2C circuitry. |
| N/C | 1,2,47,48 | - | Pins are internally disconnected. |

I2C BUS CONFIGURATION SETTING

| | | | | | | | | |
|----------------------------|---|----|----|----|----|----|----|-----|
| Address Assignment | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | - |
| Slave Receiver/Transmitter | Provides both slave write and readback functionality | | | | | | | |
| Data Transfer Rate | Standard mode at 100kbits/s | | | | | | | |
| Data Protocol | <p>This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).</p> <p>Following the acknowledge of this address byte, in Write Mode: the Command Byte and Byte Count Byte must be sent by the master but ignored by the slave, in Read Mode: the Byte Count Byte will be read by the master then all other Data Byte. Byte Count Byte default at power-up is = (0x09).</p> | | | | | | | |

I2C CONTROL REGISTERS

1. BYTE 0: SDRAM(0:7) Clock Register (1=Enable, 0=Disable)

| Bit | Pin# | Default | Description |
|-------|------|---------|--------------------------|
| Bit 7 | 18 | 1 | SDRAM7 (Active/Inactive) |
| Bit 6 | 17 | 1 | SDRAM6 (Active/Inactive) |
| Bit 5 | 14 | 1 | SDRAM5 (Active/Inactive) |
| Bit 4 | 13 | 1 | SDRAM4 (Active/Inactive) |
| Bit 3 | 9 | 1 | SDRAM3 (Active/Inactive) |
| Bit 2 | 8 | 1 | SDRAM2 (Active/Inactive) |
| Bit 1 | 5 | 1 | SDRAM1 (Active/Inactive) |
| Bit 0 | 4 | 1 | SDRAM0 (Active/Inactive) |

2. BYTE 1: SDRAM(8:15) Clock Register (1=Enable, 0=Disable)

| Bit | Pin# | Default | Description |
|-------|------|---------|---------------------------|
| Bit 7 | 45 | 1 | SDRAM15 (Active/Inactive) |
| Bit 6 | 44 | 1 | SDRAM14 (Active/Inactive) |
| Bit 5 | 41 | 1 | SDRAM13 (Active/Inactive) |
| Bit 4 | 40 | 1 | SDRAM12 (Active/Inactive) |
| Bit 3 | 36 | 1 | SDRAM11 (Active/Inactive) |
| Bit 2 | 35 | 1 | SDRAM10 (Active/Inactive) |
| Bit 1 | 32 | 1 | SDRAM9 (Active/Inactive) |
| Bit 0 | 31 | 1 | SDRAM8 (Active/Inactive) |

3. BYTE 2: SDRAM(16:17) Clock Register (1=Enable, 0=Disable)

| Bit | Pin# | Default | Description |
|-------|------|---------|---------------------------|
| Bit 7 | 28 | 1 | SDRAM17 (Active/Inactive) |
| Bit 6 | 21 | 1 | SDRAM16 (Active/Inactive) |
| Bit 5 | - | 1 | Reserved |
| Bit 4 | - | 1 | Reserved |
| Bit 3 | - | 1 | Reserved |
| Bit 2 | - | 1 | Reserved |
| Bit 1 | - | 1 | Reserved |
| Bit 0 | - | 1 | Reserved |

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|-------------------------------|----------|--------------|--------------|-------|
| Supply Voltage | V_{DD} | $V_{SS}-0.5$ | 7.0 | V |
| Input Voltage, dc | V_I | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V |
| Output Voltage, dc | V_O | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V |
| Storage Temperature | T_S | -65 | 150 | °C |
| Ambient Operating Temperature | T_A | 0 | 70 | °C |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC/DC Electrical Specifications

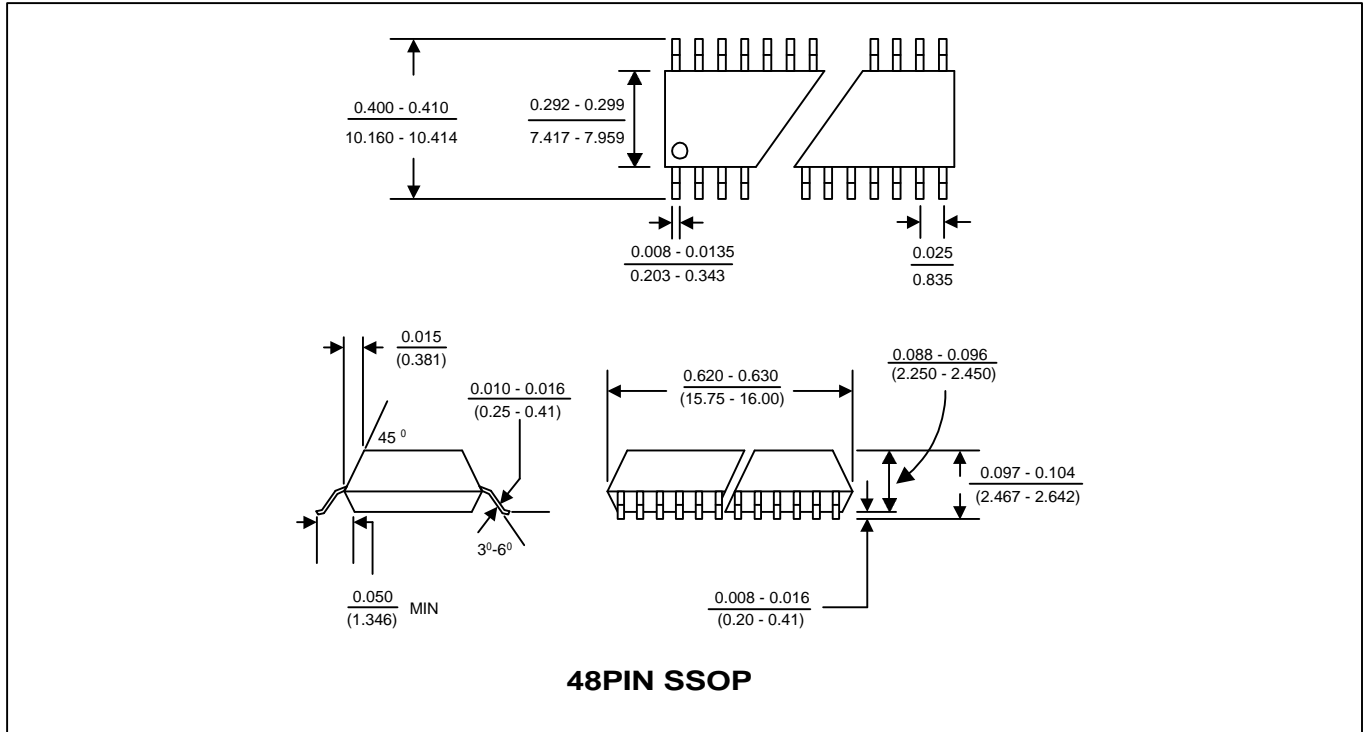
| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|--------------------------|-----------|---|--------------|------|--------------|-------|
| Input High Current | I_{IH} | $V_{IN} = V_{DD}$ | | | 5 | uA |
| Input Low Current | I_{IL} | $V_{IN}=0V$; with no pull-up resistors | | | | uA |
| | I_{IL} | $V_{IN}=0V$; with 100k pull-up resistors | | | | uA |
| Input High Voltage | V_{IH} | | 2 | | $V_{DD}+0.3$ | V |
| Input Low Voltage | V_{IL} | | $V_{SS}-0.3$ | | 0.8 | V |
| Input Frequency | F_{IN} | $V_{DD}=3.3V$; All outputs loaded | 10 | | 150 | Mhz |
| Input Capacitance | C_{IN} | Logic Inputs | | | 5 | PF |
| Operating Supply Current | I_{DD1} | $C_L = 0pf @ 66MHz$ | | 80 | 120 | mA |
| | I_{DD2} | $C_L = 0pf @ 100MHz$ | | 120 | 180 | mA |
| | I_{DD3} | $C_L = 30pf$; $R_S = 33\Omega @ 66MHz$ | | 180 | 260 | mA |
| | I_{DD4} | $C_L = 30pf$; $R_S = 33\Omega @ 100MHz$ | | 240 | 360 | mA |
| | I_{DD5} | Stopped, input at 0 or VDD | | | | 500 |

2. Output Buffer Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range $T_A = 0^{\circ}\text{C}$ to 70°C

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---------------------|---------------|--|------|------|------|-------|
| Output High Voltage | V_{OH} | $I_{OH} = -36 \text{ mA}$ | 2.4 | 3 | | V |
| Output Low Voltage | V_{OL} | $I_{OH} = 23 \text{ mA}$ | | 0.27 | 0.4 | V |
| Output High Current | I_{OH} | $V_{OH} = 2.0 \text{ V}$ | | -115 | -54 | mA |
| Output Low Current | I_{OL} | $V_{OL} = 0.8 \text{ V}$ | 40 | 57 | | mA |
| Output Impedance | R_{DSP} | $V_O = (0.5) * V_{DD}$ | 10 | | 24 | ohm |
| Output Impedance | R_{DSN} | $V_O = (0.5) * V_{DD}$ | 10 | | 24 | ohm |
| Rise Time | T_r | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4\text{V}$ | | 0.95 | 1.33 | ns |
| Fall Time | T_f | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4\text{V}$ | | 0.95 | 1.33 | ns |
| Skew | T_{skew} | $V_T = 1.5 \text{ V}$ | | 110 | 250 | ps |
| Duty Cycle | D_T | $V_T = 1.5 \text{ V}$ | 45 | 50 | 55 | % |
| Propagation | T_{PROP} | $V_T = 1.5 \text{ V}$ | 1 | 5 | 6 | ns |
| | T_{PROPEN} | $V_T = 1.5 \text{ V}$ | 1 | | 8 | ns |
| | $T_{PROPDIS}$ | $V_T = 1.5 \text{ V}$ | 1 | | 8 | ns |

PACKAGE INFORMATION



ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL103-01 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRIAL
PACKAGE TYPE
X=SSOP

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